

# SDHCAL for ILD

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## OUTLINE

- SDHCAL for ILD
- SDHCAL-GRPC prototype
- Prototype results
- Preparation for ILD
- Present and future development
- Conclusion

# SDHCAL Milestones

- 2006 : Start of the SDHCAL development with the aim to achieve the first technological prototype using the semi-digital readout concept;
- 2007 : Development of small detectors and associated electronics readout;
- 2008-2011 DHCAL ANR-blanc;
- 2010 : International review (organized by the IN2P3), CALICE internal review;
- 2011 : Construction of the SDHCAL prototype;
- 2012 : Test Beam at CERN;
- 2013 : Prototype data analyses and R&D for final validation of the SDHCAL-ILD.

## **Several groups of the CALICE collaboration contribute to the project :**

France : IPNL, LAPP, LLR, LPC, OMEGA;  
Spain : CIEMAT;  
Belgium : UCL, Gent;  
China : Tsinghua university, NCEPU;  
Tunisia : Tunis university.

# SDHCAL concept

## 1- Detector choice

Gaseous detectors: homogenous, cost-effective and highly transverse and longitudinal **granular**.

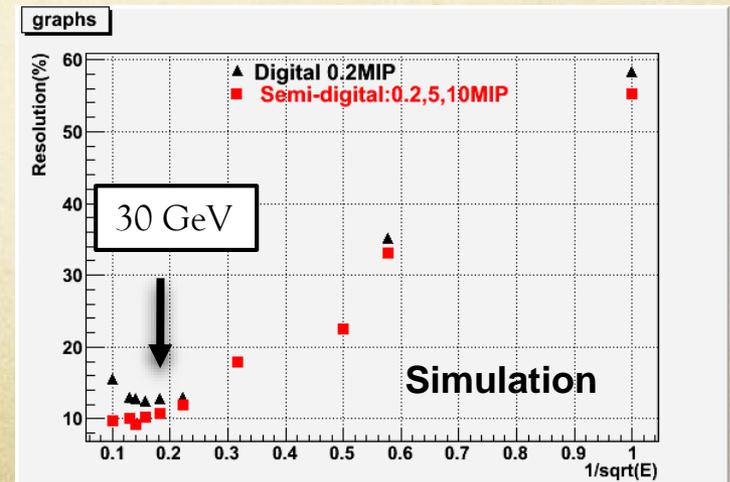
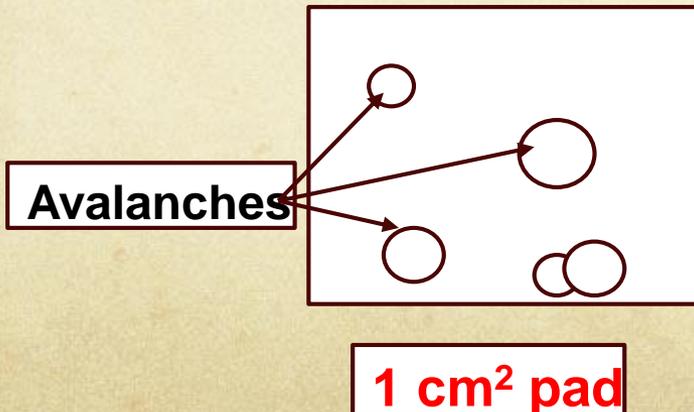
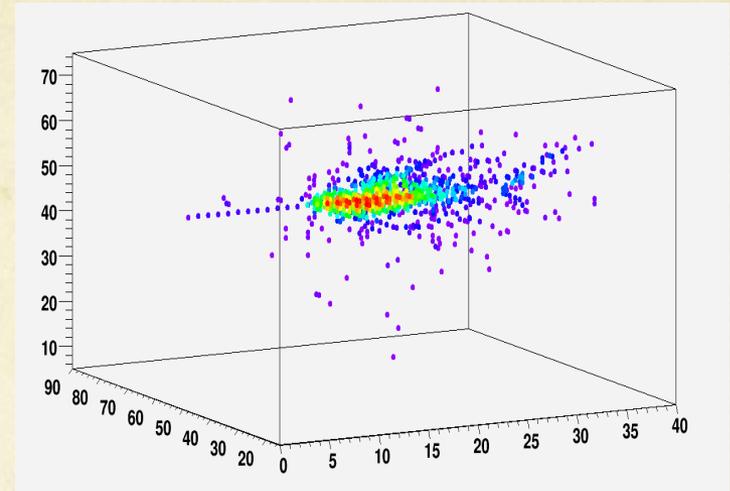
**GRPC** : is an adequate candidate for ILC.

## 2- Electronics readout choice

At **high energy** the shower core is very **dense**

→ Simple binary readout will suffer saturation effect

→ Semi-digital readout (2-bit) can improve the energy resolution.



# SDHCAL-ILD

The SDHCAL-GRPC is one of the two HCAL options proposed in the **ILD Letter Of Intention (LOI)**. Modules are made of 48 RPC chambers ( $6\lambda_T$ ) equipped with power-pulsing electronics readout.

The structure proposed for the SDHCAL-ILD :

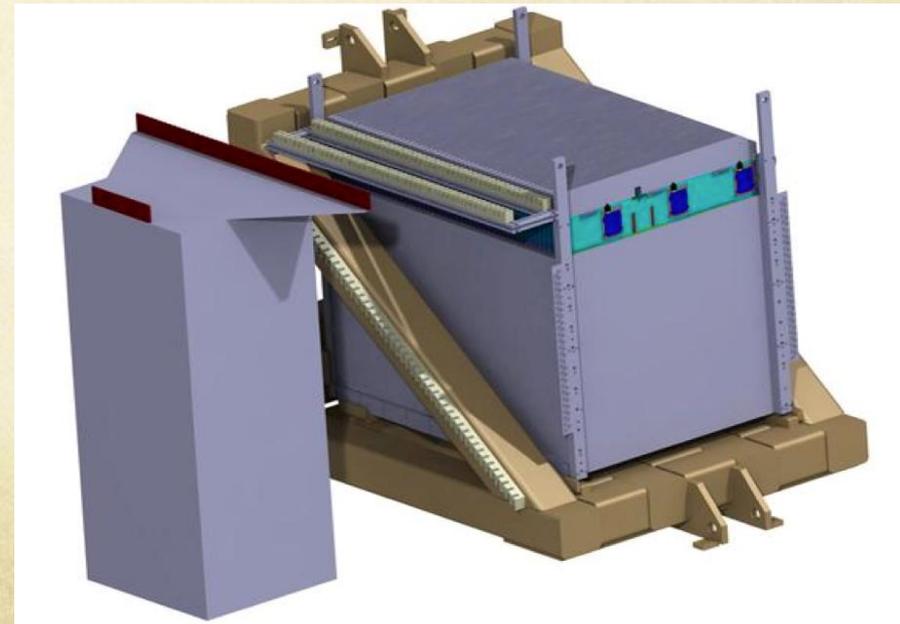
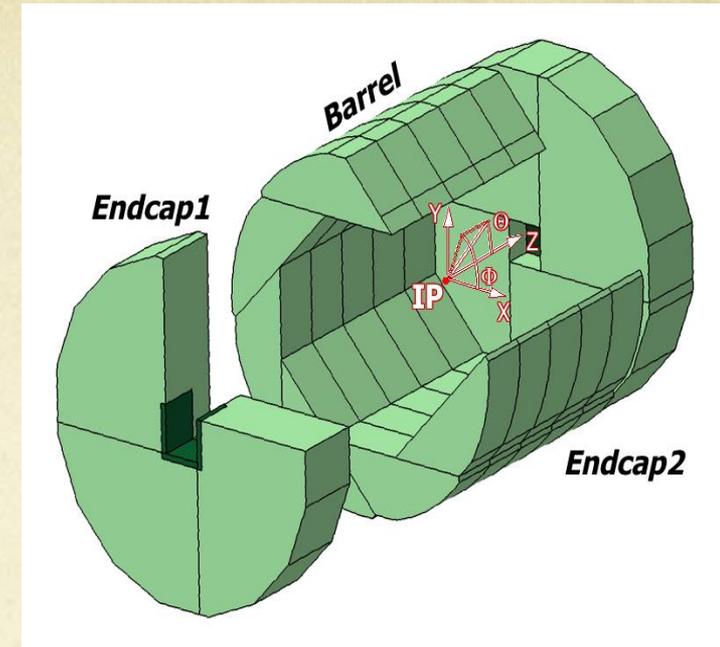
- Is self-supporting
- Has negligible dead zones
- Eliminates projective cracks
- Minimizes barrel / endcap separation (services leaving from the outer radius)

## SDHCAL Prototype

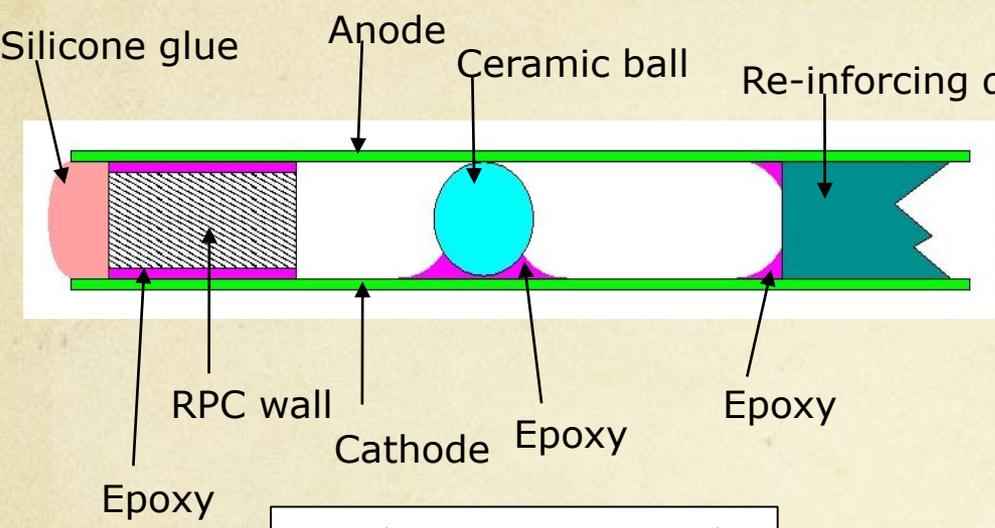
- Come as close as possible to the ILD module and be able to study hadronic showers
- 48 units (active layer + absorber) fulfilling the ILD requirements.

## Challenges

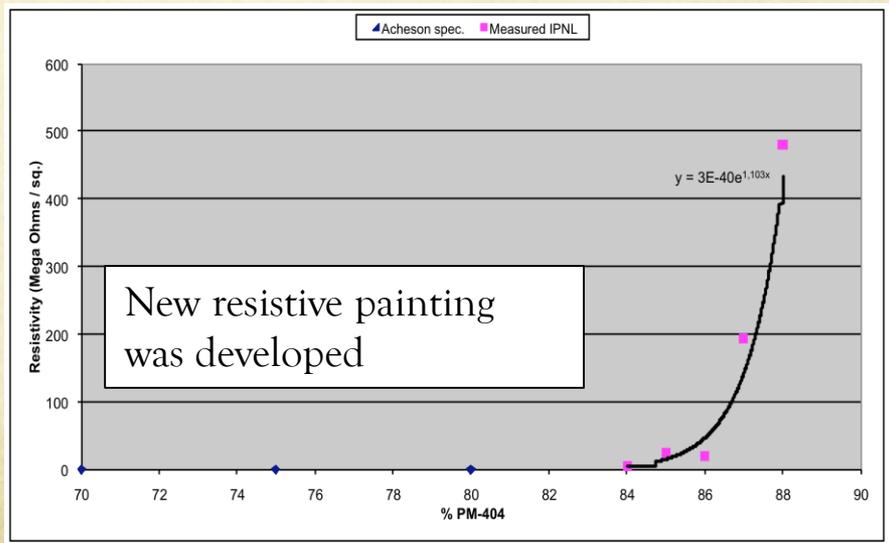
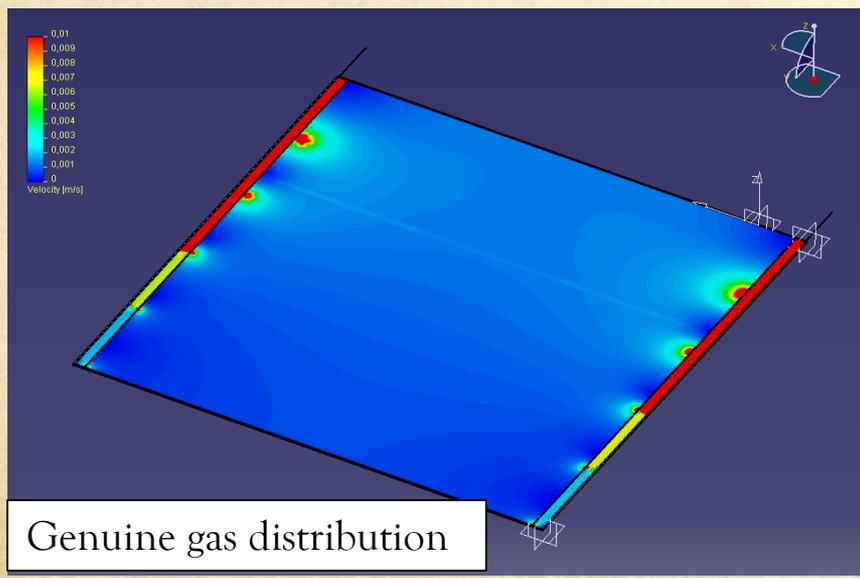
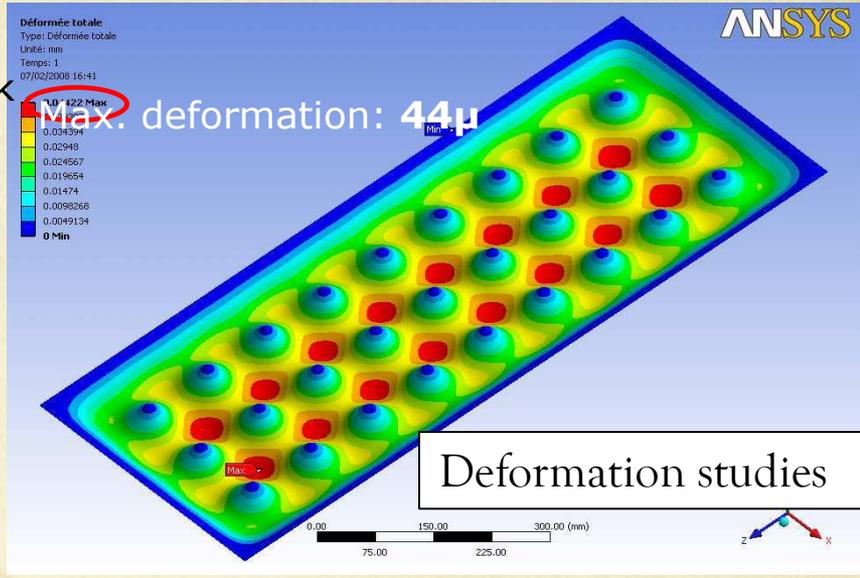
- Homogeneity for large surfaces
- Thickness of only few mms
- Services from one side
- Embedded power-cycled electronics
- Self-supporting mechanical structure



# GRPC development



Dead zones minimized



# Electronics readout development

ASIC: HARDROC

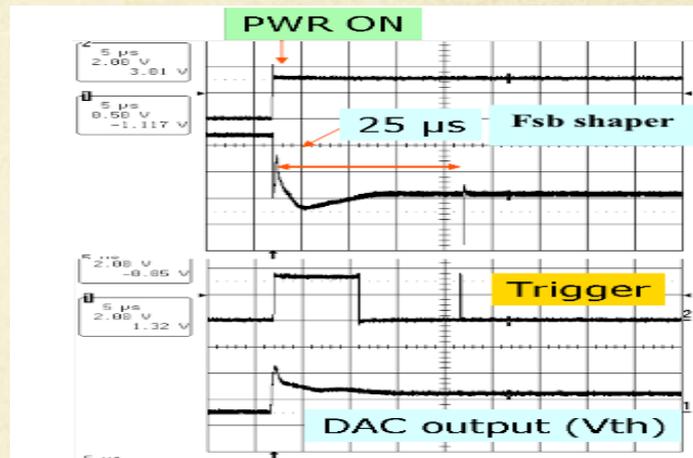
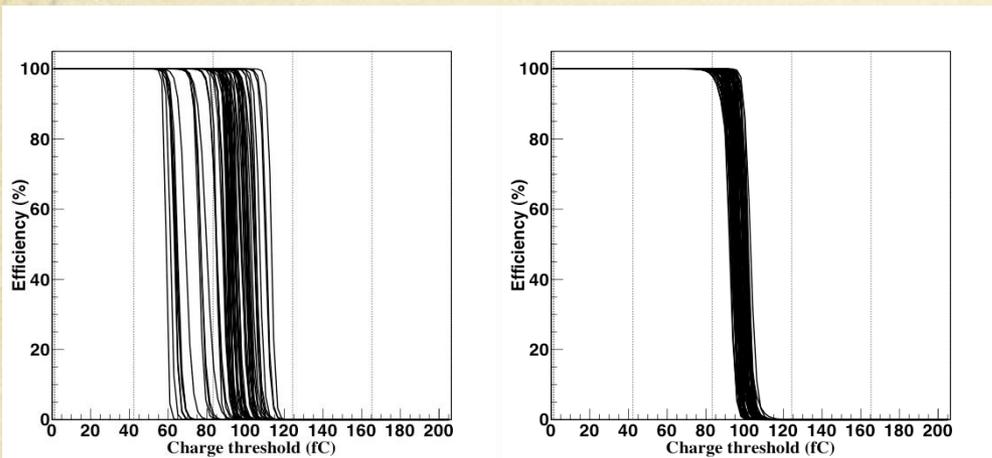
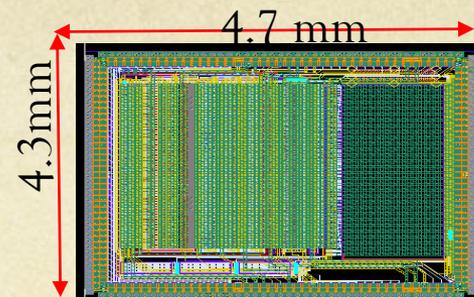
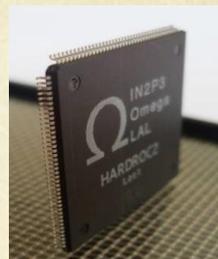
64 channels, trigger less mode, memory depth: 127 events

2-bit readout : 3 thresholds

Dynamic range: 10 fC-15 pC

Gain correction → uniformity

Power-pulsed → reduced power consumption



Printed Circuit Boards (PCB) were designed to reduce the x-talk with 8-layer structure and buried vias.

Tiny connectors were used to connect the PCB two by two (the 24X2 ASIC are daisy-chained).

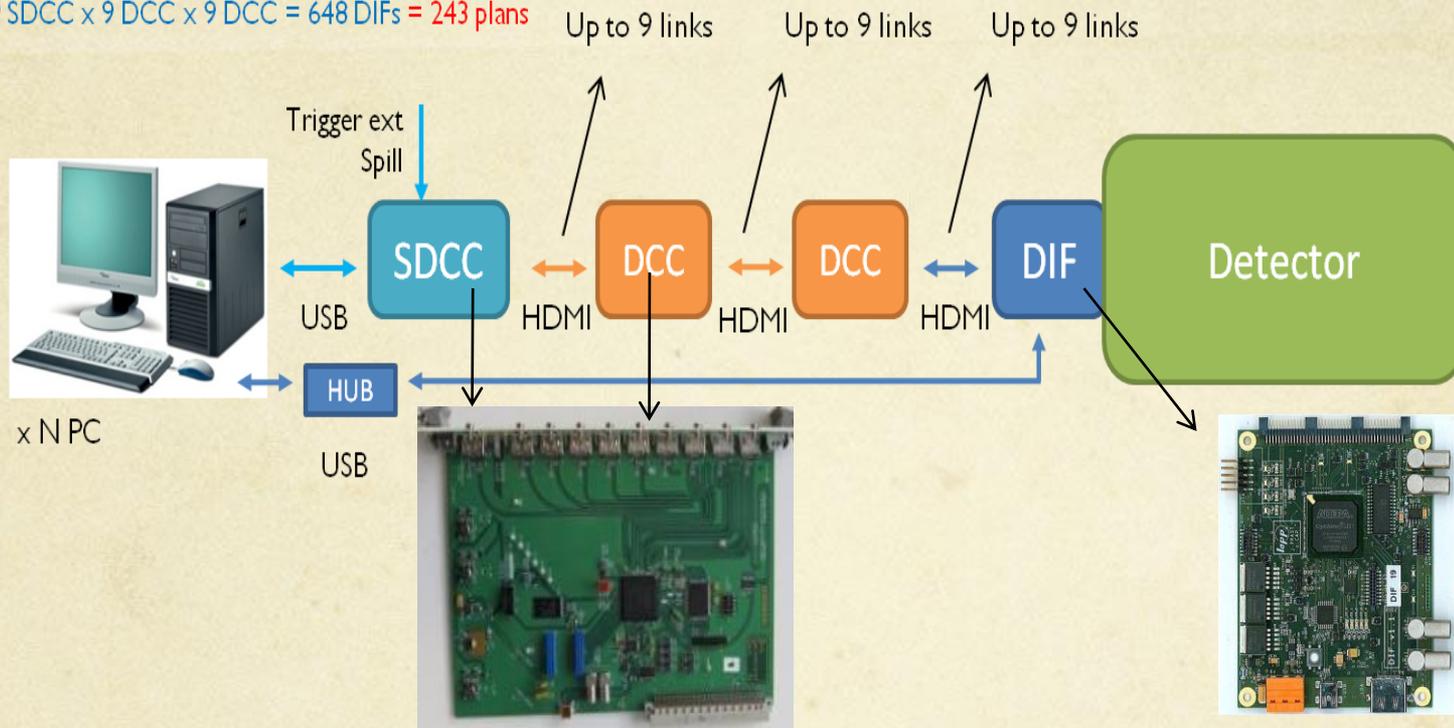
DAQ board (DIF) was developed to transmit fast commands and data to/from ASICs.



# SDHCAL acquisition system

9 SDCC x 9 DCC = 81 DIFs = 27 plans

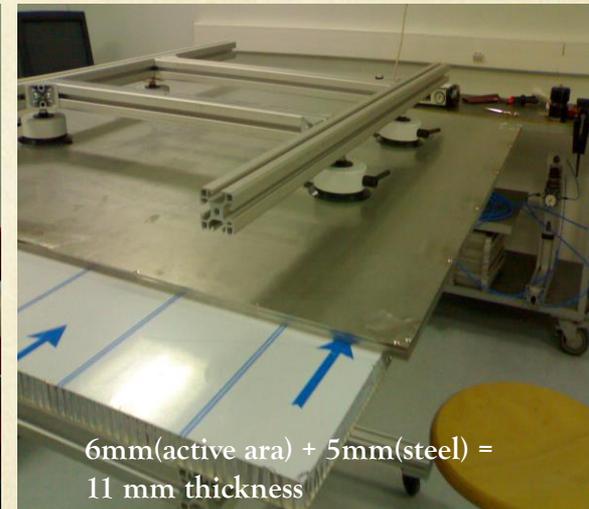
9 SDCC x 9 DCC x 9 DCC = 648 DIFs = 243 plans



- Acquisition software was developed to deal with the output of large number of electronics channels (> 460 000).
- Oracle database used for ASIC configurations and slow control.
- CMS Xdaq used to provide the DAQ framework.

# Cassette development

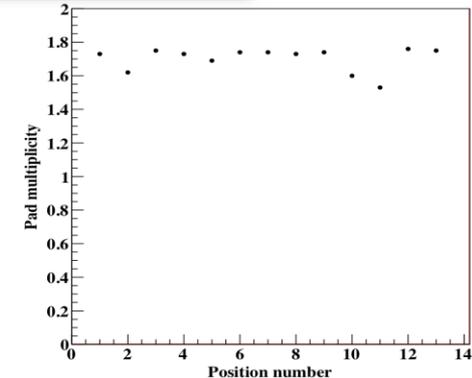
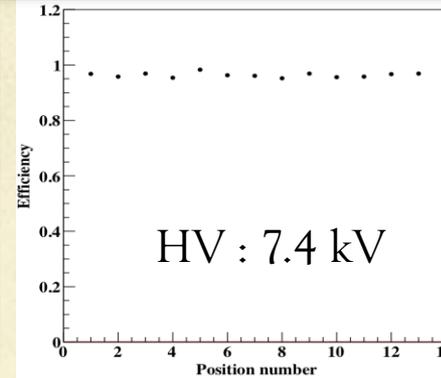
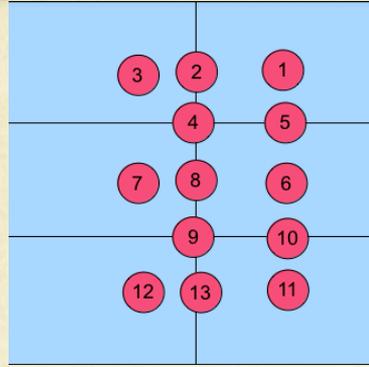
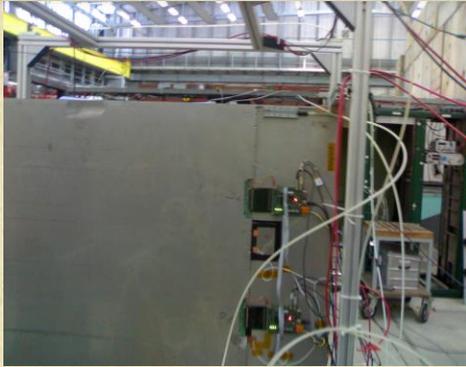
- To provide a robust structure.
- To maintain good contact between the readout electronics and the GRPC.
- To be part of the absorber.
- It allows to replace detectors and electronics boards easily.



The cassettes are built of no-magnetic stainless steel walls 2.5 mm thick each → Total cassette thickness = 6mm (active layer)+5 mm (steel) = 11 mm

# Test Beam validation

The homogeneity of the detector and its readout electronics were studied



Beam spot position

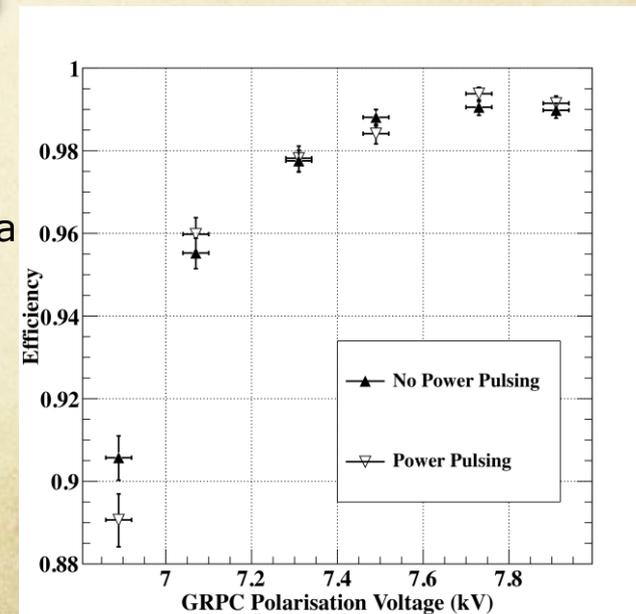
Efficiency

Multiplicity

Power-Pulsing mode was tested in a magnetic field of 3 Tesla



The Power-Pulsing mode was applied on a GRPC in a 3 Tesla field at H2-CERN  
**(2 ms every 10 ms)**  
No effect on the detector performance



# SDHCAL prototype construction

- ✓ 10500 ASIC were tested and calibrated using a dedicated robot that was used by CMS (IPNL, OMEGA) (ASICs layout : 93% ).
- ✓ 310 PCBs were produced, cabled and tested (IPNL). They were assembled by sets of six to make 1m<sup>2</sup> ASUs
- ✓ 170 DIF(LAPP), 20 DCC(LLR) were built and tested.
- ✓ 50 detectors were built and assembled with their electronics into cassettes. Cassettes were tested by sets of 6 using a cosmic test bench (IPNL).
- ✓ The mechanical structure was built in CIEMAT.
- ✓ HV, cooling services were built by UCL, Gent.
- ✓ Full assembly took place at CERN.



# Prototype @TB

3 periods of TB in 2012  
( 5 weeks)

→ SDHCAL

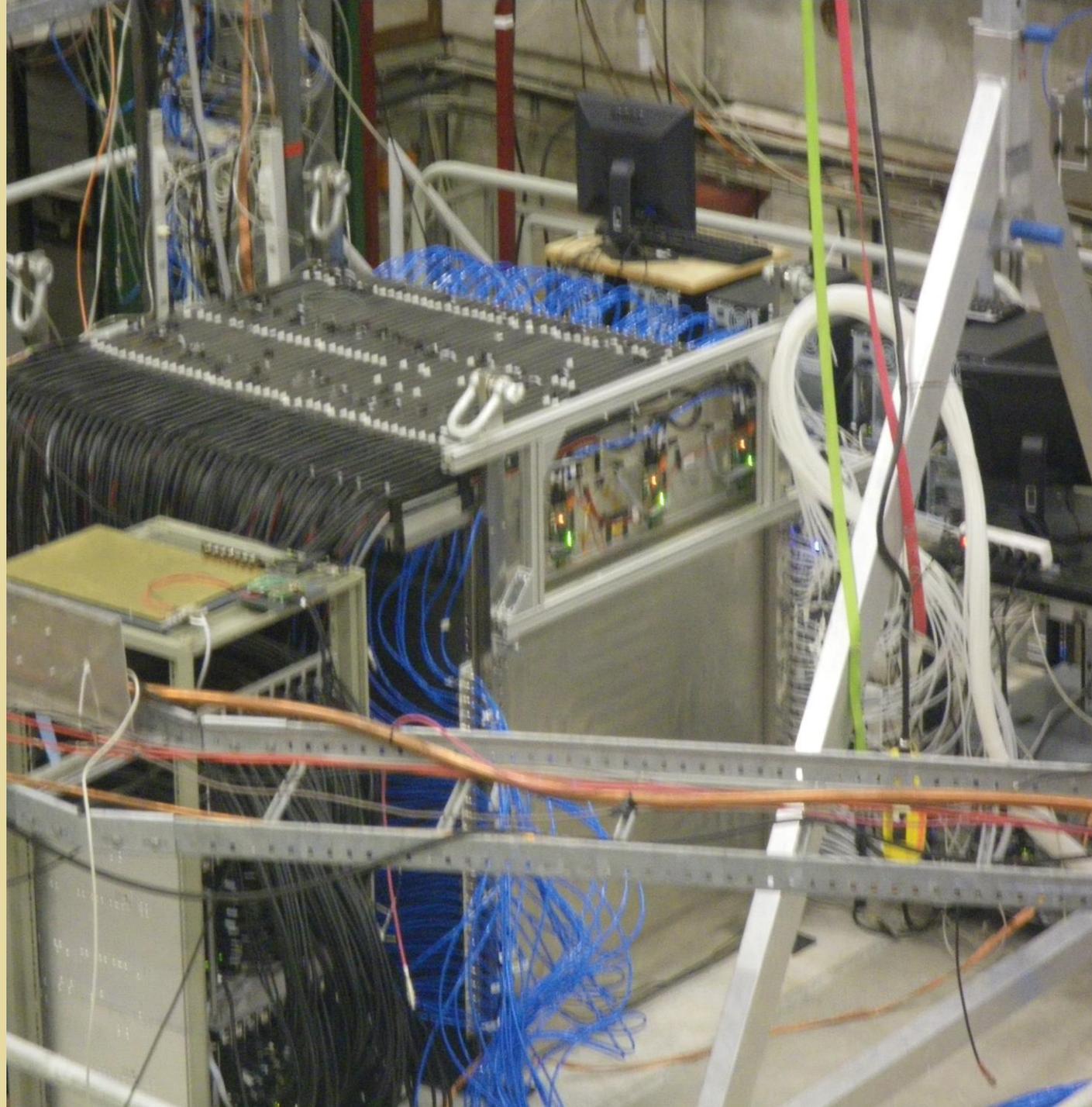
Commissioning with  
TrigerLess, Power-Pulsing  
modes;

→ Thresholds choice  
optimization;

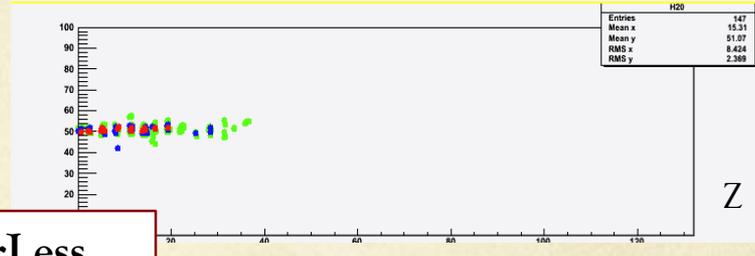
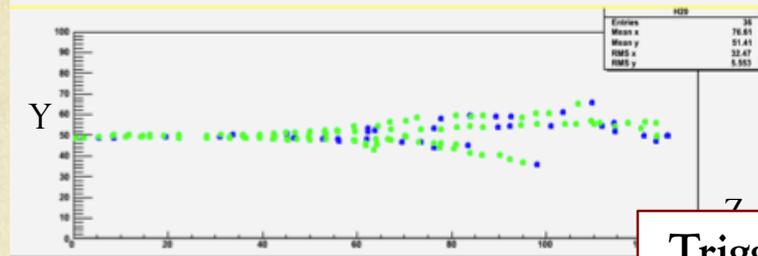
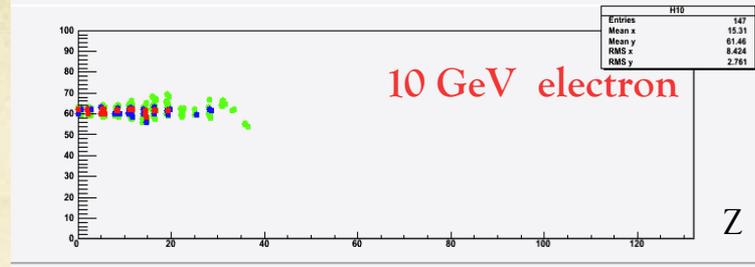
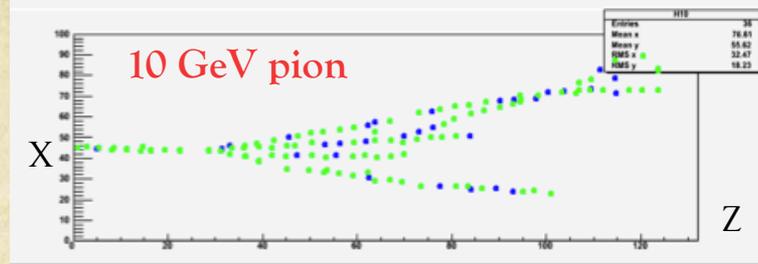
→ Muons run calibration;

→ Pion, electron runs  
to study EM and  
hadronic showers;

→ No particle identification  
detector was used.

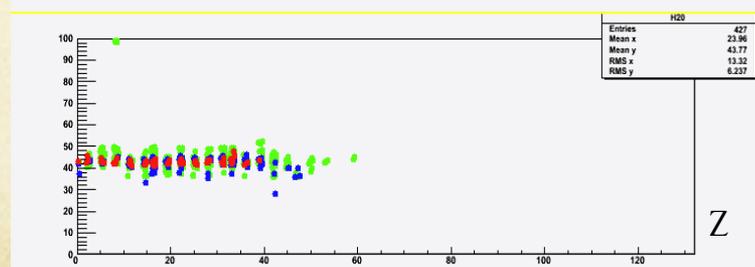
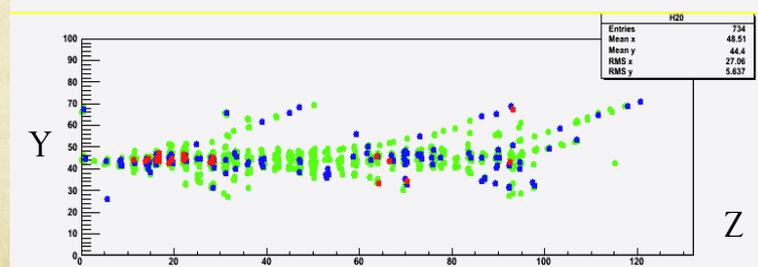
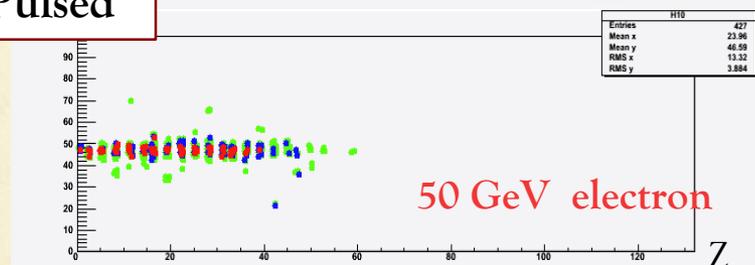
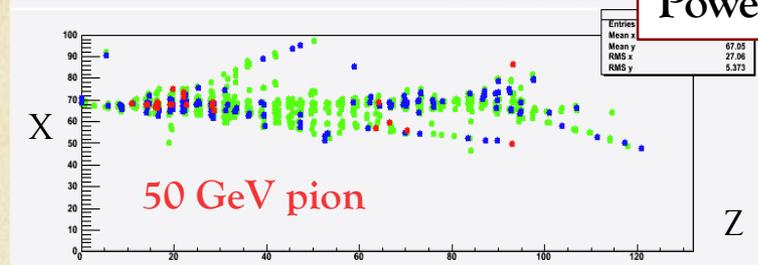


# Event display



# TriggerLess Power-Pulsed

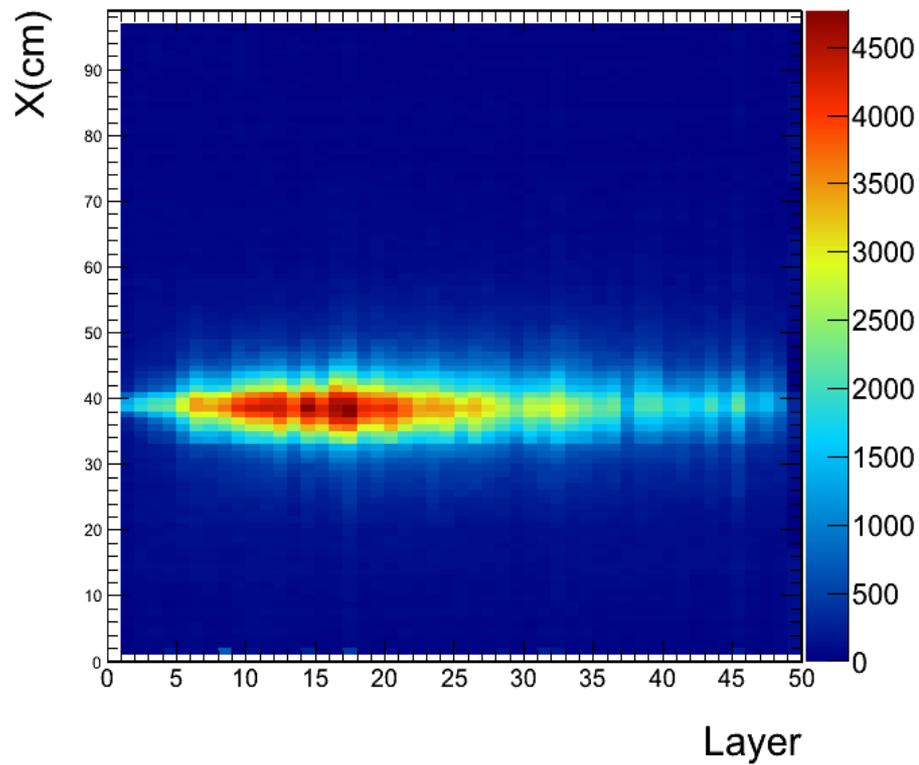
units in cm



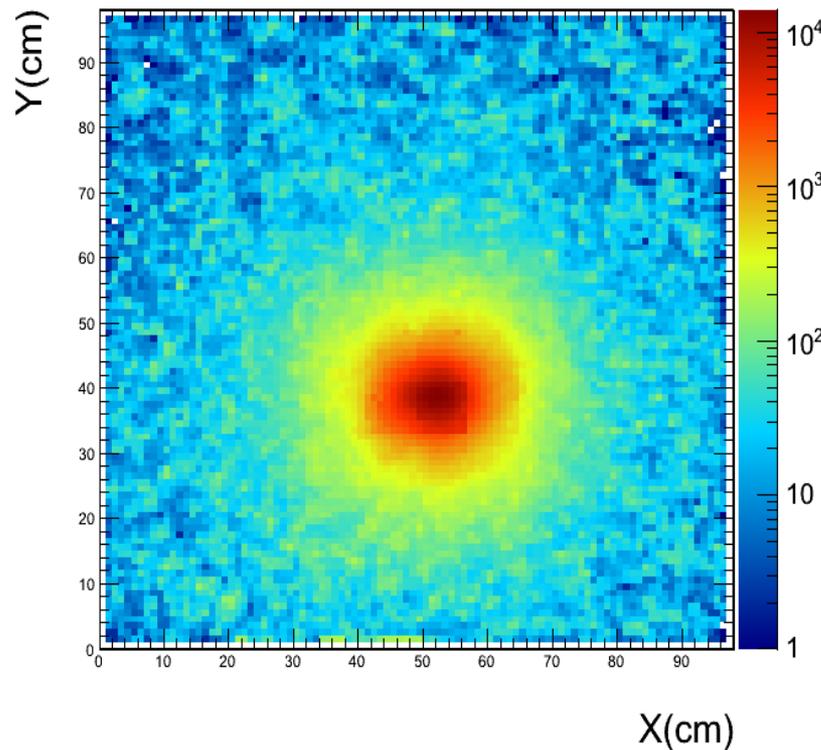
Colours correspond to the three thresholds: Green (100 fC), Blue (5 pC), Red (15 pC)

Raw data, no treatment except time hit clustering

Logitudinal beam profile



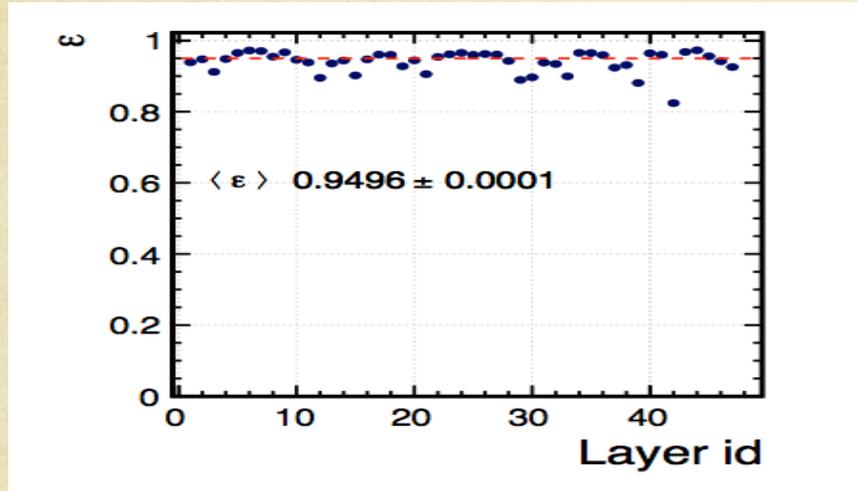
XY Beam Profile 100GeV



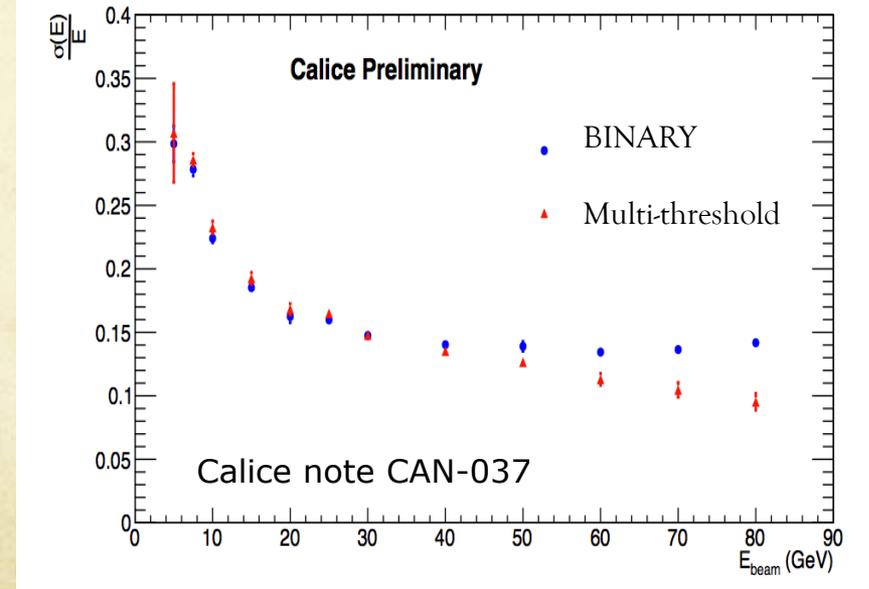
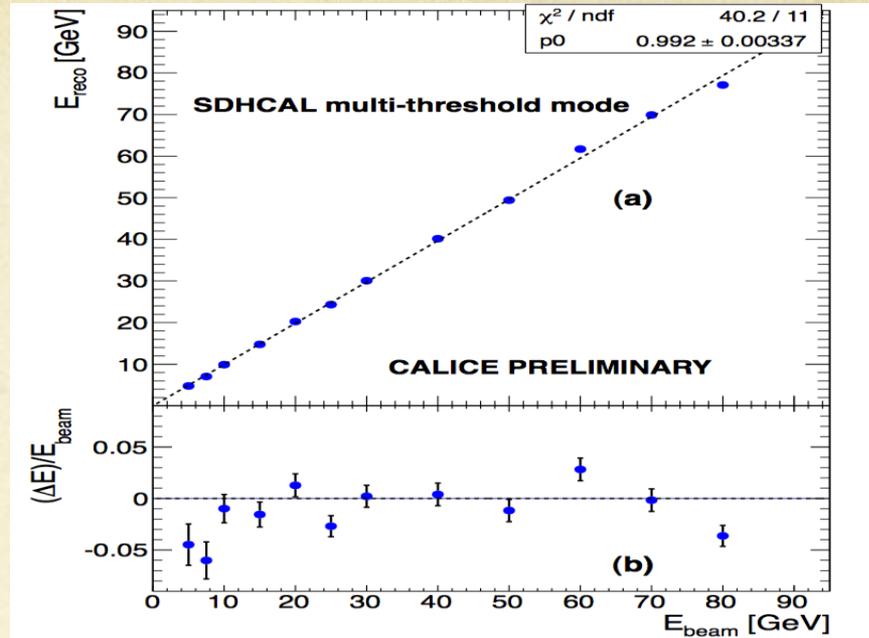
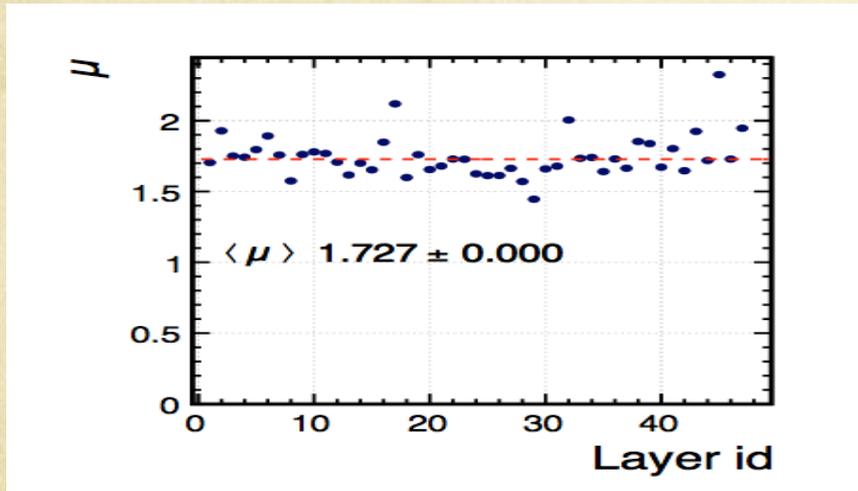
100 GeV pions

# First results on linearity and energy resolution with no calibration and with no gain correction.

## Efficiency



## Pad multiplicity

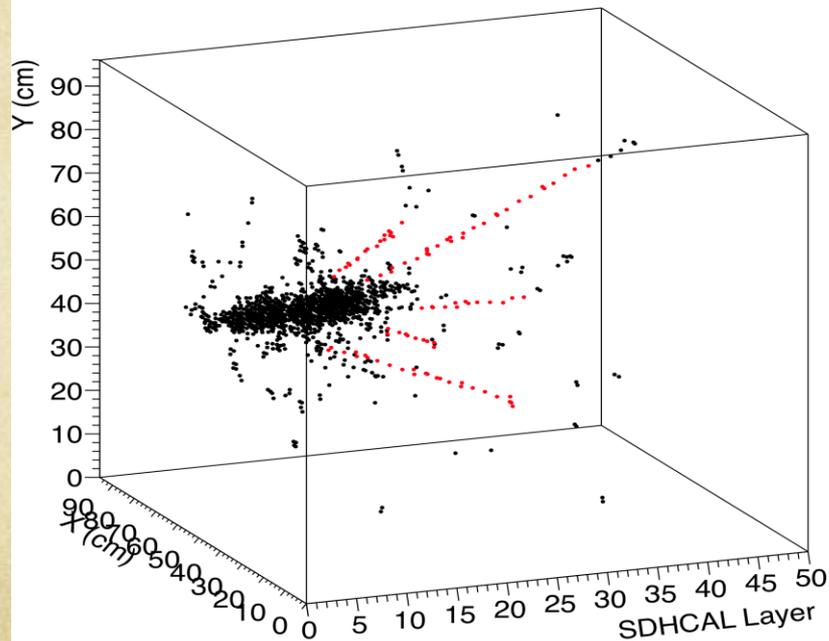


Semi-digital improvement with respect to digital version.

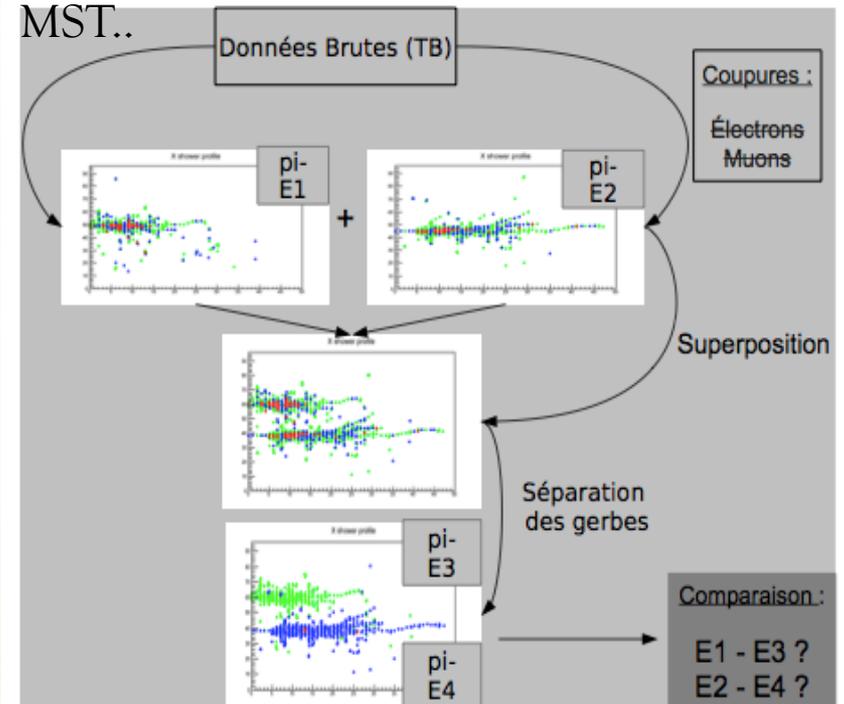
# Ongoing analyses

- Calibration study;
- Electron-Pion separation;
- Energy resolution improvement by taking into account hadronic shower structure and calibration correction: *an improvement of 7-15% already achieved with respect to the preliminary ones obtained immediately after TB;*
- Imaging algorithm developments (HT, Arbor, MST) → PFA

## Hough Transform

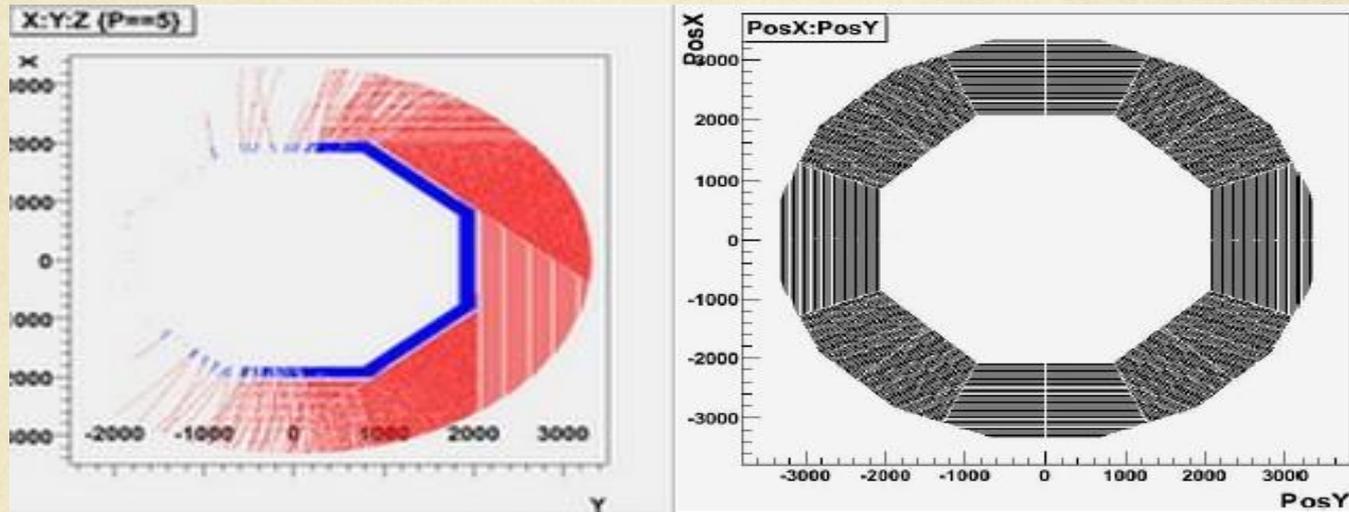


## Arbor, MST..

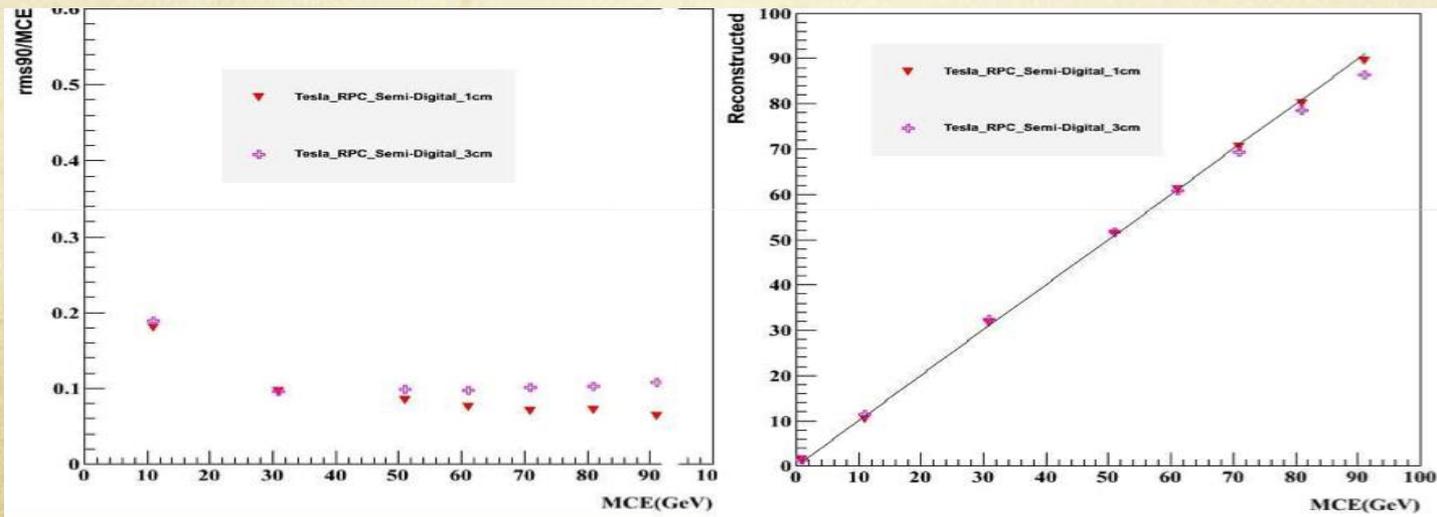


# Simulation and optimization studies

SDHCAL was simulated with two mechanical structures for ILD (V and Tesla)



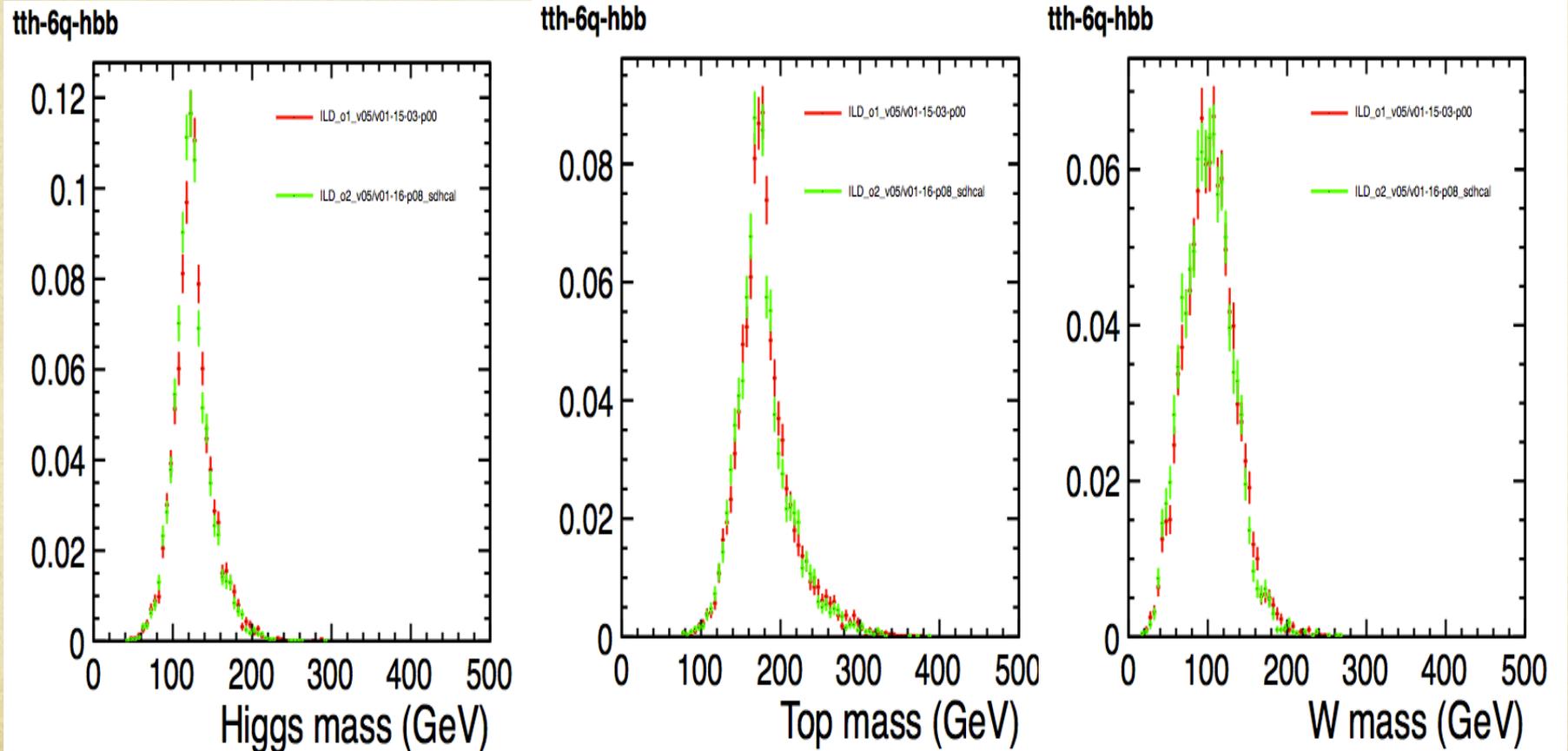
Studies on granularity and readout (binary vs semi-digital) were conducted. They allowed to confirm the SDHCAL choice before to start building the prototype



# Simulation and optimization studies

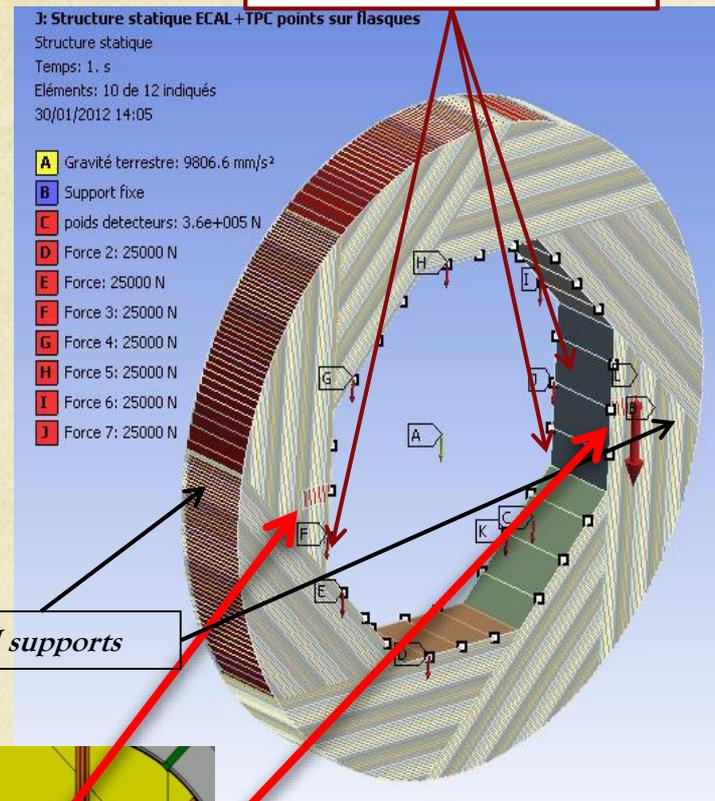
The SDHCAL simulation was re-performed taking into account the constraints and the results of the prototype. The new version was used for the DBD studies, showing that same performance are obtained as for the AHCAL (albeit the PFA optimization was done for the AHCAL topology)

Higgs, top and W in the tth 8jet mode (1000 GeV).



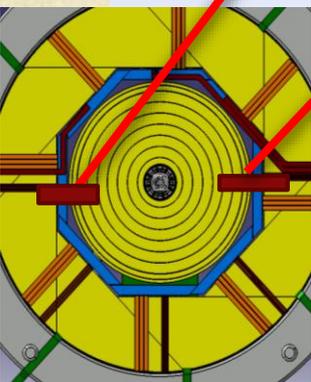
# Mechanical, integration, service studies

*ECAL Loads on points*



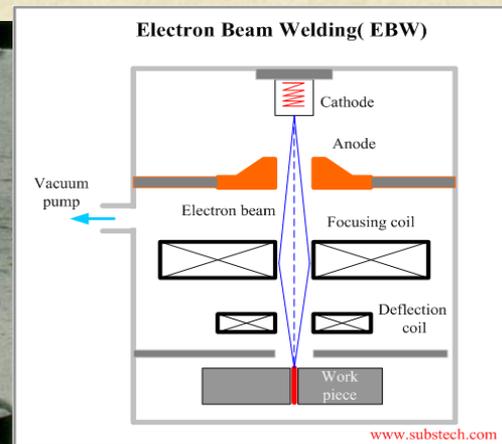
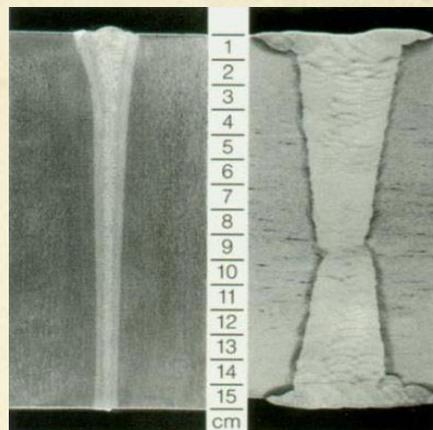
*9-15H supports*

DHCAL with 8 x ECAL modules (8x2.5 t)  
 And TPC (4t)

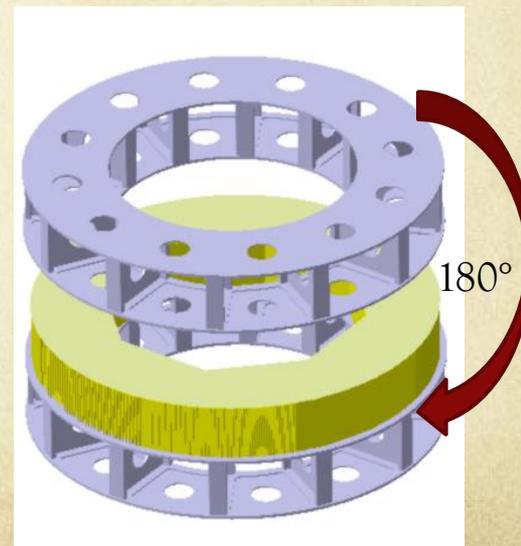
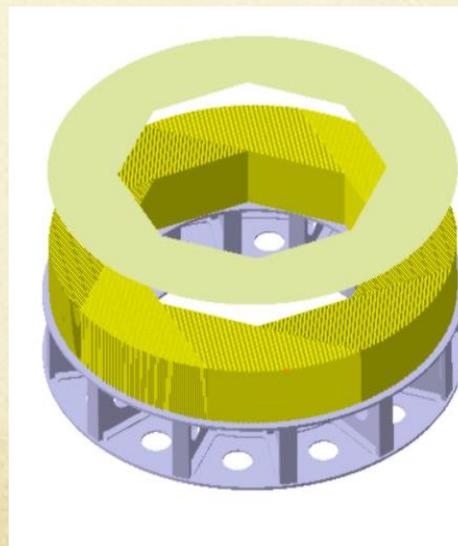


Deformation max SDHCAL + ECAL + TPC = 0,4 mm

## Welding techniques

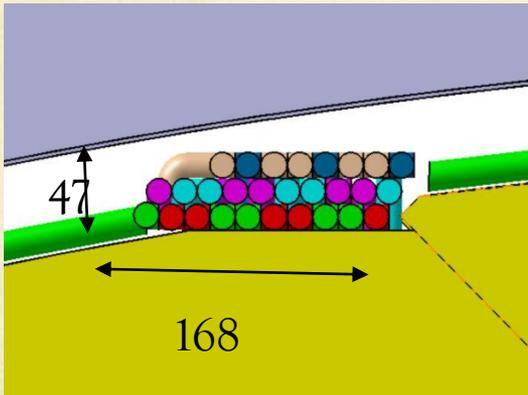
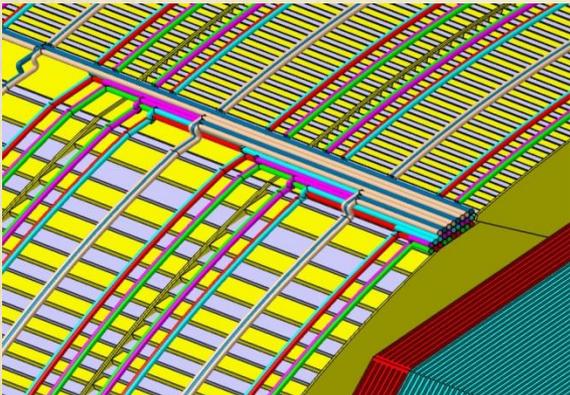
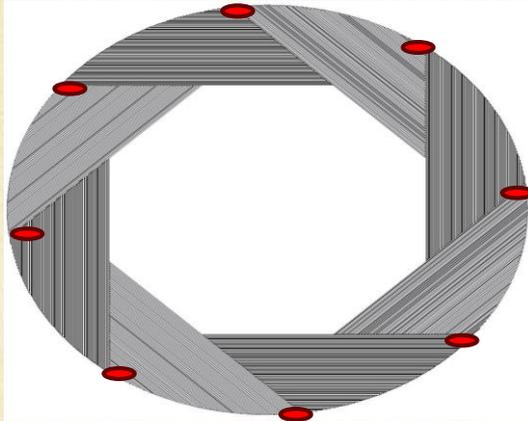
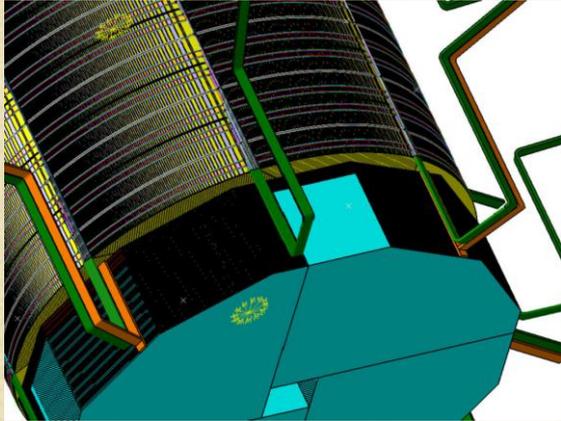


## Building scenarios

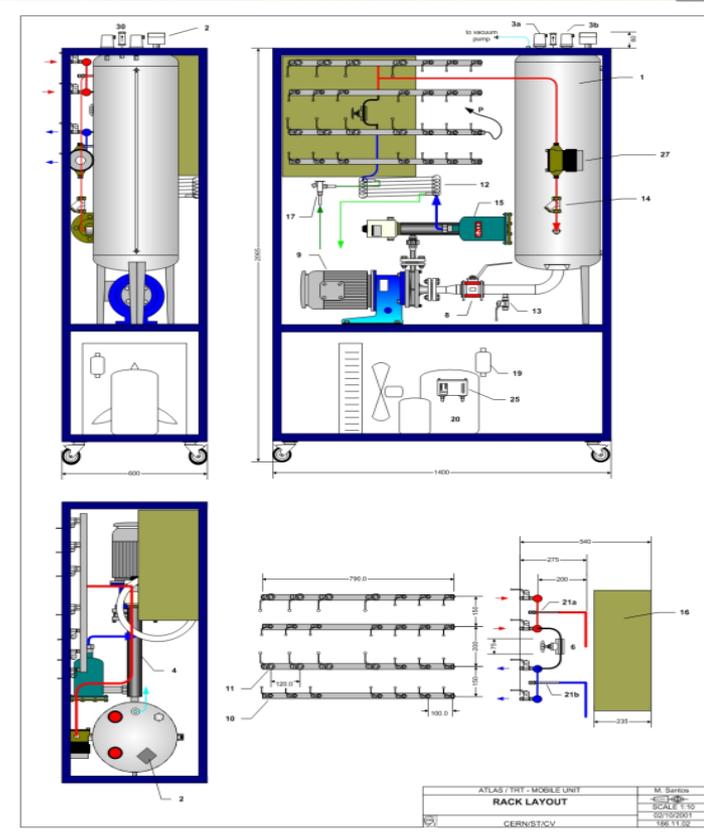


# Mechanical, integration, service studies

Services were studied in detail to provide a realistic model for the ILC DBD



Few cooling scenarios were studied and compared with each other

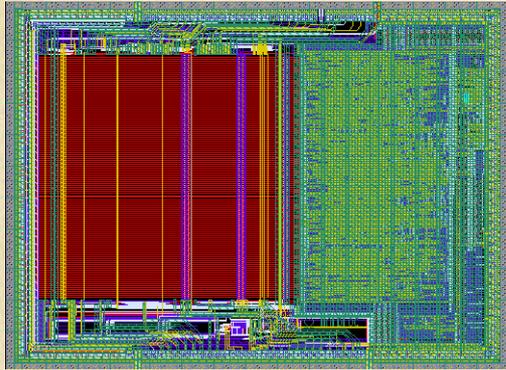


**Mono-phasic gas** like  $C_6F_{14}$  :  
limited effect in case of leak, good  
quality/price ratio, adapted to low  
heat extract, simple to use

# Road map in the 2-3 coming years

- Improve on the energy reconstruction using new techniques;
  - Improve on simulation (digitizer) and compare hadronic shower models to data;
  - Develop PFA techniques to be used to separate close-by hadronic showers;
  - Complete TB (ECAL+SDHCAL+...);
  - Publish results;
- //////// // //////////
- Build few very large GRPC detectors (2-3 m<sup>2</sup>) : gas circulation system, thickness...;
  - Test the new version of electronics (I2C, roll mode..) ;
  - Design a new ASU capable to read the large GRPC (up to 3 m<sup>2</sup>);
  - Develop a new DIF ( low consumption, reduced size, new functionalities);
  - Build a small mechanical prototype to host the few large chambers and test it.

## New version of the readout electronics



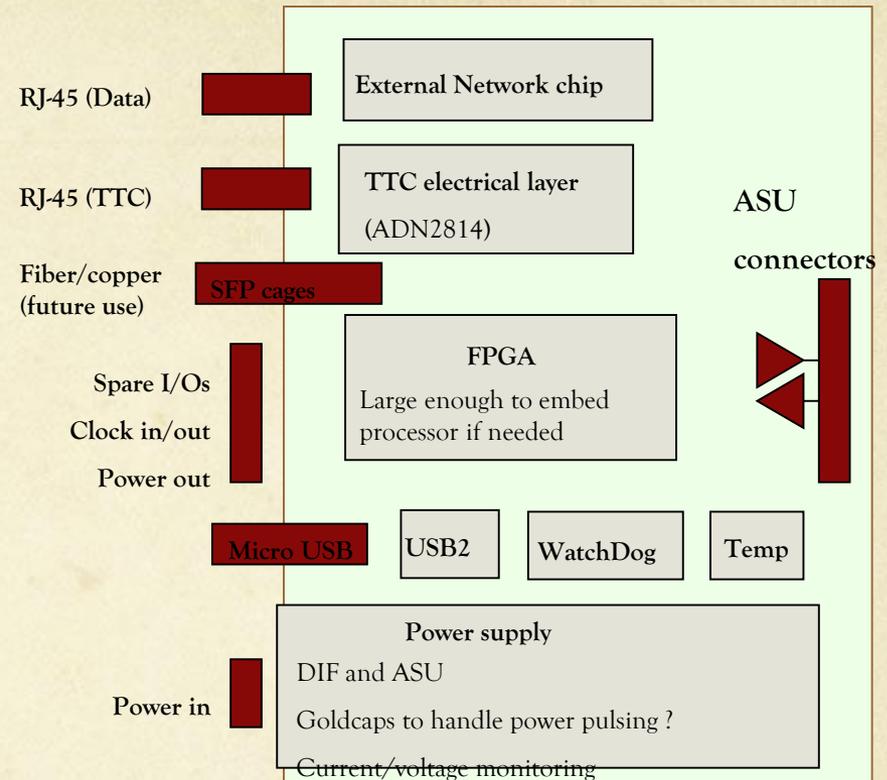
The new version improves on the previous one:

- Independent channels and zero suppression
- Independent ASICs (I2C)
- Better dynamic range (up to 50 pC).
- successfully tested;
- 

This activity is funded essentially by **AIDA**

New ASU design for large detectors under study

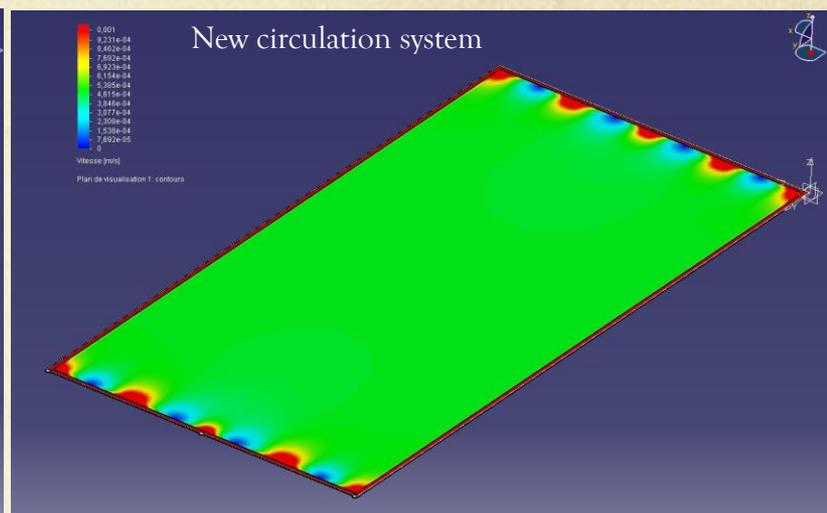
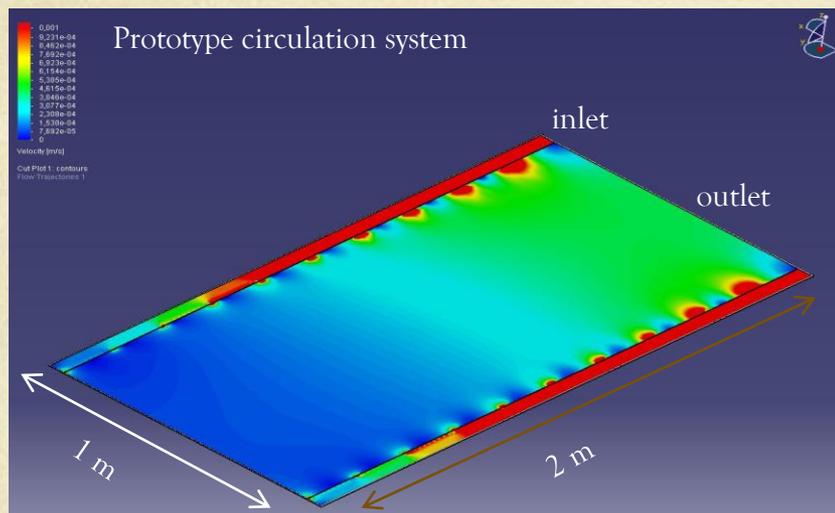
## New features in the DAQ boards



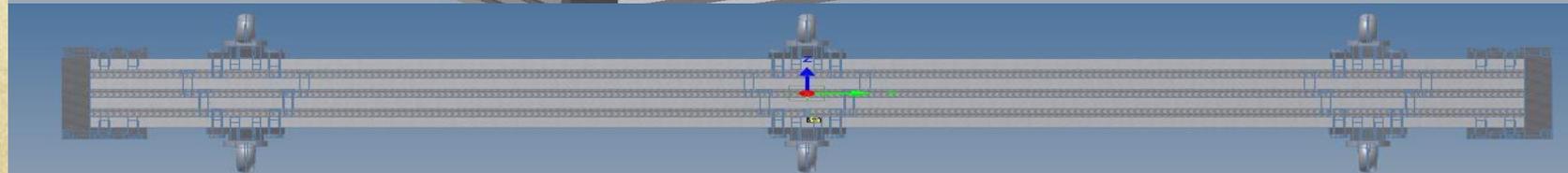
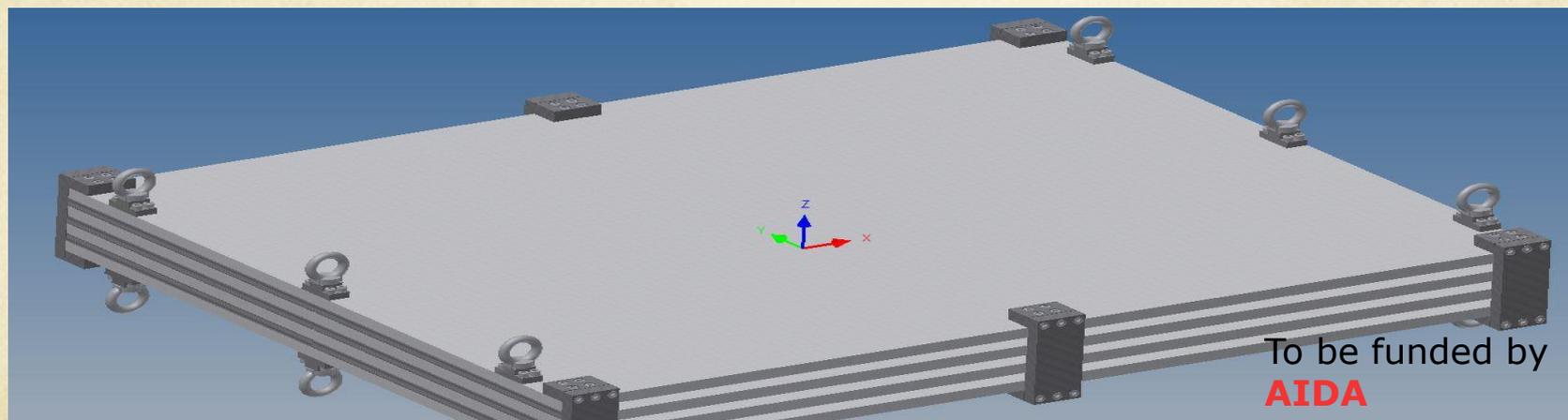
- Only one DIF per plane. For the maximum length plane (1x3m) the DIF will handle 432 HR3 chips;
- Slow control through the new HR3 I2C bus;
- Data transmission to DAQ by Ethernet using commercial switches for concentration;
- Clock and synchronization by TTC;

Synergy with R&D on fast links R&D of LHC (GBT)  
Funded essentially by **CIEMAT**

**Detector improvement** : to achieve same performances with very large GRPCs



**Mechanical structure** : to be built with EBW techniques and to host few large detectors GRPCs



# Conclusion and prospects

- The SDHCAL prototype is the first and up-to-now unique **technological** calorimeter prototype. Its success proves that SDHCAL is a serious option for ILD;
- SDHCAL with its fine granularity is an excellent tool to develop and exploit PFA algorithms;
- The expertise accumulated during the conception, construction and commissioning is very precious for physicists and technical staff in our labs;
- The SDHCAL project is an excellent environment for students;
- Few papers already published but more are being in preparation;
- The project has led to several spin-offs (TOMUVOL, CMS,..);
- We still need support from the IN2P3 to exploit the already collected SDHCAL data and the ones we intend to have with the ECAL. We need also to finish the R&D (very large detectors) to completely validate the SDHCAL option.

Backup slides

# Articles

Published :

-Performance of Glass Resistive Plate Chambers for a high granularity semi-digital calorimeter, Bedjidian et al, 2011\_JINST\_6\_P02001.

-Construction of technological semi-digital hadronic prototype using GRPC, Laktineh I., Journal of Physics Conference Series, volume 293, A.N. 012077, 2011.

-First test of a power-pulsed electronics system on a GRPC detector in a 3-Tesla magnetic field, Caponetto et al, 2012\_JINST\_7\_P04009.

In preparation :

-Large GRPC detector for the future ILC SDHCAL hadronic calorimeter.

-

-Construction and commissioning of the SDHCAL technological hadronic calorimeter.

Calice notes :

-First results of the SDHCAL technological prototype and its addendum (CAN-037).

-Tracking within Hadronic Showers in the SDHCAL prototype using Hough Transform Technique (CAN-047).

# Detector

## Resistive coatings :

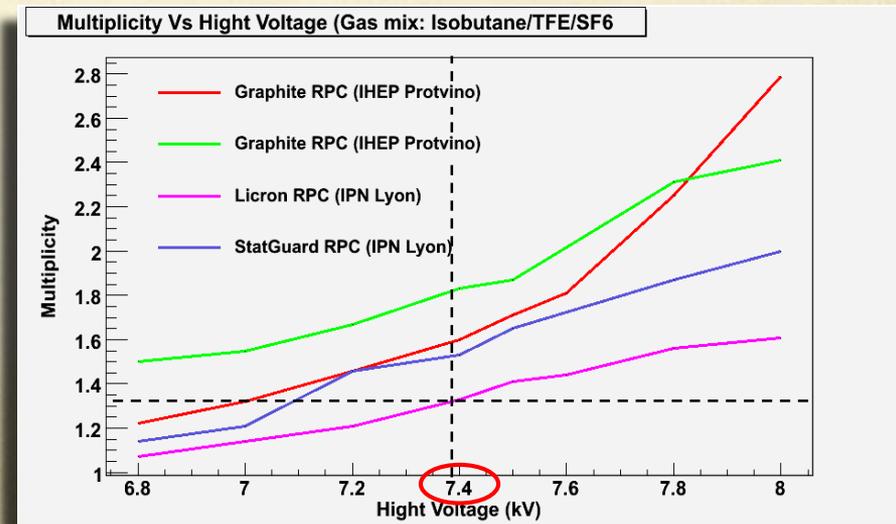
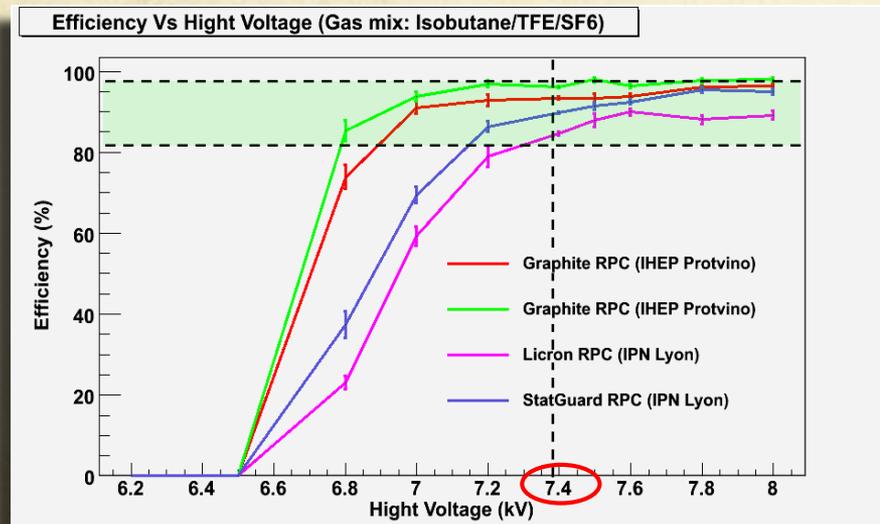
Following detailed study on the effect of resistive coating on pads multiplicity realized using small GRPC in TestBeam conditions it appeared that the higher the resistivity of the coating the lower the pads multiplicity (see figure). This is of big importance to improve on tracking capability.

Many kinds of coatings were tested on large GRPC and different painting techniques were tried in order to ensure the best homogeneity. Some paintings like the Licron® were dropped due to long term stability of high voltage connection.

gas

Beam

Beam



# Detector

## Painting technique

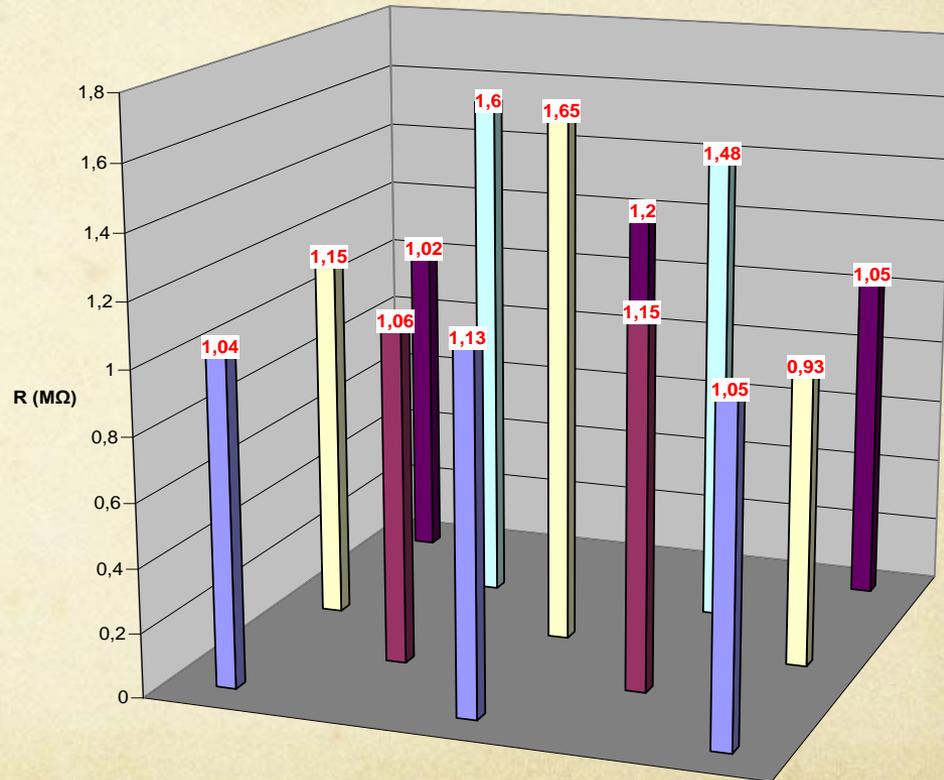
Different techniques were tested and finally the silk screen print one is adopted. It provides **homogenous** and well controlled coating. Simple tools are needed. First tests were done manually. Painting of 20 large glass plates was then performed successfully in a semi-automatic way.



# Detector

## Painting techniques

The measured resistivity on the 20 plates using semi-automatic Silk screen print machine show very nice homogeneity.



$$R_{\text{MAX}}/R_{\text{MIN}} < 2$$

over 1 m<sup>2</sup> surface

# Readout Electronics : ASIC : HR2

64-Channel

Dynamic range

- Gain correct.: 8 bits  
G=0 to 255 (analog G=0 to 2)
- 3 shapers, different Rf,Cf and gains:  
Fsb1, G= 1/2,1/4,1/8,1/16  
Fsb2, G= 1/8,1/16,1/32,1/64
- 3 thresholds (=> 3 DACs):  
100fC, 1pC, 10pC (GRPC)

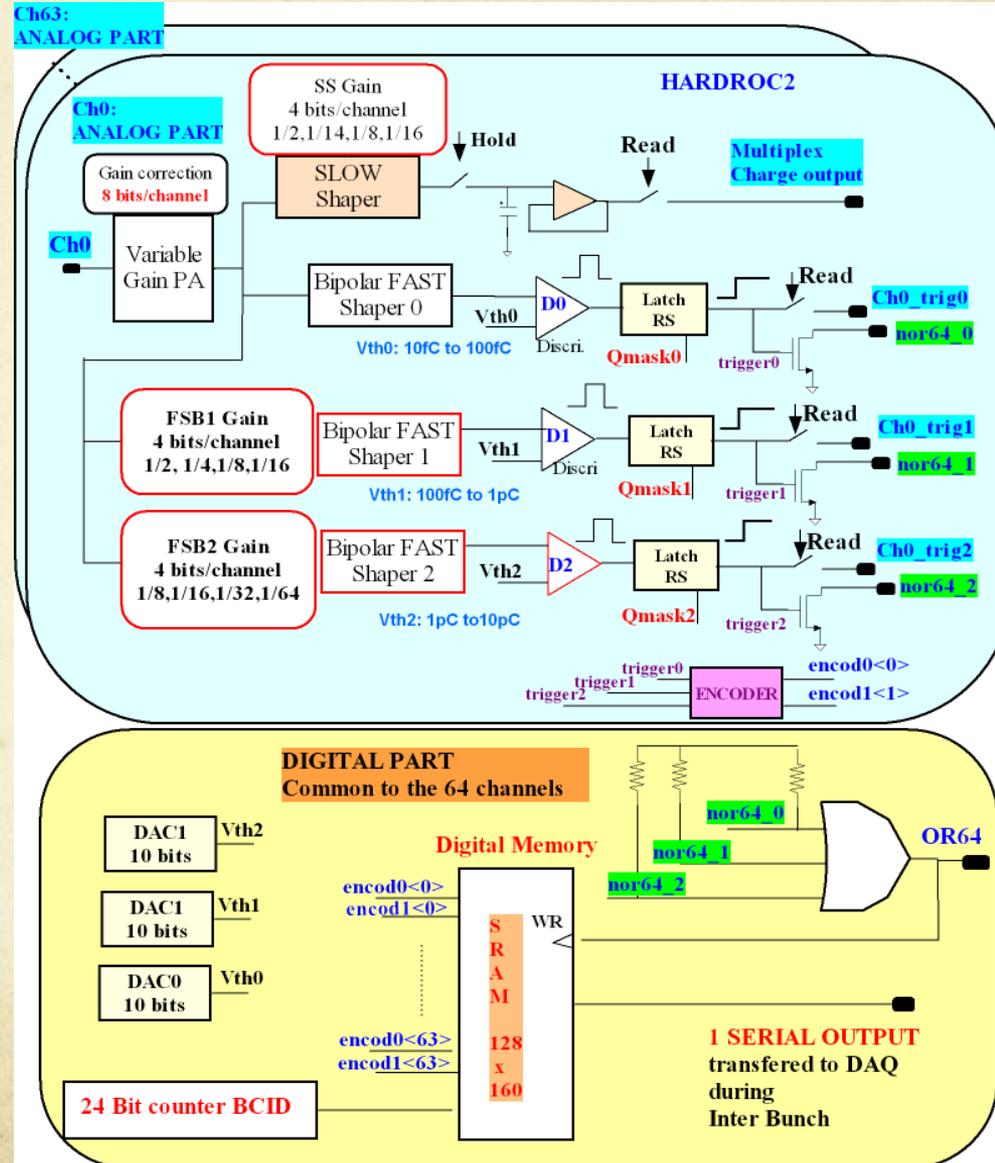
128 memory depth

Mask

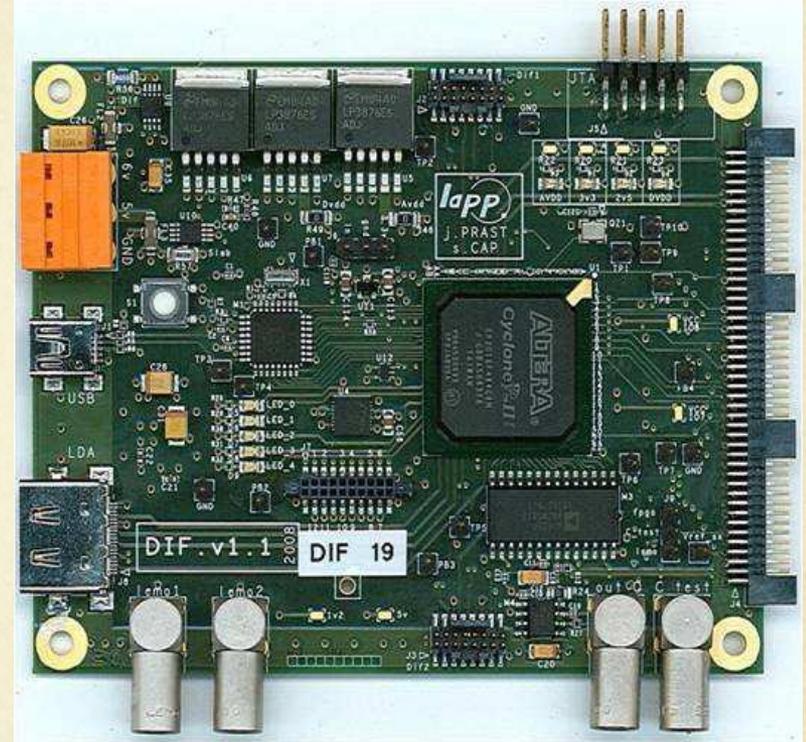
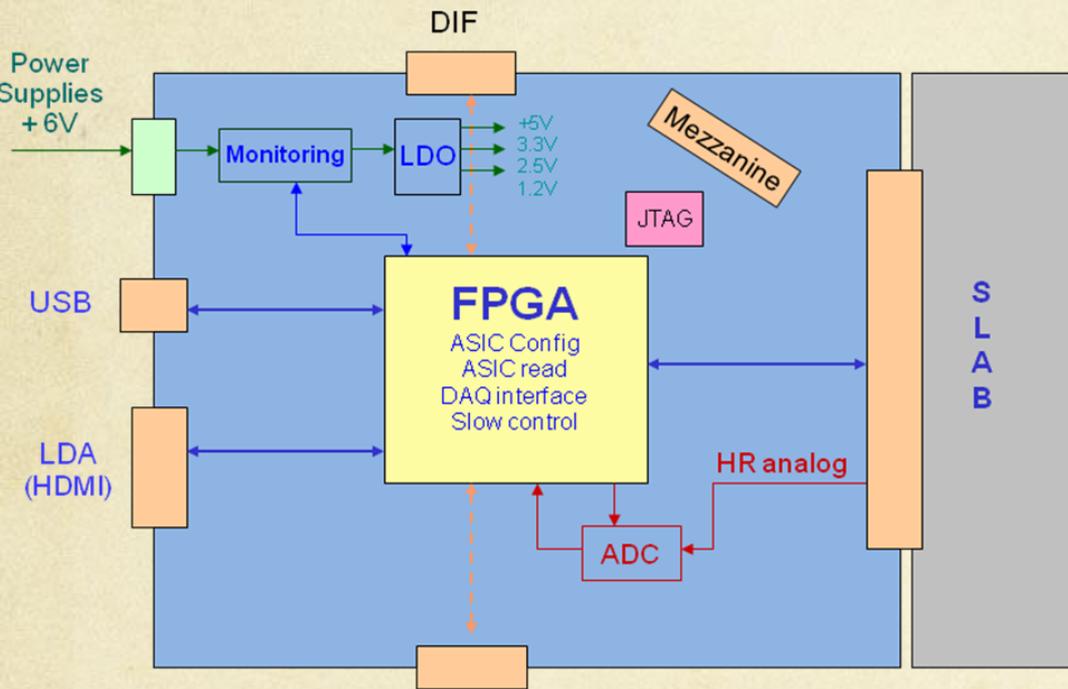
872 SC registers, default config

Power pulsing:

- Bandgap +ref Voltages + master I: power pulsed
- POD module (power budget)



# Readout Electronics : DIF



# Readout Electronics : ASU

The Active Sensor Unit (ASU) board hosts the front-end electronics.

To circumvent the fabrication difficulties of the square meter

integrated circuit, the approach of assembling 6 smaller boards has

been taken.

2 ASUs are connected

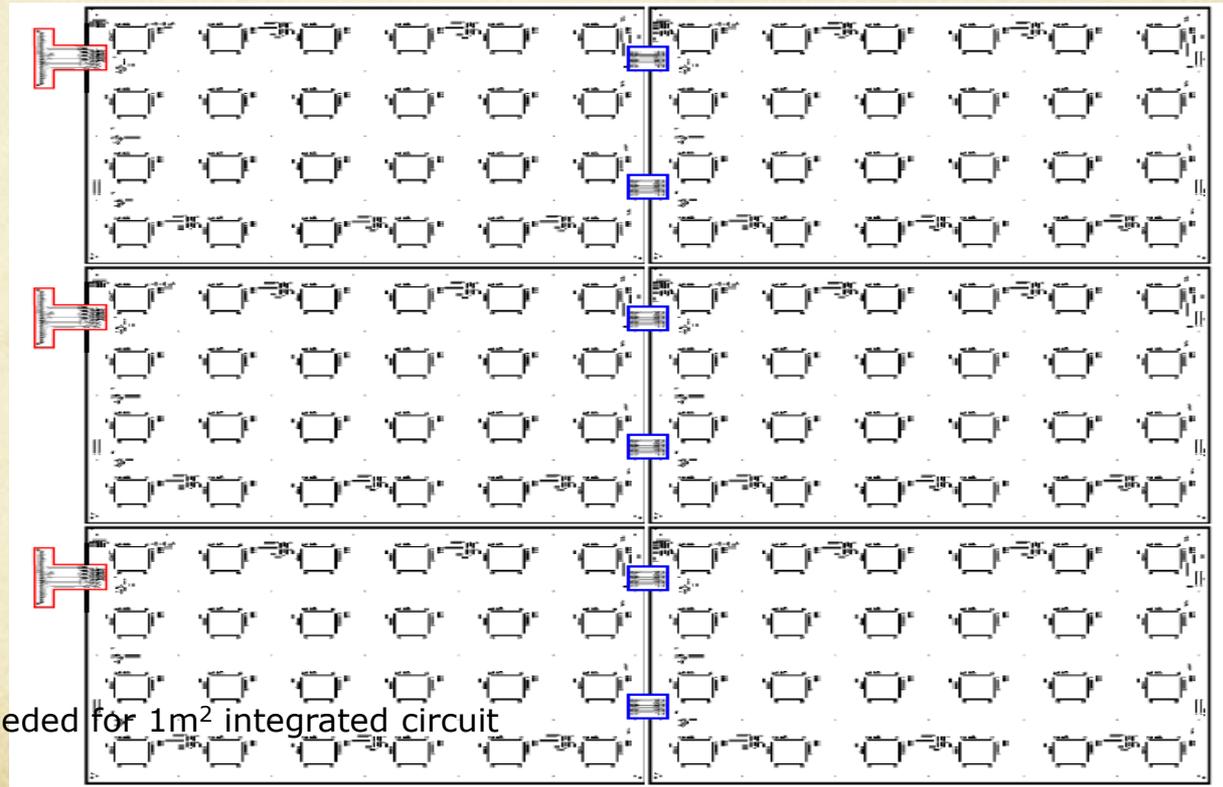
two by two using an

inter-connect to form a

slab. A slab is connected

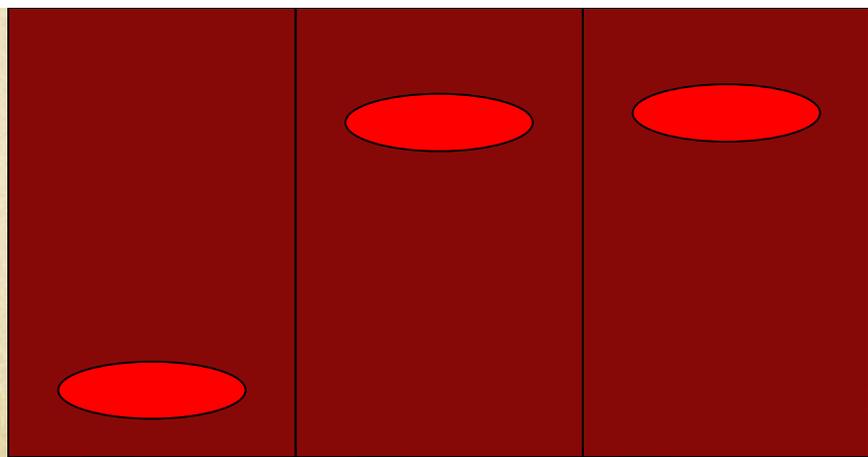
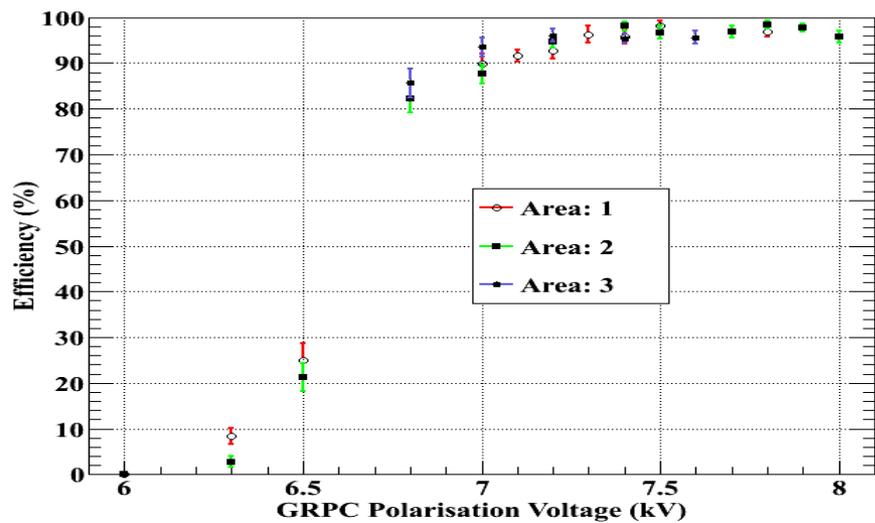
to a DIF using an

Interconnect board 3 DIFs are needed for  $1\text{m}^2$  integrated circuit



# Detector

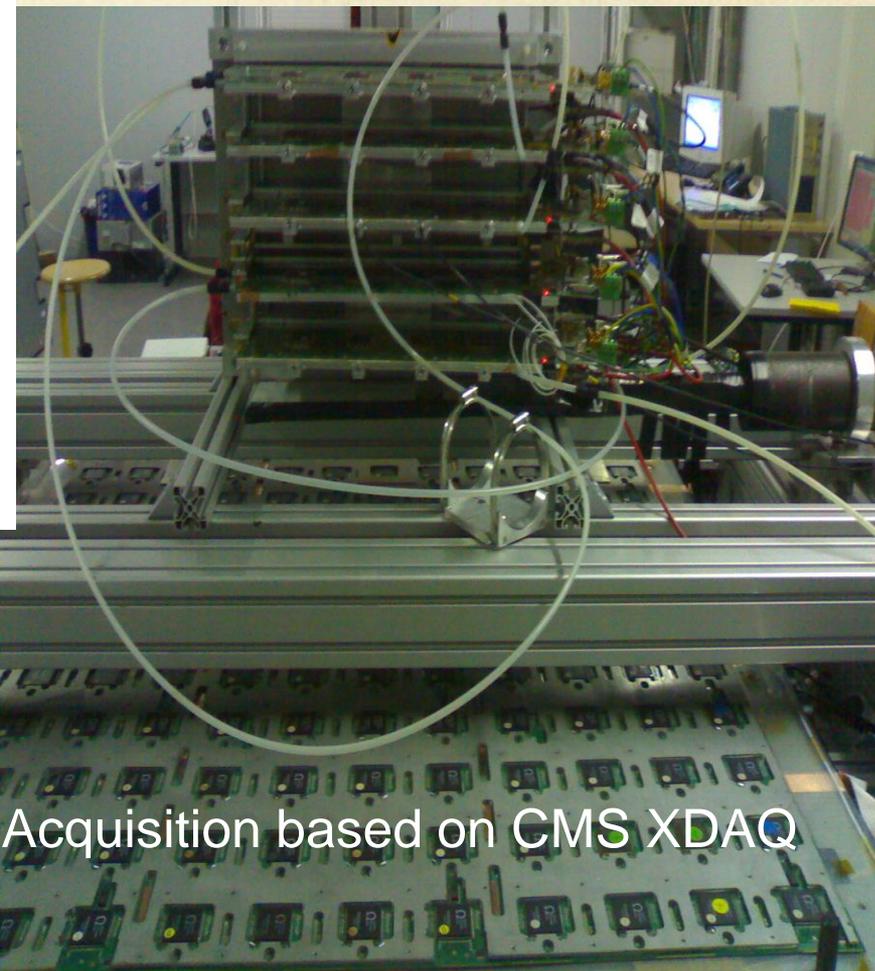
## Homogeneity validation



DIF6

DIF9

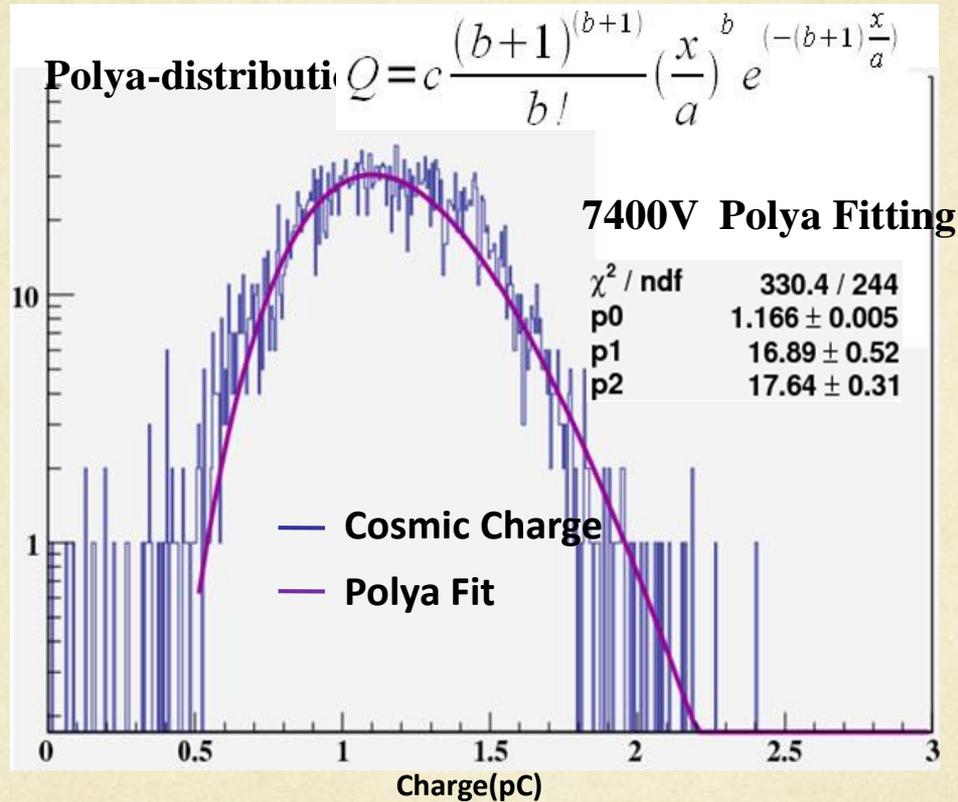
DIF10



# Digitisation

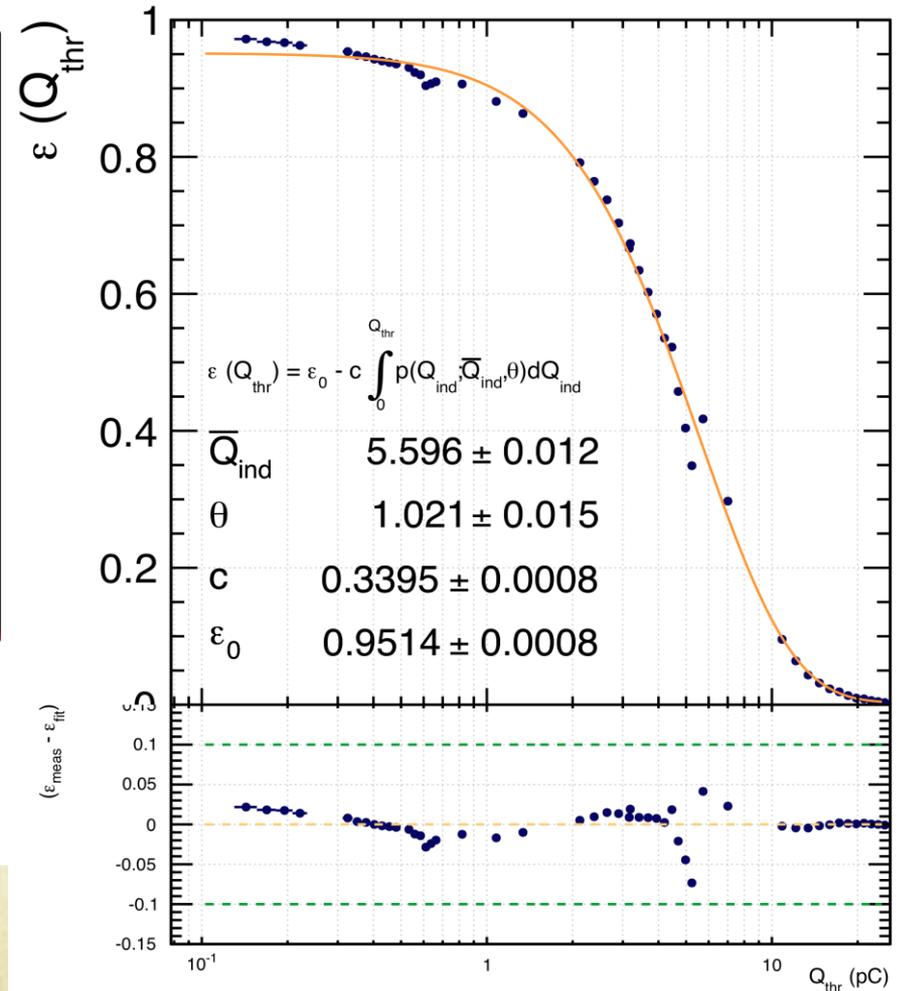
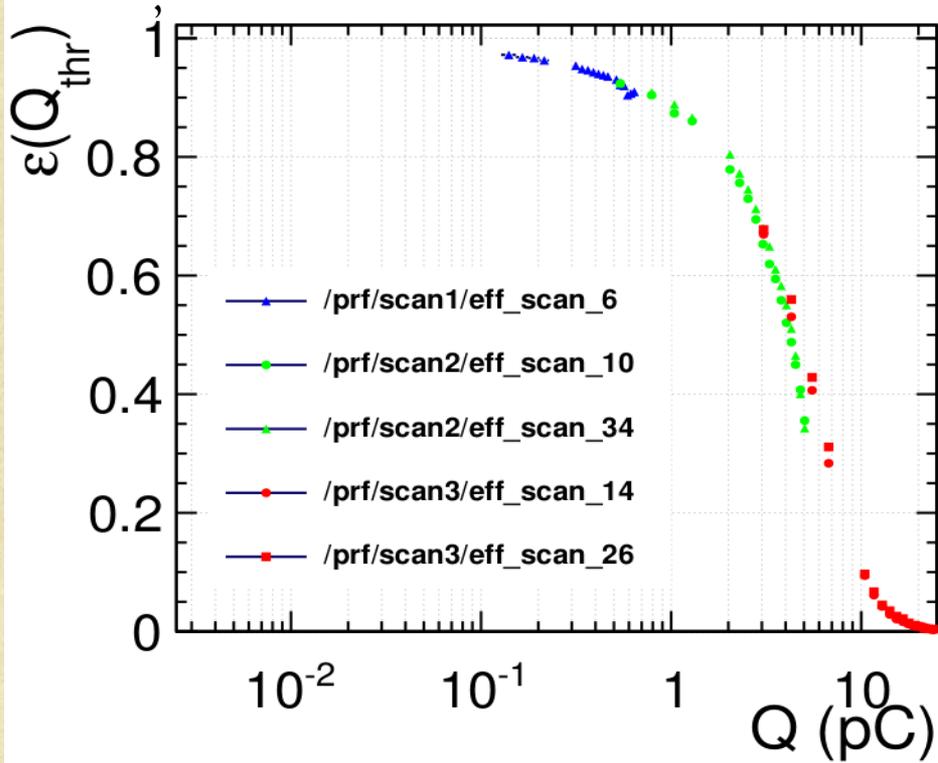
First step:

Measure GRPC analog signal with cosmic muon



Simulation:

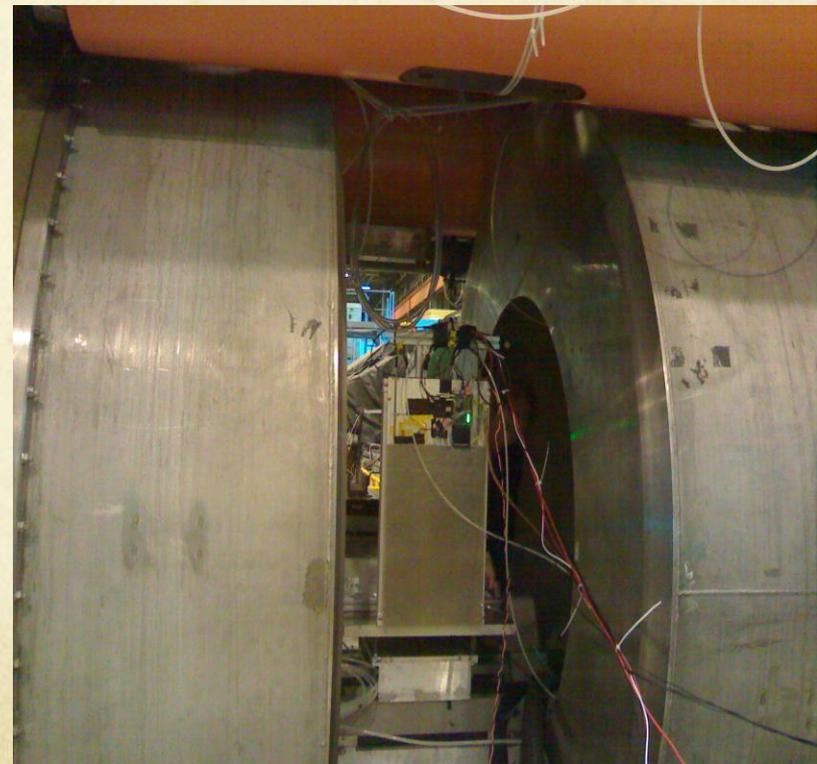
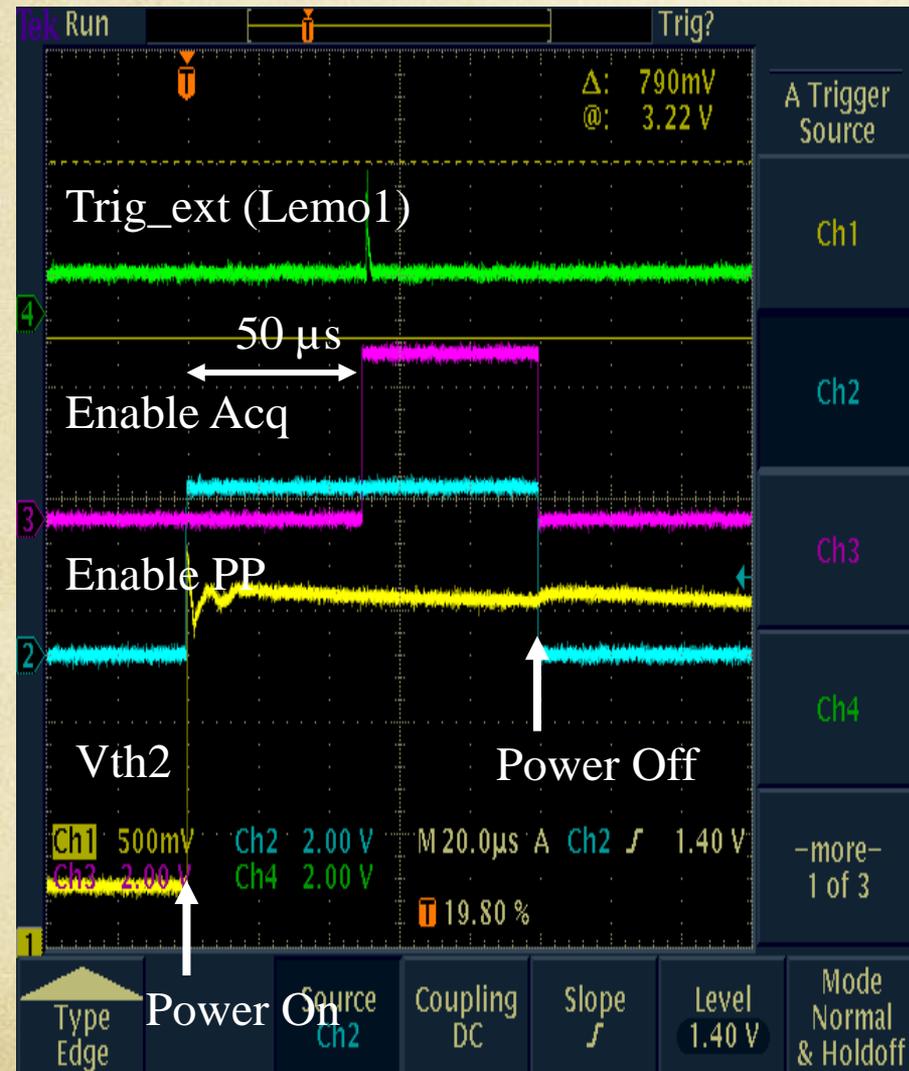
A partir des données expérimentales on peut remonter au spectre de la charge associée au passage des mips dans les GRPC. On peut donc simuler l'effet des seuils et le nombre de hits laissés par une gerbe hadronique.



Plusieurs modèles de gerbes hadroniques sont ensuite simulés dans le SDHCAL et comparés aux données

# Readout Electronics : Power-Pulsing

Power pulsing was successfully tested on a **24-ASIC** electronic board. The board associated to a GRPC was also successfully tested in a **3-Tesla B** field in June (SPS-H2)

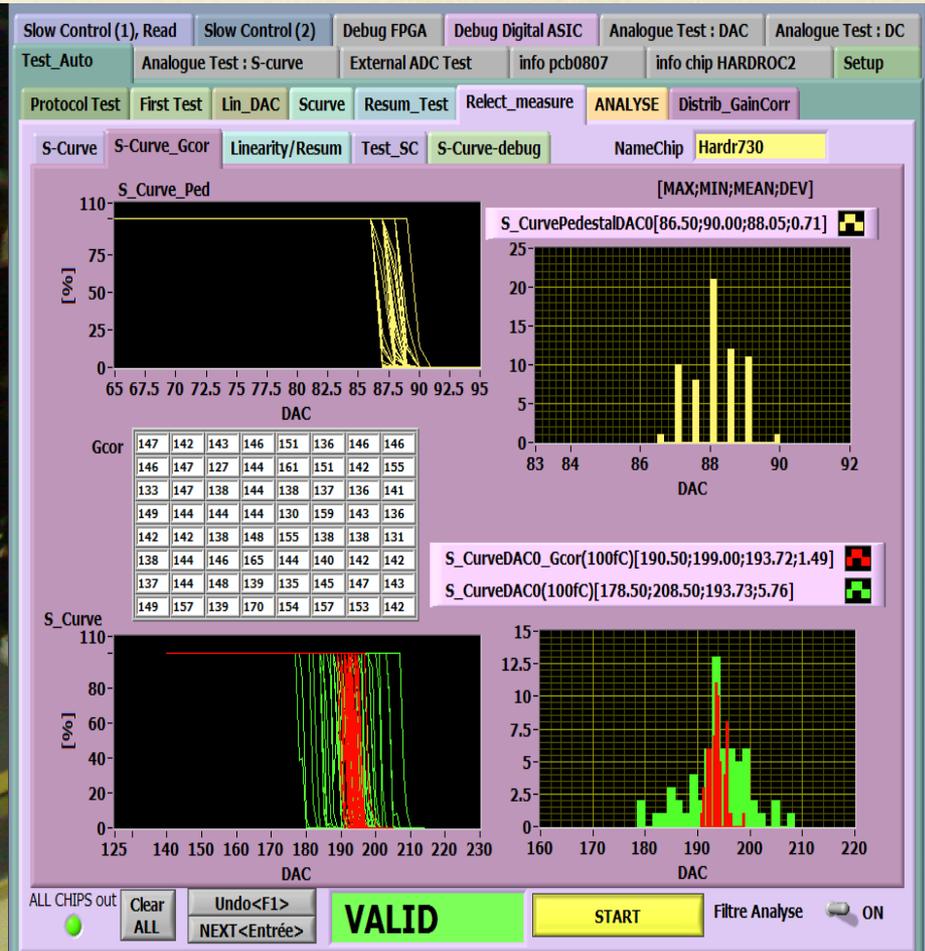
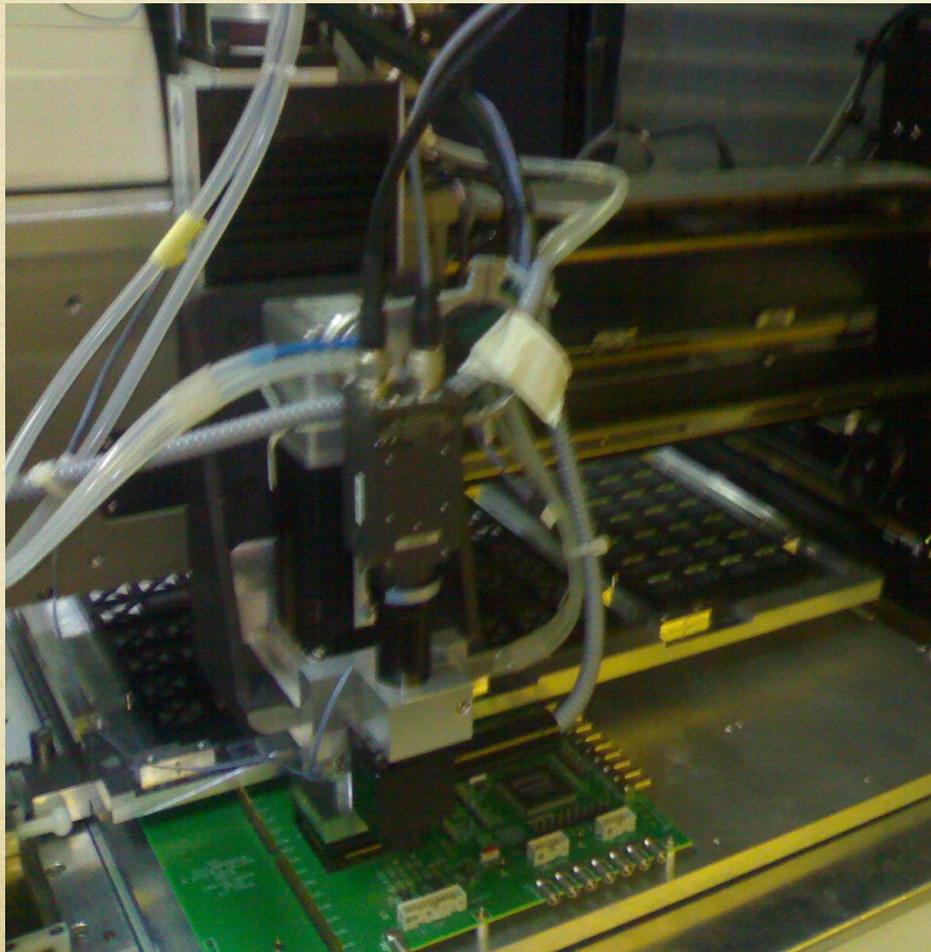


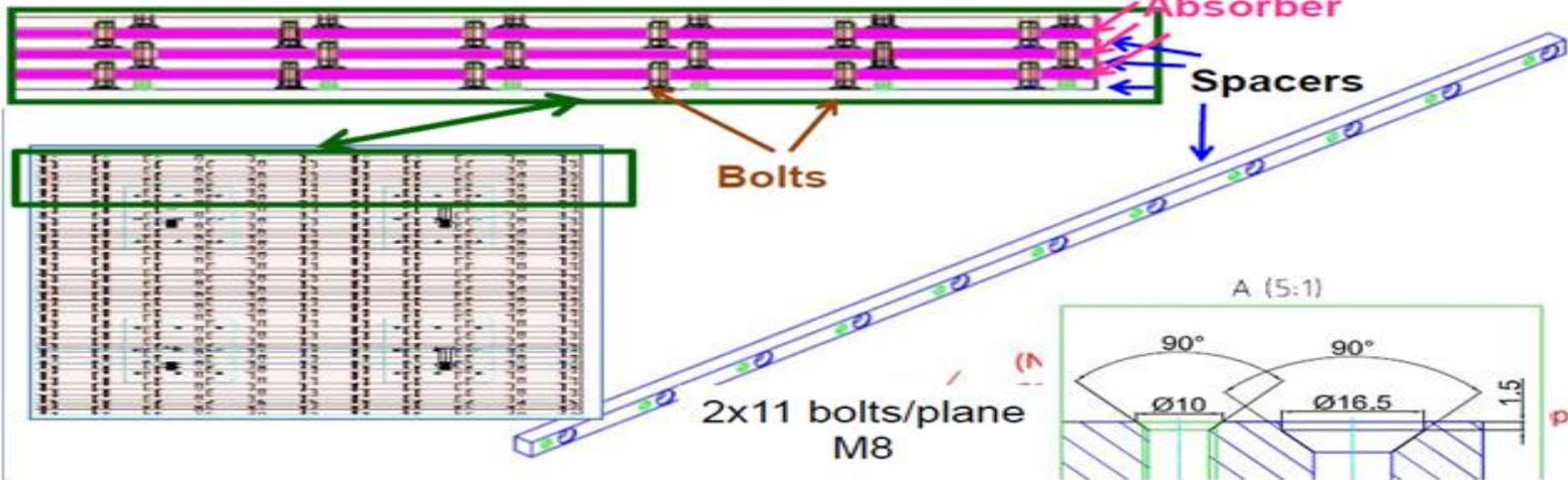
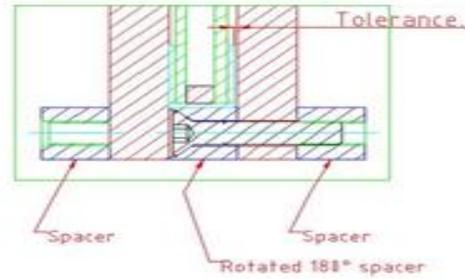
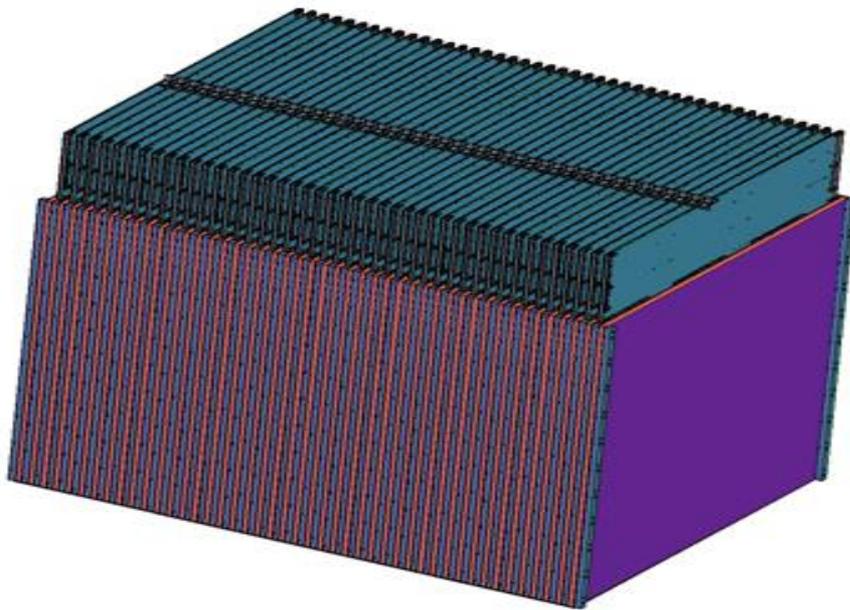
# Electronics: ASICs stand test

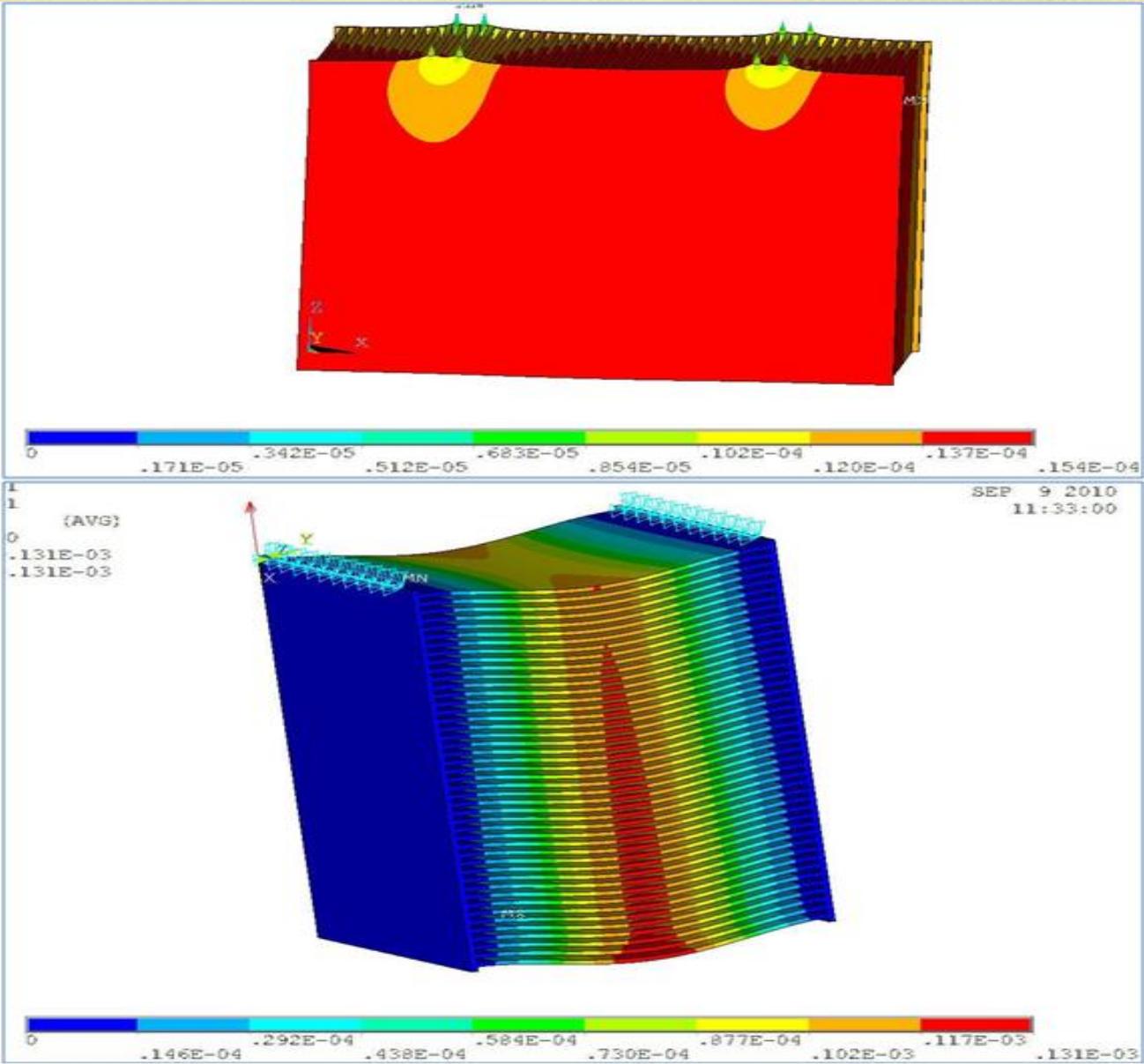
A robot was used to test the 10500 ASICs

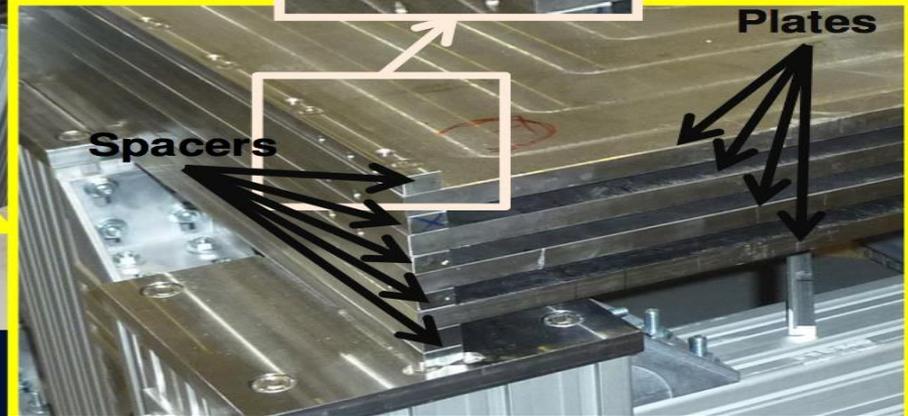
The procedure allows to select the good ASICs and calibrate them

Yield 93%



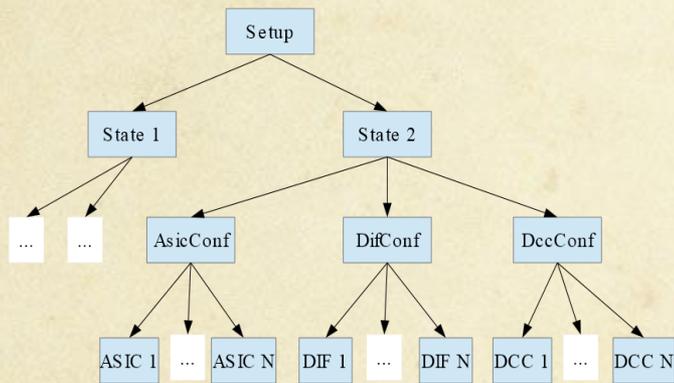
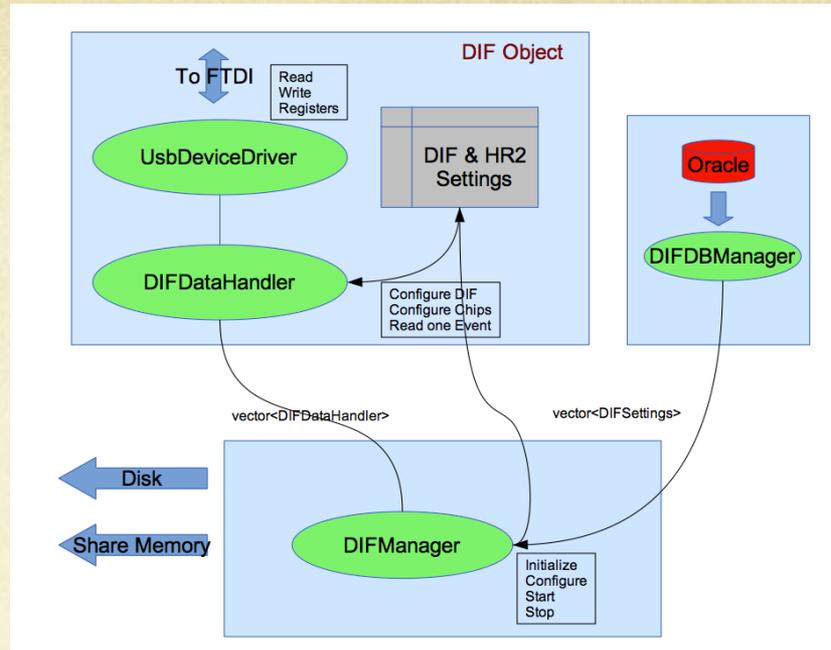




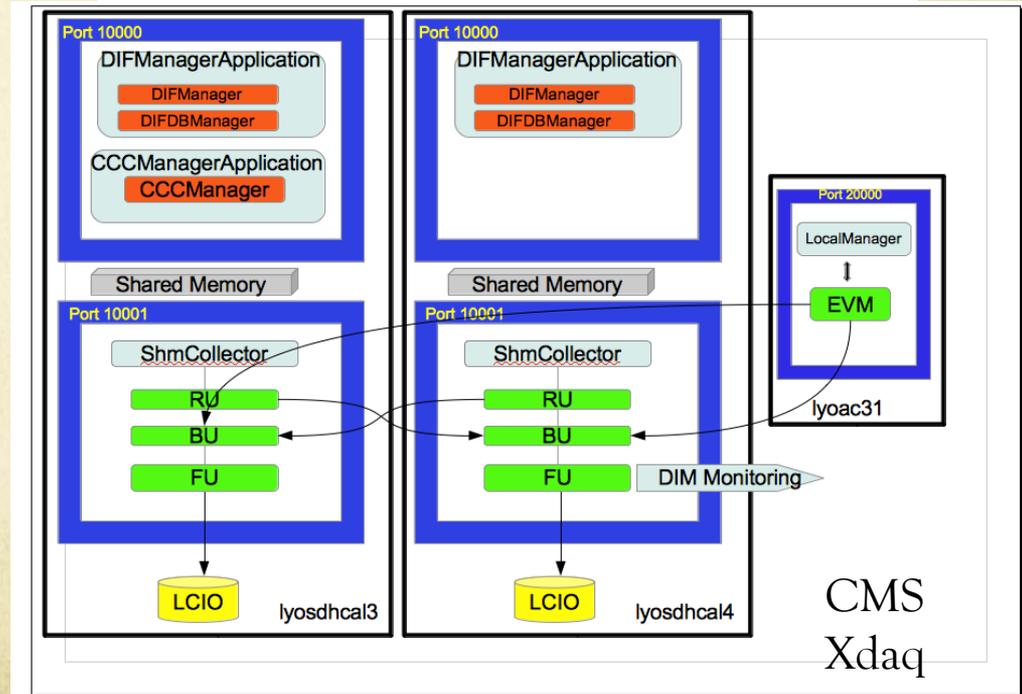


# SDHCAL acquisition system

- Low level hardware access
- Configuration data base software handling devices description and settings
- Data collection and the monitoring

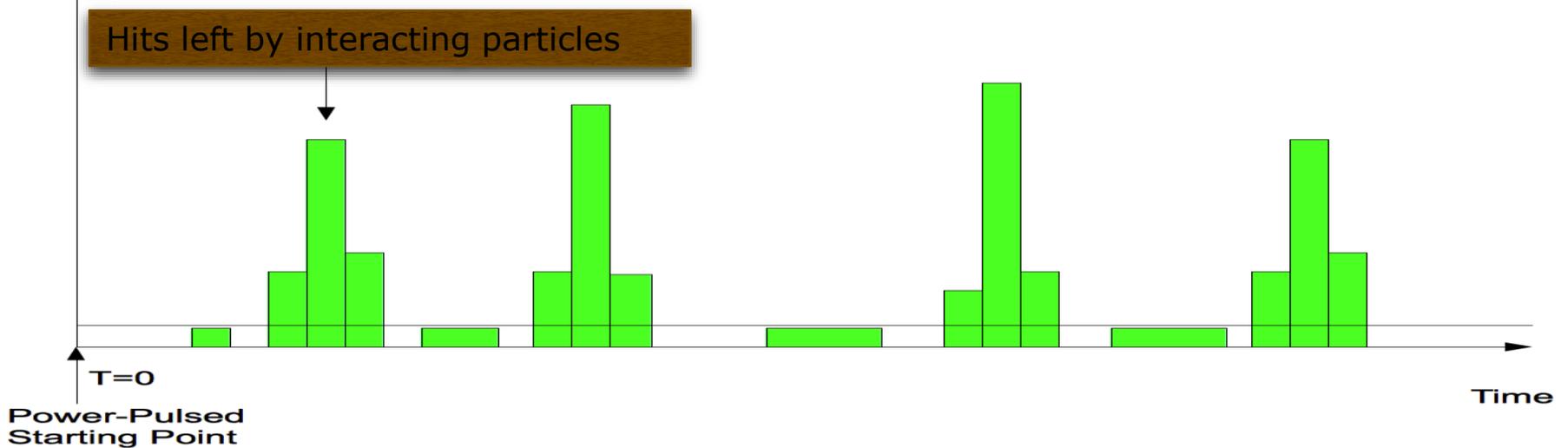


Setup configuration structure

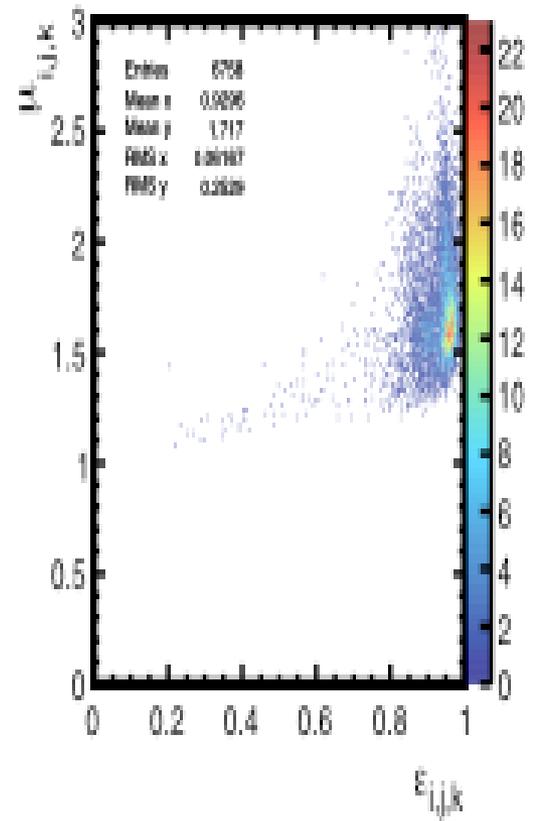
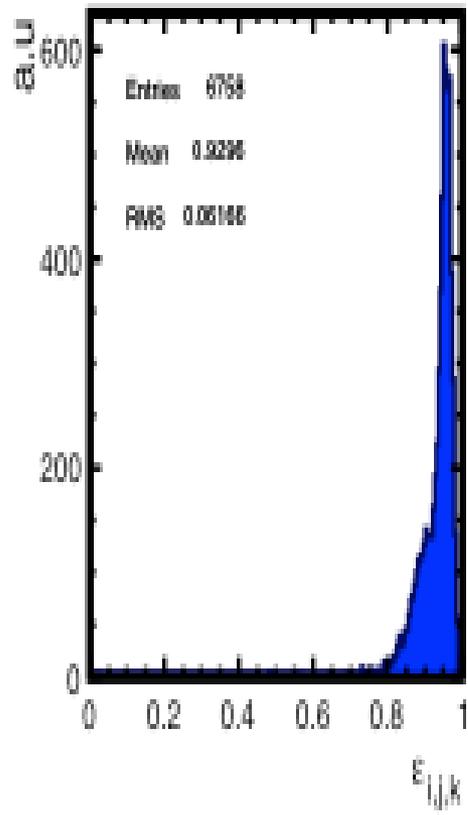
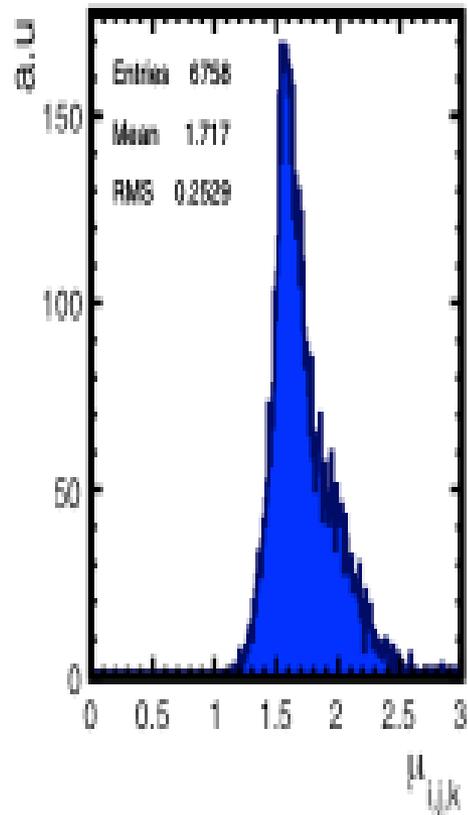


## Prototype data acquisition

- **Trigger less mode** : Recording events until memory is full, then data transfer and restart.
- **Power-Pulsed mode** : ASIC is idle between two spills.  
According to the time spill structure  
( NX400 ms (PS)\*, 10 s(SPS) every 45 s)
- No gain correction applied for this TB.
- Physics events are built as follows:

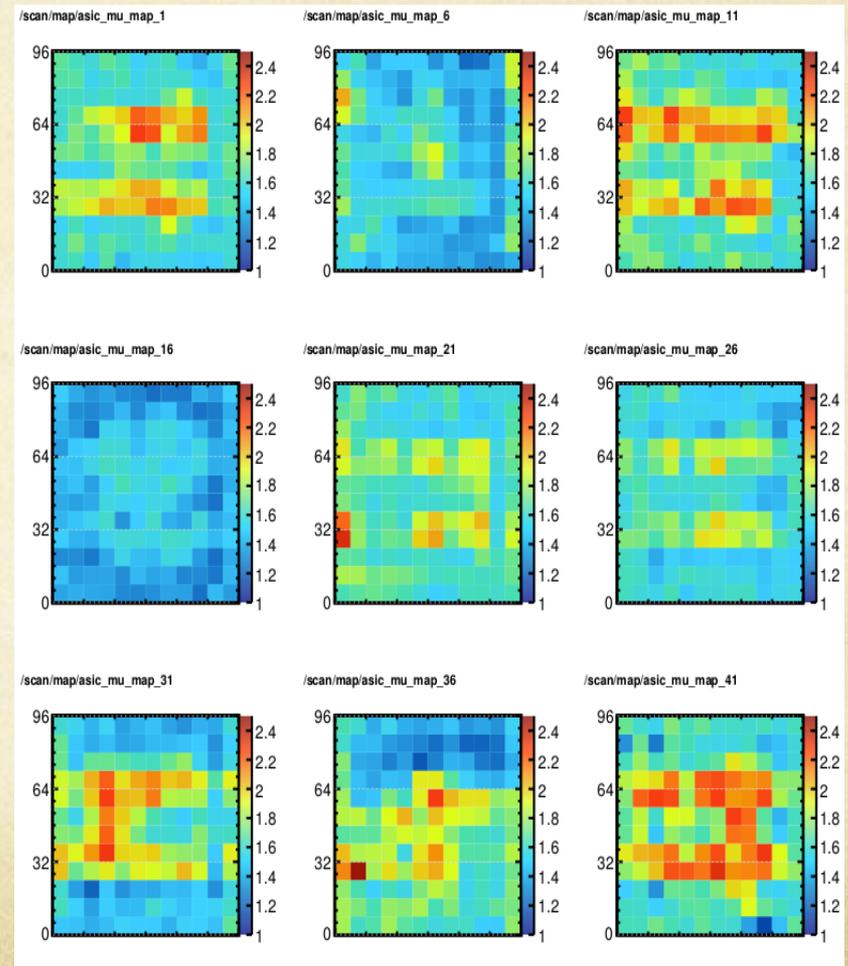
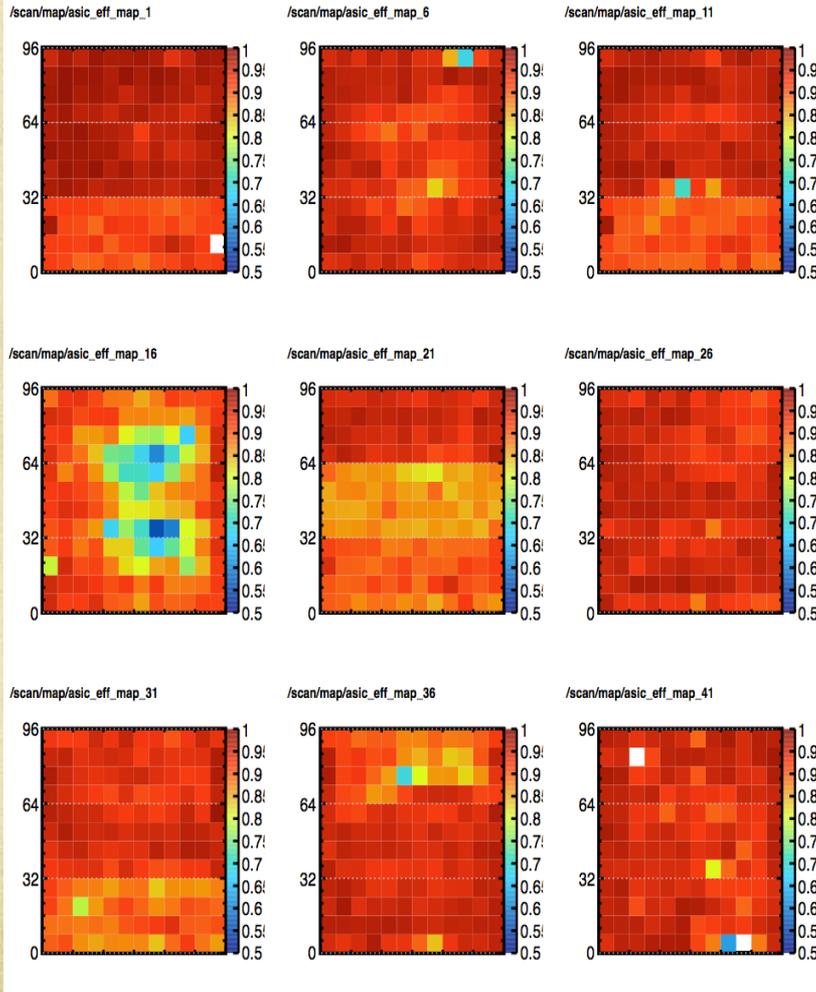


\* N is often 1 and sometimes 2-3 spills/cycle



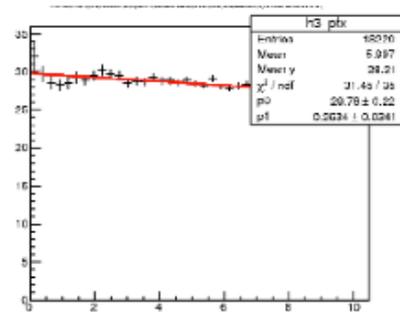
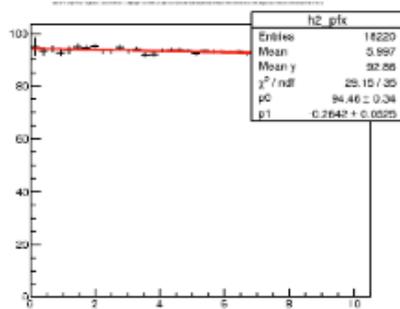
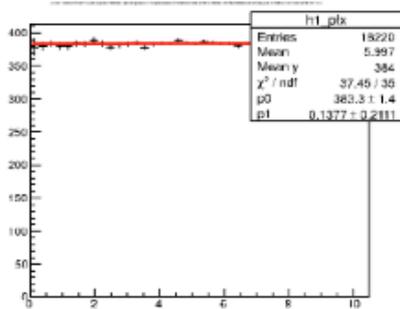
## Calibration :

Etude de la calibration de SDHCAL est en cours afin d'améliorer la résolution de l'énergie. Cela inclut l'étude de l'efficacité et la multiplicité des chambres localement à l'aide des muons et des cosmiques. La dépendance de la performance en temps (effet température...) peut aussi analysée d'une manière indirecte.

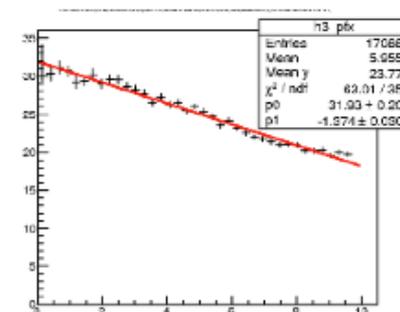
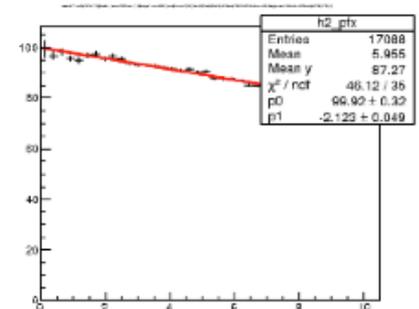
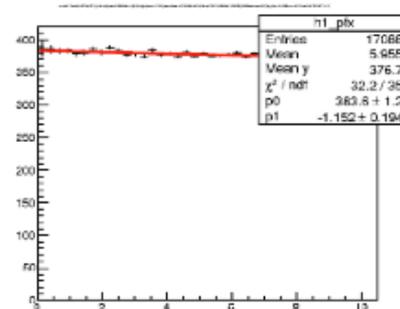


# Nb of hits versus spill time depth

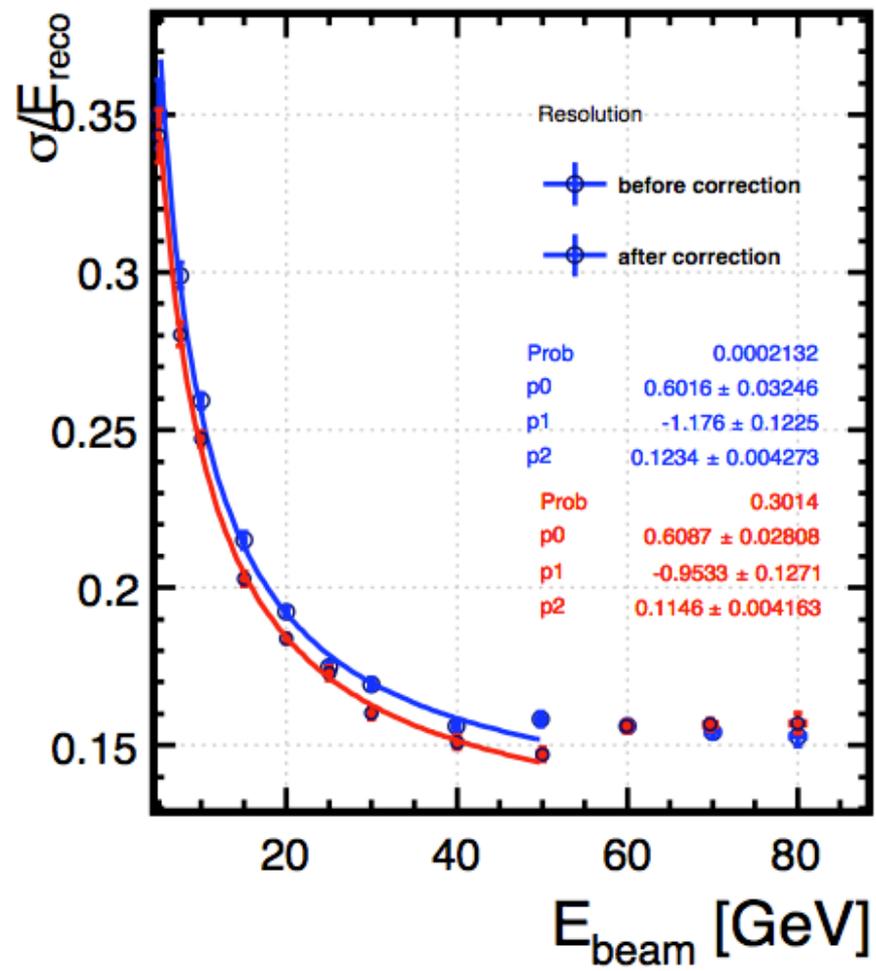
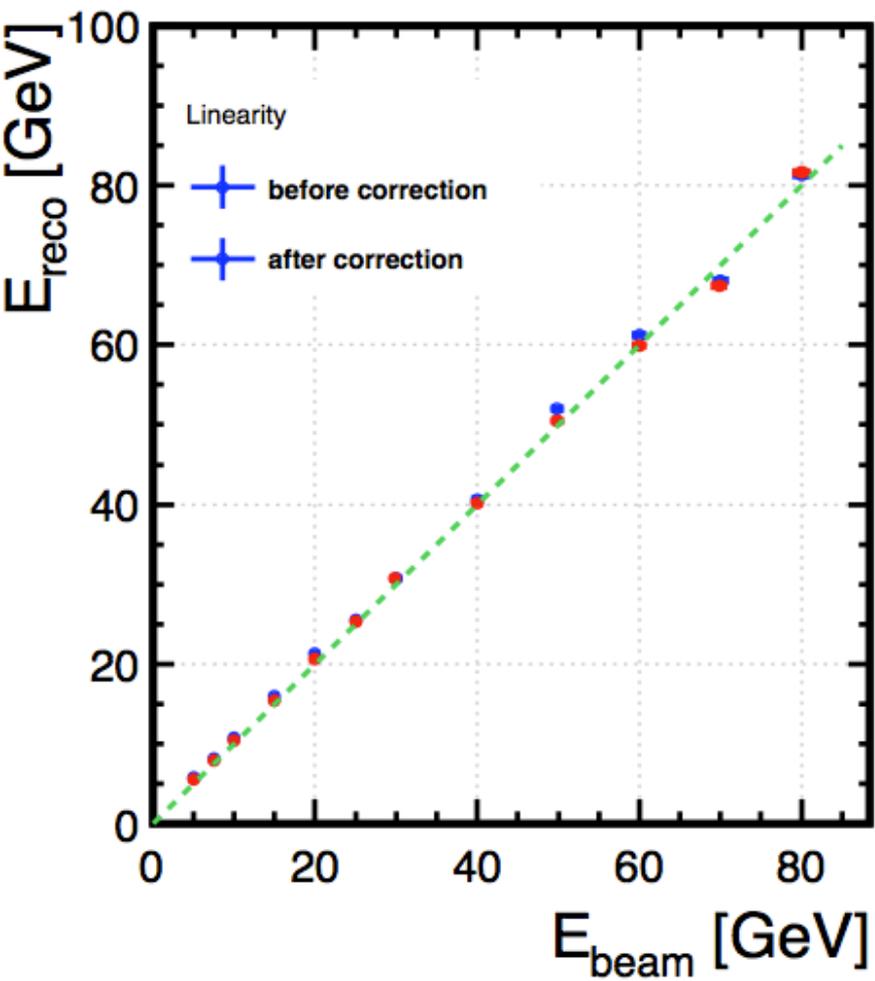
## Run 715671 (40M)



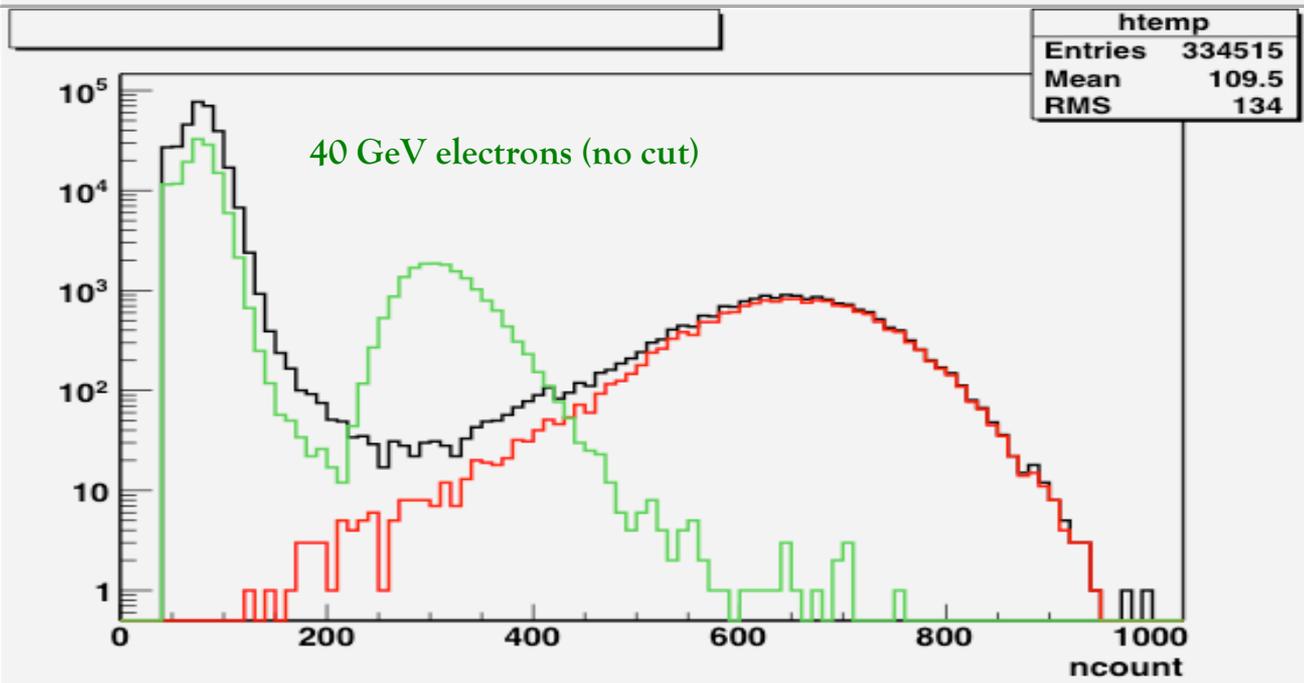
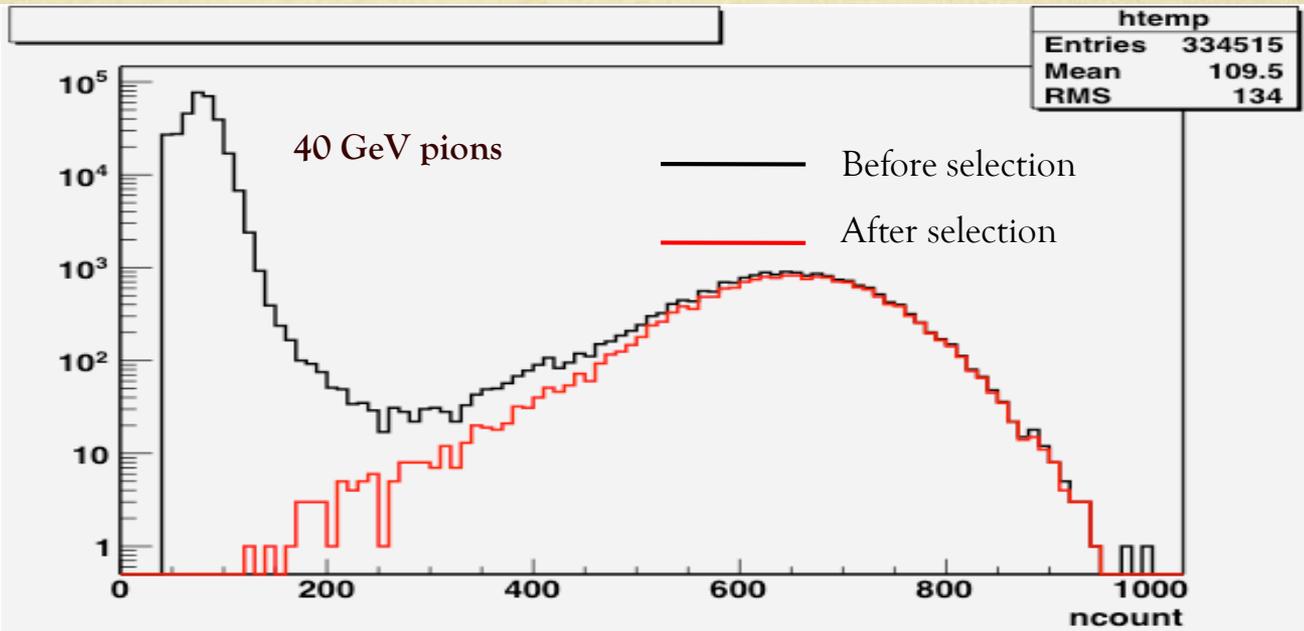
## Run 715747 (16M)

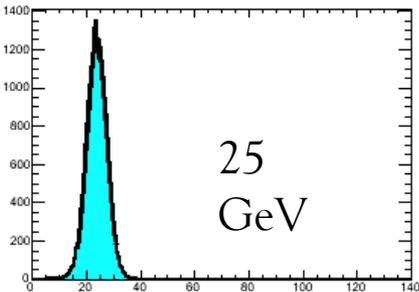
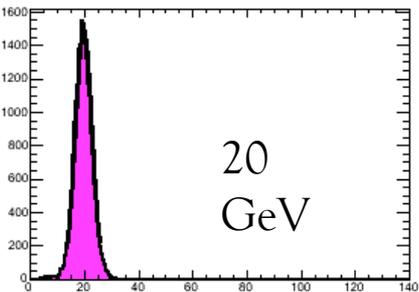
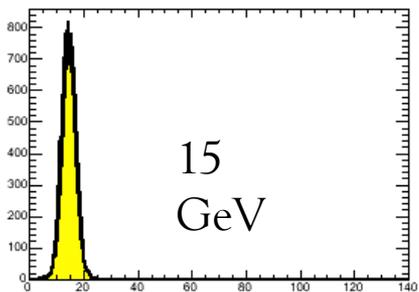
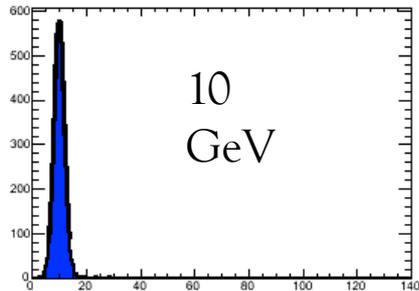
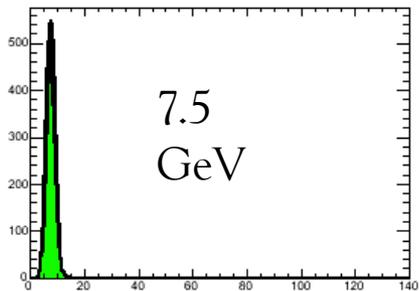
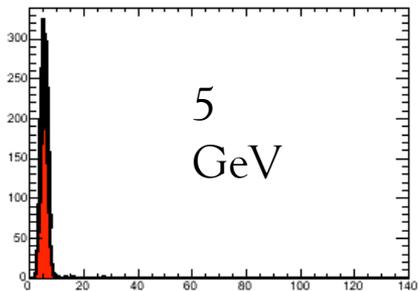


Very different beam conditions, intensity

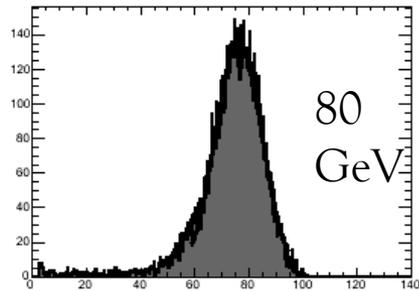
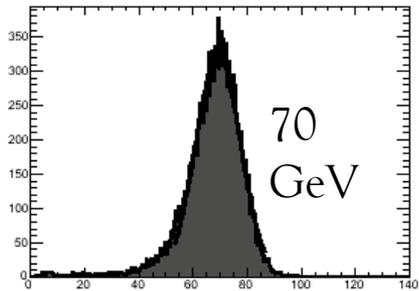
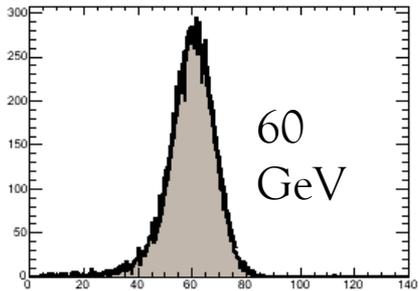
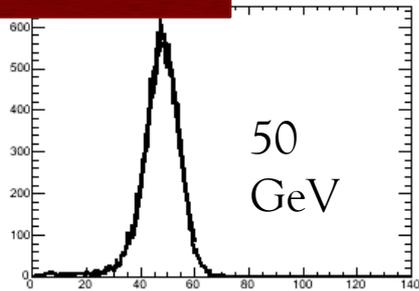
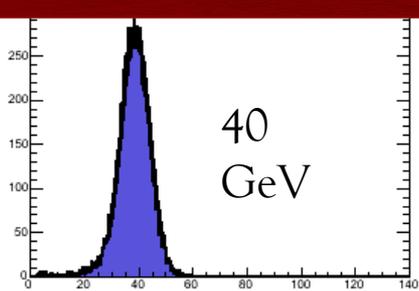
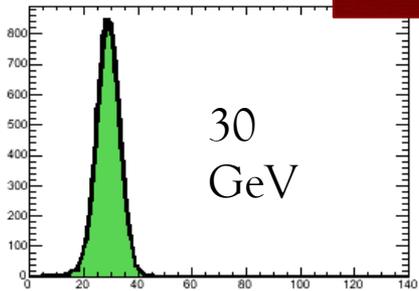


The selection should not impact the hadronic shower resolution





2- $\sigma$  Gaussian fits are used



## Energy estimation :

The thresholds weight evolution with the total number of hits obtained by minimizing a  $\chi^2$

$$\chi^2 = (E_{\text{beam}} - E_{\text{rec}})^2 / E_{\text{beam}}$$

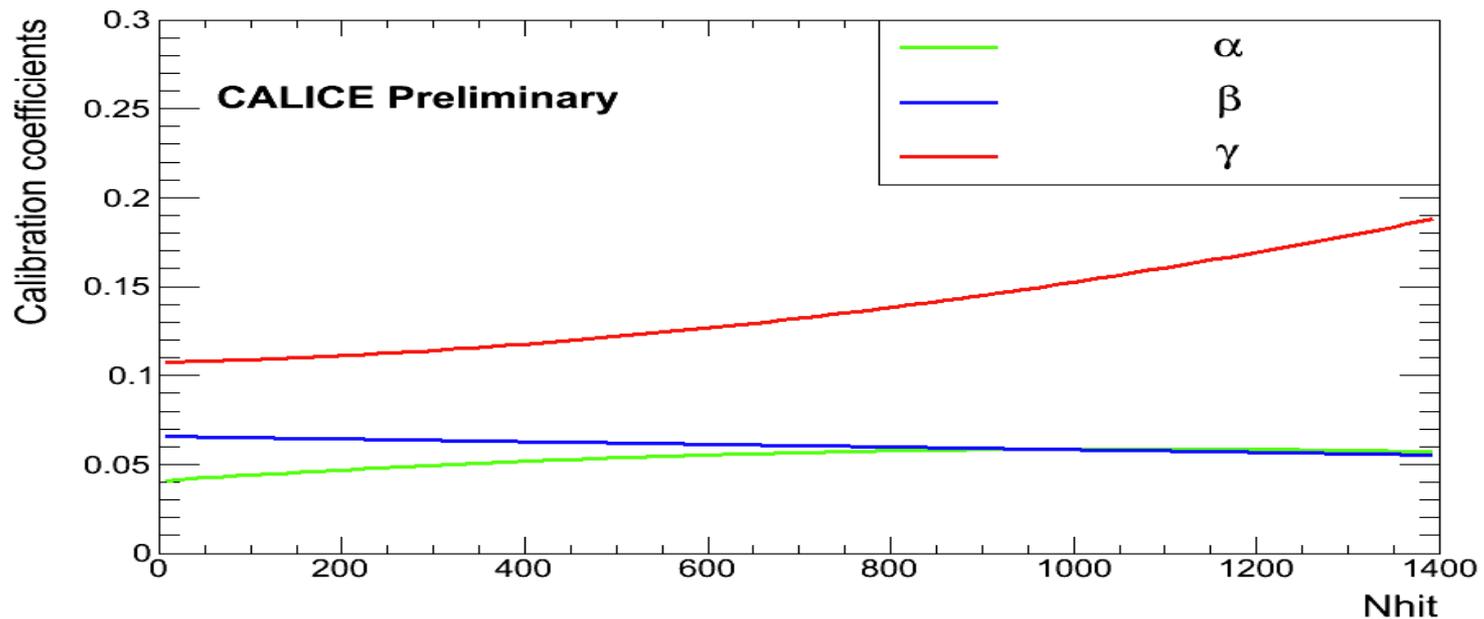
$$E_{\text{rec}} = \alpha(N_{\text{tot}}) N_1 + \beta(N_{\text{tot}}) N_2 + \gamma(N_{\text{tot}}) N_3$$

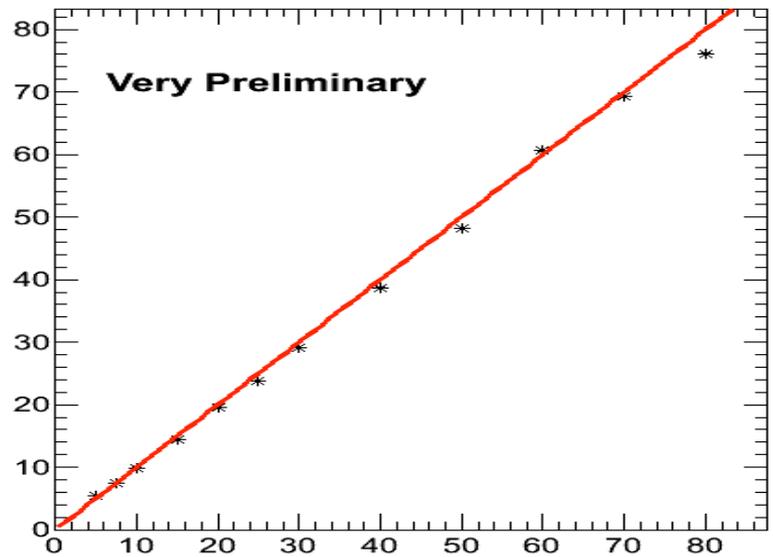
$N_1, N_2$  and  $N_3$  : exclusive number of hits associated to first, second and third threshold.

$\alpha, \beta, \gamma$  are quadratic functions of the total number of hits ( $N_{\text{tot}}$ )

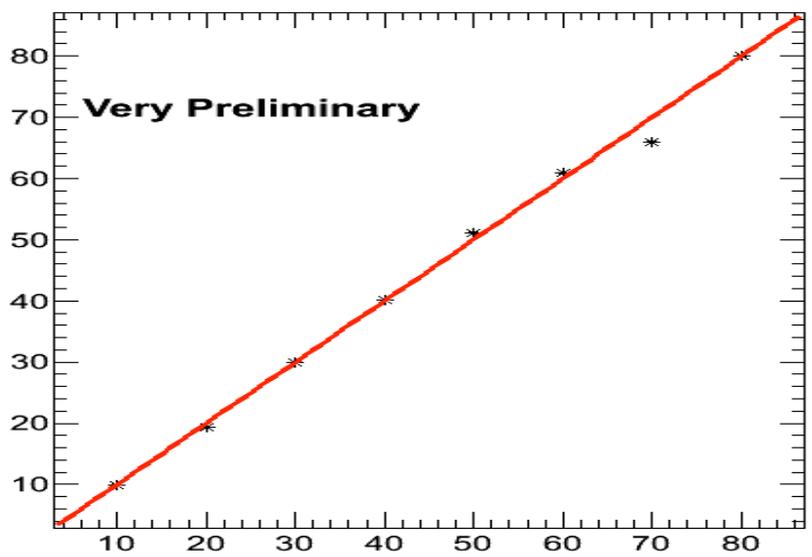
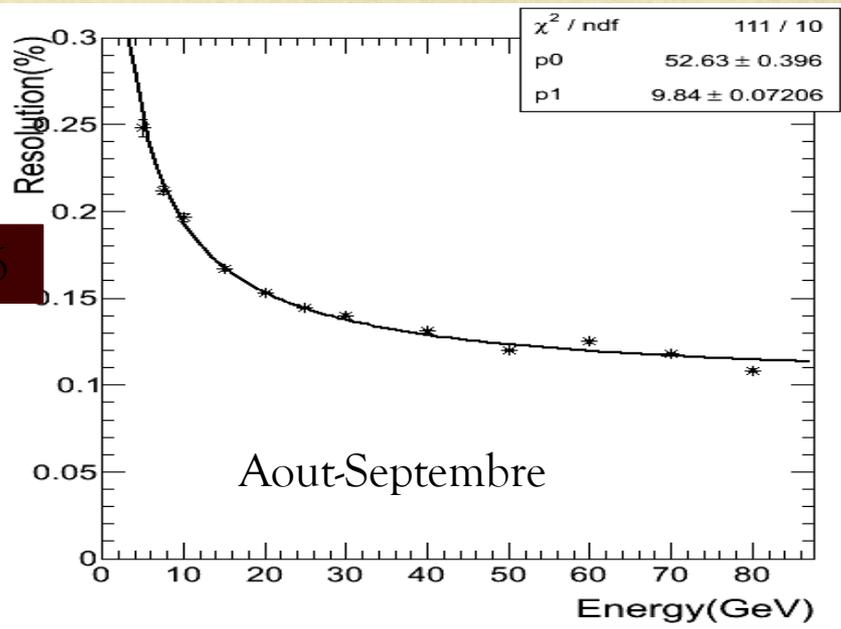
For instance  $\alpha = \alpha_0 + \alpha_1 N_{\text{tot}} + \alpha_2 N_{\text{tot}}^2$

Events of September runs corresponding to energies : 5, 10, 30, 60 and 80 GeV were used to fit the 9 parameters. This represents more than 50 k events.

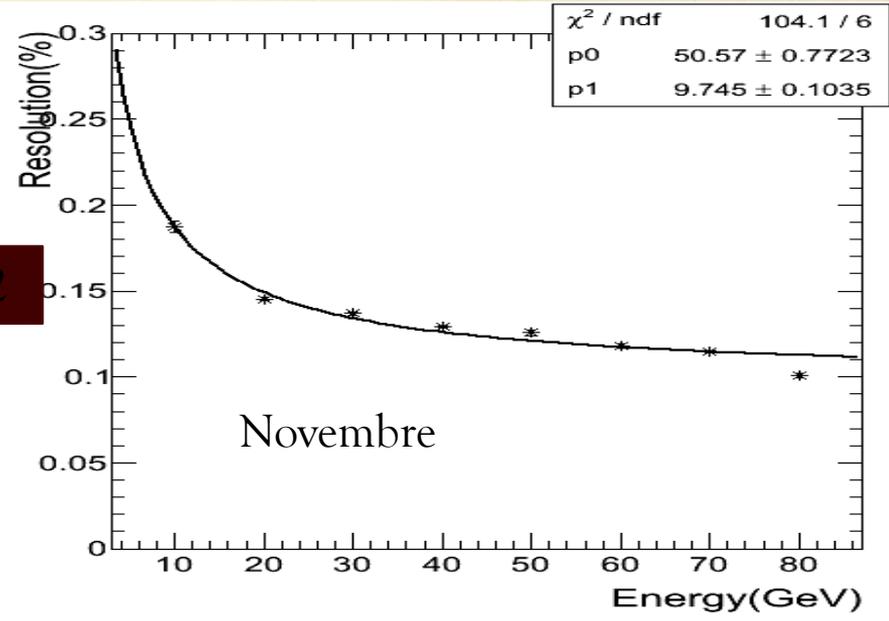




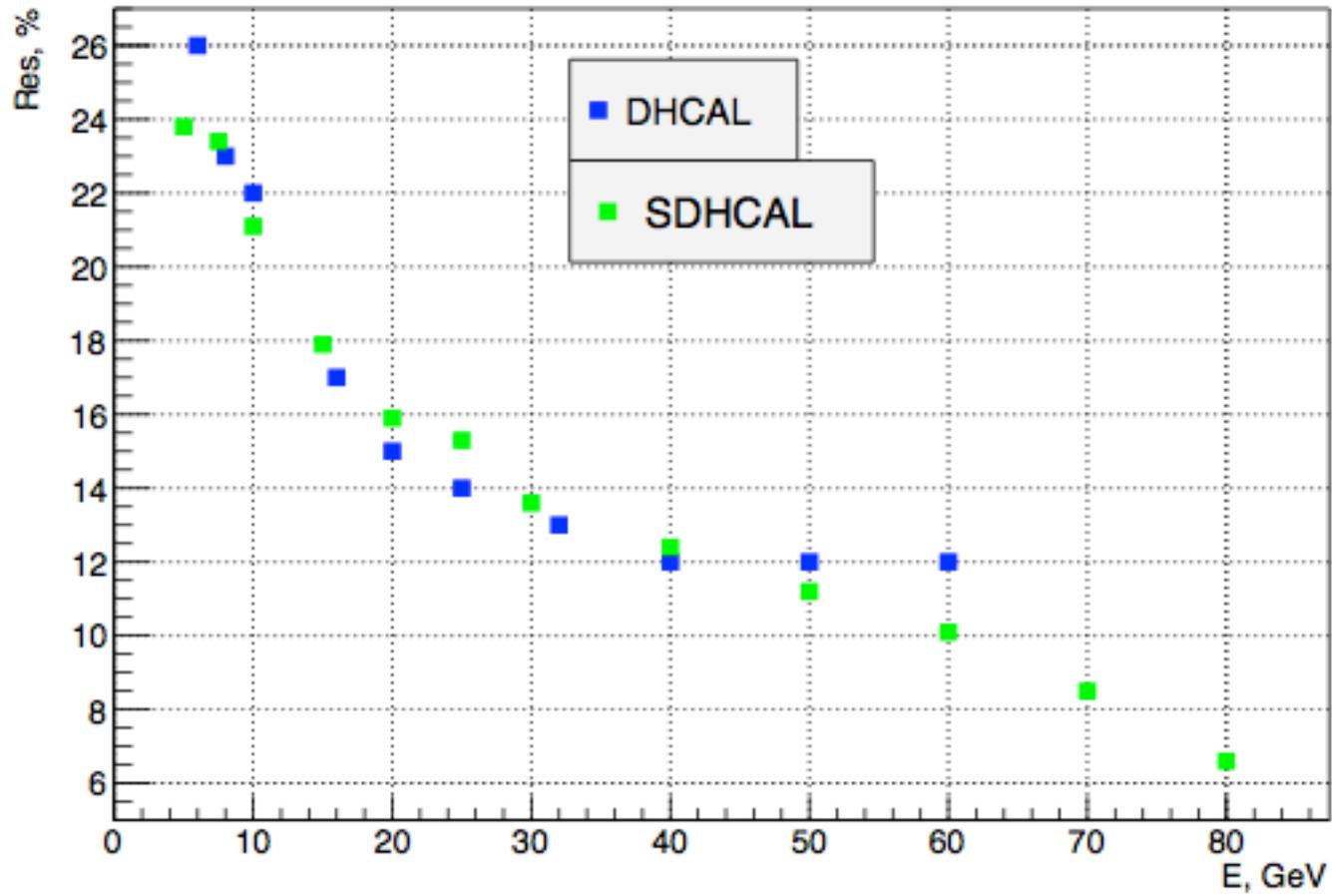
H6



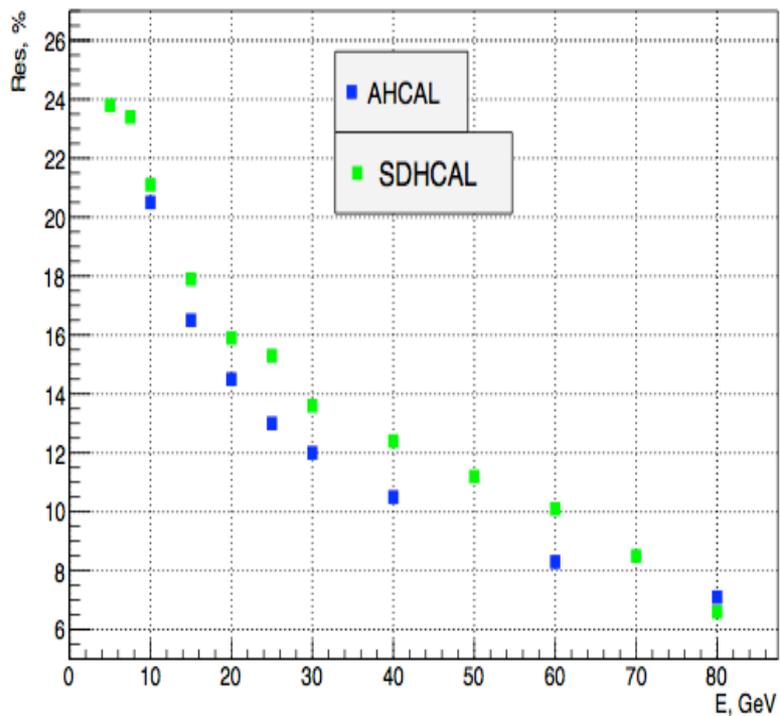
H2



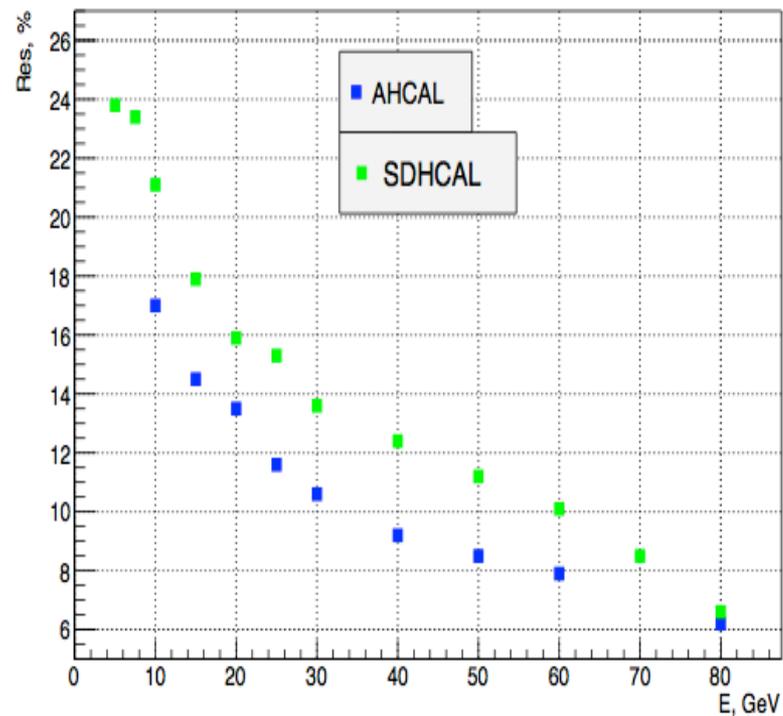
# Present SDHCAL versus DHCAL (after 3 years of calibration studies)



# Present SDHCAL versus AHCAL (after few years of calibration studies)

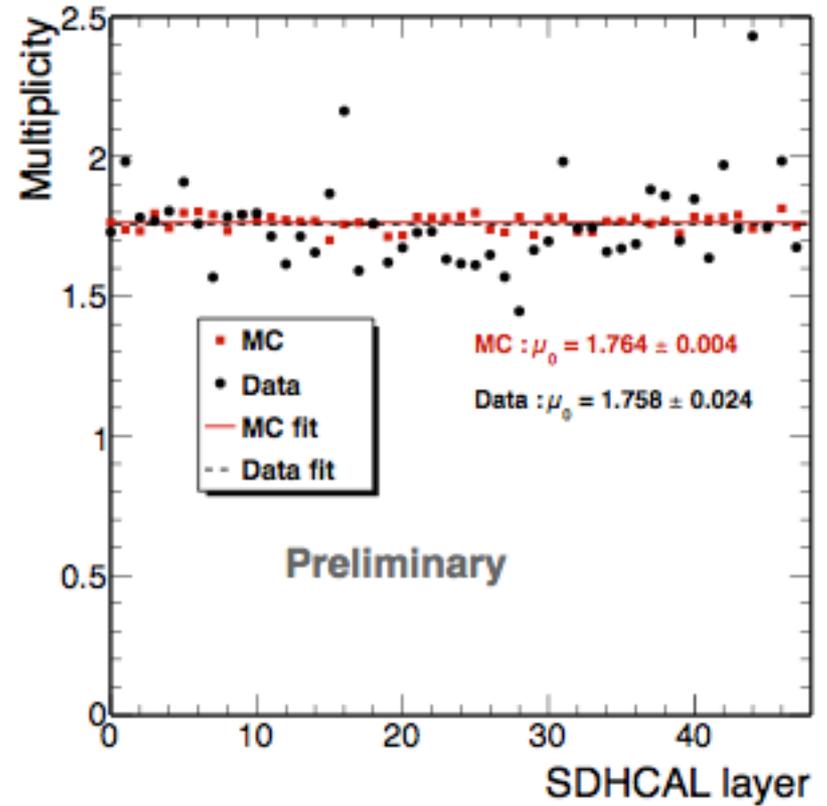
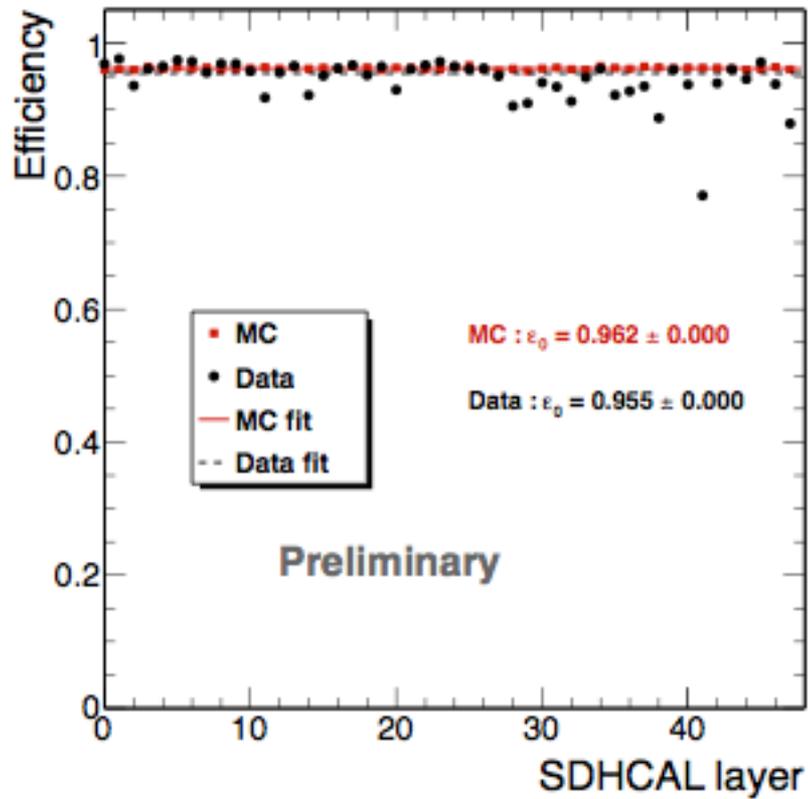


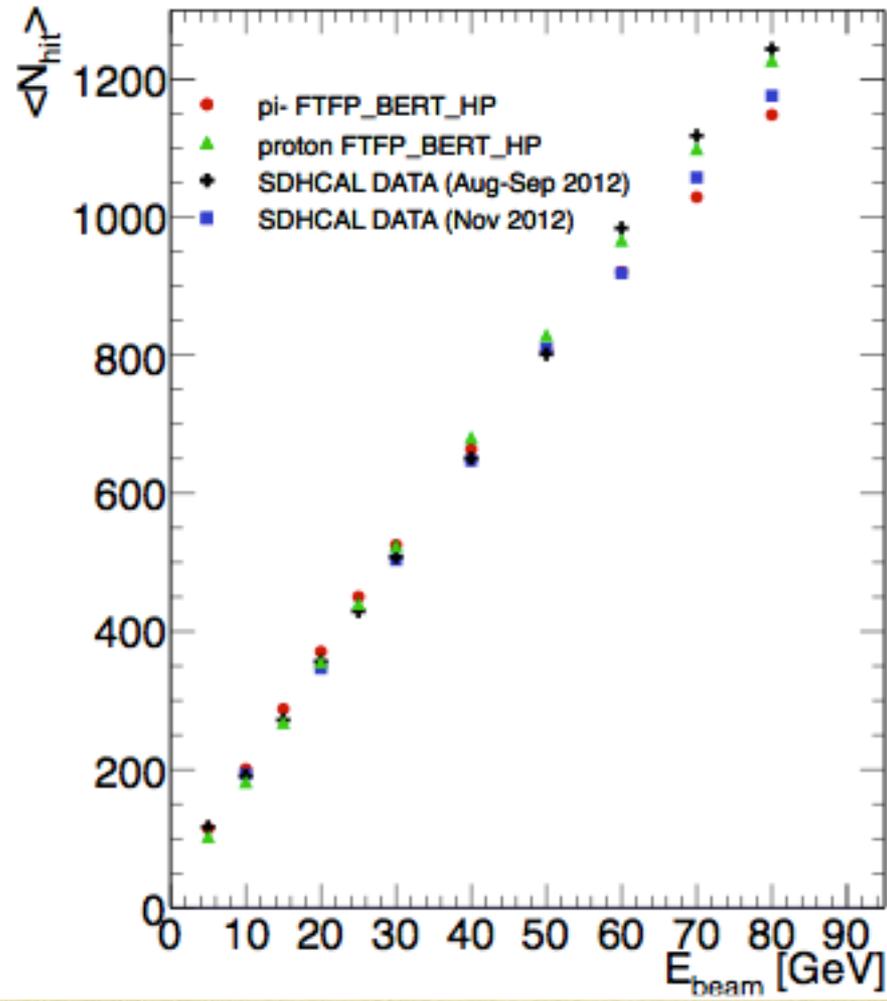
AHCAL after 4 years of data taking



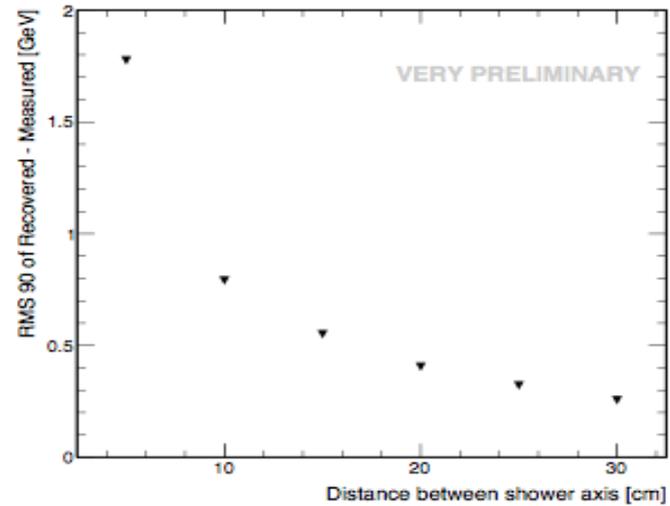
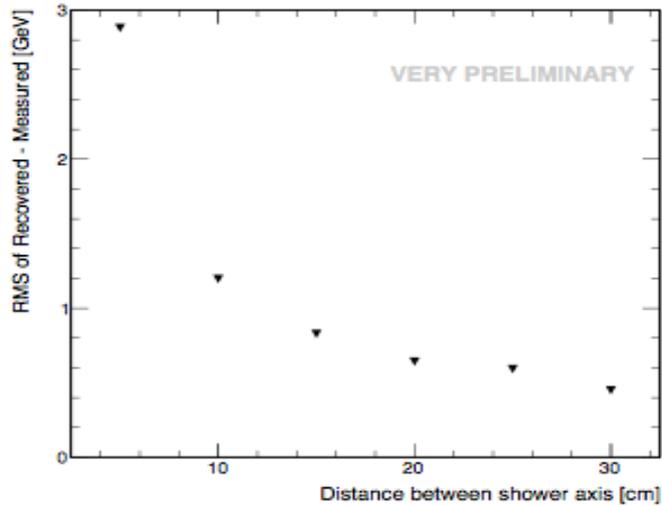
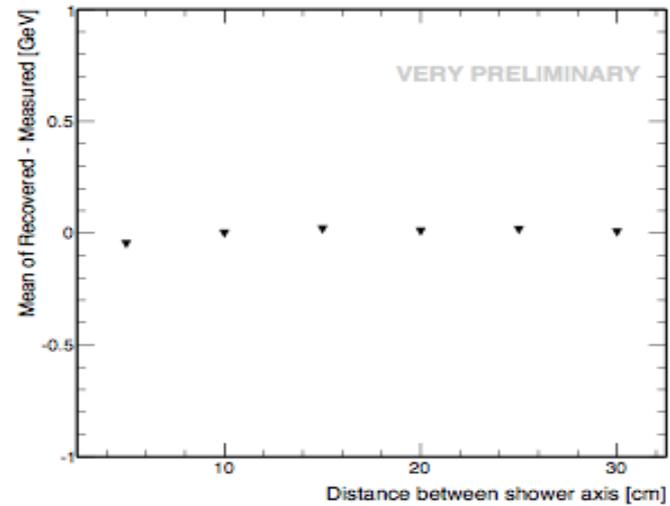
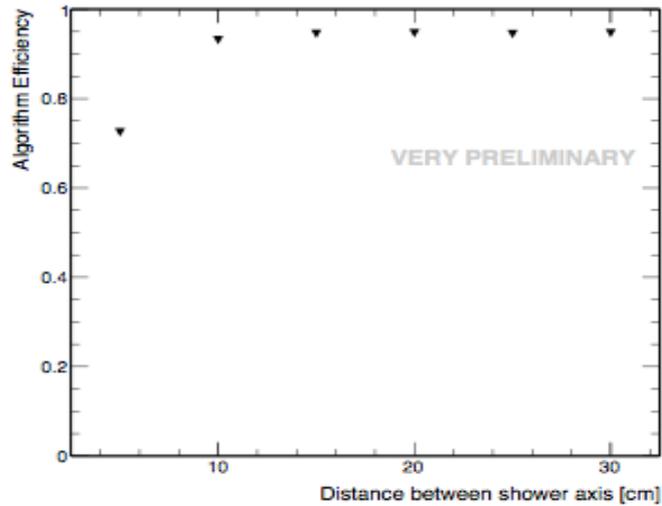
AHCAL after 6 years of data taking, using NN

# Efficiency-Multiplicity





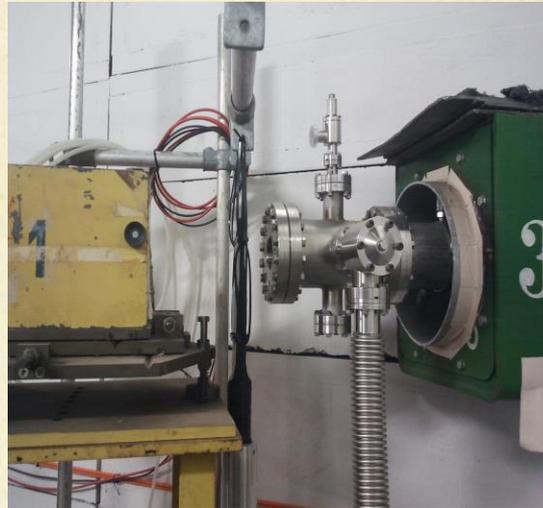
# Separation of two close-by pions of 10 GeV each



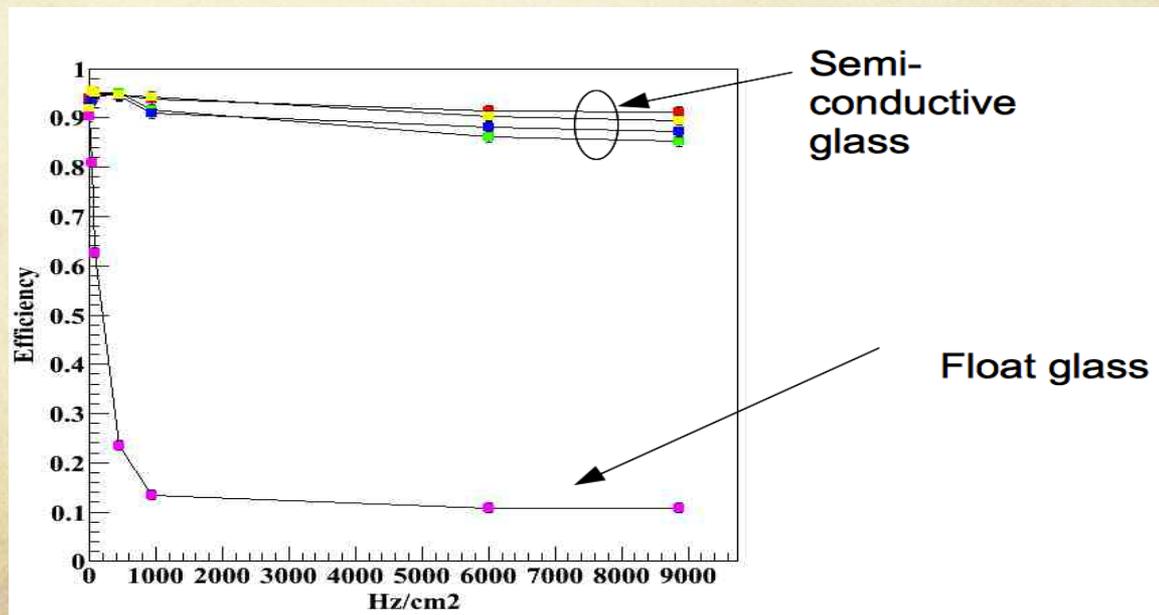
## High-Rate GRPC

High-Rate GRPC may be needed in the very forward region

- ✓ Semi-conductive glass ( $10^{10} \Omega \cdot \text{cm}$ ) produced by our collaborators from Tsinghua University was used to build few chambers.
- ✓ 4 chambers were tested at DESY as well as standard GRPC (float glass)



Performance is found to be excellent at high rate for GRPCs with the semi-conductive glass and can be used in the very forward of ILD region if the rate exceeds  $100 \text{ Hz/cm}^2$  in future ILD upgrades



# HARDROC3

## I2C link (@IPNL)

PLL: integrated before in a building block, first measurements are very good

Input frequency 2.5 MHz => output frequency: 10, 20, 40, and 80 MHz available

Bandgap: new one with a better temperature sensitivity, tested in a building block

Roll mode

Triple voting

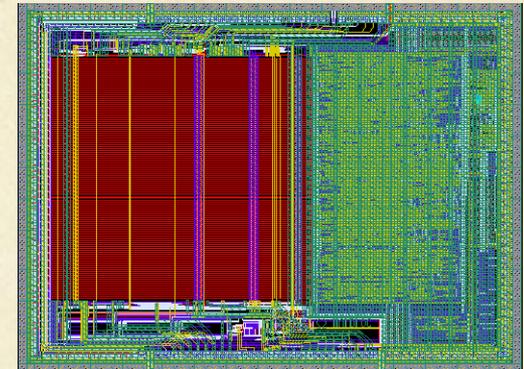
Temperature sensor: tested in a building block, slope - 6mV/°C

Die size ~ 30 mm<sup>2</sup> (6.3 x 4.7 mm<sup>2</sup>)

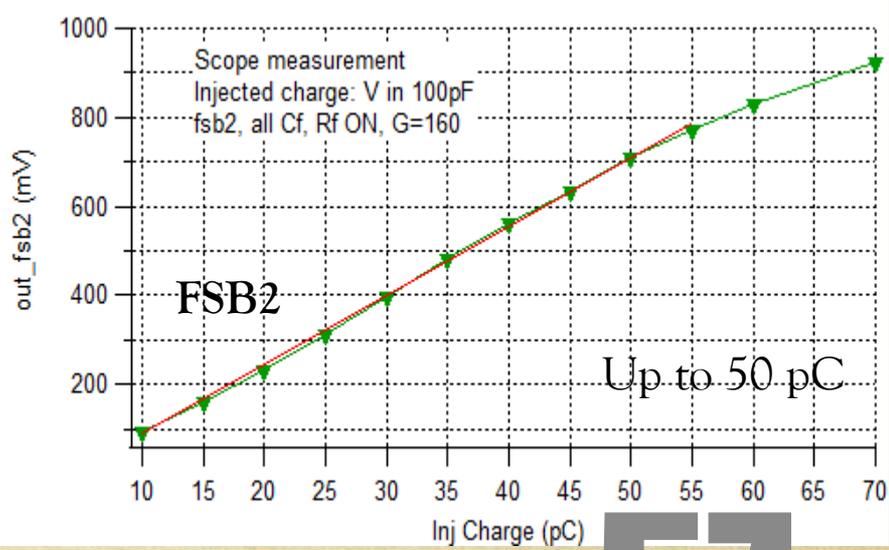
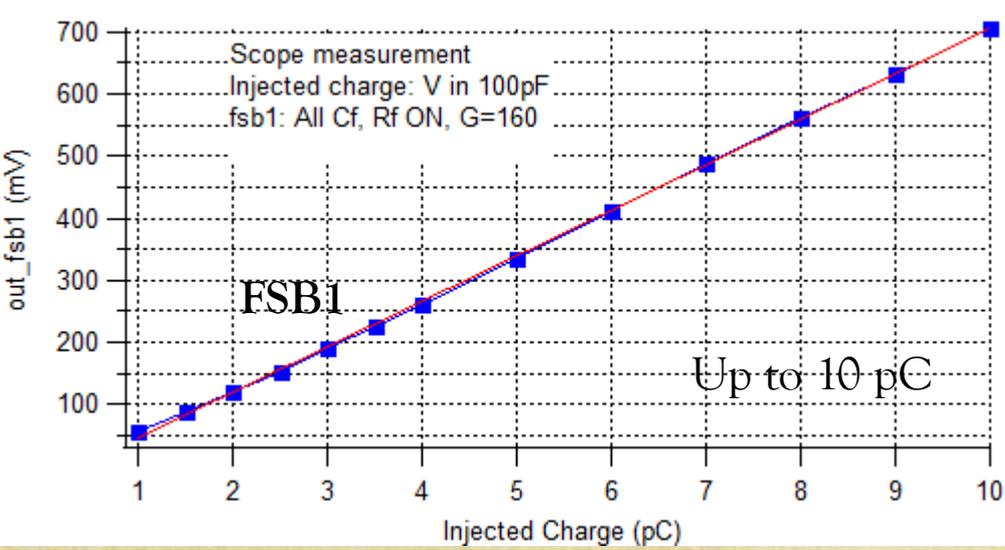
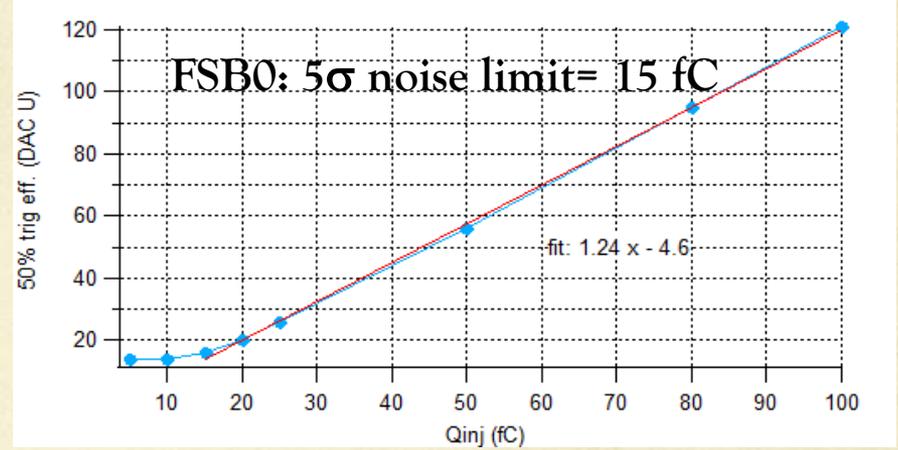
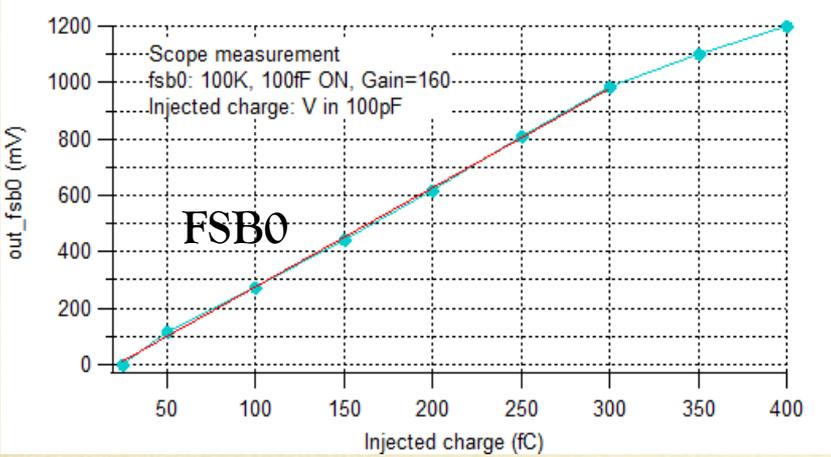
To be packaged in a TQFP208

Submitted at the end of Feb 2013 (SiGe 0.35µm)

Currently tested.

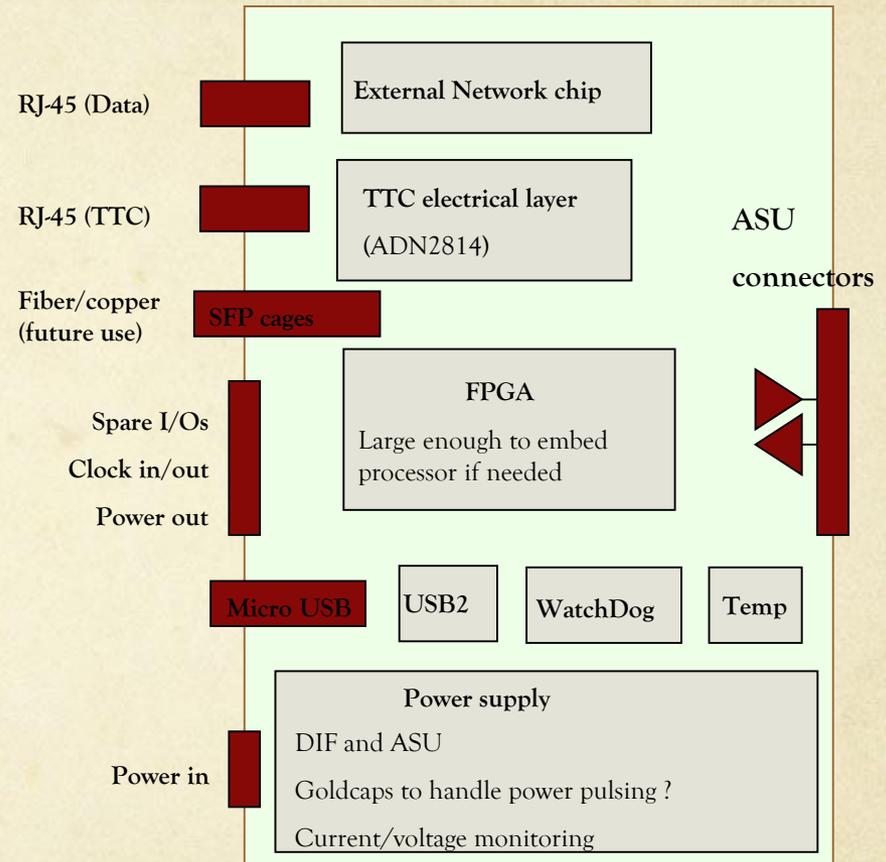


# ANALOG PART: FSB LINEARITY



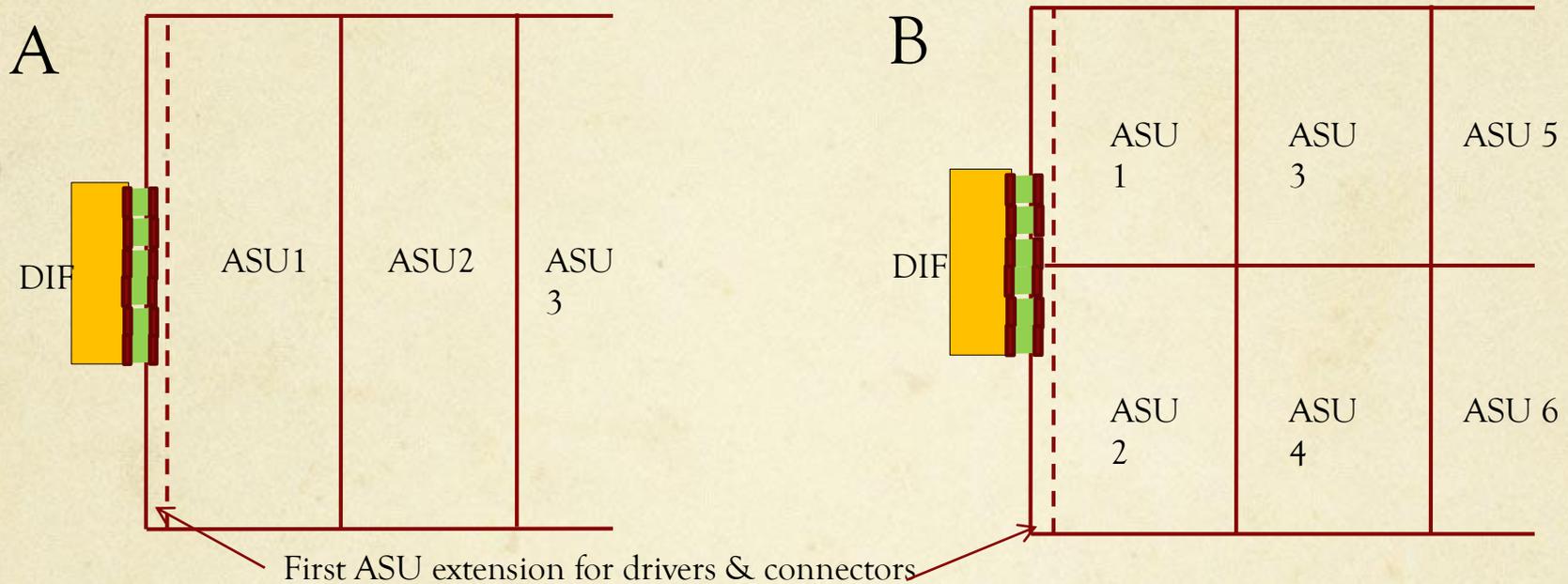
# DIF: Designed for ILD SDHCAL

- Only one DIF per plane. For the maximum length plane (1x3m) the DIF will handle 432 HR3 chips
- Slow control through the new HR3 I2C bus
- Data transmission to DAQ by Ethernet using commercial switches for concentration
- Clock and synchronization by TTC
- USB 2.0 for debugging



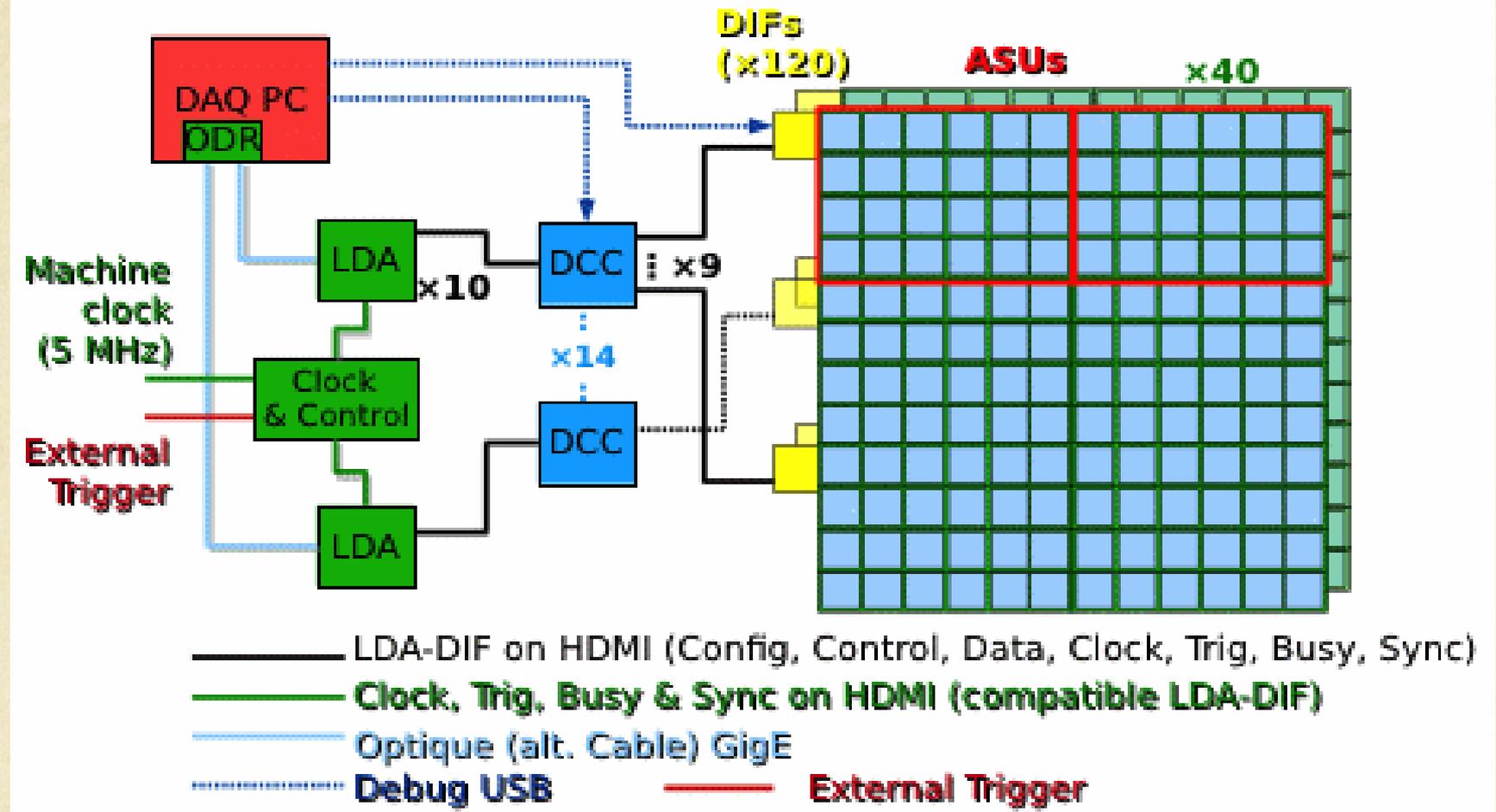
# New ASU layout options

As there will be only one DIF per plane, the distribution of the ASU boards in the plane will be rearranged to reduce the number of connections between the DIF and the plane



- In option B the common signals for the plane have to be sent twice (one per slab) while in option A they can be sent only once
- But, option A looks more risky from the point of view of the feasibility of the 1m long ASU boards.
- In both options the ASUs connected to the DIF will be a bit longer to host the connectors and the buffers for driving the long lines. This extension provides more freedom for the connectors selection and moves the drivers heat dissipation to the ventilation area

# Acquisition system



This scheme failed and was replaced by a hybrid one using both the DCC( fast commands, synchronization, ramful) and USB( data collection).