R&D Activities at IN2P3 for a Vertex Detector suited to ILC

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Outline

- Requirements and topics addressed
- Status of CPS development for running at $\sqrt{s} \lesssim 500$ GeV (0.35 $\mu$m process)
- Improvements coming from 0.18 $\mu$m CMOS process
  \[ \rightarrow \text{fast CMOS sensor (AROM) with $\mu$s level timestamping} \]
- 2-sided ladder developments
- Plans for the coming years
- Summary
ILC Vertexing Performance Goals

- **CMOS Pixel Sensors (CPS) pioneering devt triggered by ILC vertex detector requirements:**
  - unprecedented granularity & material budget (very low power)
  - much less demanding running conditions than at LHC
    - alleviated read-out speed & radiation tolerance requests
  - ILC duty cycle $\sim 1/200$
    - power saving by power pulsing sub-systems

- **Vertexing goal:**
  - achieve high efficiency & purity flavour tagging
    - charm & tau, jet-flavour !!!
  - $\sigma_{R\phi,Z} \leq 5 \oplus 10/p \cdot \sin^{3/2} \theta \ \mu m$
    - LHC: $\sigma_{R\phi} \approx 12 \oplus 70/p \cdot \sin^{3/2} \theta$
  - Comparison: $\sigma_{R\phi,Z}$ (ILD) with VXD made of ATLAS-IBL or ILD-VXD pixels
A complex set of strongly correlated issues:

- **Charged particle sensor technology:**
  - highly granular, thin, low power, swift pixel sensors

- **Micro-electronics:**
  - highly integrated, low power, SEE safe, r.o. \( \mu \)circuits

- **Electronics:**
  - high data transfer bandwidth (no trigger), some SEE tolerable
  - low mass power delivery, allowing for power cycling

- **Mechanics:**
  - rigid, ultra-light, heat but not electrical conductive, mechanical supports, possibly with \( C_{\Delta t} \approx C_{Si}^{\Delta t} \)
  - very low mass, preferably air, cooling system
  - micron level alignment capability

- **EM compliance:**
  - power cycling in high B field \( \Rightarrow F(\text{Lorentz}) \)
  - higher mode beam wakefield disturbance \( \Rightarrow \) pick-up noise?

- **Radiation load and SEE compliance at \( T_{room} \)**
  - \( \Rightarrow \) reduced material budget
Topics Addressed by the R&D

- **Vertex Detector Concept**:  
  - Cylindrical geometry based on 3 concentric 2-sided layers  
  - Layers equipped with 3 different CMOS Pixel Sensors (CPS)

- **Pixel Sensor Development**:  
  - Exploit CPS potential & IPHC expertise  
  - R&D performed in synergy with other applications  
    - EUDET-BT, STAR, ALICE, CBM, ...  
  - CPS \equiv unique technology being simultaneously granular, thin, integrating full FEE, industrial & cheap  
  - Address trade-off btw spatial resolution & read-out speed

- **Double-Sided Ladder Development**:  
  - Develop concept of 2-sided ladder using 50 \( \mu m \) thin CPS  
  - Develop concept of mini-vectors providing high spatial resolution & time stamping  
  - Address the issue of high precision alignment & power cycling in high magnetic field
DEVELOPMENT OF CMOS SENSORS

STAR-PXL

HALF-BARREL:

- 20 ladders (0.37% $X_0$)
- 200 sensors
- 180 $\cdot 10^6$ pixels
- Air flow cooling:
  $T \lesssim 35^\circ C$
- $\sigma_{sp} < 4 \mu m$
- Rad. load $\gg$ ILC values
- $t_{r.o.} \simeq 190 \mu s$
  $\rightarrow$ ILC : $O(10) \mu s$

Installed in January 2014
State-of-the-Art: MIMOSA-28 for the STAR-PXL

• Main characteristics of ULTIMATE (≡ MIMOSA-28):
  * rolling shutter read-out derived from EUDET BT chip: MIMOSA-26
  * 0.35 \( \mu m \) process with high-resistivity epitaxial layer
  * column // architecture with in-pixel cDS & amplification
  * end-of-column discrimination & binary charge encoding
  * on-chip zero-suppression
  * active area: 960 columns of 928 pixels (19.9 \( \times \) 19.2 mm\(^2\))
  * pitch: 20.7 \( \mu m \) \( \rightarrow \) 0.9 million pixels
    \( \leftarrow \) charge sharing \( \Rightarrow \) \( \sigma_{sp} \gtrsim 3.5 \mu m \)
  * JTAG programmable
  * \( t_{r.o.} \lesssim 200 \mu s \) (\( \sim 5 \times 10^3 \) frames/s) \( \Rightarrow \) suited to \( > 10^6 \) part./cm\(^2\)/s
  * 2 outputs at 160 MHz
  * \( \sim 150 \) mW/cm\(^2\) power consumption
  * \( N \lesssim 15 \) e\(^-\) ENC at 30-35\(^\circ\)C
  * \( \epsilon_{det} \) versus fake hit rate
  * Radiation tolerance: \( 3 \cdot 10^{12} n_{eq}/cm^2 \) & 150 kRad at 30-35\(^\circ\)C
  * Detector construction under way (40 ladders made of 10 sensors)

▷▷▷ 1st step: Commissioning of 3/10 of detector completed
       at RHIC with pp collisions in May-June 2013

▷▷▷ next step: Start of physics with full detector in Feb. 2014
Two types of CMOS Pixel Sensors:

- **Inner layers** ($\sim 300 \text{ cm}^2$):
  - Priority to read-out speed & spatial resolution
  - Small pixels ($16 \times 16 / 80 \mu m^2$)
    - With binary charge encoding
    - $t_{r.o.} \sim 50 / 10 \mu s$; $\sigma_{sp} \lesssim 3 / 6 \mu m$

- **Outer layers** ($\sim 3000 \text{ cm}^2$):
  - Priority to power consumption and good resolution
  - Large pixels ($35 \times 35 \mu m^2$)
    - With 3-4 bits charge encoding
    - $t_{r.o.} \sim 100 \mu s$; $\sigma_{sp} \lesssim 4 \mu m$

2-sided ladder concept for inner layer:

- PLUME collaboration

- **Square pixels** ($16 \times 16 \mu m^2$)
  - On internal ladder face ($\sigma_{sp} < 3 \mu m$)

- **Elongated pixels** ($16 \times 64/80 \mu m^2$)
  - On external ladder face ($t_{r.o.} \sim 10 \mu s$)

Total VXD instantaneous/average power $< 600/12$ W (0.18 $\mu m$ process)
CMOS Pixel Sensors for the ILD-VXD (2/3)

• From the STAR-PXL to the ILC-VXD:

<table>
<thead>
<tr>
<th>Detector</th>
<th>$\sigma_{sp}$</th>
<th>$t_{int}$</th>
<th>Dose ($30^\circ$ C)</th>
<th>Fluence ($30^\circ$ C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>STAR-PXL</td>
<td>$\gtrsim 3.5 , \mu m$</td>
<td>190 $\mu s$</td>
<td>150 kRad</td>
<td>$3 \cdot 10^{12} n_{eq}/cm^2$</td>
</tr>
<tr>
<td>ILD-VXD/In</td>
<td>$&lt; 3 , \mu m$</td>
<td>50/10 $\mu s$</td>
<td>$&lt; 100$ kRad</td>
<td>$\lesssim 10^{11} n_{eq}/cm^2$</td>
</tr>
<tr>
<td>ILD-VXD/Out</td>
<td>$\lesssim 4 , \mu m$</td>
<td>100 $\mu s$</td>
<td>$&lt; 10$ kRad</td>
<td>$\lesssim 10^{10} n_{eq}/cm^2$</td>
</tr>
</tbody>
</table>

• Final ”500 GeV” CPS prototypes: fab. in Winter 2011/12 (0.35 $\mu m$ process for economic reasons)

※ MIMOSA-30: inner layer prototype with 2-sided read-out
  → one side: 256 pixels ($16 \times 16 \, \mu m^2$)
  other side: 64 pixels ($16 \times 64 \, \mu m^2$)

※ MIMOSA-31: outer layer prototype
  → 48 col. of 64 pixels ($35 \times 35 \, \mu m^2$)
  ended with 4-bit ADC
CMOS Pixel Sensors for the ILD-VXD (3/3)

- **MIMOSA-30**: prototype for ILD-VXD innermost layer
  - 0.35 CMOS $\mu m$ process with high-resistivity epitaxy
  - in-pixel CDS, rolling shutter read-out, binary sparsified output
  - columns length $\sim$ final sensor (4-5 mm long)
  - high resolution side: pixels of $16 \times 16 \mu m^2$ $\Rightarrow$ expect $\sigma_{sp} < 3 \mu m$
    - 128 columns (discrim) & 8 col. (analog) of 256 rows
    - read-out time $\lesssim 50 \mu s$
  - time stamping side: pixels of $16 \times 64 \mu m^2$ $\Rightarrow t_{r.o.} \sim 10 \mu s$
    - (expect $\sigma_{sp} \sim 6 \mu m$)
    - 128 columns (discrim) and 8 col. (analog) of 64 rows
    - lab tests positive: $N \sim 15 \ e^-$ ENC & discrim. all OK for $t_{r.o.} = 10 \mu s$
  - beam tests (CERN-SPS) in July ’12 $\Rightarrow \sigma_{sp}$

- **MIMOSA-31**: prototype for ILD-VXD outer layers
  - pixels of $35 \times 35 \mu m^2$ (power saving)
  - 48 columns of 64 pixels ended with 4-bit ADC (1/10 of full scale chip)
    $\longleftrightarrow$ expect $\sigma_{sp} \lesssim 3.5 \mu m$
  - $t_{r.o.} \sim 10 \mu s$ (1/10 of full scale chip) $\Rightarrow \sim 100 \mu s$
Motivations for faster read-out:

- robustness w.r.t. predicted 500 GeV BG rate (keep inner radius small, ...)
- standalone inner tracking capability (e.g. soft tracks)
- compatibility with high-energy running: expected beam BG at $\sqrt{s} \gtrsim 1 \text{ TeV} \simeq 3–5 \times \text{BG (500 GeV)}$

How to accelerate the elongated pixel read-out

- elongated pixel dimensions allow for in-pixel discri. $\Rightarrow \geq 2$ faster r.o.
- read out simultaneously 2 or 4 rows $\Rightarrow 2$-4 faster r.o./side
- subdivide pixel area in 4-8 sub-arrays read out in // $\Rightarrow 2$-4 faster r.o./side
- 0.18 $\mu$m process needed: 6-7 ML, design compactness, in-pixel CMOS T, ...
- conservative step: 2 discri./col. end ($22 \mu$m wide) $\Rightarrow$ simult. 2 row r.o.

Expected VXD performances at 1 TeV (and 0.5 TeV)

<table>
<thead>
<tr>
<th>Layer</th>
<th>$\sigma_{sp}$</th>
<th>$t_{int}$</th>
<th>Occupancy [%]</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIMOSA/AROM</td>
<td>MIMOSA/AROM</td>
<td>1 TeV (0.5 TeV)</td>
<td>inst./average</td>
</tr>
<tr>
<td>VXD-1</td>
<td>3 / 5-6 $\mu$m</td>
<td>50 / 2 $\mu$s (10 $\mu$s)</td>
<td>4.5(0.9) / 0.5(0.1)</td>
<td>250/5 W</td>
</tr>
<tr>
<td>VXD-2</td>
<td>4 / 10 $\mu$m</td>
<td>100 / 7 $\mu$s (100 $\mu$s)</td>
<td>1.5(0.3) / 0.2(0.04)</td>
<td>120/2.4 W</td>
</tr>
<tr>
<td>VXD-3</td>
<td>4 / 10 $\mu$m</td>
<td>100 / 7 $\mu$s (100 $\mu$s)</td>
<td>0.3(0.06) / 0.05(0.01)</td>
<td>200/4 W</td>
</tr>
</tbody>
</table>
ALICE-ITS Upgrade

- 2 alternative sensors developed:
  - Baseline: ASTRAL (in-pixel discrim.)
    \[ \geq 15 \, \mu s, \, 85 \, \text{mW/cm}^2 \]
  - Back-up: MISTRAL (end-of-col. discrim.)
    \[ \geq 30 \, \mu s, \, < 200 \, \text{mW/cm}^2 \]

- All main components validated in 2013:
  - Sensing node properties
  - In-pixel ampli+CDS
  - In-pixel discriminators
  - Rolling-shutter with end-of-col. discrim.
  - Simultaneous 2-row read-out
  - Sparse data scan
  - Programmable chip steering (JTAG)
    \[ \rightarrow \text{outcome integrated in ITS-TDR} \]
CPS fabricated in 2012/13 in 0.18 \( \mu m \) Process
- MIMOSA-22THRa1 exposed to ~ 4.4 GeV electrons (DESY) in August 2013

- Analog outputs of 8 test columns (no discr.)

  SNR with HR-18 epitaxy, at T=30°C

  - Noise determination with beamless data taking
  - Ex: S2 (T gate L/W=0.36/1 μm against RTS noise)
  - S1 (T gate L/W=0.36/2 μm against RTS noise)

- Results:

  - Charge collected in seed pixel ≈ 550 e−
  - Detection efficiency of S1 & S2 ≥ 99.5%
    while Fake rate ≤ O(10⁻⁵) for
    Discrimination Thresholds in range ~ 5N → > 10N
  - Mitigation of Fake Hits due to RTS
    noise fluctuations confirmed

  - A few 10⁻³ residual inefficiency may come
    from BT-chip association mismatches
    and non-optimised cluster algorithm
Pixel Optimisation: Epitaxial Layer and Sensing Node

Pixel charge coll. perfo. for HR-18 & VHR-20 (no in-pixel CDS):

- SNR distributions \(\rightarrow\) MPV & low values tail
- \(22 \times 33 \ \mu m^2\) (2T) pixels at \(30^\circ C\)

\[\Rightarrow\] Results:
- only \(\sim 0.1\%\) of cluster seeds exhibit \(SNR \lesssim 7–8\)
- \(SNR(VHR-20) \sim 5\text{-}10\%\) higher than \(SNR(HR-18)\)

Pixel charge coll. perfo. for 2 diff. sensing nodes:

- \(10.9\ \mu m^2\) large sensing diode
- \(8\ \mu m^2\) cross-section sensing diode
  underneath \(10.9\ \mu m^2\) large footprint

\[\Rightarrow\] Results:
- \(8\ \mu m^2\) diode features nearly 20\% higher \(SNR(MPV)\)
  & much less pixels at small \(SNR\) (e.g. \(SNR < 10\))
  \(\Rightarrow\) \(Q_{clus} \simeq 1350/1500\ \text{e}^-\) for \(8/10.9\ \mu m^2\)
  \(\Rightarrow\) marginal charge loss with \(8\ \mu m^2\) diode
- radiation tolerance to \(250\ \text{kRad} & 2.5 \cdot 10^{12} \ n_{eq}/cm^2\) at \(30^\circ C\) OK
Spatial Resolution

- Beam test (analog) data used to simulate binary charge encoding:
  - Apply common SNR cut on all pixels using \( \langle N \rangle \rightarrow \)
    simulate effect of final sensor discriminators
  - Evaluate single point resolution (charge sharing) and
detection efficiency vs discriminator threshold for
  20x20; 22x33; 20x40; 22x66 \( \mu m^2 \) pixels

- Comparison of 0.18 \( \mu m \) technology (\( \geq 1 \ kΩ \cdot cm \))
  with 0.35 \( \mu m \) technology (\( \ll 1 \ kΩ \cdot cm \))

<table>
<thead>
<tr>
<th>Process</th>
<th>Pixel Dim. [( \mu m^2 )]</th>
<th>( \sigma_{sp}^{bin} [\mu m] )</th>
<th>( &gt; 0.35 \mu m )</th>
<th>( &gt; 0.18 \mu m )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.35 ( \mu m )</td>
<td>20.7 \times 20.7</td>
<td>3.7 \pm 0.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.18 ( \mu m )</td>
<td>20 \times 20</td>
<td>3.2 \pm 0.1</td>
<td>( \sim 5 )</td>
<td>5.4 \pm 0.1</td>
</tr>
</tbody>
</table>
DEVELOPMENT OF ULTRA-LIGHT DOUBLE-SIDED LADDERS
Sensor Integration in Ultra Light Devices

2-sided ladders with time stamping for the ILD-VXD:

- Manyfold bonus expected from 2-sided ladders: alignment, pointing accuracy (shallow angle), compactness, redundancy, etc.
- Studied by PLUME coll. (Bristol, DESY, IPHC) & AIDA (EU)

→ Pixelated Ladder using Ultra-light Material Embedding

- Square pixels for single point resolution on beam side
- Elongated pixels for 5-50 times shorter r.o. time on other side
- Correlate hits generated by traversing particles
- Expected total material budget $\sim 0.3 \% X_0$

Prototypes fabricated:

- Based on $2 \times 6$ MIMOSA-26 sensors mounted on each ladder face
- Mechanical support: 2 mm thick low density SiC foam
- Total material budget $\sim 0.6 \% X_0$
- Beam tests at CERN-SPS (traversing m.i.p.) in Nov. ’11
2-Sided Ladder Beam Test Results

- **PLUME prototype-2010 tested at SPS in Nov. 2011:**
  - Beam telescope: 2 arms, each composed of 2 MIMOSA-26 sensors
  - DUT: 1 PLUME ladder prototype (0.6 % $X_0$)
    - 6 MIMOSA-26 sensors on each ladder face (> 8 Mpixels)
  - CERN-SPS beam: $\gtrsim$ 100 GeV "π−" beam
  - BT (track extrapolation) resolution on DUT $\sim$ 1.8 $\mu$m
  - Studies with PLUME perpendicular and inclined ($\sim$ 36°) w.r.t. beam line
  - Preliminary results (no pick-up observed): combined impact resolution & pointing resolution

- **New PLUME proto. under construction with 0.35 % $X_0$ (X-sect.) $\rightarrow$ beam tests in Q4/2014 (SPS ?)
CMOS Pixel Sensors (CPS): A Long Term R&D

- **Initial objective**: ILC, with staged performances
  - CPS applied to other experiments with intermediate requirements

**EUDET 2006/2010**
Beam Telescope

**STAR 2013**
Solenoidal Tracker at RHIC

**ILC > 2020**
International Linear Collider

**ALICE 2018**
A Large Ion Collider Experiment

- EUDET (R&D for ILC, EU project)
- STAR (Heavy Ion physics)
- CBM (Heavy Ion physics)
- ILC (Particle physics)
- HadronPhysics2 (generic R&D, EU project)
- AIDA (generic R&D, EU project)
- FIRST (Hadron therapy)
- ALICE/LHC (Heavy Ion physics)
- EIC (Hadron physics)
- CLIC (Particle physics)
- BESIII (Particle physics)

**CBM > 2018**
Compressed Baryonic Matter
**Plans for the Upcoming Years**

- **R&D Plans on CPS:**
  - realise full scale sensor in 0.18 \( \mu m \) techno. \( \lesssim 20 \mu s \) & MISTRAL \( \gtrsim 30 \mu s \)
  - achieve \( O(1) \) \( \mu s \) time stamping with elongated pixels \( \Rightarrow \) bunch tagging
  - validate concept with 3-bit charge encoding ADC in 0.18 \( \mu m \) techno.
  - study alternative approach using Fine Pixel CPS (4-5 \( \mu m \) pitch)

- **R&D of 2-Sided Ladders:**
  - validate ladder design resulting in 0.35 % \( X_0 \) material budget
  - validate ladder concept based on fast/precise sensors on 1st/2nd face (e.g. ASTRAL & MIMOSA-26)
  - validate power pulsing in high magnetic field
  - investigate 2-sided ladder design allowing for \( < 0.3 \% X_0 \)

- **Framework: R&D Continuation Until Early 2020s**
  - ALICE-ITS until 2016
  - CBM-MVD until 2018
  - MIMOSA-26/-28 users: EUDET-BT, FIRST, EIC, NA-61, NA-63, BES-III, biomedical & X-Ray-imaging, dosimetry, hadrontherapy, ...
  - H2020, LIA, ...
Plans for the Upcoming Years

2014:
- Sensors: realise & validate full scale architectures for ALICE-ITS (ASTRAL ans MISTRAL)
- Ladders: realise and test 0.35 \( \times X_0 \) 2-sided ladder based on MIMOSA-26

2015:
- Sensors: realise final prototype for the ALICE-ITS
- Ladders: test of vertex detector "sector" ≡ 3 consecutive pairs of ladders on beam

2016:
- Sensors: production tests of ALICE-ITS sensors evolve towards CBM-MVD/FAIR (ASTRAL)
- Ladders: realise 2-sided ladder equipped with 2 different chips (e.g. ASTRAL / MIMOSA-26)

2017:
- Sensors: follow ITS production, production of sensors for CBM-MVD (FAIR)
- Ladders: beam tests of 2-sided ladder equipped with 2 different chips

2018: Start realisation of large sensors dedicated to ILC VXD
Overview of the IPHC Team

- **4 Physicists:**
  - 2 University staff: J. Baudot, A. Besson
  - 1 CNRS staff: M. Winter
  - 1 Postdoc: A. Perez Perez

- **10 Electronics and Micro-technics Engineers:**
  - PICSEL group: G. Claus, M. Goffe, Ch. Illinger, K. Jaaskelainen, M. Specht, M. Szelezniak
  - Micro-technics group: M. Imhoff, O. Clausse, J.S. Pelle, F. Agnese

- **13 Chip Designers:**
  - University: G. Dozière
  - 3 PhD students: T.Y. Wang, W. Zhao, Y. Zhou

- **Scientific Production since 2008:**
  - 79 talks at international conferences
  - 31 publications in NIM, IEEE, etc. journals
  - 9 PhD theses defended since 2008 (3 under way)
SUMMARY

- **R&D ON CPS:**
  - Well established architecture achieved and implemented in STAR-PXL (0.35 μm CMOS process)
    - extendable to sensors suited to ILD-VXD \( \lesssim 500 \text{ GeV} \)
  - Not accessible with 0.35 μm process: standalone tracking, bunch tagging (SiD), 1 TeV running, etc.
    - 0.18 μm process accessed in 2011 should allow meeting these goals
  - 2012-13 allowed assessing process & realising all major sensor architecture elements
    - Realisation of complete ASTRAL sensor in 2014 (ITS)
  - Upcoming years: beyond 2014
    - Final ALICE-ITS sensor & CBM-MVD variant (include all main elements for ILD-VXD)
      - ILC dedicated sensors in 0.18 μm process from 2017/18 on
    - Investigate FPCPS delayed read-out approach

- **2-SIDED LADDERS: PLUME collaboration**
  - Prototype based on MIMOSA-26 sensors on the way to achieve 0.35 % \( X_0 \)
  - Upcoming years: beyond 2014
    - Validate concept of complementary sensors with ASTRAL/MIMOSA-26 & power pulsing in string mag. field
    - Assess added value of double-sided ladders
    - Investigate possibilities to still reduced the ladder material budget \( < 0.3\% \ X_0 \)
BACK-UP SLIDES
Main Features of CMOS Sensors (CPS)

- P-type Si hosting n-type "charge collectors"
  - signal created in epitaxial layer (low doping):
    \[ Q \sim 70-80 \text{ e-h/ \( \mu m \)} \Rightarrow \text{signal} \lesssim 1000 \text{ e}^- \]
  - charge sensing through n-well/p-epi junction
  - excess carriers diffuse and/or drift to diode
    with help of reflection on boundaries
    with p-wells and substrate (high doping)
    \[ \Rightarrow \text{continuous signal sensing (no dead time)} \]

- Prominent advantages of CMOS sensors:
  - **granularity**: pixels of \( \lesssim 10 \times 10 \text{ \( \mu m \)}^2 \Rightarrow \text{high spatial resolution (e.g.} \lesssim 1 \text{ \( \mu m \)} \text{ if needed)}
  - **low material budget**: sensitive volume \( \gtrsim 10 - 20 \text{ \( \mu m \)} \Rightarrow \text{total thickness} \lesssim 50 \text{ \( \mu m \)} \Rightarrow \text{thinning} \lesssim 50 \text{ \( \mu m \)}
  - **signal processing \( \mu \text{circuits integrated in the sensors} \Rightarrow \text{compacity, high data throughput, flexibility, etc.}
  - **industrial mass production** \( \Rightarrow \text{cost, industrial reliability, fabrication duration, multi-project run frequency, technology evolution, etc.}

- Main limitation of the approach: CMOS industry addresses a market far from HEP needs
  - fab. process parameters not optimised to fully exploit the potential of CPS
  - **BUT** recently accessible processes (epitaxial layer, feature size) have opened up new perspectives

Since a few years: high resistivity (> 1 \( k\Omega \cdot \text{cm} \)) epitaxial layer

Main limitation of the approach: CMOS industry addresses a market far from HEP needs

- fab. process parameters not optimised to fully exploit the potential of CPS
- **BUT** recently accessible processes (epitaxial layer, feature size) have opened up new perspectives
CMOS Pixel Sensors: Present Status

- **Established Architecture:**
  - CMOS process: 0.35 \( \mu m \), 2-well, 4 ML, 15/20 \( \mu m \) & \( \sim 1 \text{k}\Omega \cdot \text{cm} \) EPI
  - in-pixel CDS
  - end-of column discrim. (binary encoding)
  - single-row rolling shutter read-out
  - sparse data scan on chip periphery
  - 18.4/20.7 \( \mu m \) pitch \( \Rightarrow \sim 3.3.5 \mu m \) resolution
  - used in EUDET BT (115 \( \mu s \)) & STAR-PXL (190 \( \mu s \))
    - **recent step:** Commissioning of 3/10 STAR-PXL completed at RHIC with pp & ArAr collisions in May-June 2013

- **New Process Under Study Since 2011/12:**
  - CMOS process: 0.18 \( \mu m \), 4-well, 6 ML, 15/40 \( \mu m \) & \( \sim 1-6 \text{k}\Omega \cdot \text{cm} \) EPI
  - allows in-pixel discrimination \( \Rightarrow \) faster read-out & reduced power, etc.
  - development driven by ALICE-ITS upgrade & CBM-MVD/FAIR (\( \sim 20 \mu s \))
    - **recent step:** Assessment of CMOS process detection performances & validation of rolling-shutter read-out completed in 2013
Faster read-out for:

- robustness w.r.t. predicted 500 GeV BG rate (keep small inner radius, ...)
- standalone inner tracking capability (e.g. soft tracks)
- compatibility with high-energy running:
  expected beam BG at $\sqrt{s} \gtrsim 1$ TeV $\approx 3-5 \times$ BG (500 GeV)

Moving to a 0.18 $\mu m$ imaging CMOS process:

- Deep P-well & 6 metal $\Rightarrow$ in-pixel discri. (AROM sensor)
- Epi. layer: 18–40 $\mu m$ thick, $\rho \sim 1-6$ k$\Omega \cdot cm$
- Stiching $\Rightarrow$ multi-chip slabs (yield ?)

2013 (beam) test results:

- 12 diff. chips exploring sensing + r.o. fab. in 2013
Fine Pixel CCDs: Main Features

Prominent Features of FPCCDs:

- Signal charge created in a fully depleted ~ 15 \( \mu m \) thin epitaxial layer
  - limited charge spread
- Very small pixels (5 \( \times \) 5 \( \mu m^2 \)):
  - \( \sigma_{sp} \lesssim 1 \mu m \)
  - beam related BG rejected by pattern recognition
- High-res epi and small pixels (occupancy/BX ~ few ppm) used to integrate over full train duration
  - devt addresses very low power ADCs
- Can be thinned down to 50 \( \mu m \)
- Need -40\(^\circ\)C cooling for radiation tolerance purposes
  - impact on material budget (modest ?)

Several Essential R&D Topics Addressed:

- 5 \( \times \) 5 \( \mu m^2 \) pixel matrix detection performances
- Low power, large bandwidth, r.o. electronics (e.g. 8-bit? ADC)
- Low mass CO\(_2\) cooling

Approach not limited to CCDs: should work with CMOS sensors (cost effective, smaller pixels, cooling)
**Chronopixel Sensors: Main Features**

- **Prominent Features of CMOS Pixel Sensors:**
  - CMOS Pixel Sensor with in-pixel (single BX) 12-bit time stamping
    - tracking based on Vx detector seed (SiD option)
  - Read-out delayed in between consecutive bunch trains (power saving)
  - Double-hit timestamping possibility (25 \times 25 \mu m^2 pixels)

- **Requires a Very Advanced (Mixed?) CMOS Technology:**
  - VDSM (\leq 90 \text{ nm}, with deep P-well), for high \( \mu \)circuitry density
    - trade-off: pixel size (occupancy) vs in-pixel circuitry complexity
  - Epitaxial layer: thick and resistive enough for cluster spread and SNR

- **Customized Design in Industry (Sarnoff):**
  - cost, design optimisation possibility, devt timeline, ...
DEPFET Sensors: Main Features

**Prominent features of DEPFET pixel sensors:**
- Signal charge created in a fully depleted Si substrate and collected by a n-type node ("internal gate") buried under a p-channel FET, delivering a current modulated ($\propto$) by the charge collected on the node
- External gate to enable read-out $\Rightarrow$ r.o. chips
- Clear contact removes charge from internal gate $\Rightarrow$ switcher chip
- Steering and signal processing ASICs bonded on ladder edge & end
- Read-out based on rolling shutter mode $\Rightarrow$ low power
- High granularity $\Rightarrow$ micronic spatial resolution
- Can be thinned down to 50 $\mu$m.
- Sensors are embedded in Si mechanical support $\Rightarrow$ low material budget

**Technology under prod/devt for the Belle-II vertex detector:**
- Several specs close to those of the ILD-VXD inner layer (e.g. $< 0.2\% \times \sigma$)
- Granularity $\times$ speed still to improve
Activités du Groupe PICSEL

- **CAPTEURS À PIXELS CMOS (CPS) POUR LE STAR-PXL:**
  - 400 capteurs MIMOSA-28 (9·10⁵ pix., 200 µs, σsp ∼ 3.5µm)
  - installation d’un détecteur de 3 sect./10 le 8 mai 2013 à RHIC
  - mise en service avec coll. pp depuis le 9 mai
  - implication IPHC actuelle: 1 IR Elec. (+ suivi des concepteurs)

- **CPS POUR L’ITS-2020 D’ALICE:** MISTRAL (30µs) & ASTRAL (∼ 15µs)
  - 7 (baseline) ou 3 couches (∼ 9 m²) pixellisées (∼10¹⁰ pixels)
  - dévt de CPS en techno. CMOS-0.18µm en coll. avec CERN et al.
  - 2012: techno validée au niveau du pixel (1 MRad † 10¹³ neq/cm² à 30°C)
  - 2013-14: prototypage pour valider l’architecture globale avec sparsification
  - implication IPHC actuelle: 6-7 Ing. µElec., 3-4 Ing. Elec., 3 phys. (1 prof.)
  - coll. avec Univ. Frankfurt pour le MVD(CBM): même CPS (vide, T < 0°C)

- **DÉVTS POUR UN DÉT. DE VERTEX À L’ILC:** DBD EN Q1/2013
  - adaptation des CPS(ALICE) pour ILC-500 puis ILC-1000 (∼ 2 µs)
  - dévt d’échelles ultra-légères simple- & double-face
  - études d’optimisation de la géométrie du détecteur
Activités du Groupe PICSEL

- **ACCOMPAGNEMENT DES APPLICATIONS DE MIMOSA-26** *(Télescope EUDET → 6-7 exemplaires)* :
  - Déf. Vx (FIRST/GSI)
  - Proto. MVD (CBM/FAIR)
  - Déf. Vx (NA-61/SPS ≥ 2013)
  - Dosimétrie en ligne à protons (ANR QAPIVI, etc.)

- **CONTRIBUTIONS AUX APPLICATIONS DE MIMOSA-28** *(STAR-PXL)* :
  - Imageur protons (TraCal) au GSI/Bio
  - Proto. télescope AIDA (WP-9.3)
  - Proto. tracker BESS-3 (FCPPL)

- **AIDA (FP-7)**
  - dév d’un capteur abouté de $4 \times 6 \text{cm}^2$ pour télescope final
    → démonstrateur Déf. Vx eRHIC (LDRD BNL)
  - réalisation d’un secteur simplifié de Déf. Vx pour l’ILC équipé d’échelles PLUME
    → études d’alignement micronique
  - dév d’une connectique de haute densité pour capteurs à 2 couches (3DIT)
    → coll. avec institut Fraunhofer

- **PROBIM (COLL. IMNC) : EN ÉMERGENCE**
  - imagerie $\beta$ avec sources internes : dépôt éventuel d’un projet ANR en 2014

- **IMAGEUR X : ACTIVITÉ EN EMERGENCE**
  - dév d’un spectromètre à rayons X dérivé de MISTRAL/ASTRAL (couche épitaxiée de $30–40 \mu m$ hautement résistive