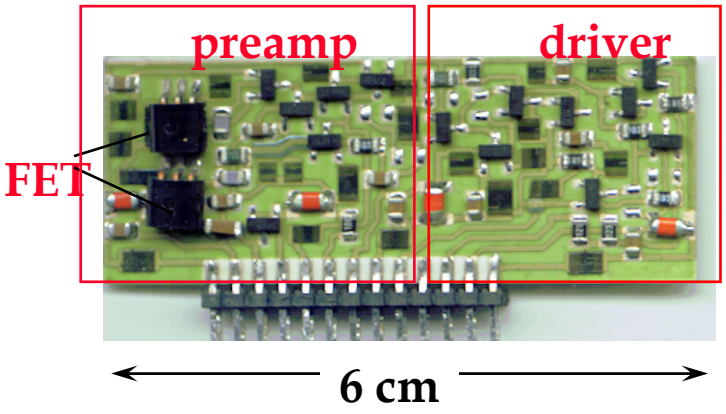
Microelectronics at IN2P3 & IRFU

C. de La Taille

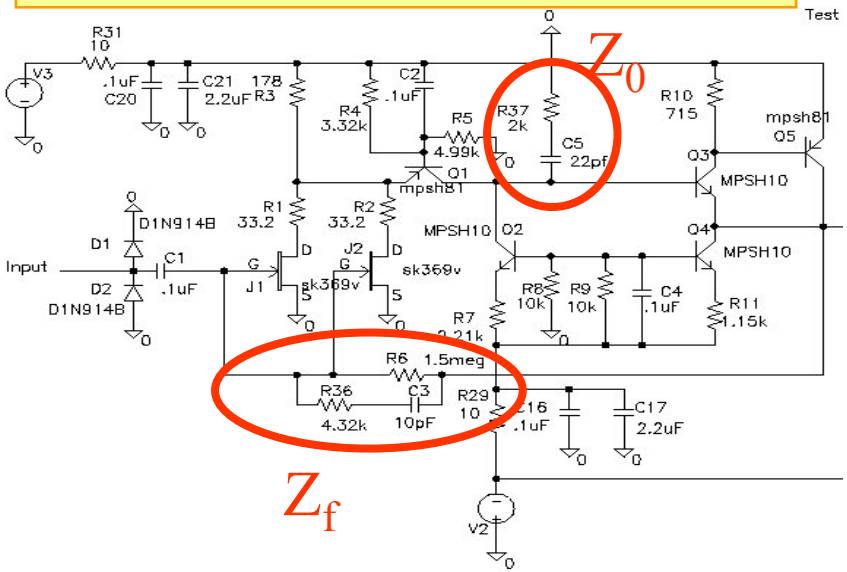
IN2P3 Micro-Electronics Coordinator

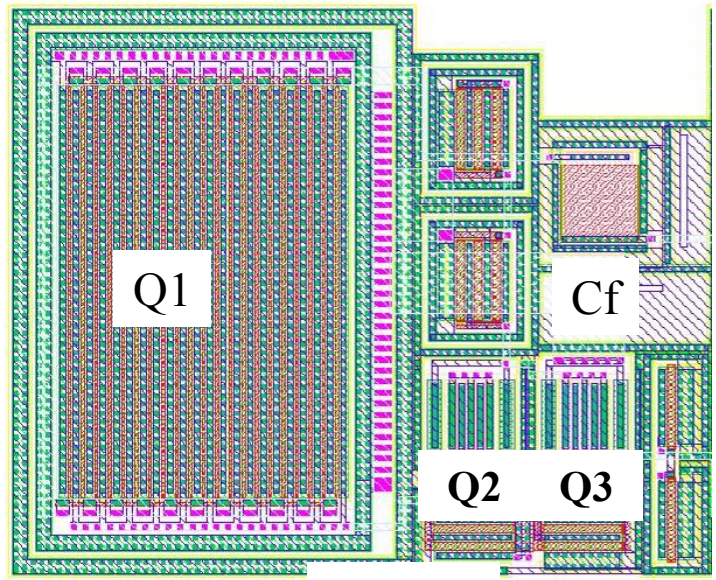
(R)evolution of analog electronics (1)

- Acces to microelectronics

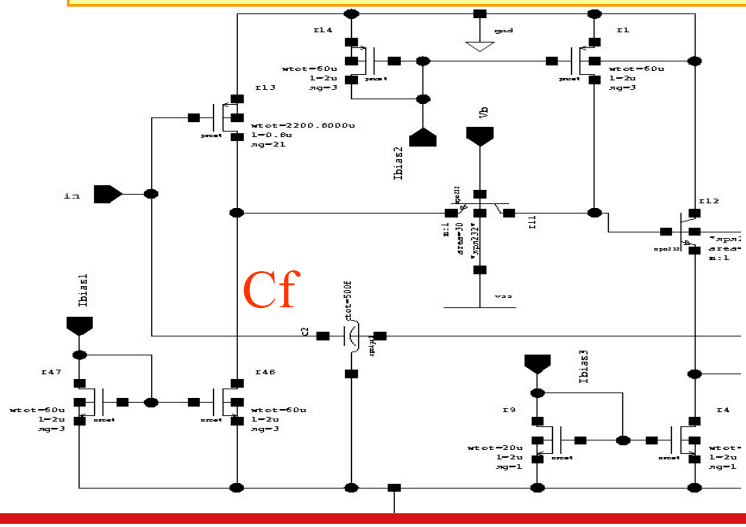


Charge preamp in SMC hybrid techno





Charge preamp in 0.8µm BiCMOS

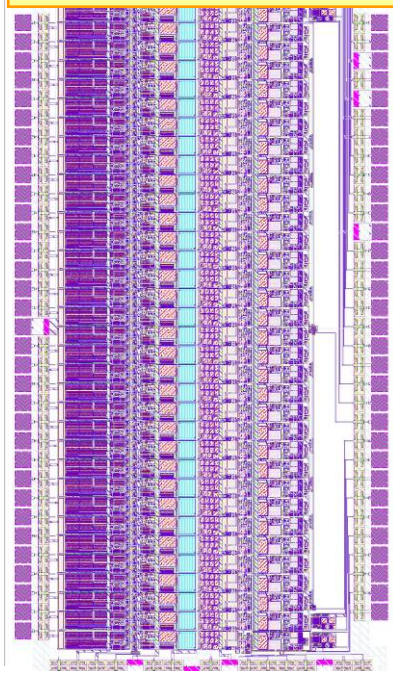


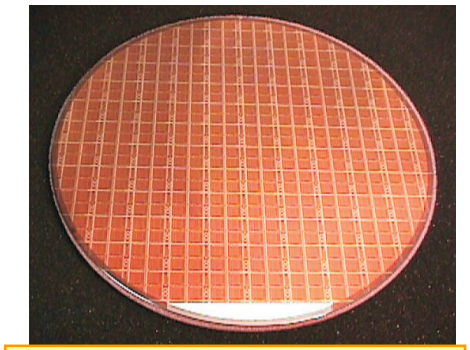
(R)evolution of analog electronics (2)

- ASICs : Application Specific Integrated Circuits
  - Access to foundries through multiproject runs (MPW)
  - Reduced development costs : 600-10000 €/mm^2 compared to dedicated runs (100-1000 k€)
  - Full custom layout, at transistor level
  - mostly CMOS & BiCMOS

- Very widespread in high Energy Physics
  - High level of integration, limited essentially by power dissipation and parasitic couplings (EMC)
  - Better performance : reduction of parasitics
  - Better reliability (less connections)
  - But longer developpement time

Layout 32ch ASIC

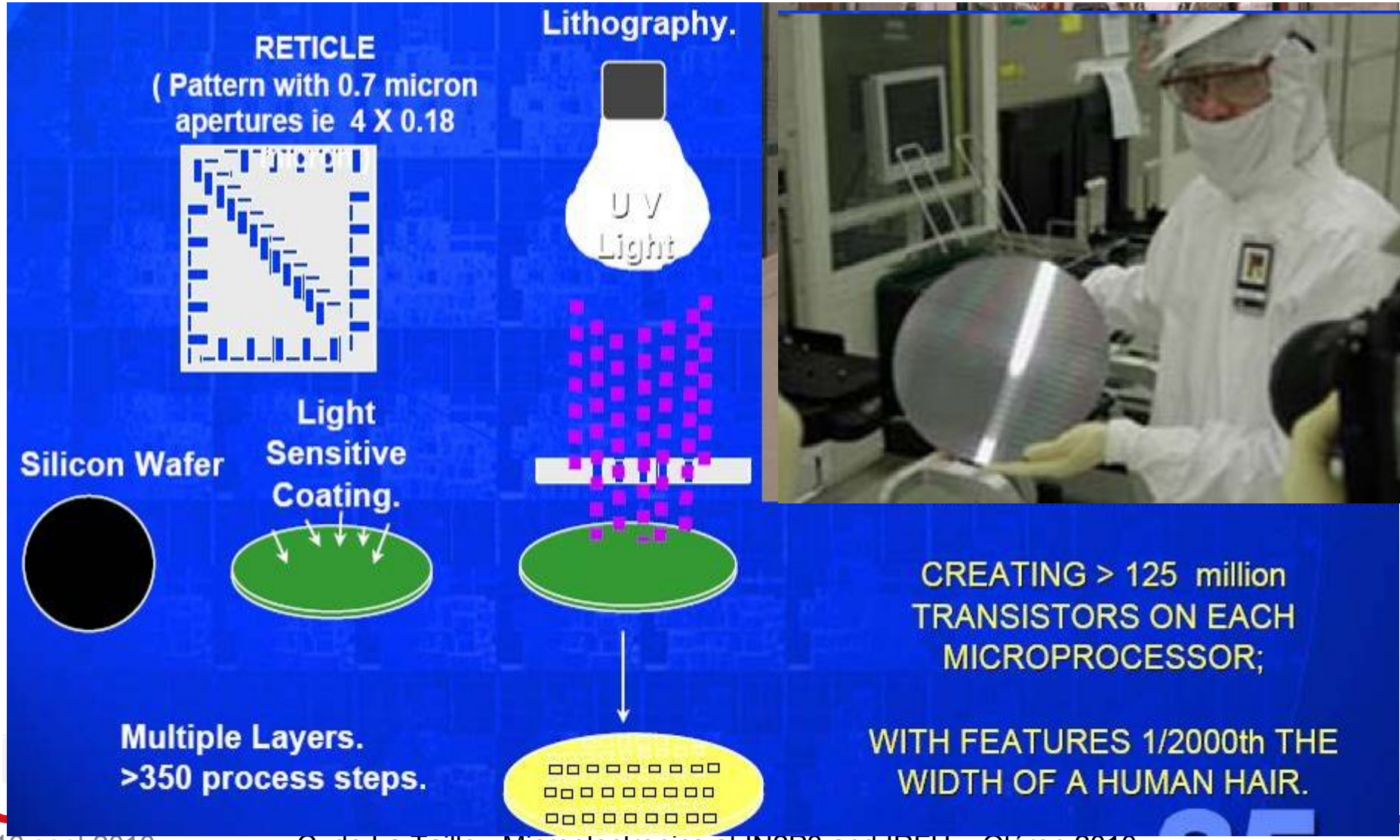




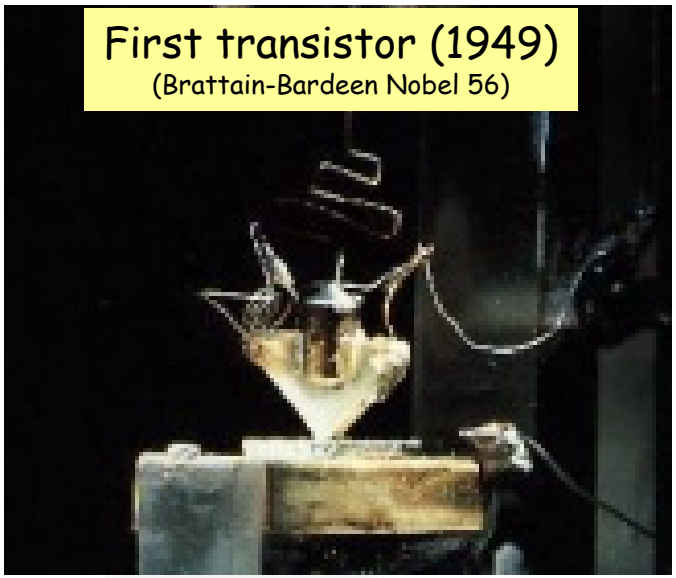
300 mm wafer (IBM)

Processing of ASICs

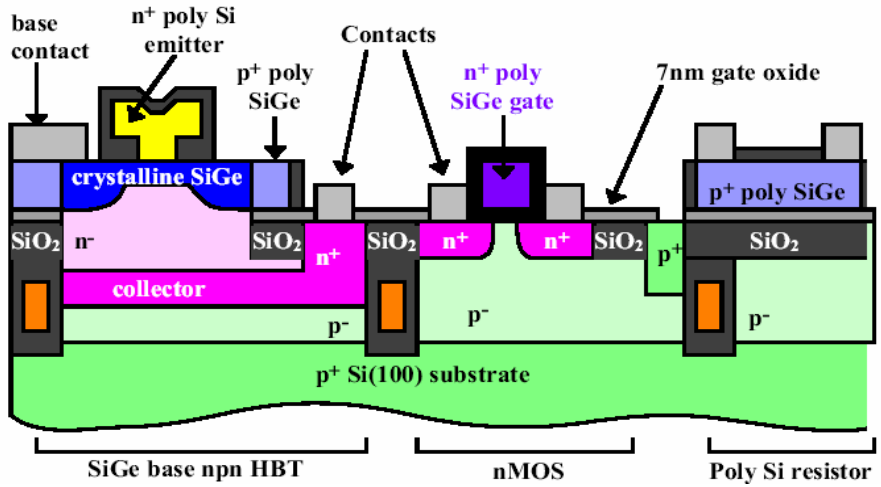
- From Sand to ICs…



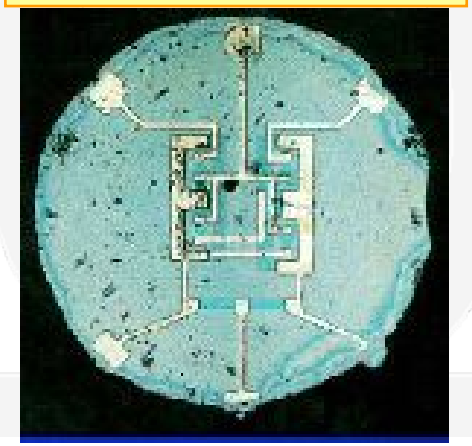
Evolution of technologies



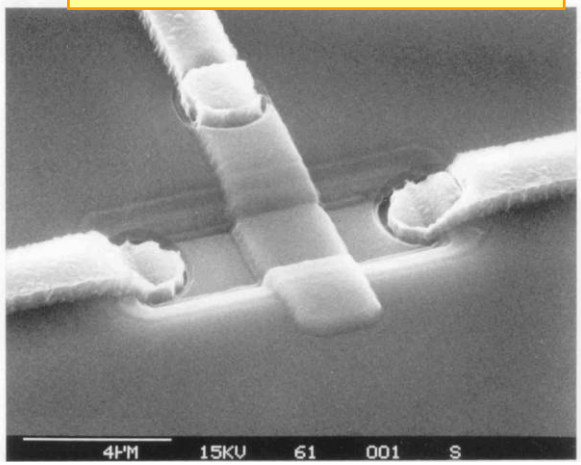
SiGe Bipolar in 0.35µm monolithic process



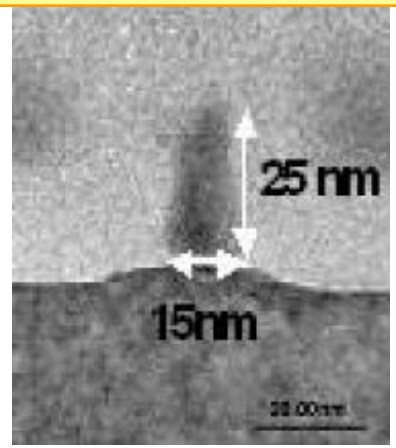
First planar IC (1961)



5 µm MOSFET (1985)

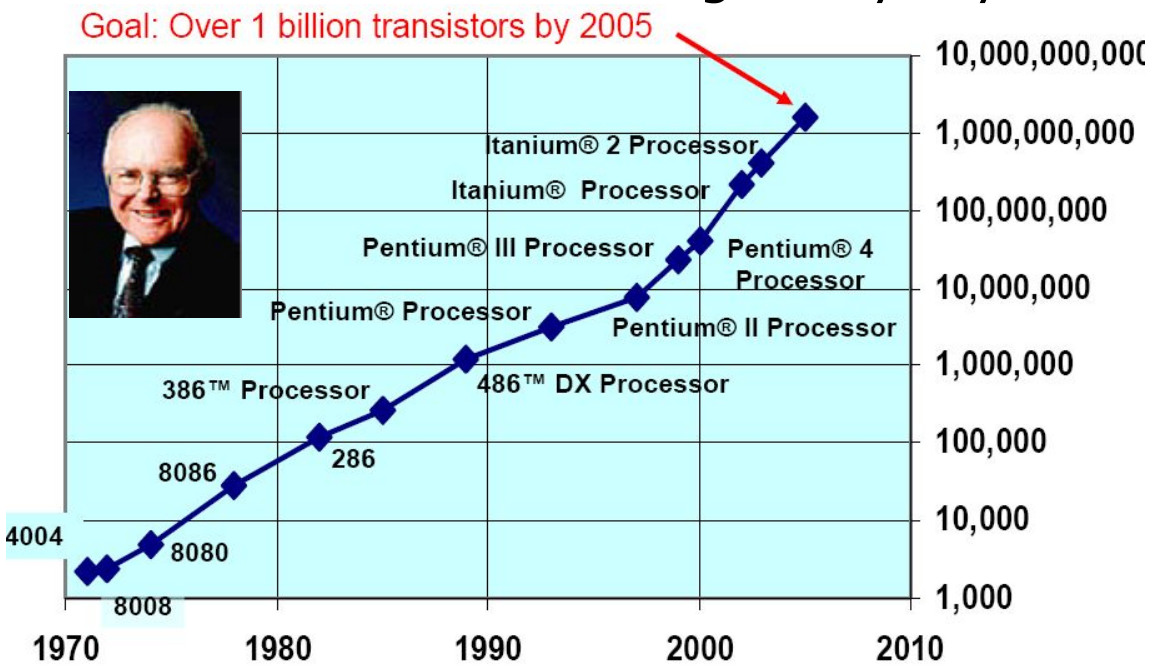


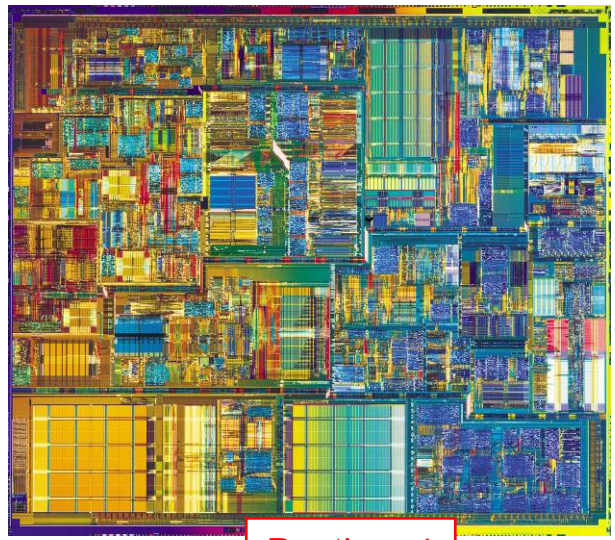
15 nm MOSFET (2005)



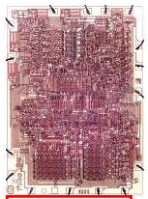
Evolution of CMOS technologies

- Moore's law : doubling every 2 years





Pentium 4

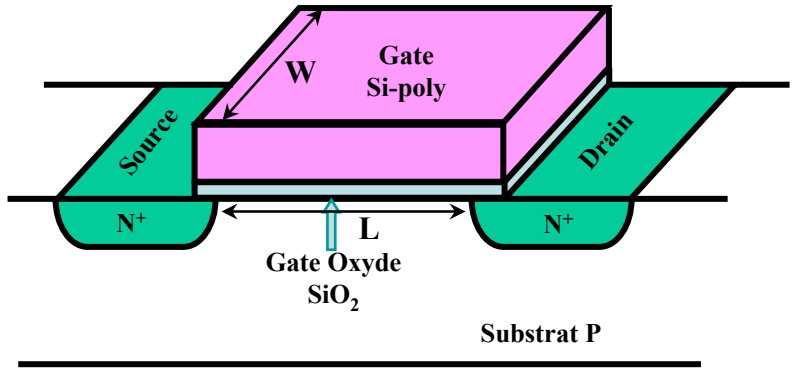


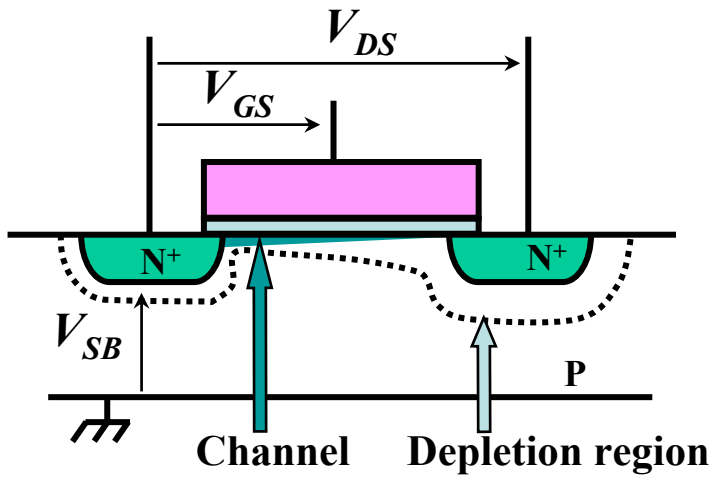
4004

Microprocesseur	4004	8086	i386	Pentium	Pentium 4
Année	1971	1978	1985	1993	2000
Nb. Bits	4	16	32	64	64
Horloge (Hz)	108k	10M	33M	66M	1.5G
Mémoire adressable (bytes)	640	1M	16M	4G	64G
Technologie (µm)	10	3	1	0.8	0.18
Nb transistors	2300	29000	275000	3.1M	42M
Tension alim (V)	12	5	5	5/3.3	1.3 interne

CMOS scaling

- Reduction of dimensions
  - Gate length : L
  - Oxide thickness : t_{ox}
- Reduction of power supplies
  - Reduction of power dissipation
- Improvement of speed in $1/L^2$
  - Transconductance : g_m α W/L
  - Capacitance : C α WL
  - speed : $F_T = g_m/C$ α $1/L^2$
- Reduction of costs (?)
  - Increase of integration density
- Radiation hardness in bonus !
  - Less trapping in gaye oxide

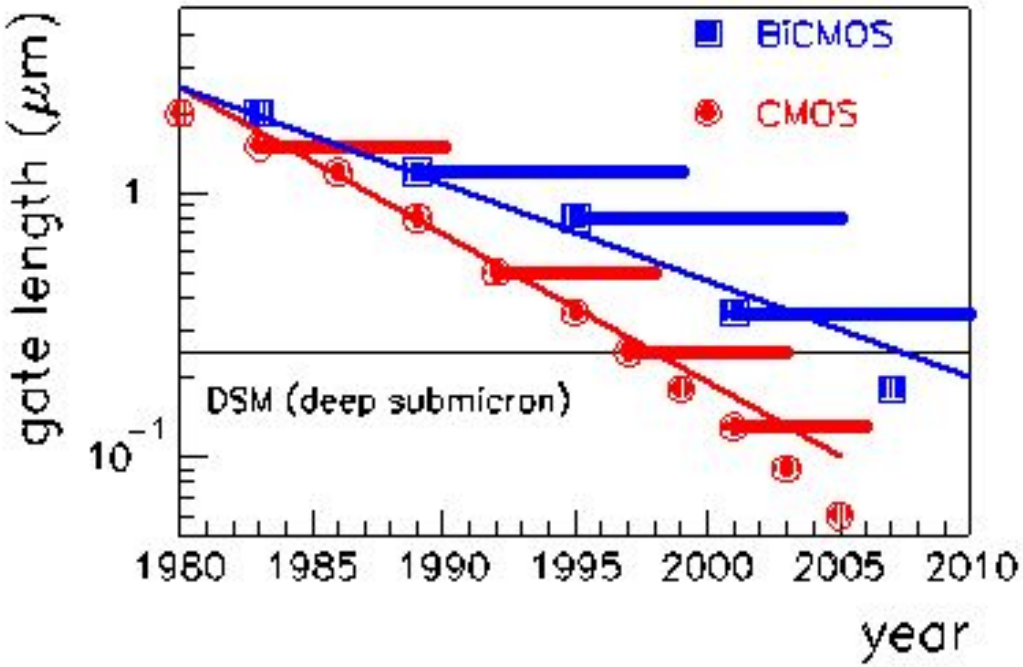


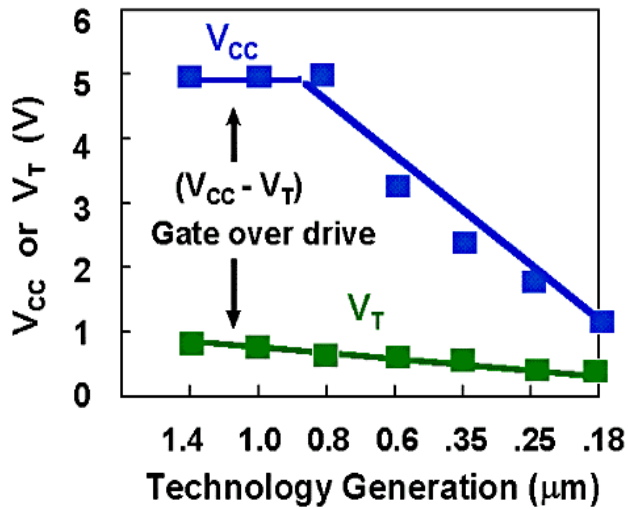


Principle of Nchannel MOSFET

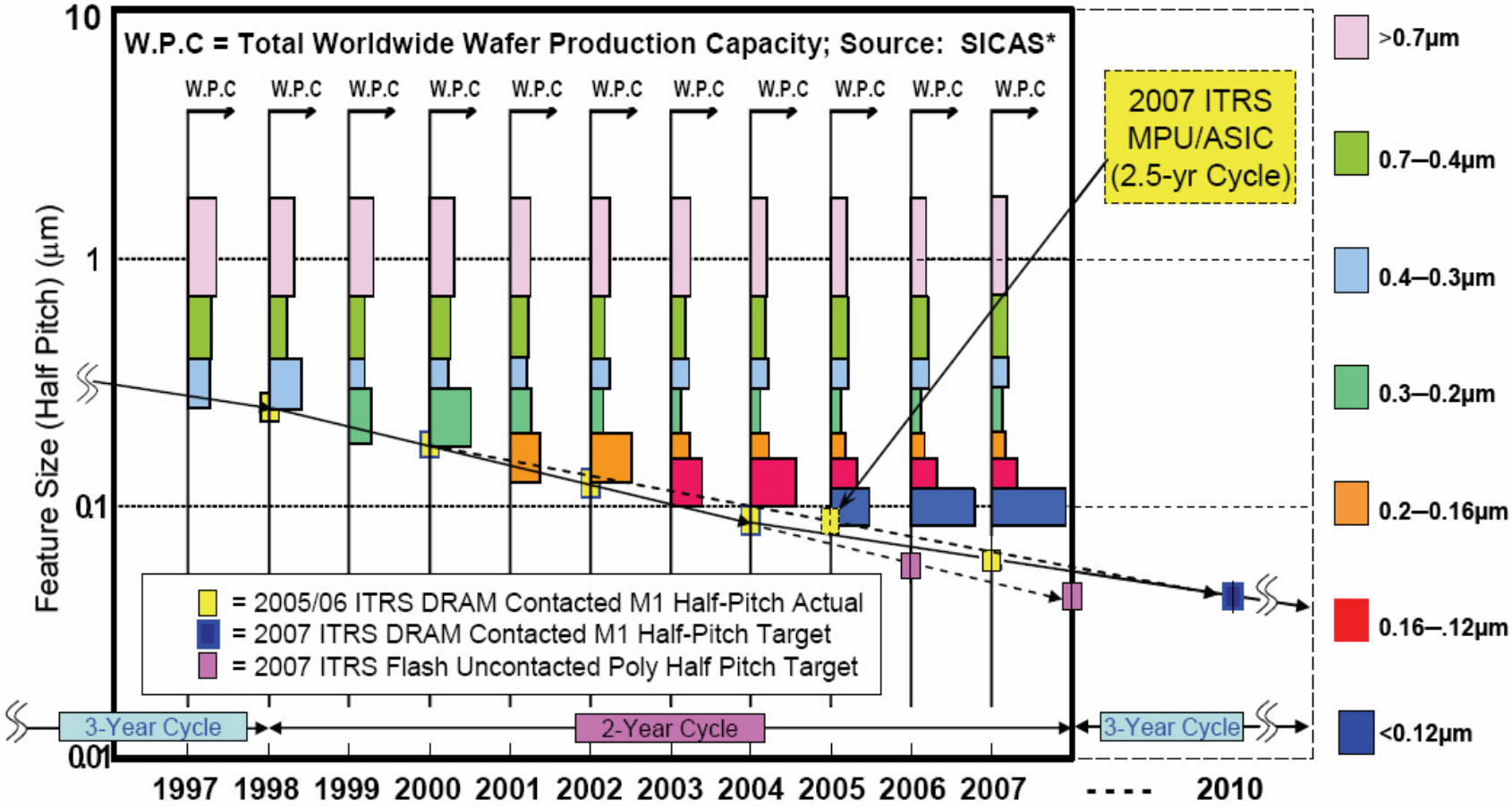
Evolution of CMOS technologies (2)

- Differences between analog/mixed signall and digital technologies
  - Very fast evolution of digital technologies (faster design migration)
  - More « perene » analog technologies (SiGe, BiCMOS…) (driven by mobile telecom and automotive)
  - A visible split occuring
- More difficult analog design in low voltage
  - « no more headroom for signals »



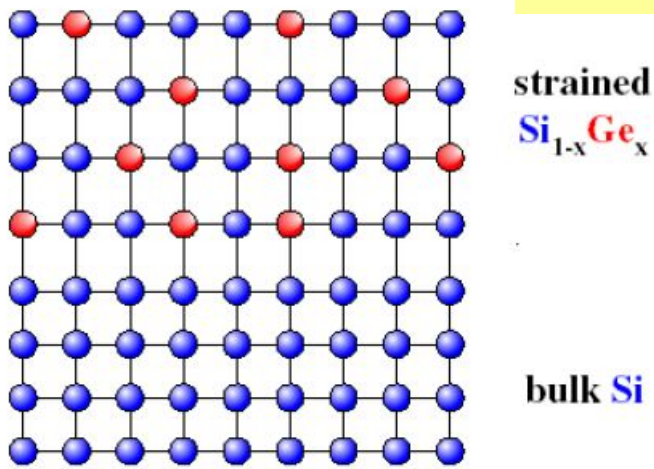


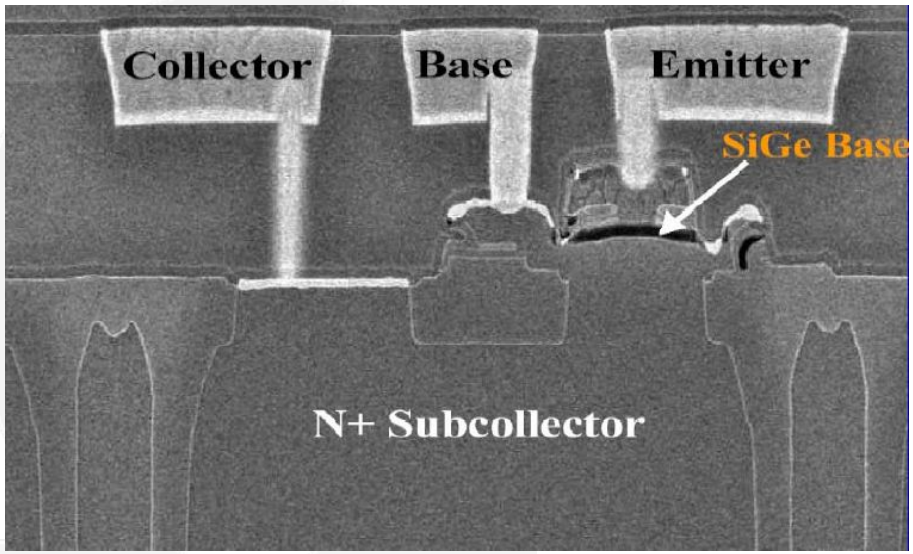
Semiconductor Industry Roadmap

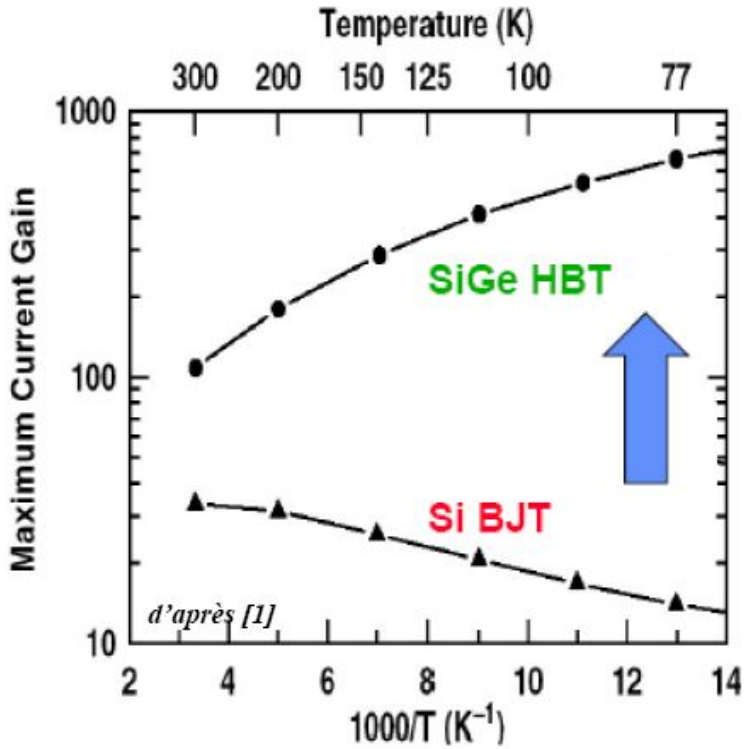


SiGe technology

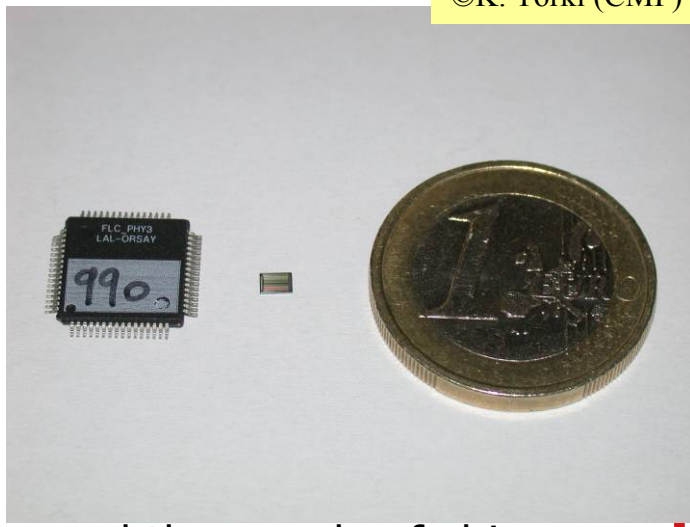
- Faster bipolar transistors for RF telecom
  - Better mobility and FT
  - Better current gain (beta)
  - Better Early voltage
  - Interesting improvement at low T
  - Compact CMOS (0.25 or 0.35µm) for mixed-signal design







Cost of ASICs



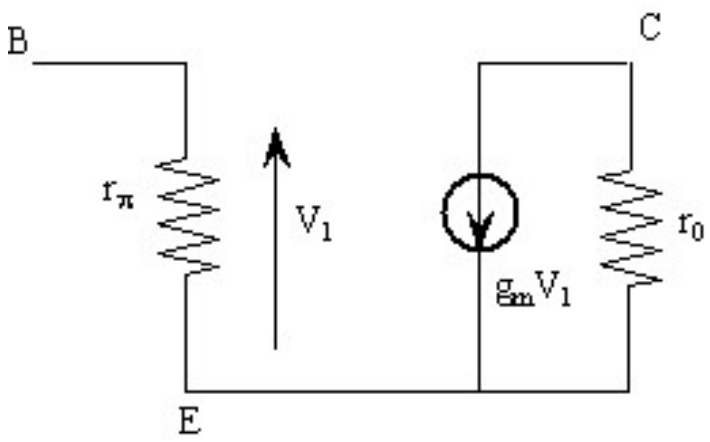
©K. Torki (CMP)

- MPW (multi-project wafers)
  - CMOS 0.35µm (AMS) : 650 €/mm^2
  - BiCMOS SiGe 0.35 µm (AMS) : 900 €/mm^2
  - CMOS 0.13µ (STm) : 2500 €/mm^2
  - CMOS 90 nm (STm) : 5000 €/mm^2
  - Usually a few 10 to 100 pieces in a MPW run
- Production runs
  - Masks : 91 k€ (CMOS 0.35µm)
  - 8" wafers : 4 k€, useful area : 25 000 mm^2 = several thousands of chips
- Packaging
  - Ceramic : 20-30€/chip
  - Plastic : 2k€ + 1-2 €/chip
- Example : chip 10mm^2 16 channels
  - 100 chips (MPW) : 120€/chip, 7€/channel
  - 10 000 chips (4wafers) : 12€/chip < 1€/channel

Design in micro-electronics

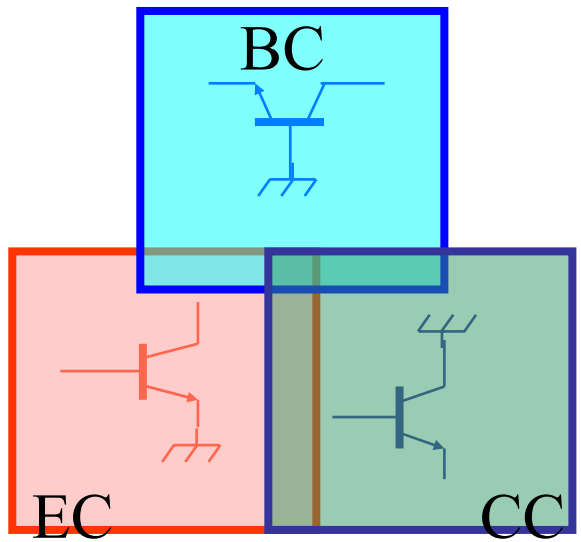
- performant design is at transistor level

- Simples models
  - Hybrid π model
  - Similar for bipolar and MOS
  - Essential for desgin



Low frequency hybrid model of bipolar

- Three basic bricks
  - Common emitter (CE) = V to I (transconductance)
  - Common collector (CC) = V to V (voltage buffer)
  - Common base (BC) = I to I (current conveyor)

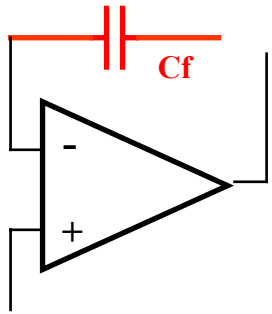


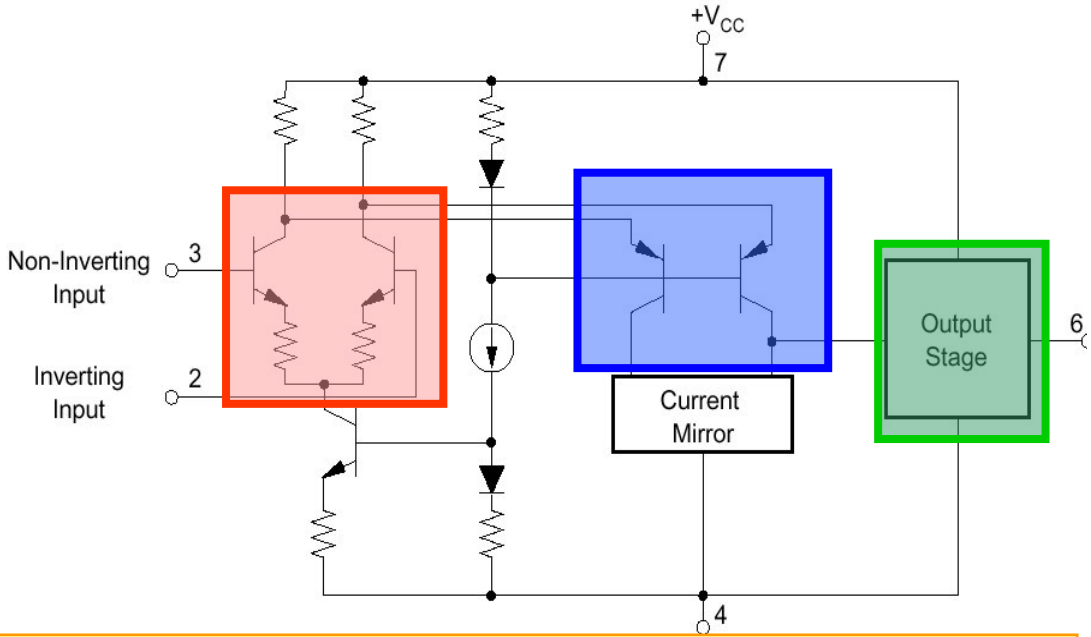
- Numerous « composites »
  - Darlington, Paraphase, Cascode, Mirrors

The *Art* of electronics design

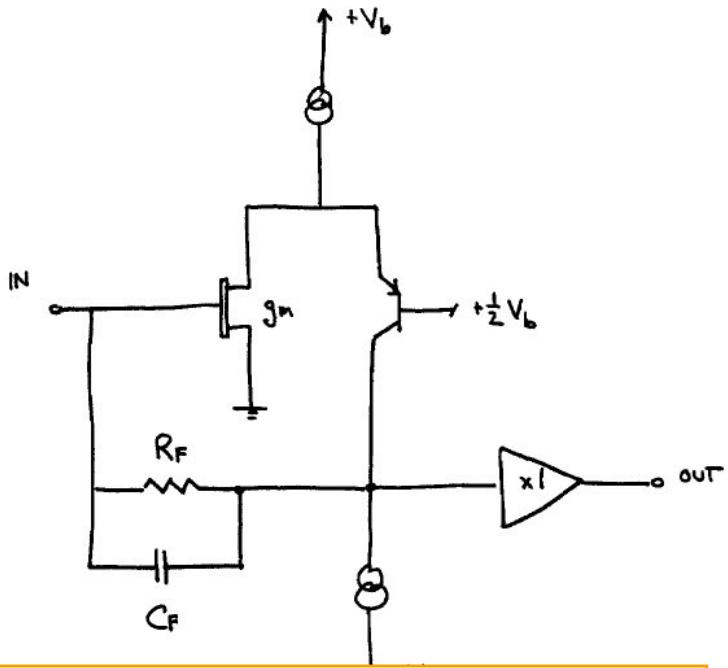
Example : designing a charge preamp (1)

- From the schematic of principle
  - Using of a fast opamp (OP620)
  - Removing unnecessary components…
  - Similar to the traditionnal schematic «Radeka 68 »
  - Optimising transistors and currents





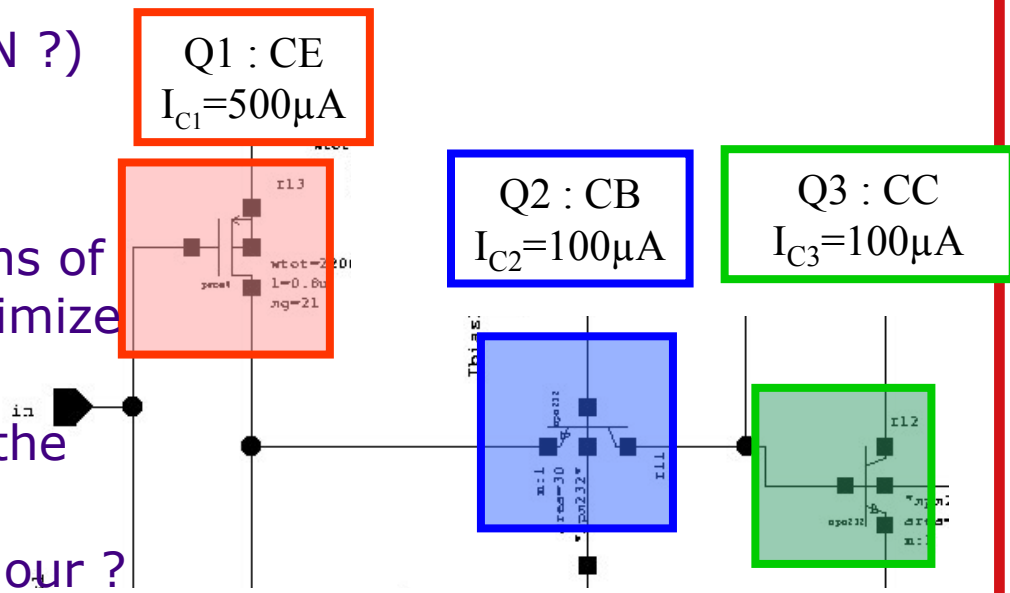
Schematic of a OP620 opamp ©BurrBrown



Charge preamp ©Radeka 68

Example : designing a charge preamp (2)

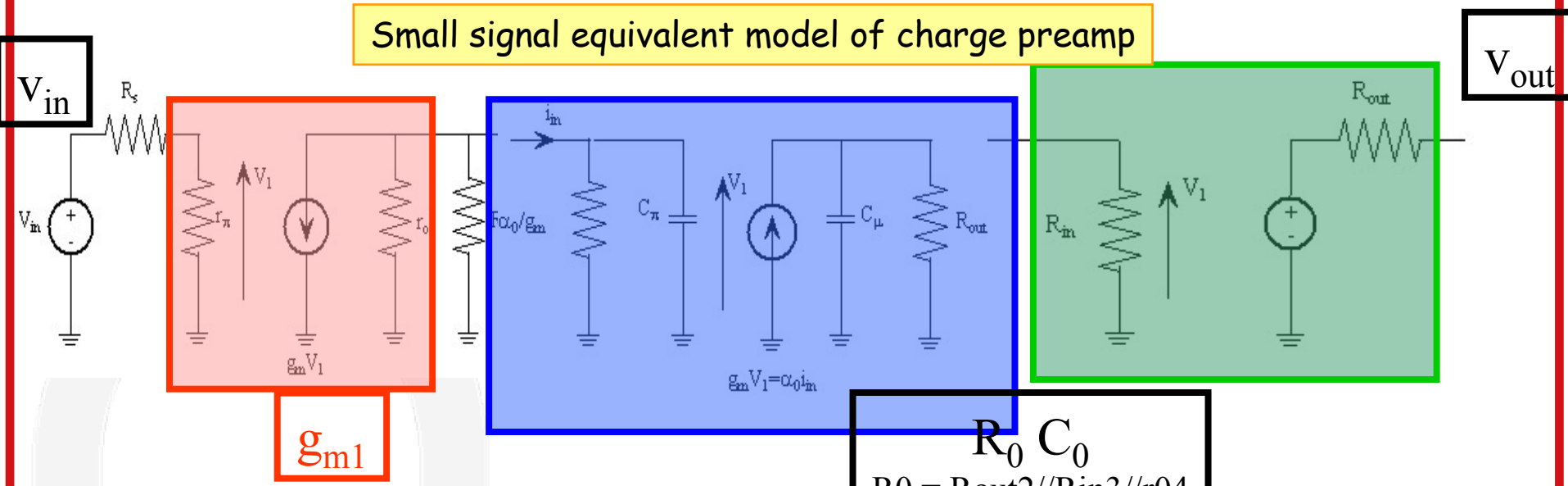
- Simplified schematic
- Optimising components
  - What transistors (PMOS, NPN ?)
  - What bias current ?
  - What transistor size ?
  - What is the noise contributions of each component, how to minimize it ?
  - What parameters determine the stability ?
  - Waht is the saturation behaviour ?
  - How vary signal and noise with input capacitance ?
  - How to maximise the output voltage swing ?
  - What the sensitivity to power supplies, temperature…



Simplified schematic of charge preamp

Example : designing a charge preamp (3)

- Small signal equivalent model
  - Transistors are replaced by hybrid π model
  - Allows to calculate open loop gain



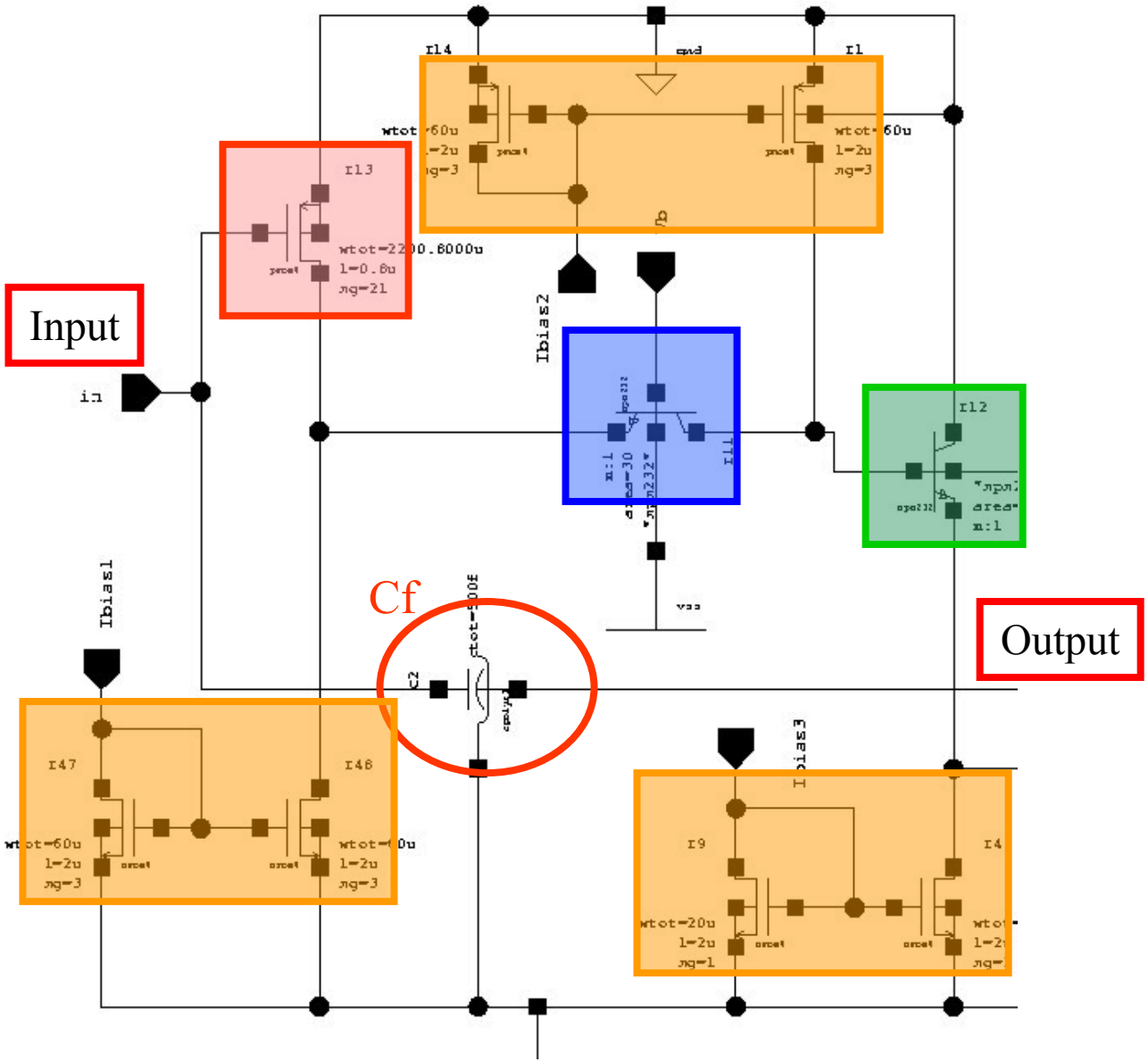
- **Gain (open loop) :**

$$v_{out}/v_{in} = - g_{m1} R_0 /(1 + j\omega R_0 C_0)$$

- *Ex : g_{m1}=20mA/V , R_0=500kΩ, C_0=1pF => G_0=10^4 ω_0=210^6 $G_0\omega_0$=$2\ 10^{10}$ = 3 GHz !*

Example : designing a charge preamp (4)

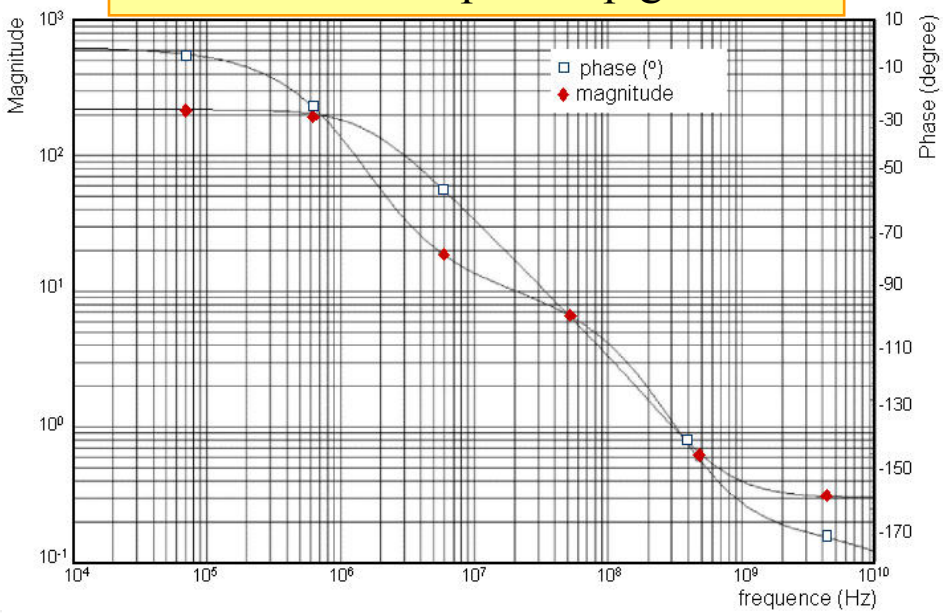
- Complete schematic
  - Adding bias elements



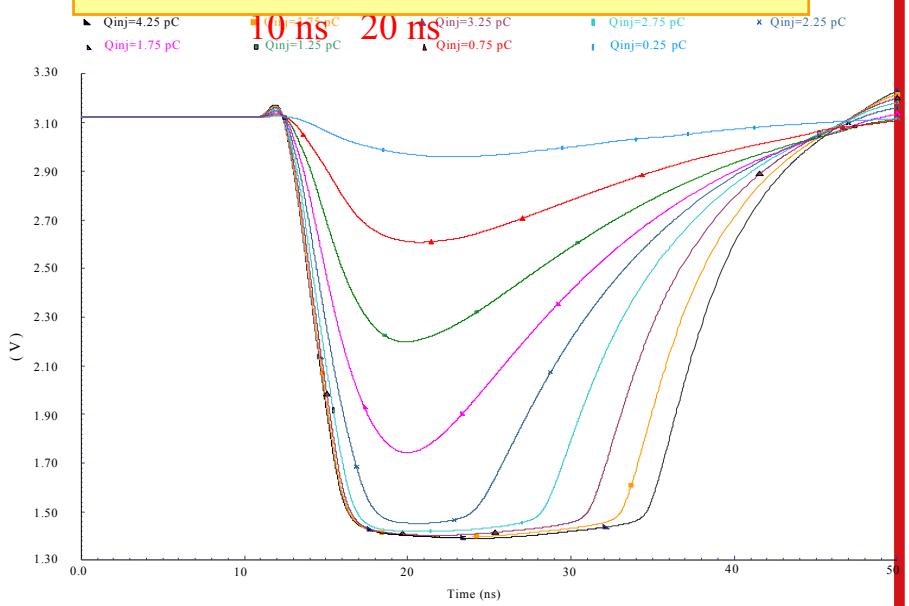
Example : designing a charge preamp (5)

- Complete simulation
  - Checking hand calculations against 2nd order effects
  - Testing extreme process parameters (« corner simulations »)
  - Testing robustness (to power supplies, temperature…)

Simulated open loop gain



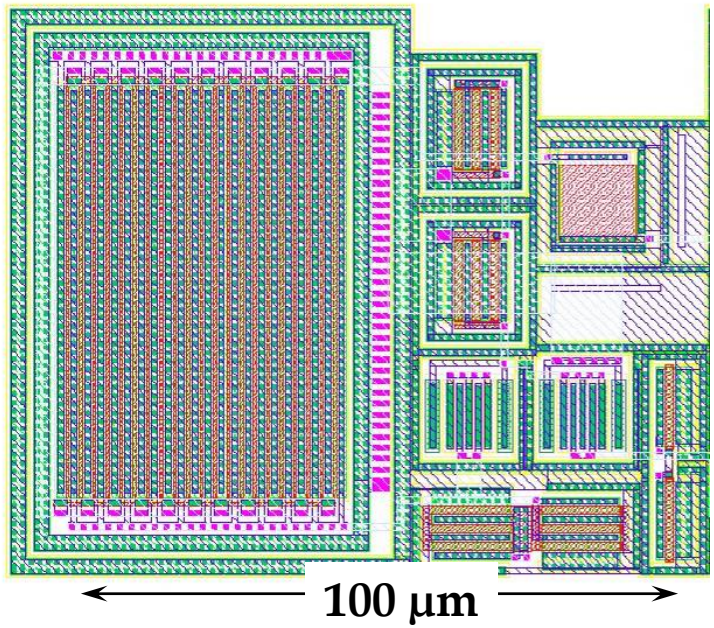
Saturation behaviour



1 MHz

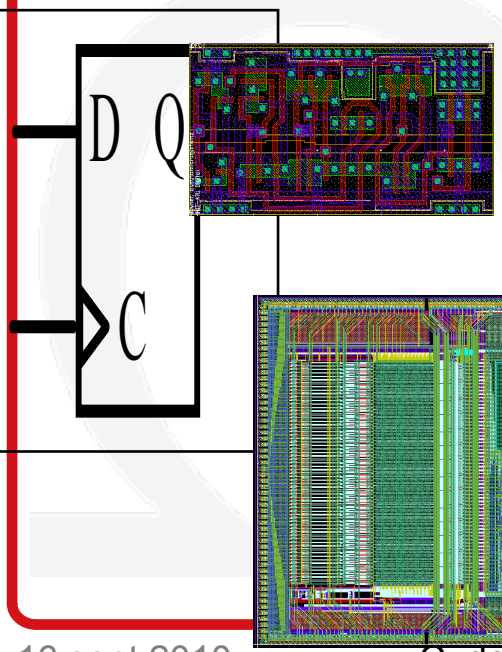
Example : designing a charge preamp (6)

- Layout
  - Each component is drawn
  - They are interconnected by metal layers
- Checks
  - DRC : checking drawing rules (isolation, minimal dimensions…)
  - ERC : extracting the corresponding electrical schematic
  - LVS (layout vs schematic) : comparing extracted schematic and original design
  - Simulating extracted schematic with parasitic elements
- Generating GDS2 file
  - Fabrication masks : « reticule »



Digital implementation global Flow


```
process(Rstb, Clk)
begin
  if Rstb ='0' then
    Q <= '0';
  elsif rising_edge Clk then
    Q <= D;
  end if;
end process;
```



Architecture Design

High Level Synthesis

Synthesis

Verification

RTL

Placement

Extraction and Timing Verification

Routing

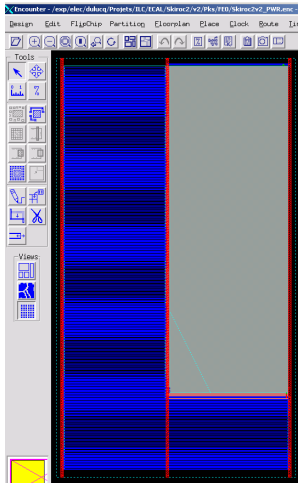
GDSII

Manufacturing

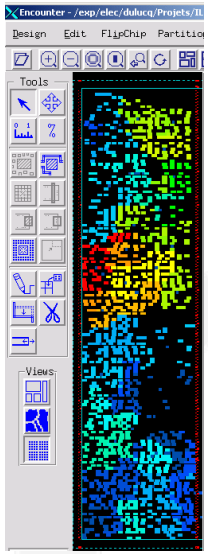
ASIC specific flow for digital routing

©F. Dulucq

Skiroc2 power planning



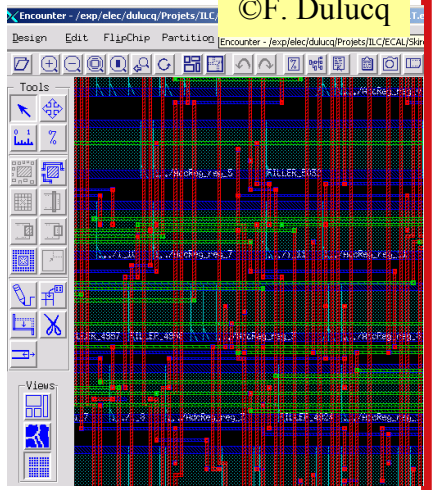
Skiroc2 clock tree



IO Pad Placement

Power planning (Stripes & rings)

(M1, M2, M3) = (blue, red, green)



Global Placement

DFT (scan chains)

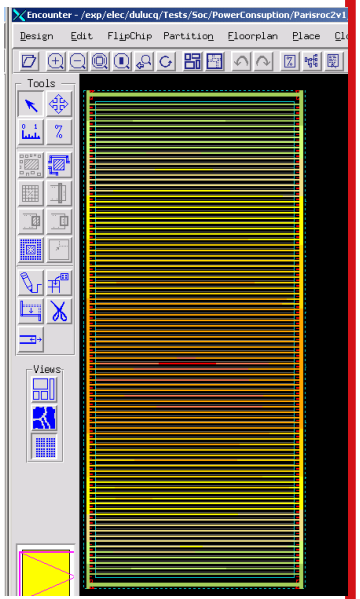
Clock Tree Synthesis

Extraction and Delay Calc. Timing Verification

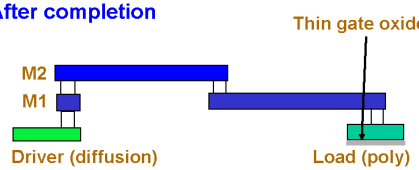
Global Routing

LVS / DRC Specific Analysis (IR, Antennas)

GDS2

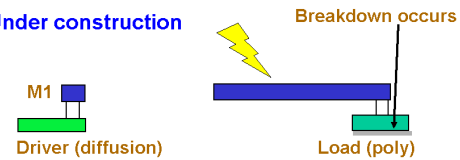


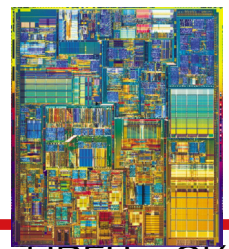
(a) After completion



Antennas fixing

(b) Under construction



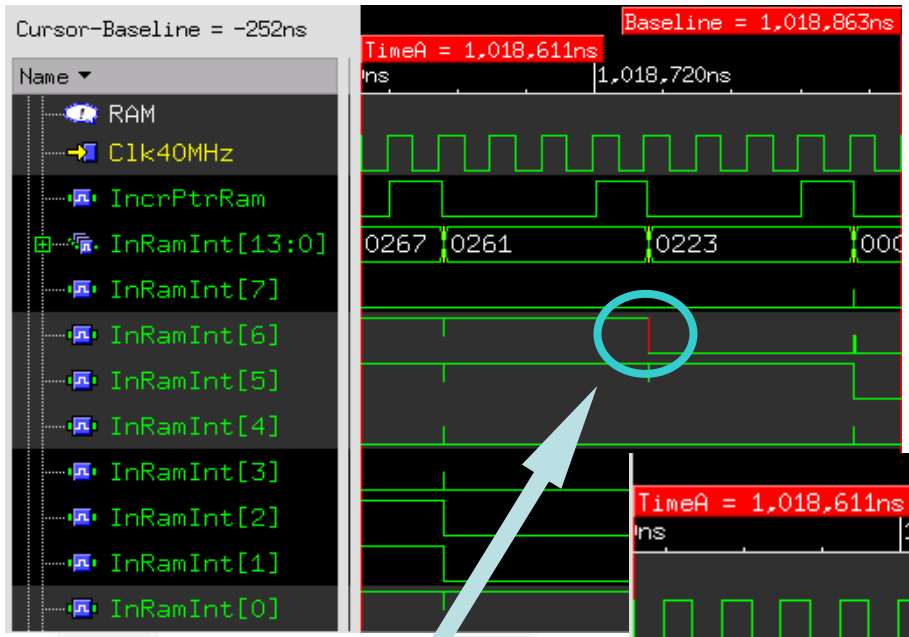


Pentium4

Parisroc2 IR drop Analysis (red = drop > 5mV)

Post layout simulation (extracted RC)

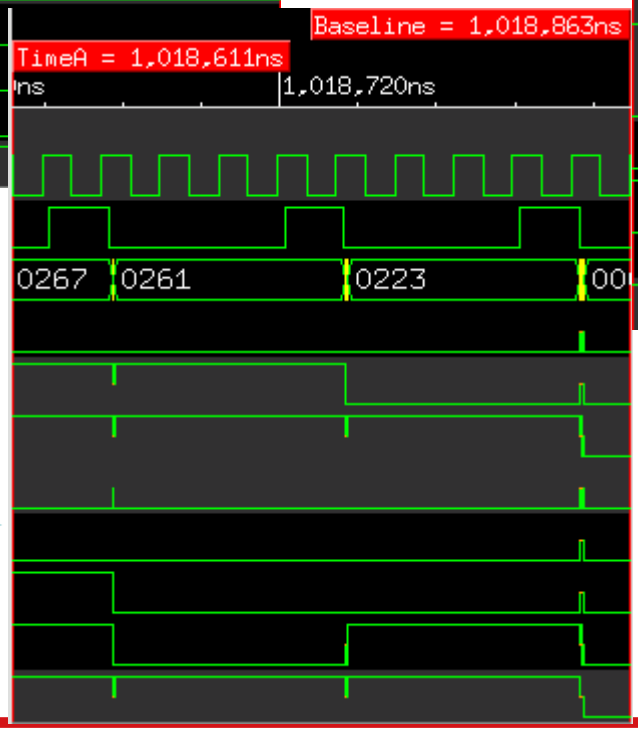
MIN PVT (1.6 ; 3.6V ; -50°C)



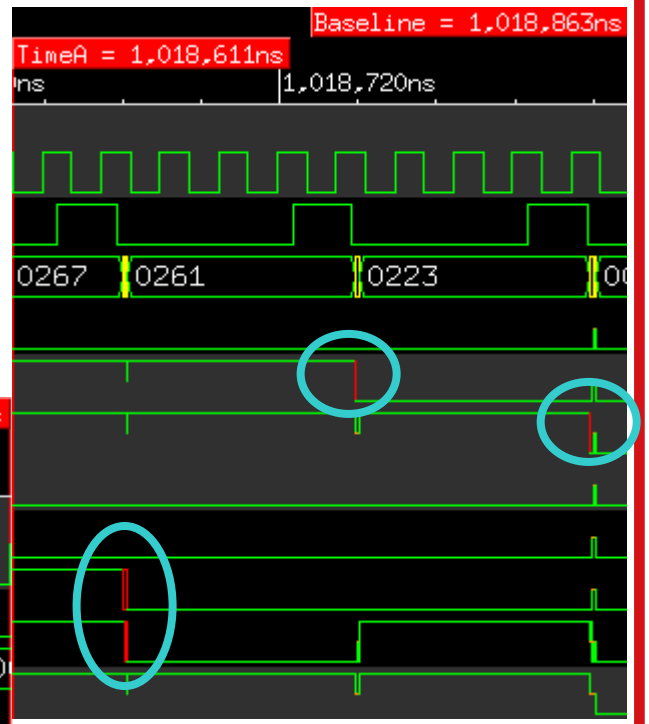
1 violations

TYP PVT (1 ; 3.3V ; 25°C)

0 violations



MAX PVT (1.4 ; 3V ; 125°C)



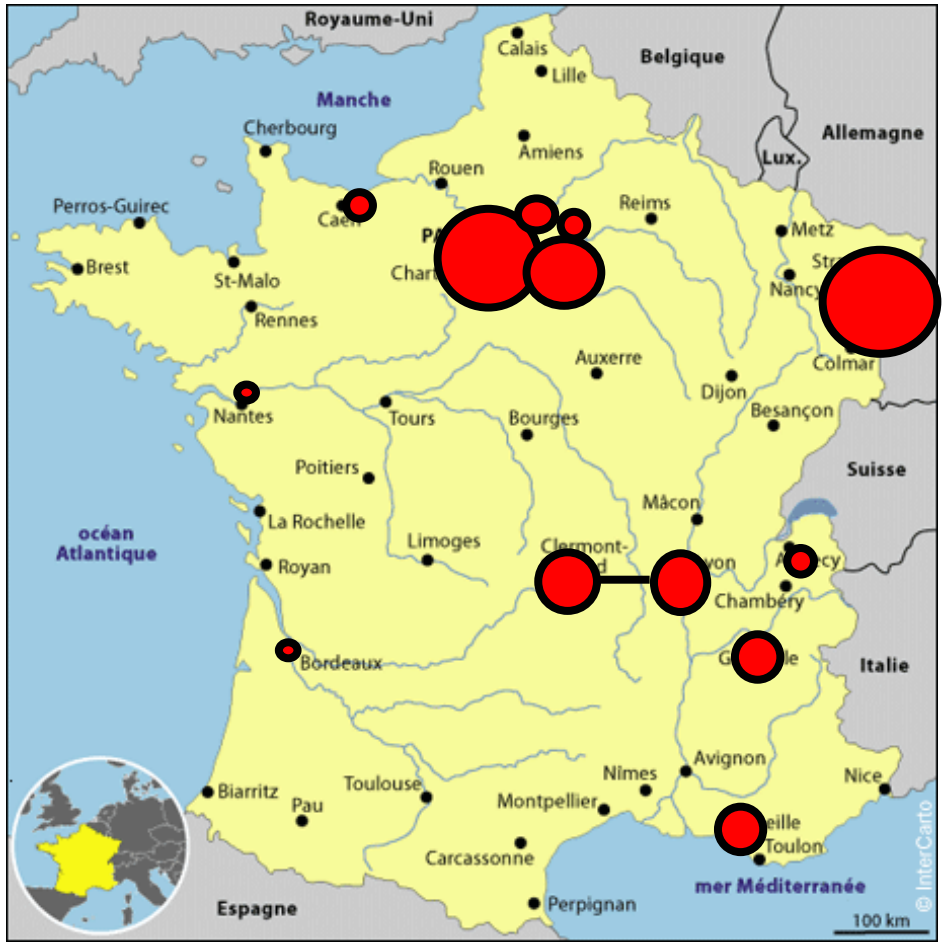
4 violations

- Coexistence analog-digital
  - Capacitive, inductive and common-impedance couplings
  - A full lecture !
  - A good summary : there is no such thing as « ground », pay attention to current return

Microelectronics at IN2P3/IRFU (2009)

- Large force of micro-electronics engineers (~50)
  - Experience in designing and building large detectors
  - Common Cadence tools
  - But scattered in ~15 labs

- National organization :
  - Building blocks : « club »0.35µm SiGe
  - Networking 0.35 and 130 nm
  - Creation of poles with critical mass (~10 persons)
    - Orsay (OMEGA)
    - Clermont-Lyon (MICHRAU)
    - Strasbourg (IPHC)



Etat des lieux (constat 2005)

- **L'in2p3 a bien pris le tournant de la micro-électronique dans les années 90**
  - Logiciels de conception unifiés (Cadence)
  - De nombreux ASICs produits pour les expériences
  - Des forces dans tous les labos

- **Une cinquantaine de micro-électroniciens, inégalement répartis**
  - 3 labos avec des équipes d'une dizaine de concepteurs (IReS, LPCClt, LAL)
  - 4 labos avec des équipes intermédiaires (3-6) (CPPM, IPNL, LAPP, LPSC)
  - Les autres labos avec moins de 3 micro-électroniciens (CSNSM, CENBG, IPNO, LLR, Subatech…)
  - C'est une force considerable (cf CERN, RAL…)

- **La visibilité n'est pas à la hauteur des forces investies**
  - Trop de dispersion, duplication, syndrome NIH
  - Participations sous-critiques dans une multitude de projets
  - Bannière de labo vs etiquette IN2P3 (cf INFN-xx)
  - Pourtant, une bonne habitude et une réelle volonté de collaborer entre équipes
  - Une communauté soudée par les outils communs et les réseaux in2p3 (VLSI, "club 035", écoles thématiques)

Club building blocks 0.35µm

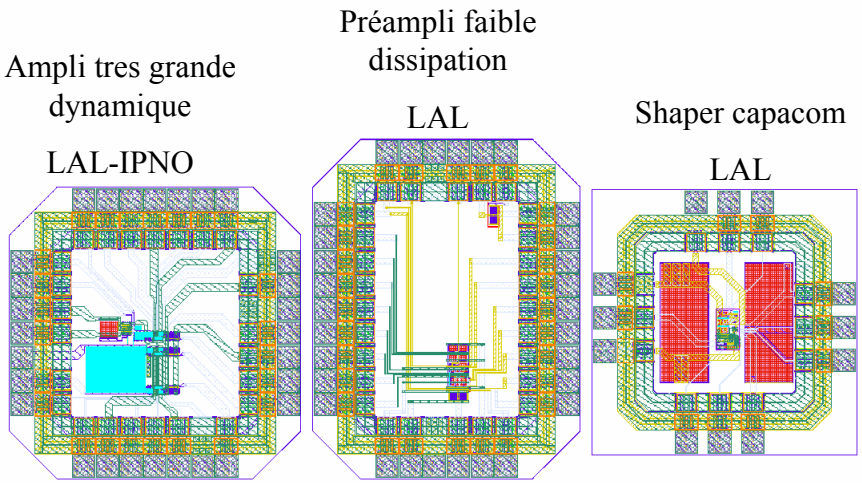
- Mission :

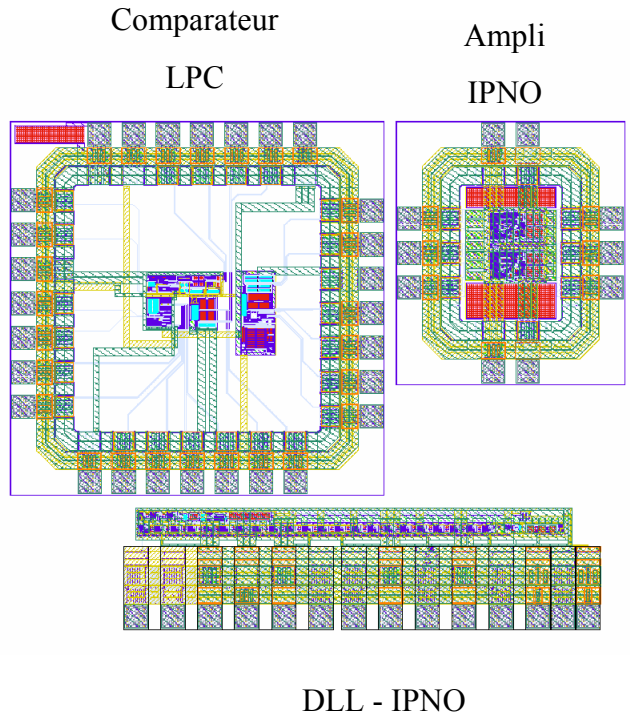
  Design of basic building blocks usable by all in2p3 labs for physics experiments

- Motivations
  - Target « analog-friendly » technology (0.35µm CMOS and SiGe AMS)
  - Optimize ressources and competences within in2p3
  - Increase visibility of in2p3 in microelectronics
  - reduce developpement times

- First results
  - 2-3 runs /yr financed by in2p3
  - Porquerolles workshop
  - Fruitful exchanges

- Done :
  - Building blocks
  - ADC developments : spectacular progress (LPC,LPSC)
  - Porquerolles workshop
- Missing
  - Documentation !





New club 130nm for tracking and 3D (2008)

- Networking : club 130nm created at VLSI workshop
  - Target common technology with CERN or other labs : IBM 130nm with CERN, Chartered 130nm (IBM compatible)
- 3D consortium : CPPM, IPHC, IRFU, OMEGA, LPNHE
  - Complementarity
  - Task sharing
  - Coordination
- IN2P3 Recommendation : participate to 3D effort in a coherent, coordinated and funded way.
- Building blocks in the AIDA FP7 european program

Motivations pour des pôles (2005)

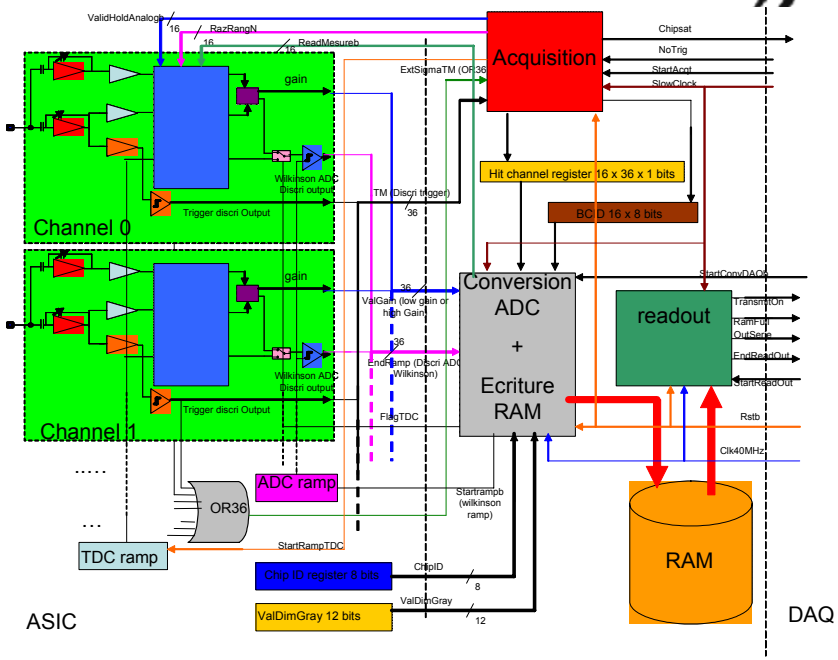
- **Accroissement continu de la complexité des ASICs**
  - De plus en plus de fonctions, y compris la numérisation
  - de plus en plus de canaux
  - Voir exemples en Annexe

- **Importance de la "masse critique"**
  - Communication quotidienne entre concepteurs
  - Partage d'expérience et de circuits ou briques déjà éprouvés
  - Large variété de projets, "cross-fertilization"
  - Réunions de design, internal reviews…
  - Recherche de l'excellence

- **Pôle ≠ Réseau**
  - Concentration géographique, contacts quotidiens, autonomie
  - Peu d'intérêt à créer des sous-réseaux régionaux
  - Bien continuer à faire vivre le réseau national

Motivation for poles

- Continuous increase of chip complexity (SoC, 3D…)
  - Minimize interface problems
- Importance of critical mass
  - Daily contacts and discussions between designers
  - Sharing of well proven blocks
  - Cross fertilization of different projects
- Large R&D activity
  - ILC detectors
  - sLHC starting (3D electronics)
  - astrophysics



Difficultés (2005)

- **Structure "supra-labo"**
  - Diminution d'autonomie des directeurs
  - Les projets labo sont en compétition avec des projets "hors labo"
  - Nécessité d'un système de gouvernance (léger)
  - Difficile gestion des recrutements et des carrières des ITA du pôle
  - Nécessité d'un budget dédié

- **Le pôle ne doit pas être une "agence de moyens"**
  - Les ASICs restent très proches des détecteurs et de la physique
  - Les concepteurs ont besoin de se sentir membres d'une collaboration scientifique
  - ils ne veulent pas etre "prestataires de service"

- **La valorisation doit être traitée par le C4I** [2008 -> MIND]
  - Les possibles retombées financières ne favorisent pas l'esprit d'ouverture
  - Les logiciels ne sont pas utilisables contractuellement pour la valorisation
  - Partenariat "inventeur"-C4I (en accord avec le labo ou le pôle)

Mise en Œuvre a Orsay : OMEGA (2006)

- **Demande de M. Spiro de tester la mise en œuvre a Orsay (2006)**

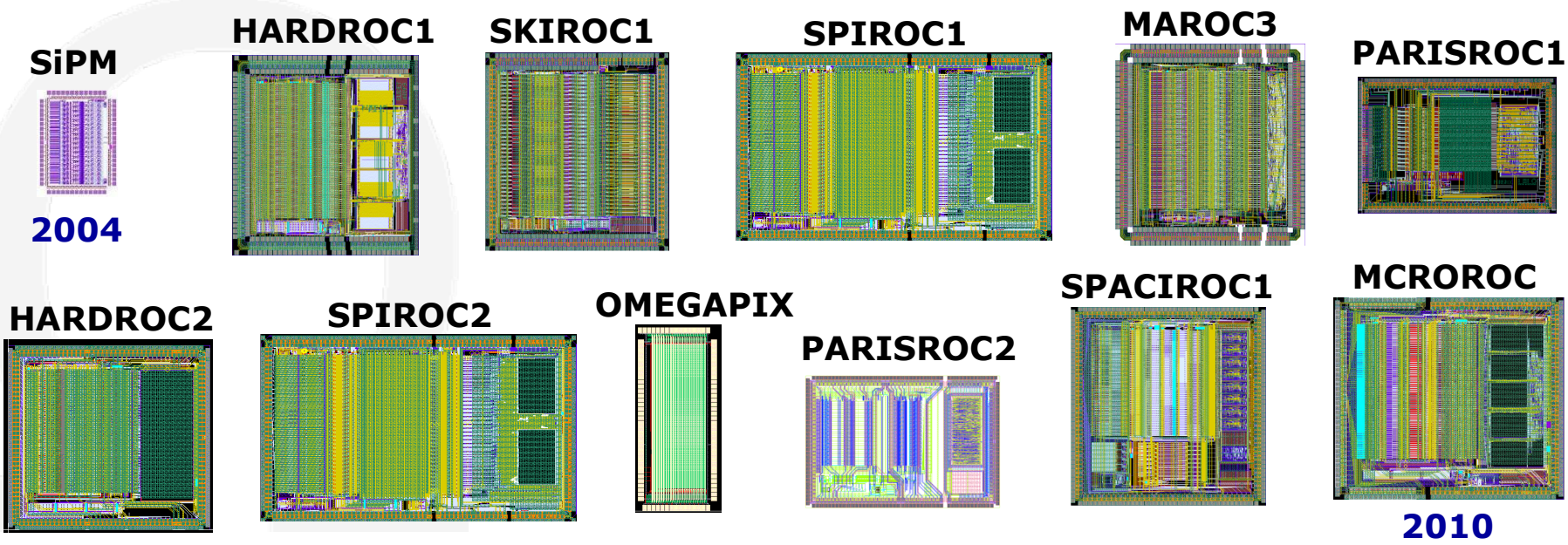
- **Omega = Orsay Micro-Electronics groups associated**
  - concentration géographique des designers au LAL
  - Le LAL apporte 8 designers, l'IPNO 2-3, le LLR 1, le CSNSM 0
  - Fort effet de synergie, réutilisation des designs des particules vers le nucléaire
  - Augmentation de la « demande » d'un facteur ~2
  - Ce pôle sert environ 1/3 des physiciens de l'IN2P3 (avec 20% des microelectroniciens)

- **Mise en œuvre pratique**
  - Regroupement des microelectroniciens
  - Mise a disposition de bureaux « environnés » pour les visiteurs des 3 autres labos
  - Remise en état des salles de test

- **Points a clarifier**
  - Structure de gouvernance, poids du LAL
  - Budget propre de fonctionnement et missions
  - Comment garder une articulation forte avec les projets de physique
  - Interaction avec le service électronique du LAL

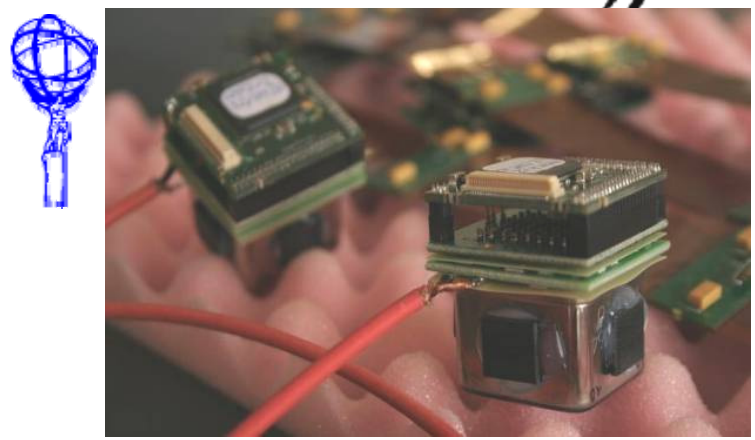
Recent chips at OMEGA Orsay

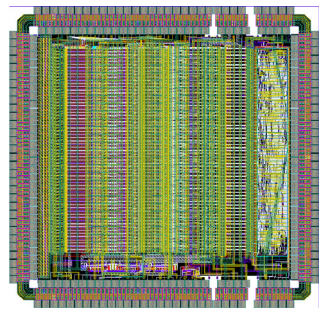
- Several chips developped for ATLAS LAr, OPERA, LHCb, CALICE in BiCMOS 0.8µm and installed on experiments
- Turn to Silicon Germanium 0.35 µm BiCMOS technology in 2005
- Readout for MaPMT and ILC calorimeters
- Very high level of integration : System on Chip (SoC)
- Start of 3D integrated 130nm electronics for sLHC pixels
- 2 designers/project & 2 projects/designer

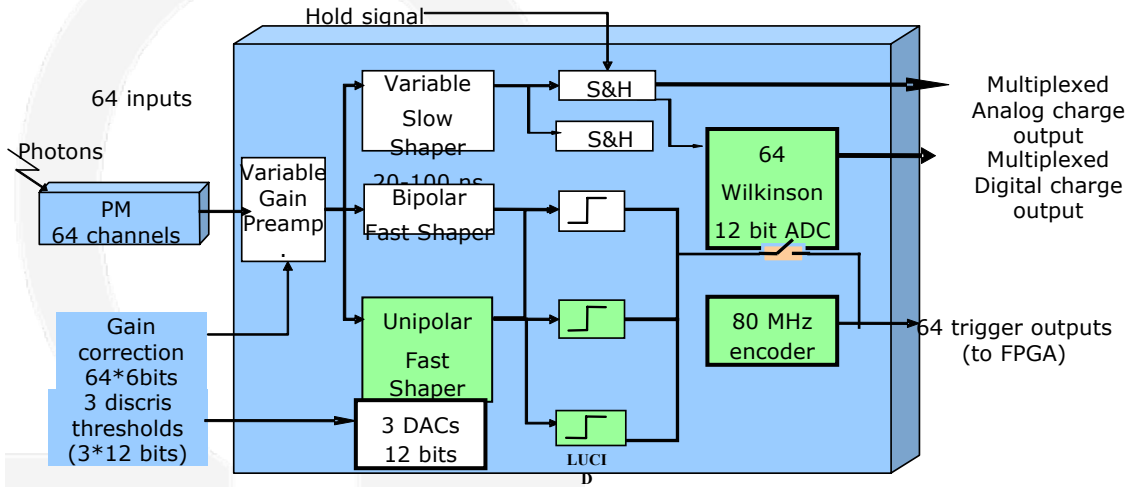


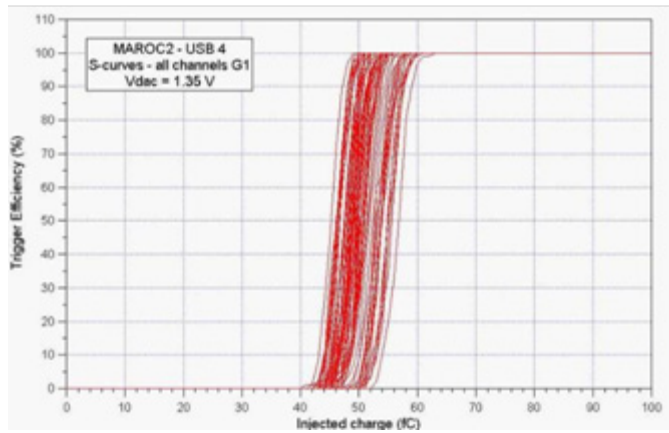
MAROC : MultiAnode Read-Out Chip

- Complete front-end chip for 64 channels multi-anode photomultipliers
  - 6bit-individual gain correction
  - Auto-trigger on 1/3 p.e. at 10 MHz
  - 12 bit charge output
  - SiGe 0.35 µm, 12 mm^2, Pd = 5 mW/ch
- Bonded on a compact PCB (PMF) for ATLAS luminometer (ALFA)
- Also equips Double-Chooz, medical imaging…









SPACIROC ASIC

ASIC Functions:

Analog part:

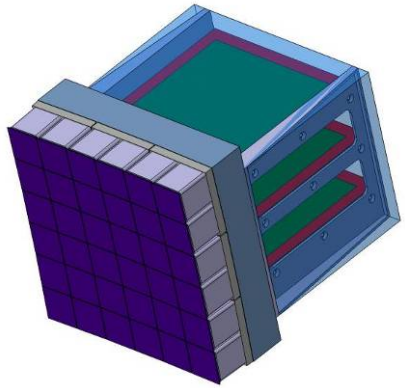
1. Photoelectron counting (implemented LAL)
2. Time Over Threshold (collab. JAXA/Riken)

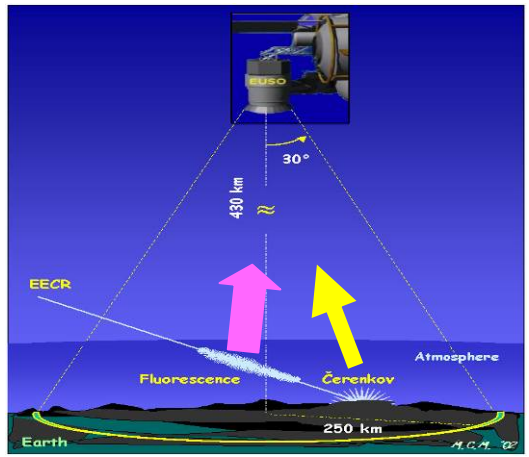
Digital part (LAL):

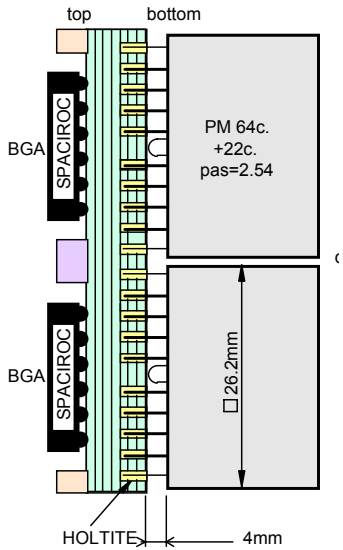
1. Digitization,
2. Memory,
3. Send data to FPGA for triggering

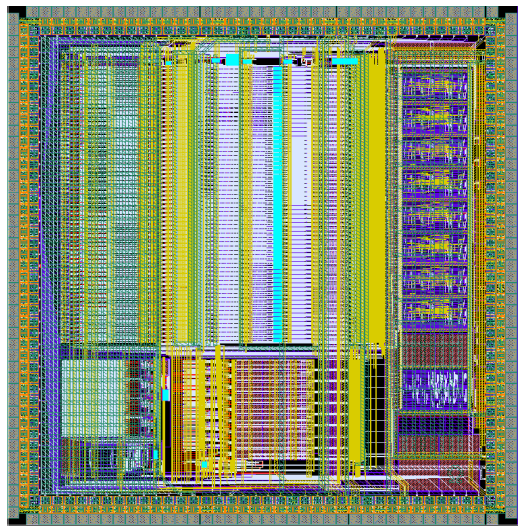
Crucial points

- Power consumption < 1 mW/ch
- data flow ~ 384 bits / 2.5 µs
- Radiation tolerance



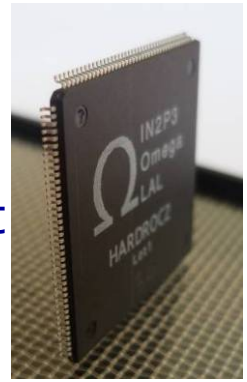


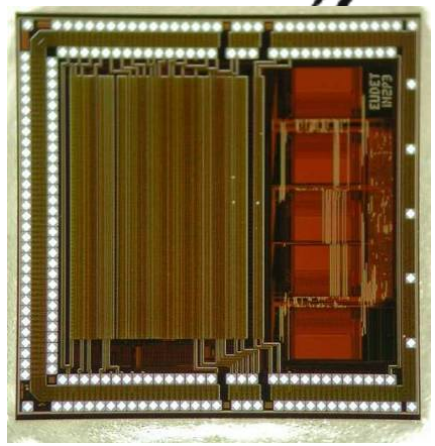


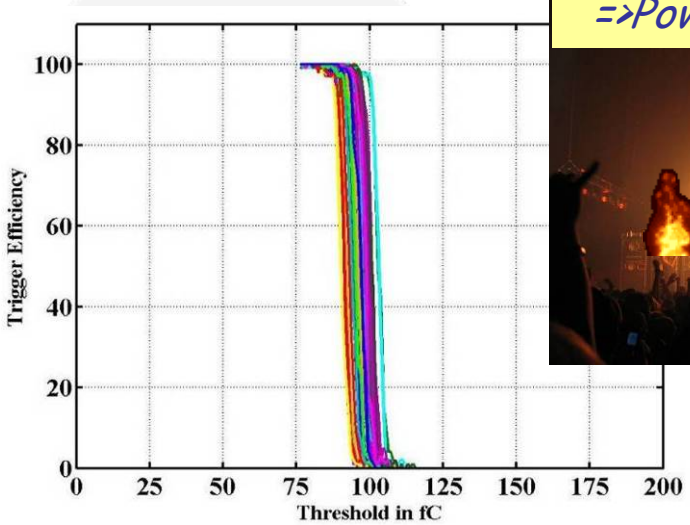


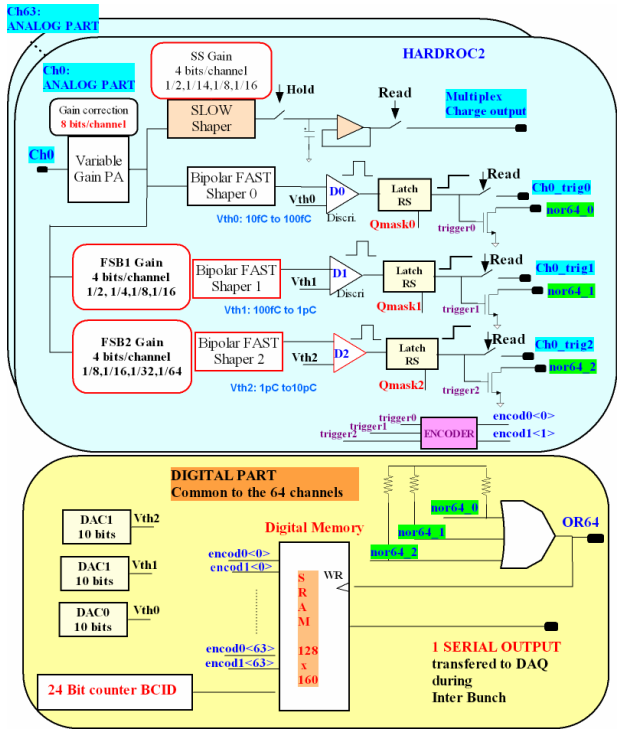
HaRDROC : ILC DHCAL readout

- Hadronic Rpc Detector Read Out Chip
  - 64 inputs, preamp + shaper+ 3 discris
  - Full power pulsing => 7 µW/ch
  - Fully integrated ILC sequential readout
  - Chip embedded in detector
  - 5000 chips produced in 2010
  - MICROROC = version for MICROMEGAS developped with LAPP

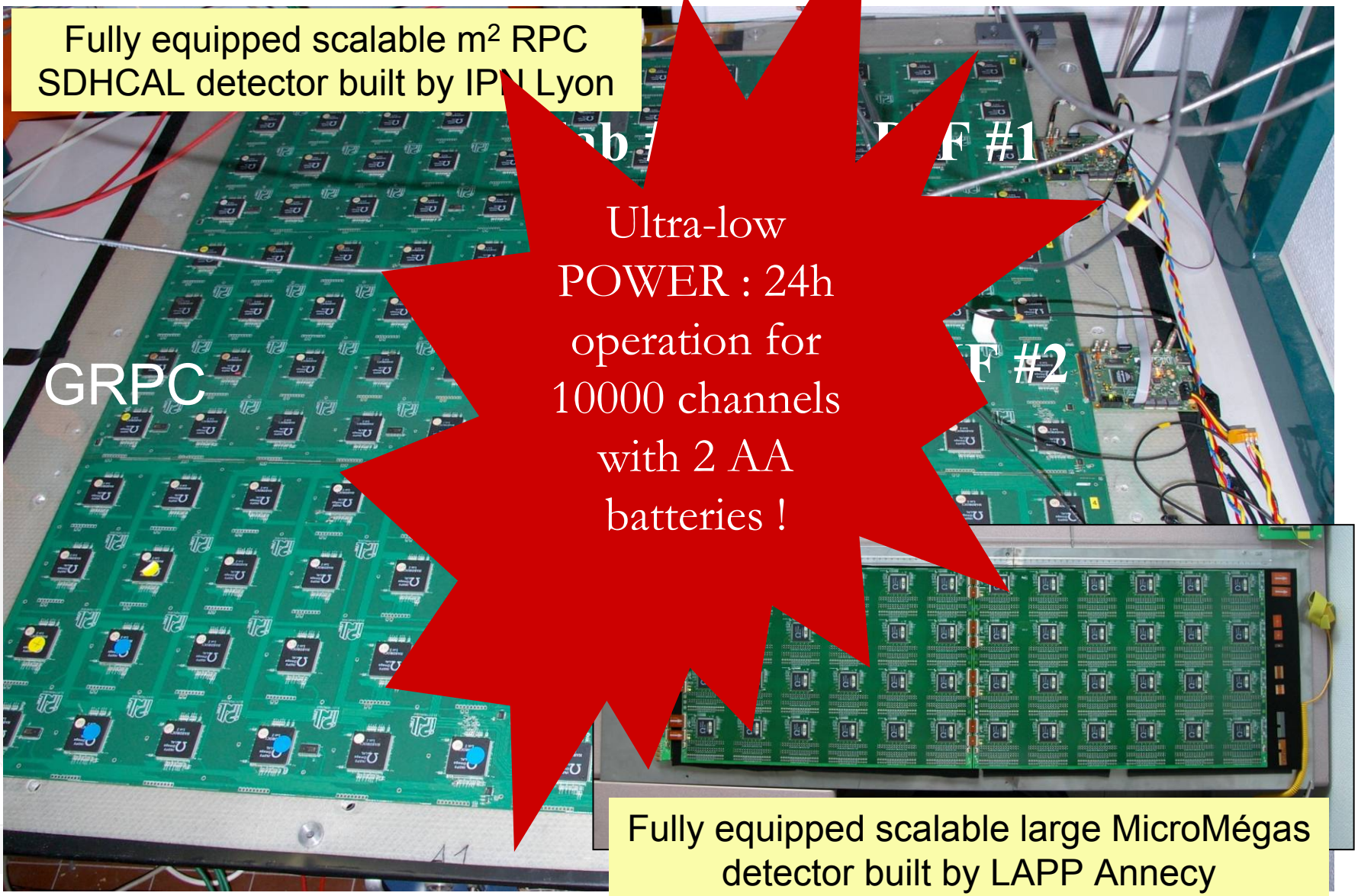






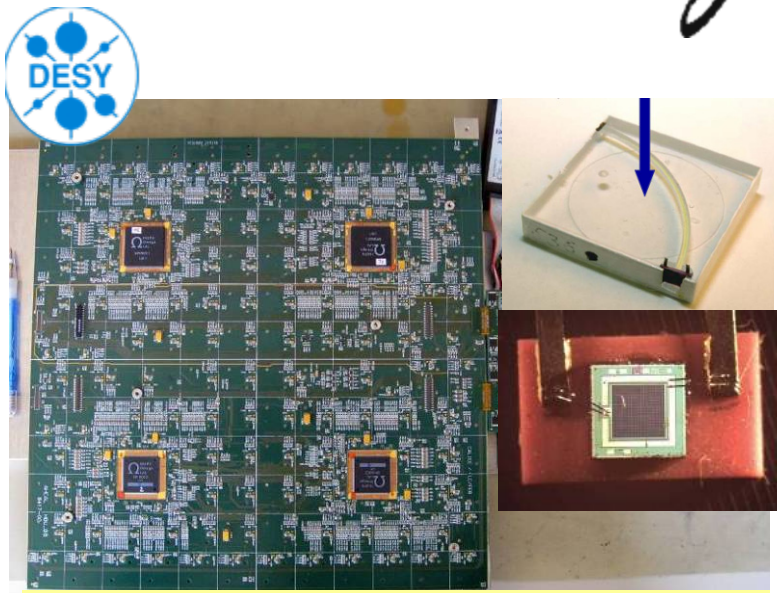


Towards an ILC technological prototype

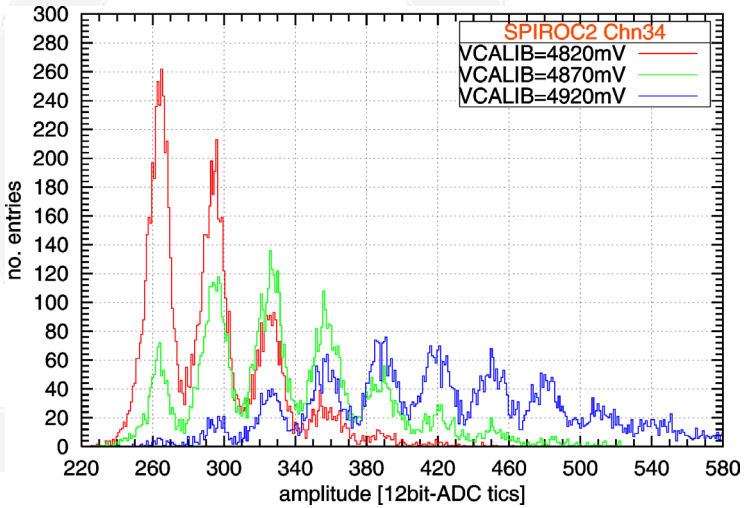


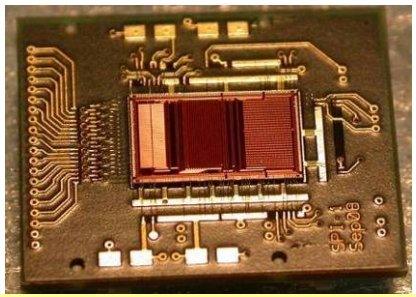
SPIROC : ILC AHCAL & ECAL readout

- SPIROC : Silicon Photomulier Integrated Readout Chip
  - 36 channels
  - Internal 12 bit ADC/TDC
  - Charge measurement (0-300 pC)
  - Time measurement (< 1 ns)
  - Autotrigger on MIP or spe (150 fC)
  - Sparsified readout
  - Pulsed power -> 25 µW/ch
  - Also External users (PET, hodoscopes, µ-imaging… (@ Aachen, Napoli, Pisa, Roma…)

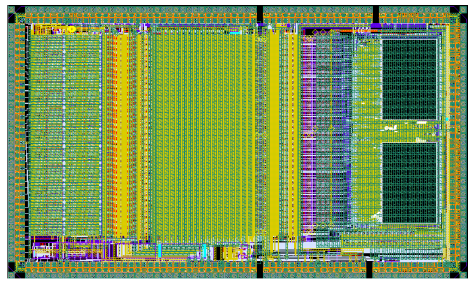


(0.36m)² Tiles + SiPM + SPIROC (144ch)



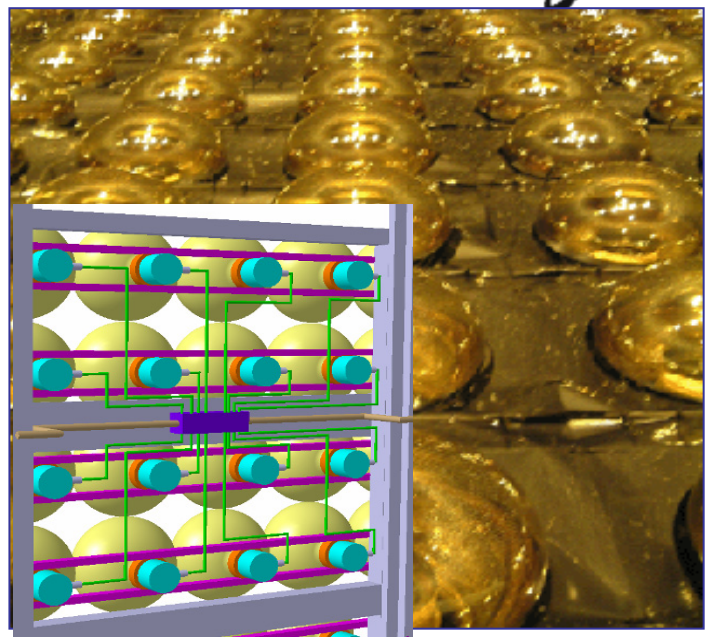


PEBS :©W. Karpinski (Aachen)

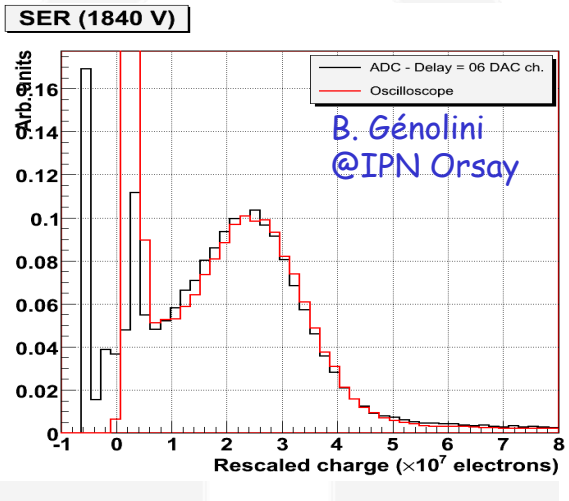


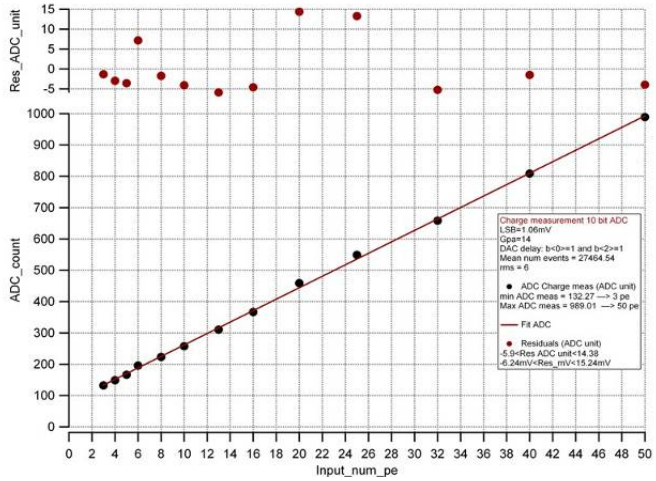
PARiSROC for PMm²

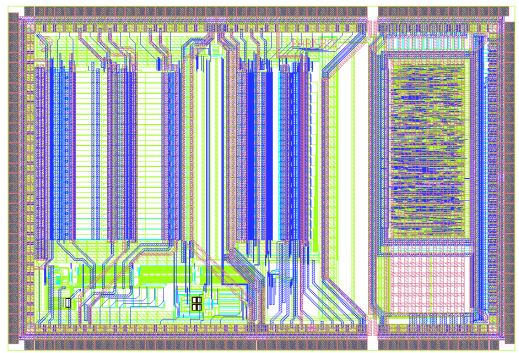
- Photomultiplier ARray Integrated SiGe Read-Out Chip
  - Replace large PMTs by arrays of smaller ones (PMm2 project)
  - Centralized ASIC 16 independent channels
  - Auto-trigger
  - Charge and time measurement (10-12 bits)
  - Water tight, common high voltage
  - Data driven : « One wire out »
- Application in large Water Cerenkov
  - Chip studied by DUSEL, LENA, LHASSO…



Joël Pouthas IPN Orsay



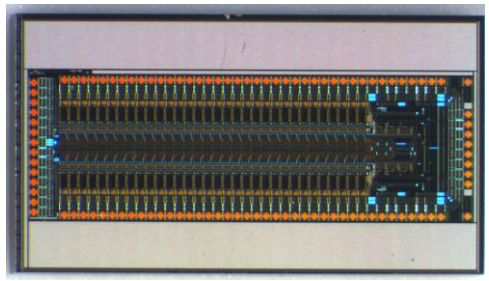


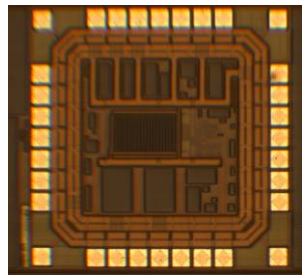


Front-End R and D in HEP
(Room temperature and Cryogenic Temperature)

Mains analog blocks
- Charge Sensitive Amplifier
- Shapers
- Buffer

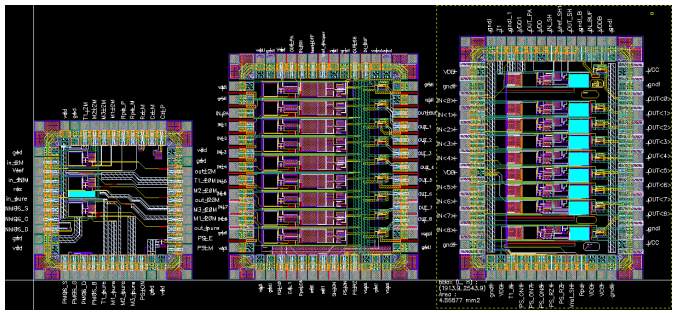
Analog /digital Asic

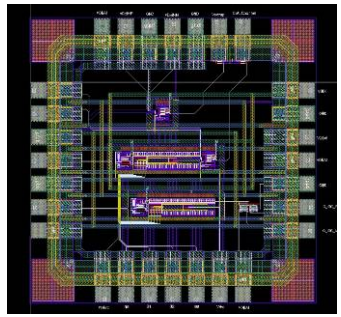




Full diff CSA

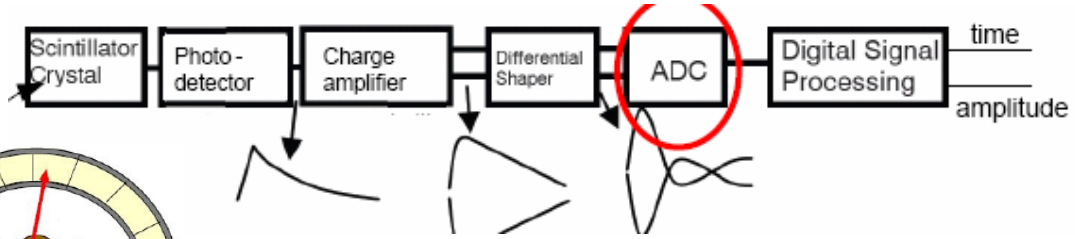
- ILC (DHCAL et ECAL)
- INNOTEP (medical imaging project)
- Beam profiler for hadrontherapy
- T2K

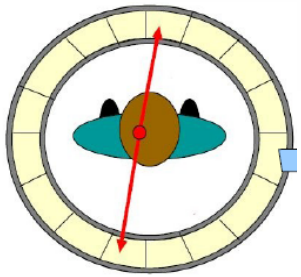




AMS 0.35 CMOS and BiCMOS proce

INNOTEP (AMS 0.35µm SiGe)

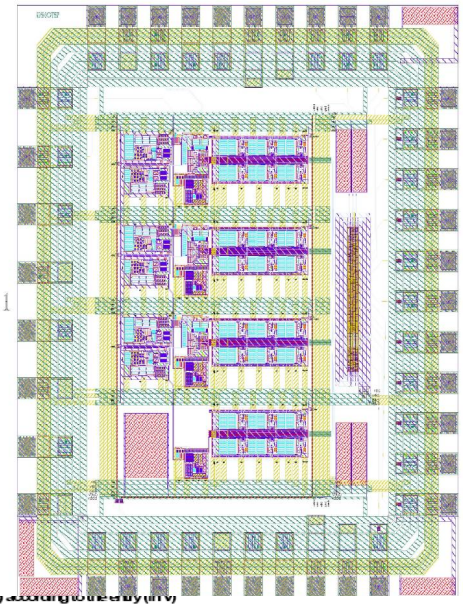


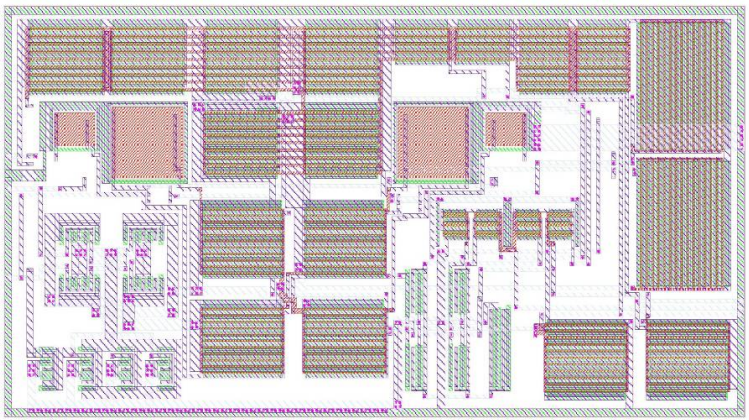


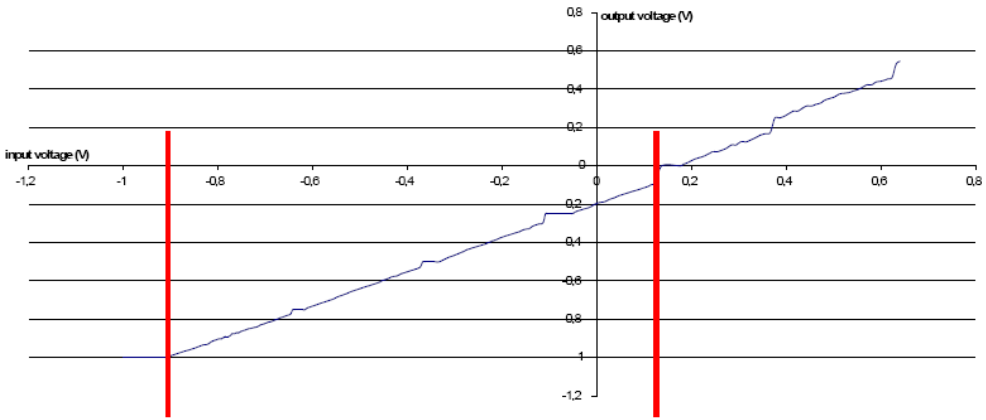
Detector ring

100 Mhz 8 bits ADC (S. Crampon thesis)
First version tested, need for an iteration

Fast preamplifier and 40ns shaper (tested)
Used for a 40 channels demonstrator.





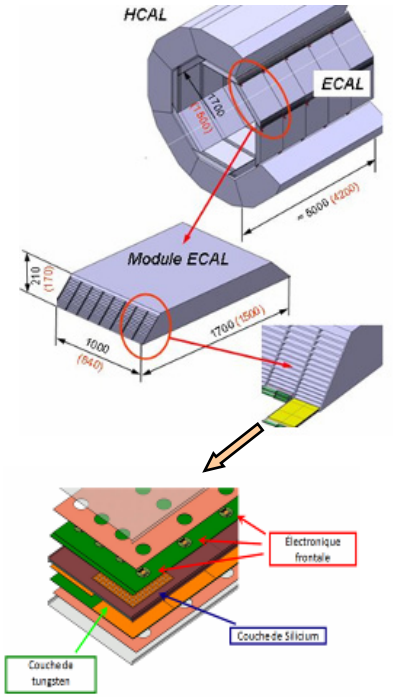


R&D dedicated to ILC/Calice

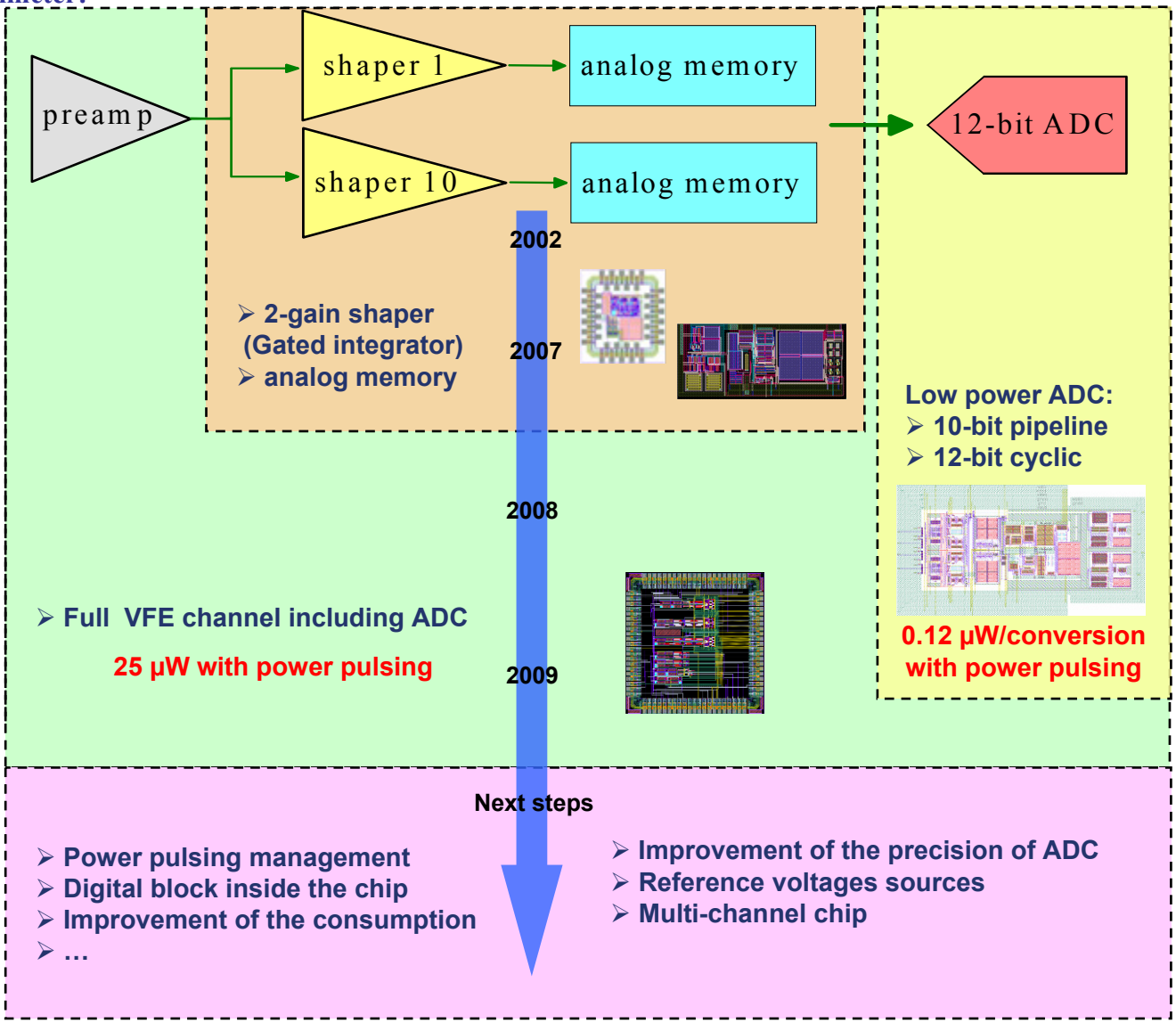
MICroelectronic RHone AUvergne

Very-front-end electronics of SI-W calorimeter:

- Dynamic range of 15 bits
- Global precision > 8 bits
- Embedded multi-channels chips
- > 100.10^6 channels
- Ultra-low power : 25 µW per channel

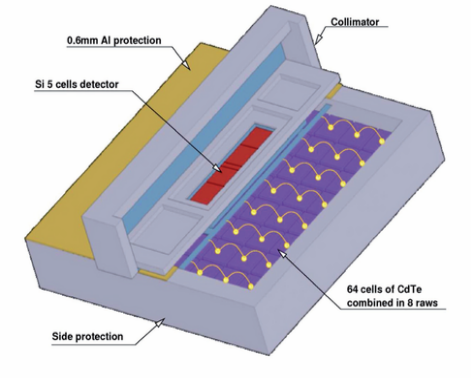


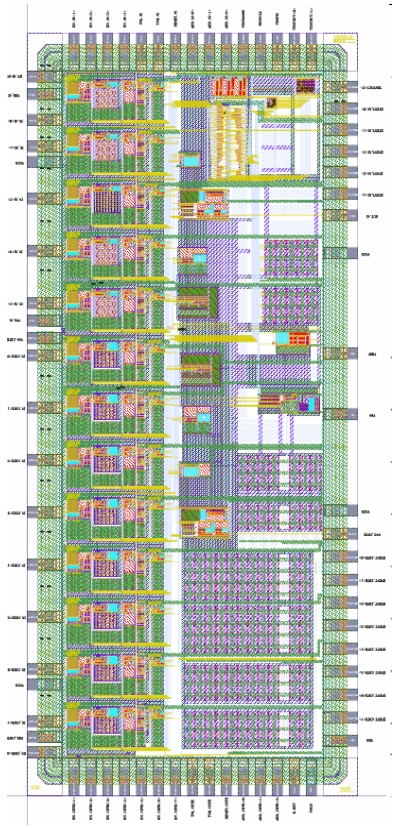
The embedded VFE chip inside the sandwich structure of the Ecal detector



TARANIS Project through CESR in Toulouse via MIND/C4I

Experiment goal : Measurement of the energetic electrons generated by atmospheric thunderstorms, space electronics (µsatellite)



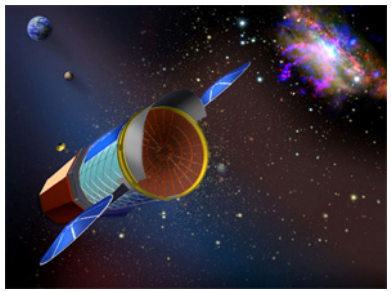


Front-end analog blocks (CSA, Shapers, comparators) come from several projects (INNOTEP, ILC T2K)

2 types of detectors : CdZnTe and Si diode

- TOF : 1ns resolution
- TOF PET : very high timing resolution << 200ps
- Very High speed ADC >> 500Ms/s… 1 GMs/s ?
- Beam profiler : high counting rate (100Me/s)
- Very fast preamplifier and shapers

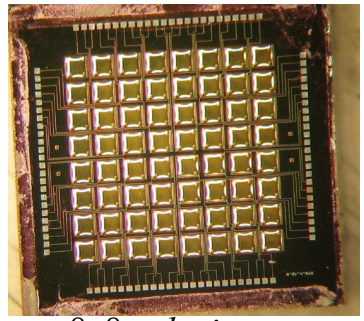
LT Mux for XRAY micro calorimeters Matrix



Satellite IXO

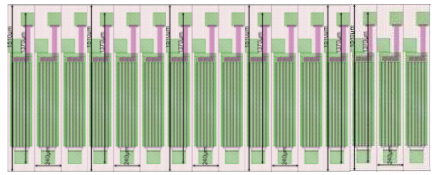
©E. Delagnes

- **Target:** **IXO** satellite (ESA)
- **High resolution** (5eV @ 6kEV) **XRay spectro-imager**
- **fine pitch:** 4000 pixels
- Calorimeter Matrix manufactured by **CEA/LETI**
- Detector temperature : 50 to 100mK
- Photon by photon detection => high speed FE



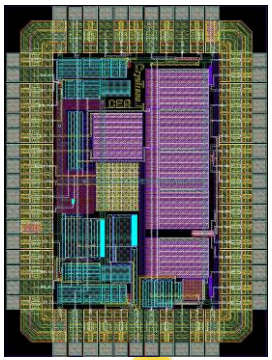
8x8 calorimeter matrix prototype

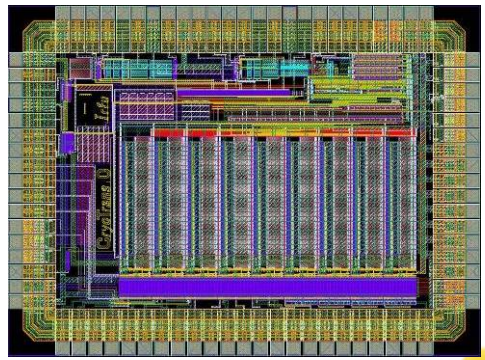
- Front_End electronics close to the detector:
- **Must operate @ 4K**
- Amplify and multiplex the detector pulses
- Low noise, low power **(30µW/channel)**



Multi HEMT chip.

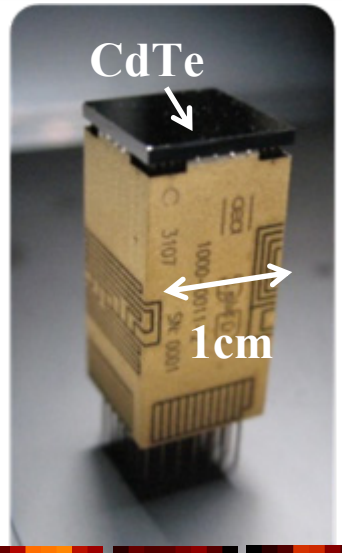
- **Technological choices:**
  - HEMT (from CNRS/LPN) for the first stage (impedance adaptation + gain).
  - AMS 0.35µm SiGe chip for extra gain + 32=>1 mulitplexing:
    - Behavior of SiGe @ 4K evaluated on previous chips.
    - 2 prototype circuits submitted in July 2009.

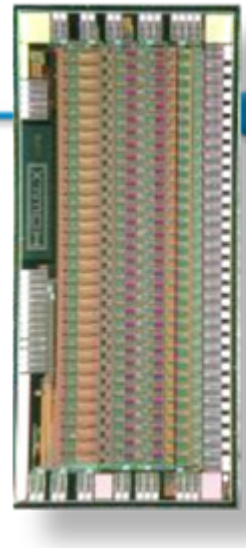




Idef-X 2.E for ECLAIRs.

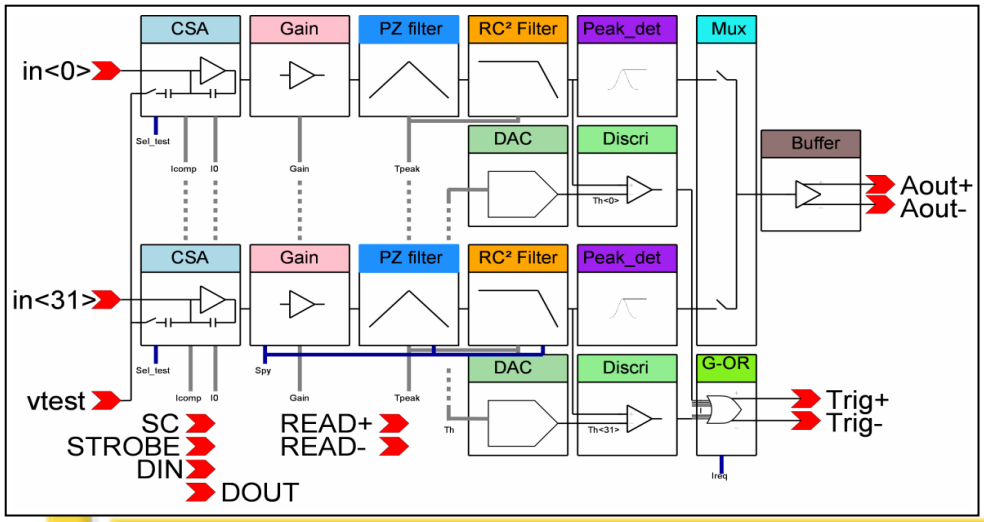
- For SVOM/ECLAIR: Gamma Ray Burst satellite.
- CdTe Detectors.
- 32 channels. 2.2 mW/ ch.
- Slow control => many parameters tunable
- Self triggered / 1 Thresh/channel.
- **1µs-10µs** selectable shaping.
- Peak detector. Mux Output.
- Sparsification and zero-supress.
- ~200mV/fC**.** 50ke- linear range (220 keV CdTe)
- 60 e- rms noise with detectors.
- Rad-tolerant > 200krad. Use of Latch-up hardened
- Space qualification in progress.

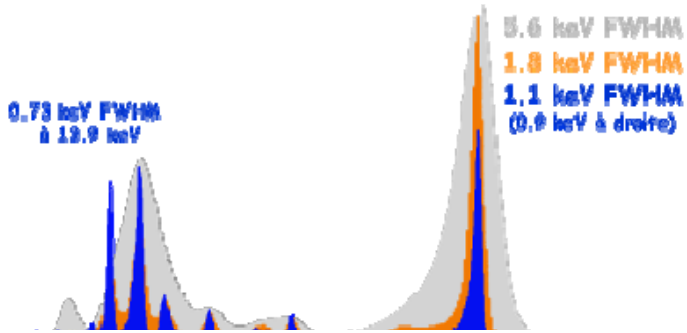




AMS0.35µm CMOS EPI. 18mm^2. 2000 chips manufactured

60keV picture from ^{241}Am source + mask (Caliste 64)



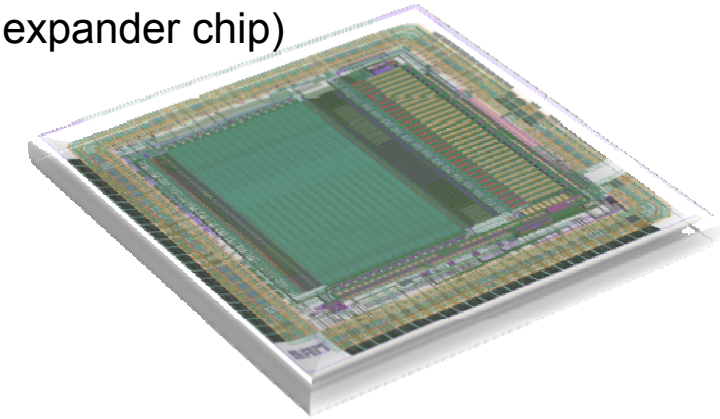


Noise and threshold 5x better than with the previous generation

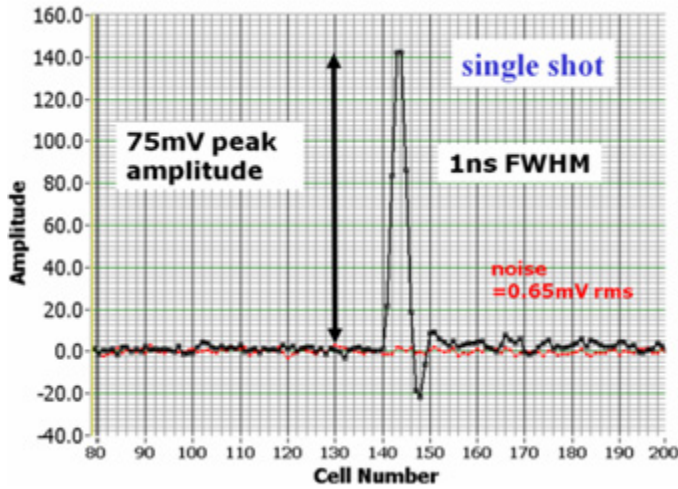
The SAM (swift analog memory) chip for the HESS2 experiment:

©E. Delagnes

- Readout for the fast PMTs of the HESS2 camera
- High RO speed Gsample/s analogue memory (time expander chip)
- Number of ch 2
- Number of cells/ch 256
- **Sampling Freq 0.7-3.2GS/s**
- Readout Speed >16 MHz
- BW **450 MHz**
- PW 300 mW
- Dynamic range 12.6 bits rms
- Simultaneous R/W No
- Smart Read pointer Yes
- 6000 chips manufactured: 95% Yield
- New chip under design => Cerenkov Telescope Array



AMS CMOS 0.35µm.
50k transistors, 11mm²

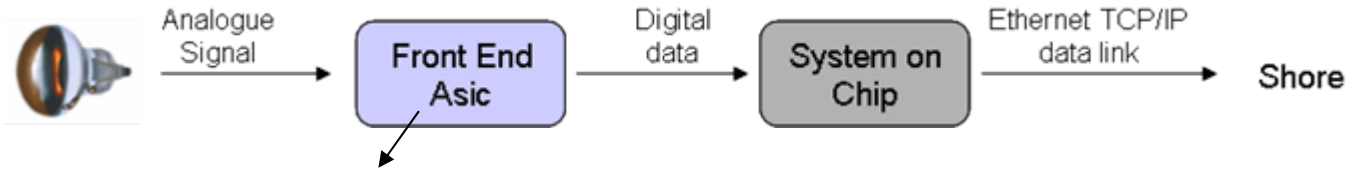


Narrow pulse sampled by SAM @ 3.2GS/s

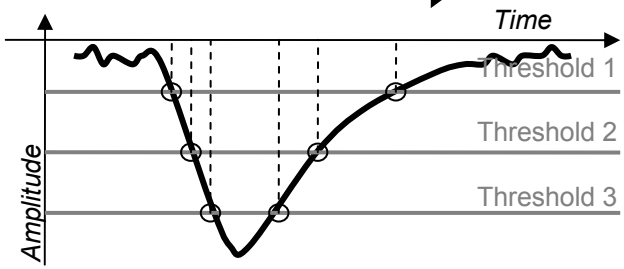
SCOTT: RO chip for the PMT of the Km³ neutrino submarine detector

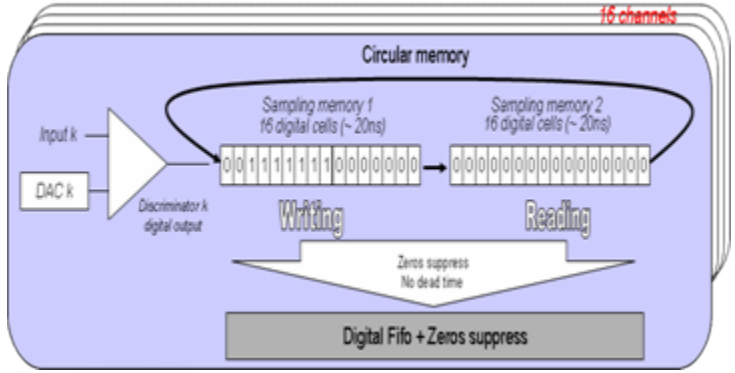
©E. Delagnes

-In the frame of KM3NET: (FP6 & FP7): baseline design



-SCOTT: based on the generalized TOT (time over threshold) concept:





•No amplitude coding, but:

• Time coding for each threshold crossing (1ns precision)

•16 independent discriminators channels with threshold set by 10 bit DACs.

• Versatile design, can be configured by slow control:

-1 PMT => 16 coding channels (~1 GS/s 4bit ADC(linear or nonlinear scale depending on the thresholds)

- 16 PMTs => 1- coding channels: (~TDC)

•Zero supress

•Derandomization (FIFO).

•Data driven readout

•SCOTT0= SCOTT single shot version prototyped in dec 2008 => concept validated.

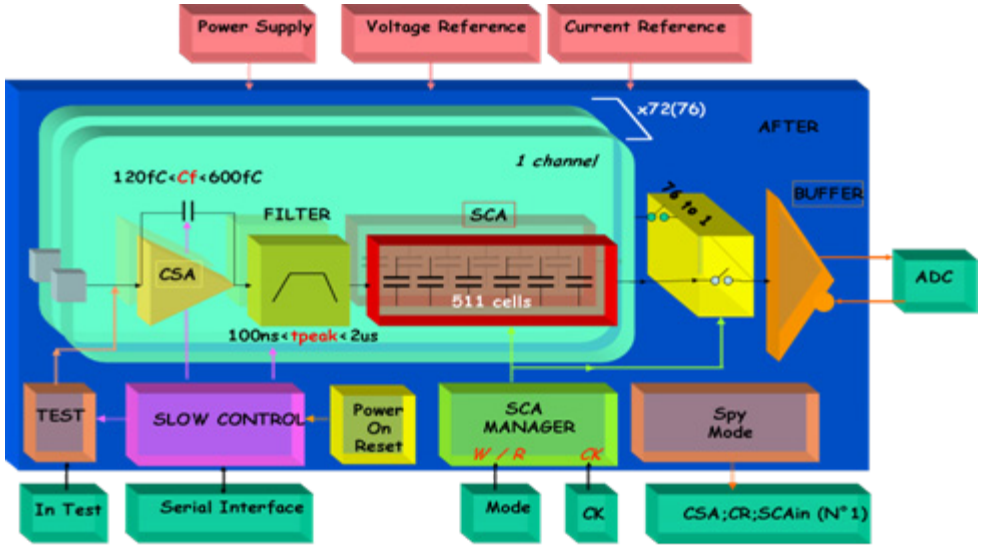
•AMS BiCMOS 0.35µm.

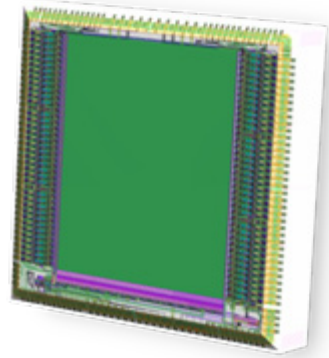
•SCOTT1 (with final RO) submitted sept. 7th 2009.

The AFTER chip for the TPC of T2K

©E. Delagnes

Design to read the 120.000 Micromegas pads of the TPC of T2K.
Combine a low noise Front-end & and a large depth and S/N SCA.
Installation @ Tokai in progress. Start at the end 2009.





AMS CMOS 0.35µm
7.8 x 7.4 mm²
500.000 transistors
6000 chips manufactured
85% Yield

Main Design features

- **72** channels x **511** analog memory cells;
- F_{write}: **1-100MHz**; F_{read}**: 20MHz**
- **4** Charge Ranges (120fC to 600fC)- 1% INL
- Supports positive or negative input signals
- **16** Peaking Time Values (**100ns to 2µs**)
- Constant dead time (2ms to read all the SCA)
- **S/N >11 bit rms.**

AGET: A future improved AFTER

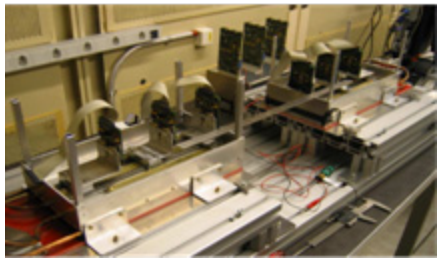
- Based on AFTER
- 1 discri/channel, 1 threshold/channel
- Multiplicity output. Autotriggerable.
- On chip zero-supress
- New 50ns shaping & “high energy” ranges
- New modes of readout
- Prototype submission: end of 2009

Monolithic Active Pixel Sensors (MAPS): A Long Term R&D

- **Main objective: ILC, with staggered performances**
  - MAPS applied to other experiments with intermediate requirements

EUDET 2007/2009

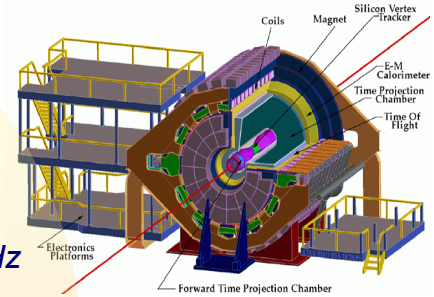
Beam Telescope



- FP6 EUDET Project (DESY-Hamburg, Germany)
  - Surface: 6 x 2 cm^2
  - Read-out speed: A. 20 MHz → D. at 100 MHz
  - Temp. & Power: No constraints
- STAR Experiment (RHIC – Brookhaven, USA)
  - Surface: ~1600 cm^2
  - Read-out speed: A. 50 MHz → D. up to 250 MHz
  - Temp. & Power: 30°C, ~100mW/cm^2
- CBM Experiment (GSI – Darmstadt, Germany)
  - Surface: ~500 cm^2
  - Read-out speed: D. 15 x 10^9 pixels/sensor/s
  - Rad Tol: 1 MRad, > 10^{13} N_{eq}/cm^2
- ILC Experiment
  - 5-6 layers of detection: ~3000 cm^2
  - Read-out speed: D. 15 x 10^9 pixels/sensor/s
  - Temp. & Power: 30°C, ~100 mW/cm^2
  - Rad Tol: ~300 kRad, ~10^{12} N_{eq}/cm^2

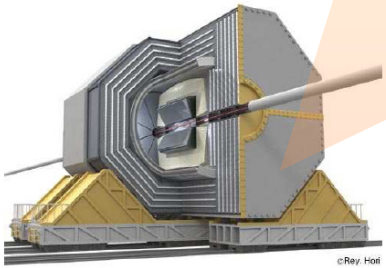
STAR 2010

Solenoidal Tracker at RHIC



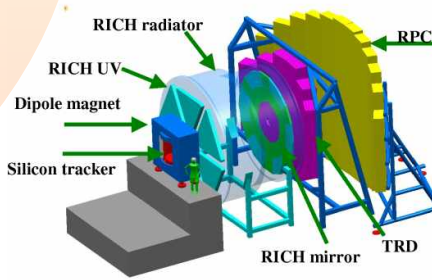
ILC >2012

Internatinal Linear Collider



CBM 2012

Compressed Baryonic Matter



➔ **Spinoff: Interdisciplinary Applications, biomedical, …**

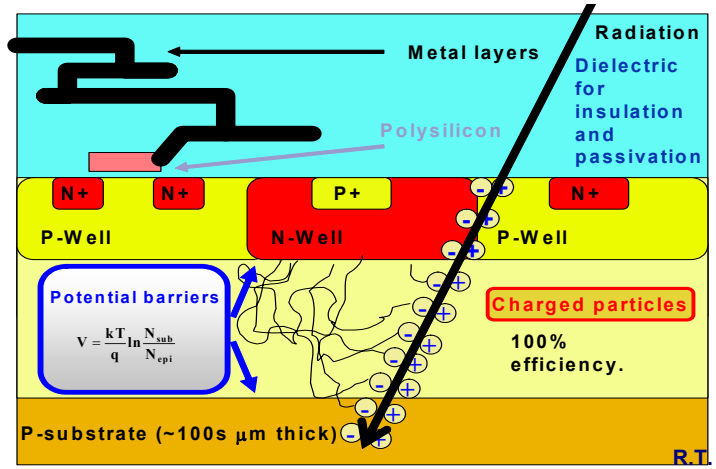
- Partnerships: GIS IN2P3/Photonis & GIS IN2P3/SAGEM & Ohio University & Michigan University…

Development of MAPS for Charged Particle Tracking

©C. Hu

- ***In 1999, the IPHC CMOS sensor group proposed the first CMOS pixel sensor (MAPS) for future vertex detectors (ILC)***
  - *Numerous other applications of MAPS have emerged since then*
  - *~10-15 HEP groups in the USA & Europe are presently active in MAPS R&D*

- ***Original aspect: integration sensitive volume (EPI layer) and front-end readout electronics on the same substrate***
  - *Charge created in EPI, excess carries propagate thermally, collected by N_{WELL}/P_{EPI}, with help of reflection on boundaries with P-well and substrate (high doping)*
    - *Q = 80 e^-h / µm ➔ signal < 1000 e^-*
  - *Compact, flexible*
  - *EPI layer ~10–15 µm thick*
    - *thinning to ~30–40 µm permitted*
  - *Standard CMOS fabrication technology*
    - *Cheap, fast multi-project run turn-around*
  - *Room temperature operation*



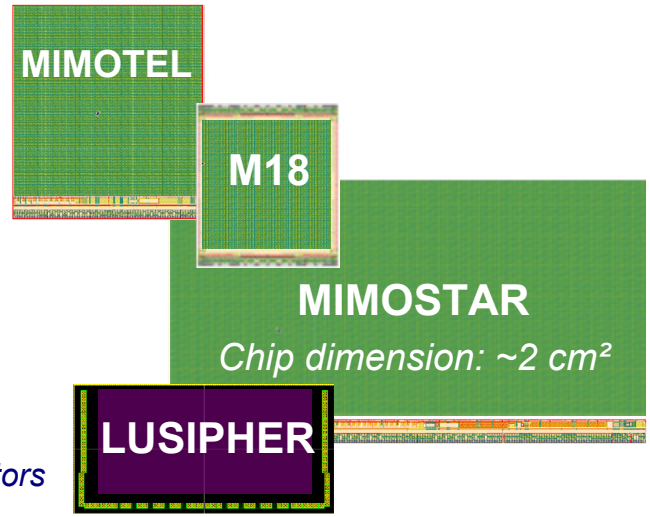
- ➔ ***Attractive balance between granularity, material budget, radiation tolerance, read out speed and power dissipation***

  BUT
  - *Very thin sensitive volume → impacts signal magnitude (mV!)*
  - *Sensitive volume almost un-depleted → impacts radiation tolerance & speed*
  - *Commercial fabrication (parameters) → impacts sensing performances & radiation tolerance*
  - *N_{WELL} used for charge collection → restricts use of PMOS transistors*

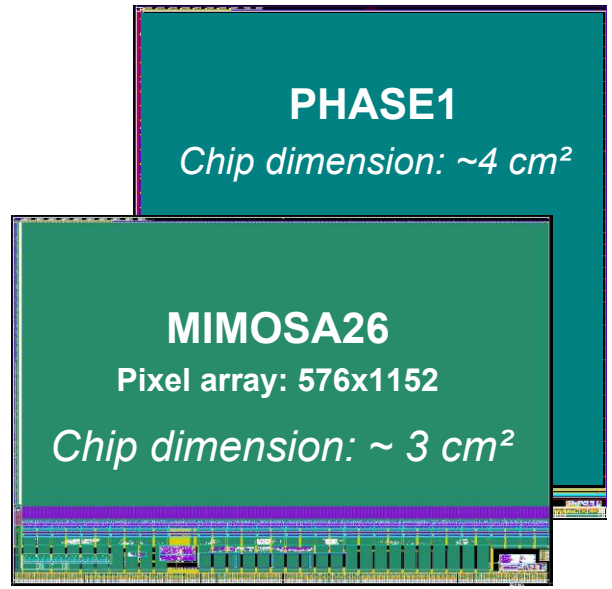
MAPS Final Chips

©C. Hu

- ***Analogue output MAPS***
  - *MIMOTEL (2006): ~66 mm², 65k pixels, 30 µm pitch*
    - *EUDET Beam Telescope (BT) demonstrator*
  - *MIMOSA18 (2006): ~37 mm², 262k pixels, 10 µm pitch*
    - *High resolution EUDET BT demonstrator*
  - *MIMOSTAR (2006): ~2 cm², 204k pixels, 30 µm pitch*
    - *Test sensor for STAR Vx detector upgrade*
  - *LUSIPHER (2007): ~40 mm², 320k pixels, 10 µm pitch*
    - *Electron-Bombarded CMOS for photo and radiation imaging detectors*



- ***Digital output MAPS:***
  - *PHASE1 (2008): ~4 cm², 410k pixels, 30 µm pitch*
    - *Without data suppression, 1st phase of STAR Vx det. upgrade*
  - *MIMOSA26 (2008/09): ~3 cm², 660k pixels 18.4 µm pitch*
    1st MAPS with Integrated Zero Suppression
    - *Final sensor chip for EUDET BT: IPHC-IRFU collaboration*
    - *Combined architectures of MIMOSA22 & SUZE01*
      - *Readout speed: ~10 k frames / s*
  - ***Base line architecture for other experiments:***
    - ➔ *STAR vertex detector upgrade (2010, > 4 cm²)*
    - ➔ *CBM µ-vertex detector SIS-100 phase (2010/2011)*
    - ➔ *ILC vertex detector*



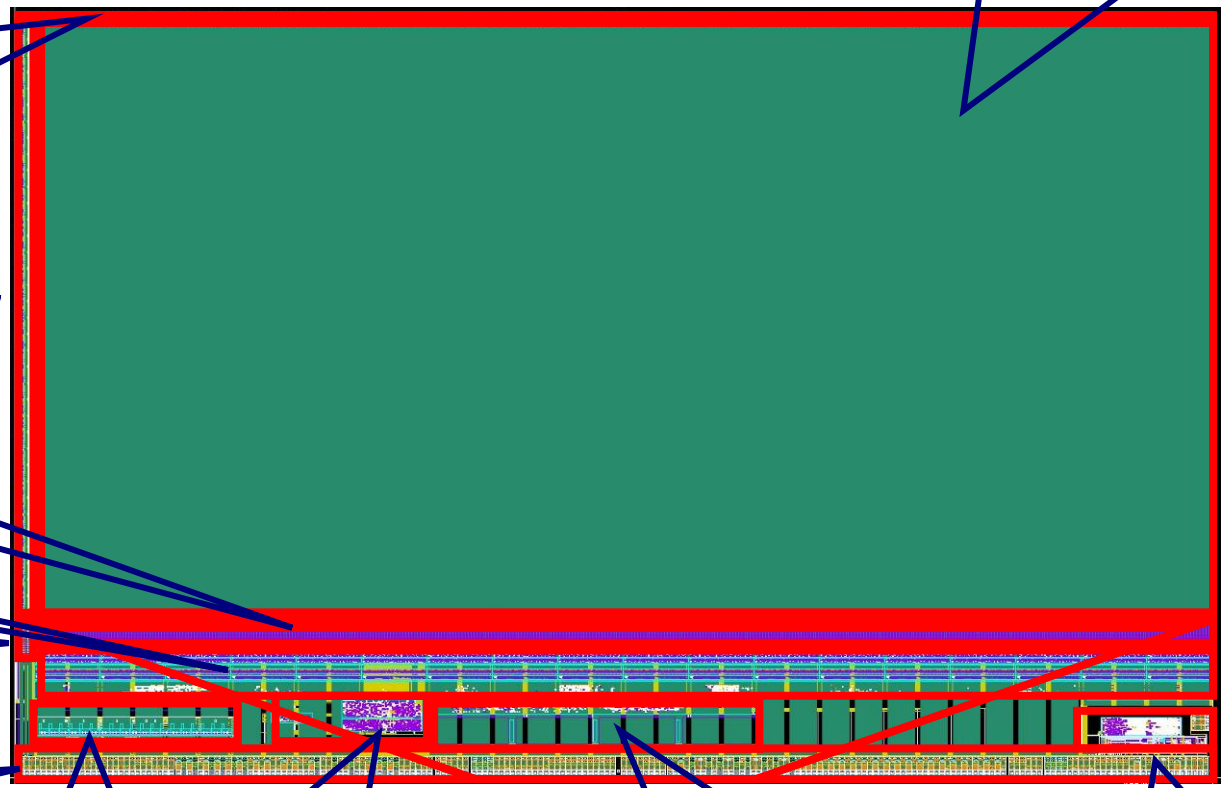
MIMOSA26: 1st MAPS with Integrated Ø

©C. Hu

CMOS 0.35 µm OPTO technology
Chip size : 13.7 x 21.5 mm²

- Pixel array: 576 x 1152, pitch: 18.4 µm
- Active area: ~10.6 x 21.2 mm²
- In each pixel:
  - Amplification
  - CDS (Correlated Double Sampling)

- Testability: several test points implemented all along readout path
  - Pixels out (analogue)
  - Discriminators
  - Zero suppression
  - Data transmission



- Row sequencer
- Width: ~350 µm

- 1152 column-level discriminators
  - offset compensated high gain preamplifier followed by latch

- Zero suppression logic

- Reference Voltages Buffering for 1152 discriminators

- I/O Pads
  Power supply Pads
  Circuit control Pads
  LVDS Tx & Rx

- Current Ref.
- Bias DACs

- Readout controller
- JTAG controller

- Memory management
- Memory IP blocks

- PLL, 8b/10b optional

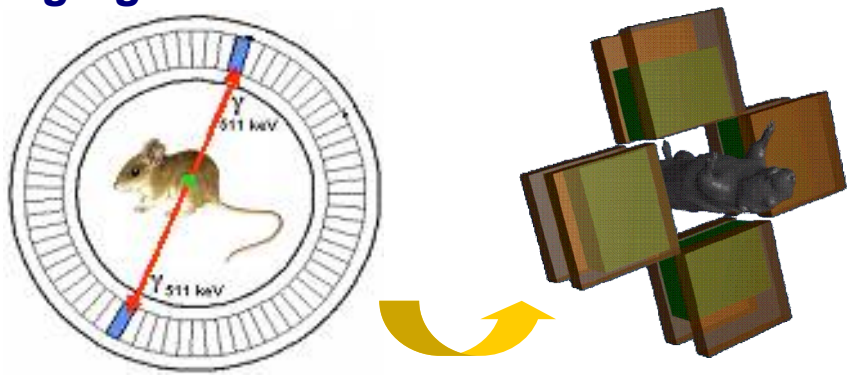
Summary MAPS

- ***The First reticule size MAPS with binary output and integrated zero suppression logic has been designed and fabricated***
  - *Small pitch pixel (18.4 µm), Large sensitive area (> 2 cm^2)*
  - *High binary read-out speed : ~10 K frames/s*
  - ➔ ***2D MAPS have reached necessary prototyping maturity for real scale applications:***
  - *STAR vertex detector upgrade: MIMOSA26x1.7 (may also equip EUDET BT, ~50 µm)*
  - *Architecture will be extended to MVD-CBM (SIS-100) and is proposed for Vx det.-ILC*
- ***The emergence of fabrication processes with depleted epitaxy / substrate opens the door to :***
  - *Substantial improvements in read-out speed and non-ionising radiation tolerance*
    - *Non-ionising radiation tolerance up to 10^{14} N_{eq}/cm^2 is expected*
  - *"Large pitch" applications ➔ trackers (e.g. Super LHC)*
- ***Translation to 3D integration technology :***
  - *Resorb most limitations specific to 2D MAPS*
    - *T type & density, peripheral insensitive zone, combination of different CMOS processes*
  - *Offer an improved read-out speed : O(µs) !*
  - *Many difficulties to overcome (ex. heat, power)*
  - *R&D in progress ➔ 2009/10 important step for validation of this promising technology*

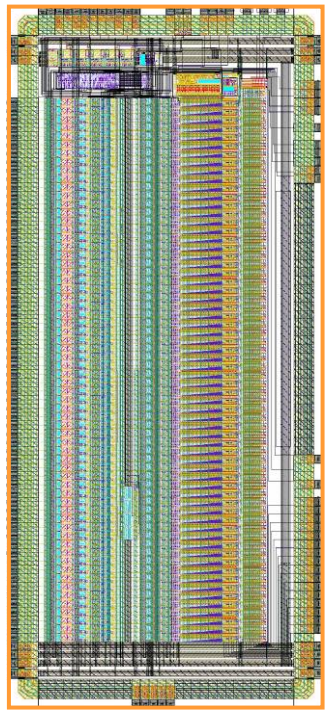
µE for Biomedical Application

©C. Hu

- ***IPHC Imabio Project: small animal PET imaging***
  - *4 modules arranged around the animal*
  - *Matrix of 32 ×24 crystals / module*
    - *1.5mm×1.5mm×25mm LYSO(Ce)*
  - *Read at both ends by MCP photo-detectors*
    - *MCP (Multi Channel Plate)*
  - *3072 crystals and 6144 electronic channels*
  - *100 ASICs of 64 channels*



- ***IMOTEPAD64: 64 channels readout circuit***
  - *Chip dimensions: 3.68 x 8.26 mm², 100 µm pitch*
  - *Input dynamic range: 11 bits, ~ fC – 104 pC*
    - *Adjustable gain : 6 bits*
    - *Shaping time: 300 ns,*
    - *Analogue sampling, < 3 % nonlinearity*
  - *Time resolution: 625 ps ➔ ~ 200 ps (next generation)*
    - *Measured Jitter < 20 ps rms*
  - *Readout frequency: 100 kHz*
    - *CK: 50 MHz*



Microelectronics outside poles

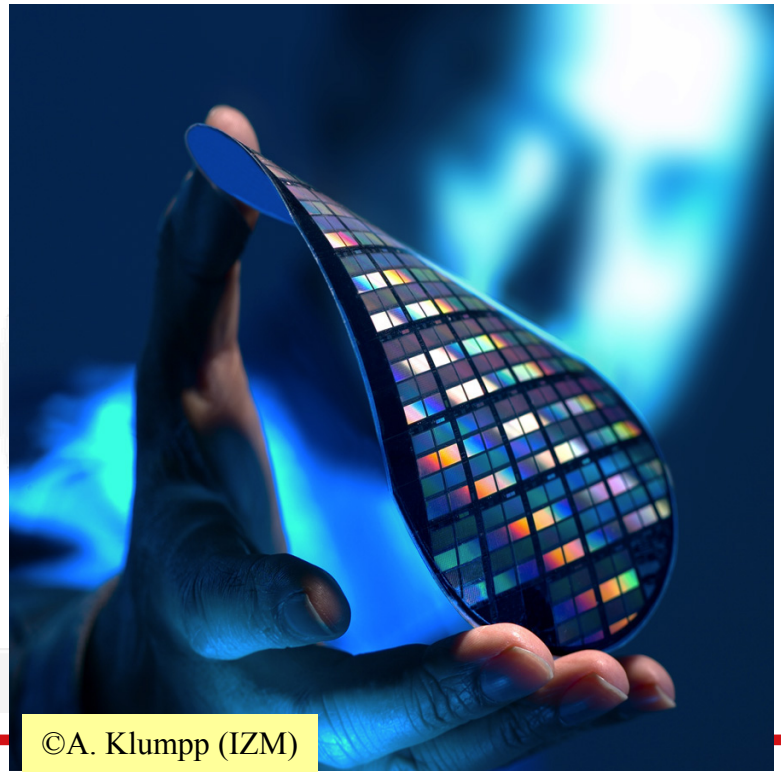
- Some highly specialized “simpler” chips
  - Ex : low temperature mux (APC)
  - CCD readout (LPNHE/LAL)
  - Radio amplifiers (Subatech)…
- Blocks for large chips of experiments
  - Pixel blocks (CPPM)
  - TDCs (Caen, LPNHE…)
  - ADCs (LPSC)…
- A very active R&D in several labs

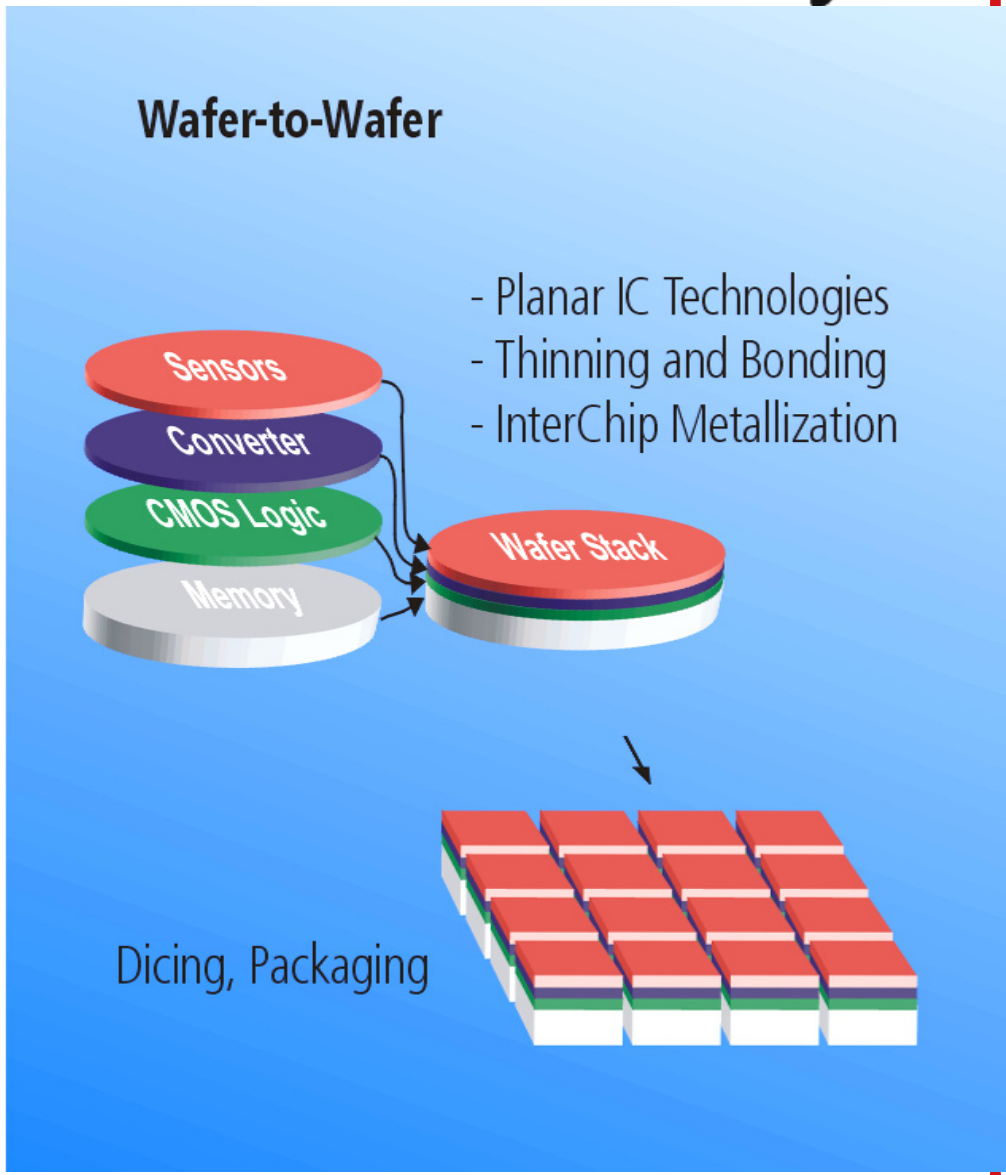
Ex : chips shown at TWEPP 09

- Fast ADCs & DACs for ILC: LPSC Grenoble (L. Gallin-Martell)
- 12 bits 35 MHz ADC : LPSC Grenoble (F. Rarbi)
- MicroMegas DHCAL readout : LAPP Annecy (R. Gaglione)
- DLLs for SNemo : LPC Caen (L. LeTerrier/V. Tocut)
- Discri for FEI4 : CPPM Marseille (M. Mehouni)
- Analog memory for km3 : CPPM Marseille (L. Caponetto)
- ASPIC LSST readout : LAL+LPNHE (F. Wicek)

3D electronics

- Increasing integration density, mixing technologies
- Wafer thinning to <50 µm
- Minimization of interconnects
- Large industrial demand
  - Processors, image sensors…

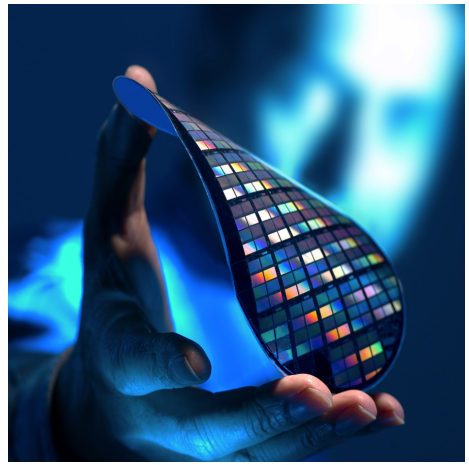


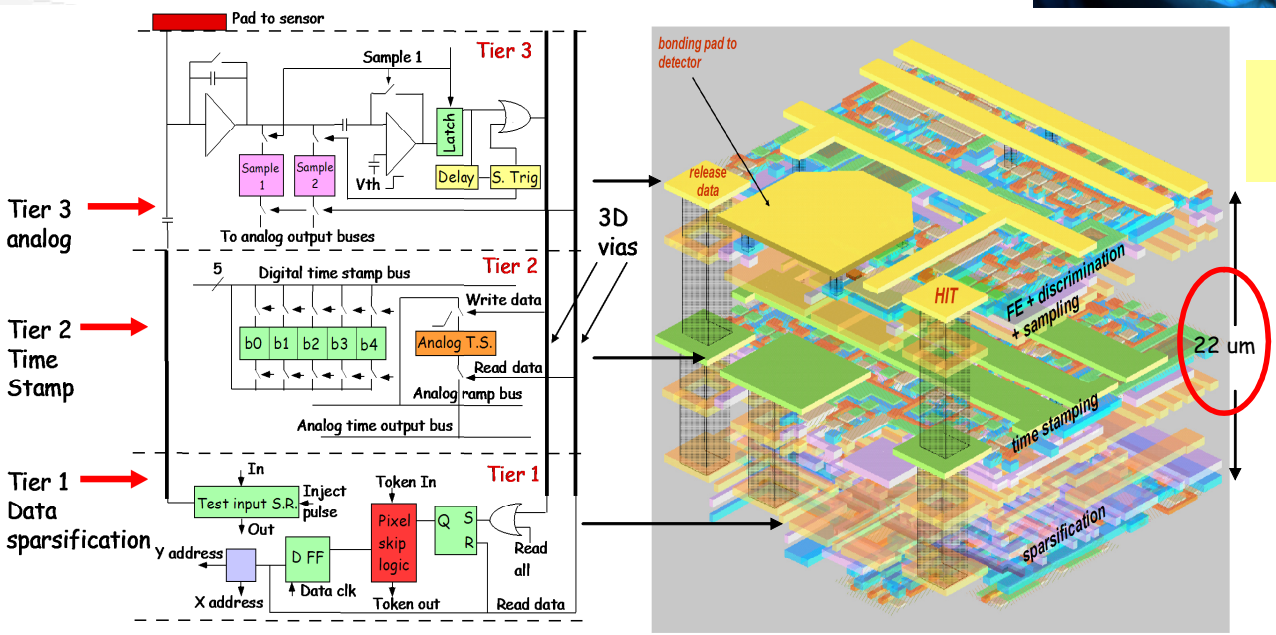


3D technology

- Increasing integration density
  - Large industrial market (imagers, processors, memories…)
  - Uses ~1 µm Through Silicon Vias
  - Requires wafer thinning to ~10 µm
  - A new major revolution coming up !
- Promoted into HEP by Ray. Yarema (FNAL)
  - IN2P3 joined FNAL 3D consortium
  - CPPM, IPHC, IRFU, LAL/OMEGA,LPNHE

©A. Klumpp (IZM)





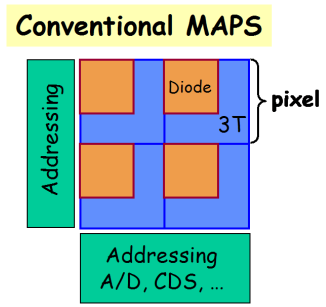
V1P1 3D chip by FNAL

Major Markets for 3D [R. Yarema FNAL]

©R. Yarema (FNAL)

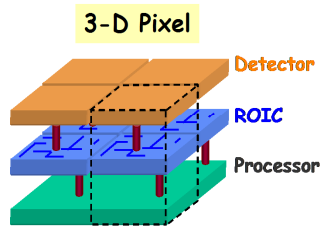
- Pixel arrays for imaging

  Pixel arrays with sensors and readout are well suited to 3D integration since signal processing can be placed close to the sensor. Current 2D approaches cannot handle the data rate needed for high speed imaging.



- Memory

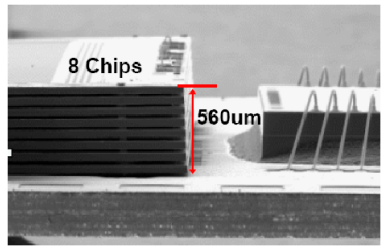
  All major memory manufactures are working on 3D memory stacks. Significant cost reductions can be expected for large memory devices. The cost of 3D can be significantly less than going to a deeper technology node.



- Microprocessors

  A major bottleneck is access time between CPU and the memory. Memory caches are used as an interface but the area required is significant. Initial applications for 3D will use Logic to Memory, and Logic to Logic stacking.

< NAND 8 Stacked Memory Card >



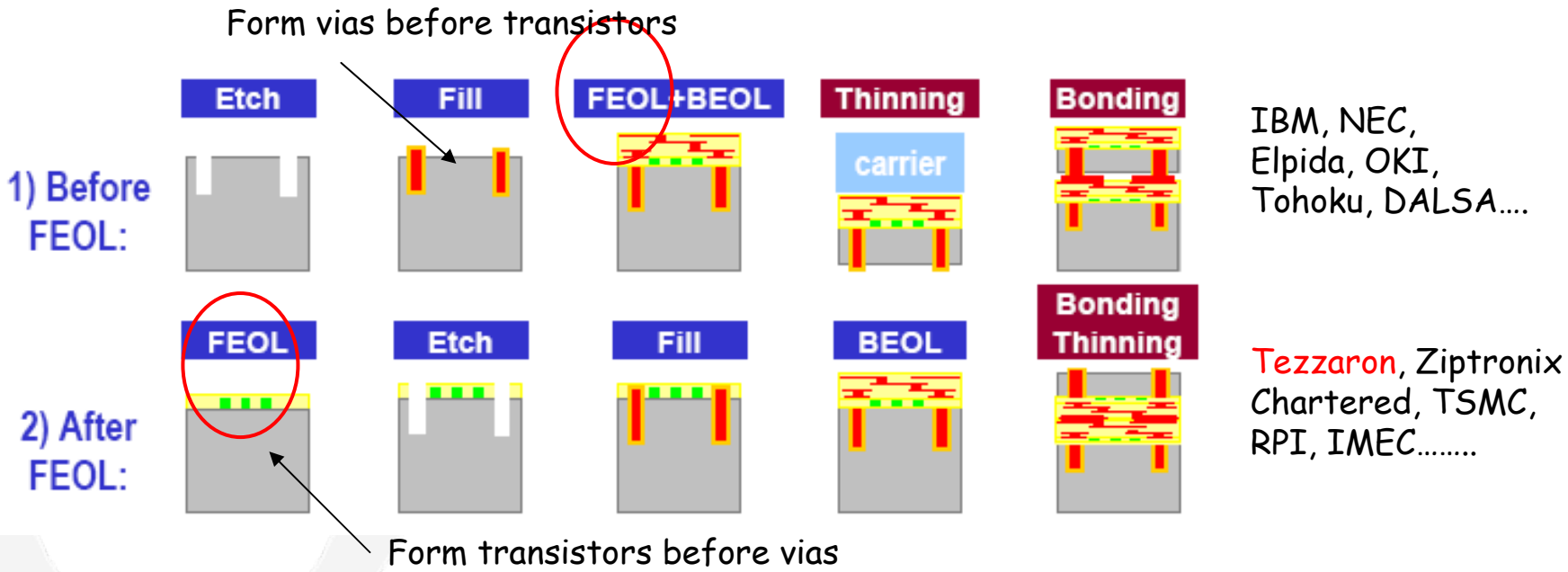
(Samsung)

Basic Principles of 3D Integration

- Vias
  - Via First – done at foundry, lowest cost
  - Via last – after wafers are made, often done by third party vendors.
  - General movement in industry toward via first approach
- Bonding options
  - Mechanical bond only, electrical connections later
    - Oxide to oxide bonding
    - Adhesive such as BCB
  - Mechanical and electrical connection formed together
    - CuSn Eutectic
    - CuCu Fusion
    - Direct Bond Interconnect – combination of oxide bonding and metal fusion
- Thinning
- Alignment

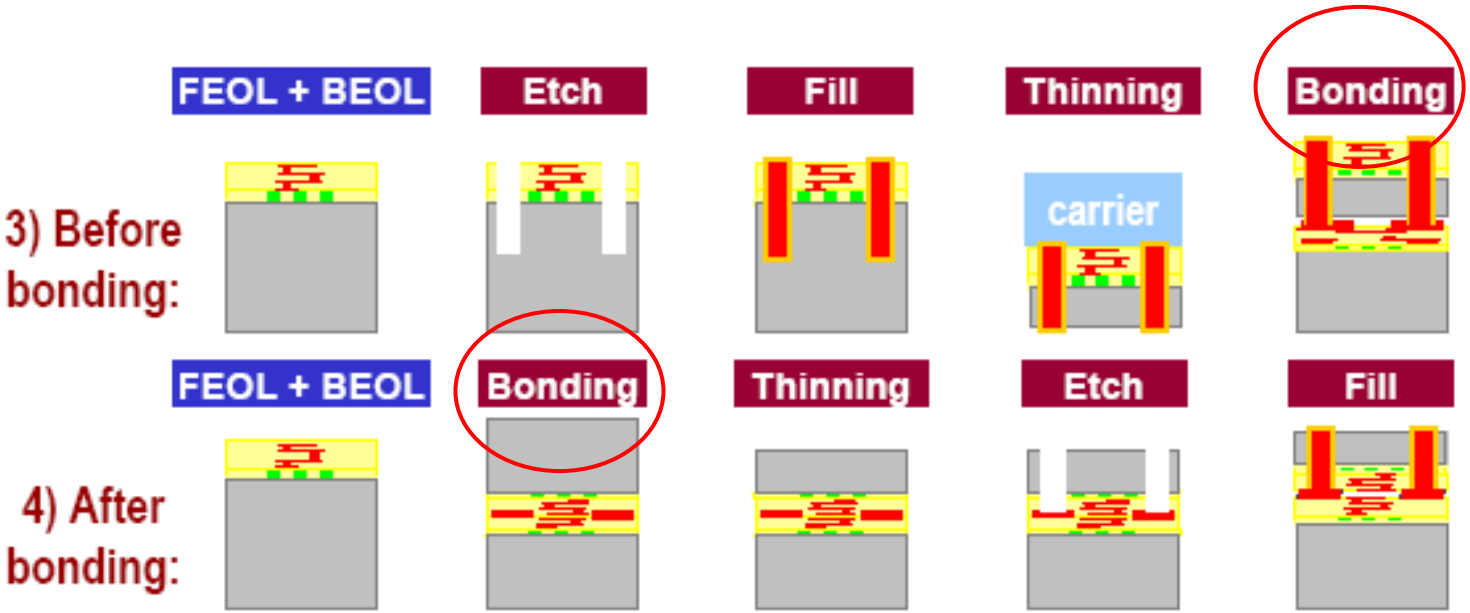
Via first approach

- Through silicon Via formation is done either before or after CMOS devices (Front End of Line) processing [7]



Via last approach

- Via last approach occurs after wafer fabrication and either before or after wafer bonding [7]



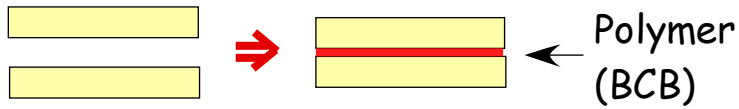
Notes: Vias take space away from all metal layers. The assembly process is streamlined if you don't use a carrier wafer.

Bonding choices

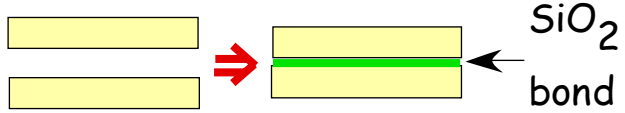
Electrical and Mechanical Bonds

Fermilab experience

a) Adhesive bond

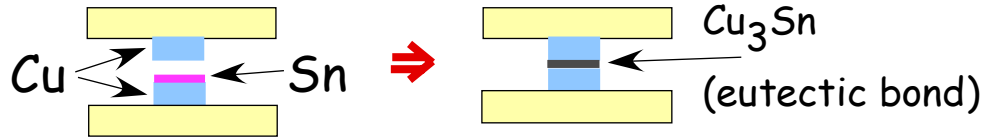


b) Oxide bond (SiO2 to SiO2)



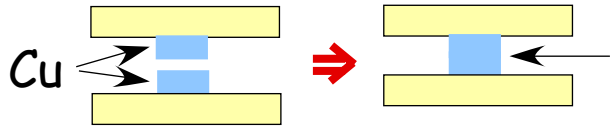
(MIT LL)

c) CuSn Eutectic



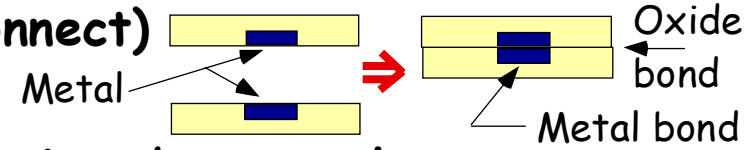
(RTI)

d) Cu thermocompression



(Tezzaron)

e) DBI (Direct Bond Interconnect)



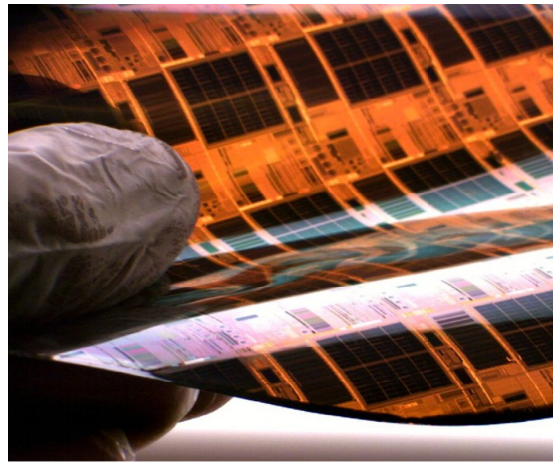
(Ziptronix)

For (a) and (b), electrical connections between layers are formed after bonding. For (c), (d), and (e), the electrical and mechanical bonds are formed at the same time.

Thinning and Alignment

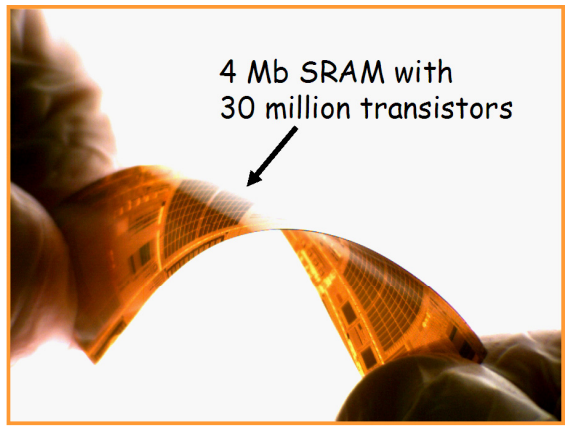
- Thinning –
  - Thinning is done by a combination of grinding, CMP and etching.
  - Through wafer vias typically have an 8 to 1 aspect ratio for etched vias. Thus, in order to keep the area associated with the vias as small as possible, the wafers should be as thin as possible.

©R. Yarema (FNAL)



6 inch wafer thinned to 6 um and mounted to 3 mil kapton

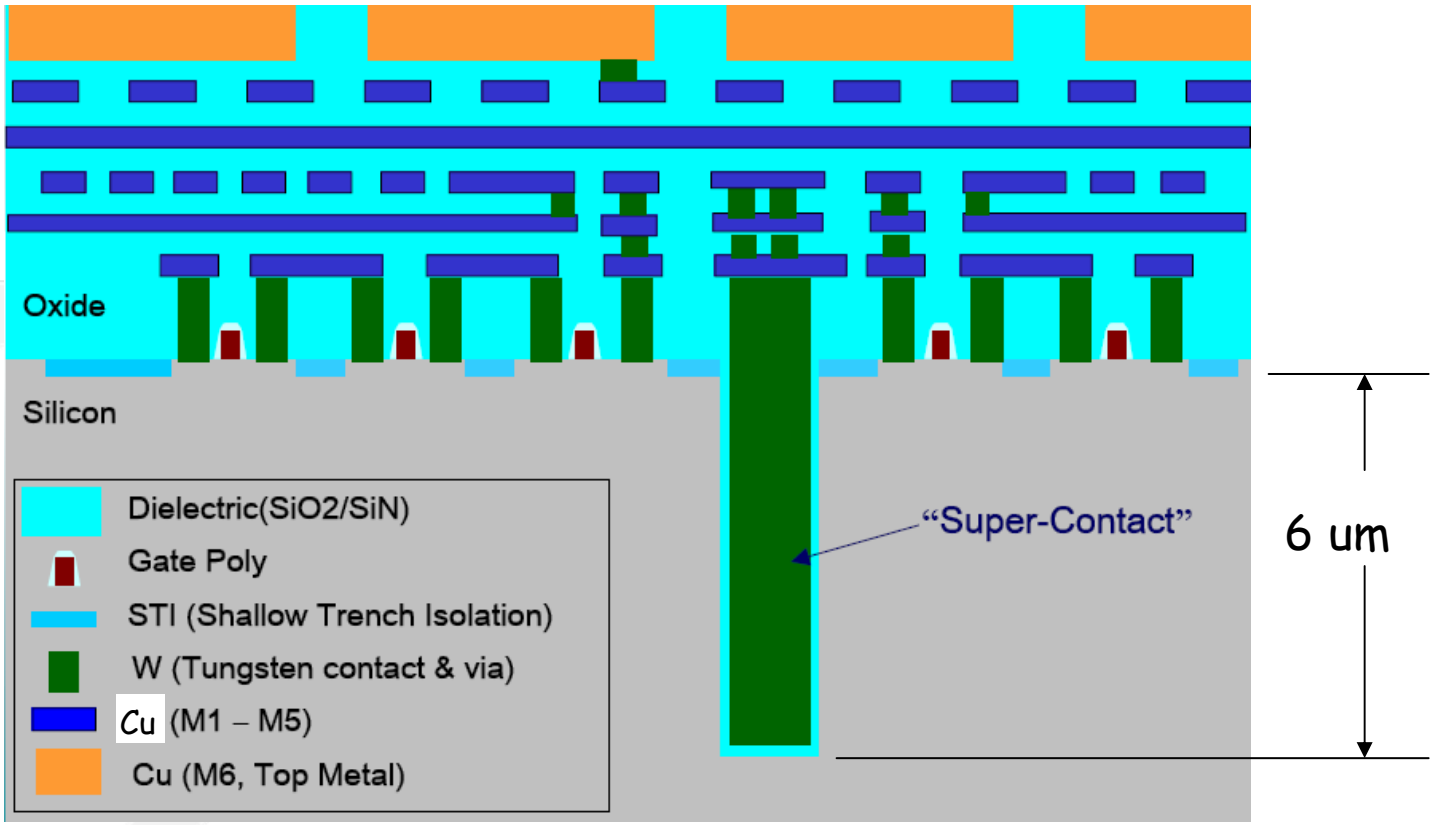
- Alignment
  - Alignment of better than 1 um (3 sigma) is now possible on wafer to wafer bonding.



Photos from MIT LL

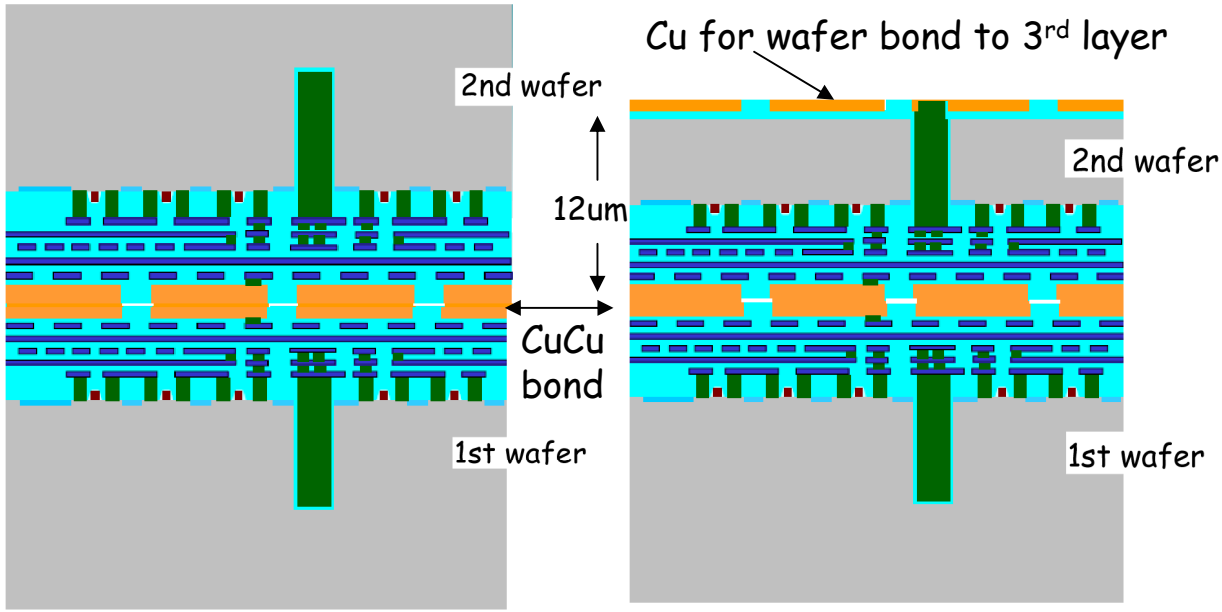
Tezzaron 3D process

- Complete back end of line (BEOL) processing by adding Cu metal layers and top Cu metal (0.8 um)



Tezzaron 3D process

Example: bonding identical wafers



Flip 2nd wafer on top of first wafer.

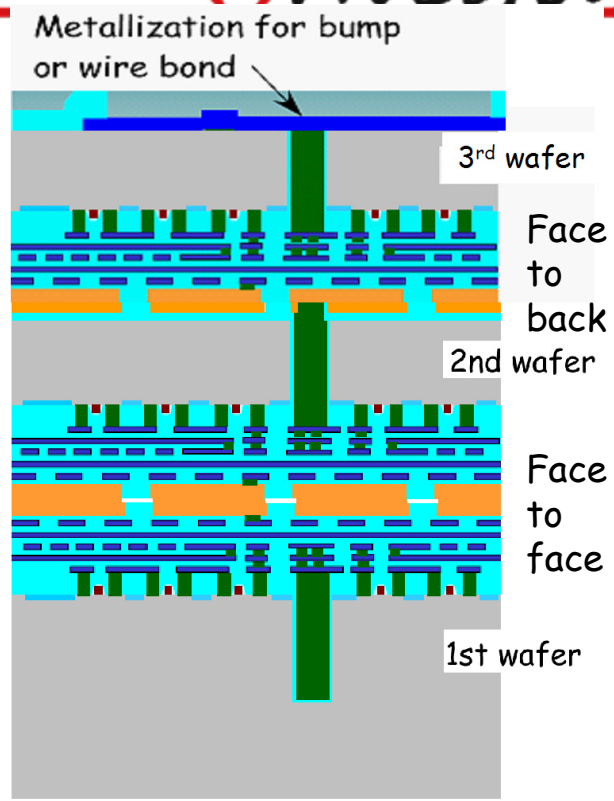
Bond second wafer to first wafer using Cu-Cu thermo-compression bond.

Thin second wafer to about 12um to expose super via.

Add metallization to back of 2nd wafer for bump bond or wire bond.

OR

Add Cu to back of 2nd wafer to bond 2nd wafer to 3rd wafer



Flip 3rd wafer

Bond 3nd wafer to 2rd wafer.

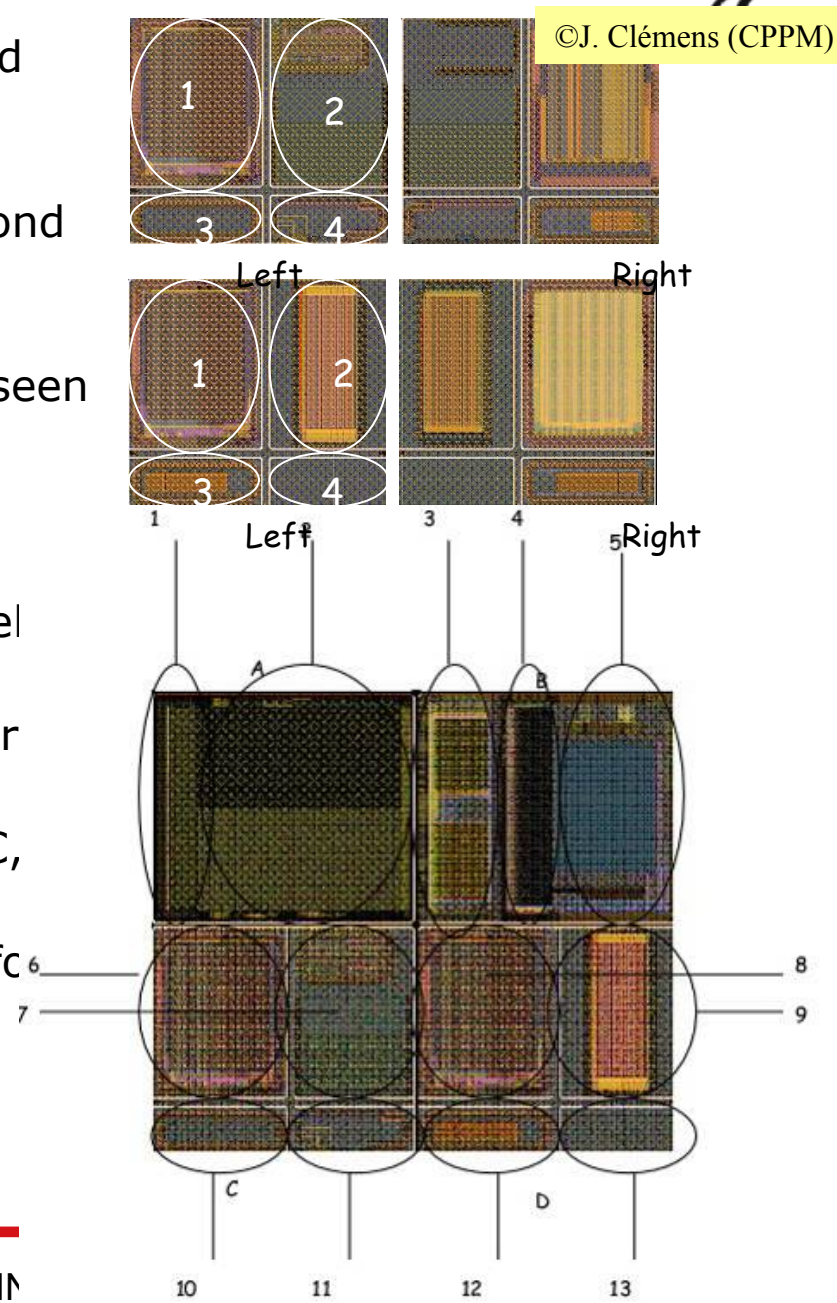
Thin 3rd wafer to expose super via.

Add final passivation and metal for pads

IN2P3 participation in 3D FNAL run

- CPPM/Bonn - ATLAS 2D pixel design based on earlier design in IBM 0.13 um (FEI4_prototype)
- CPPM – SEU resistant register and TSV/bond interface daisy chain to measure TSV and bond yield.
- CPPM/Bonn – ATLAS 3D pixel design foreseen for ATLAS upgrade
- OMEGA – 24x64 pixel array for SLHC

- IPHC_INFN CAIRN_1: - Multi purpose pixel sensor: ILC, bio-medical applications …
- IPHC_IRFU CAIRN_2: Prototype sensor for ILC with rolling shutter readout mode
- IPHC CAIRN_3: - Prototype sensor for ILC, 12 µm pitch, 5 bits time stamp
- IRFU-IPHC CAIRN_4: - prototype sensor fc ILC with rolling shutter readout mode
- CMP Memory: CMP Anti-latch up SRAM



Club “digital electronics” ?

- Partage d’IPs en VHDL
- Partage de savoir faire
- Se connaitre entre collègues de l’IN2P3 et savoir qui (a) fait quoi
- Profiter de la réunion biennale organisée par C. Colledani (IPHC)

Conclusion

- Microelectronics getting more complex : needs strong, experienced teams, gathered in poles to realize mixed signal SoC (system on chip)
- Select few technologies (eg SiGe 0.35 µm, IBM & Chartered 130nm) to share designs and experience
- Networking facilitated by IN2P3 organization
- Electronics should not be reduced to microelectronics

Backup slides