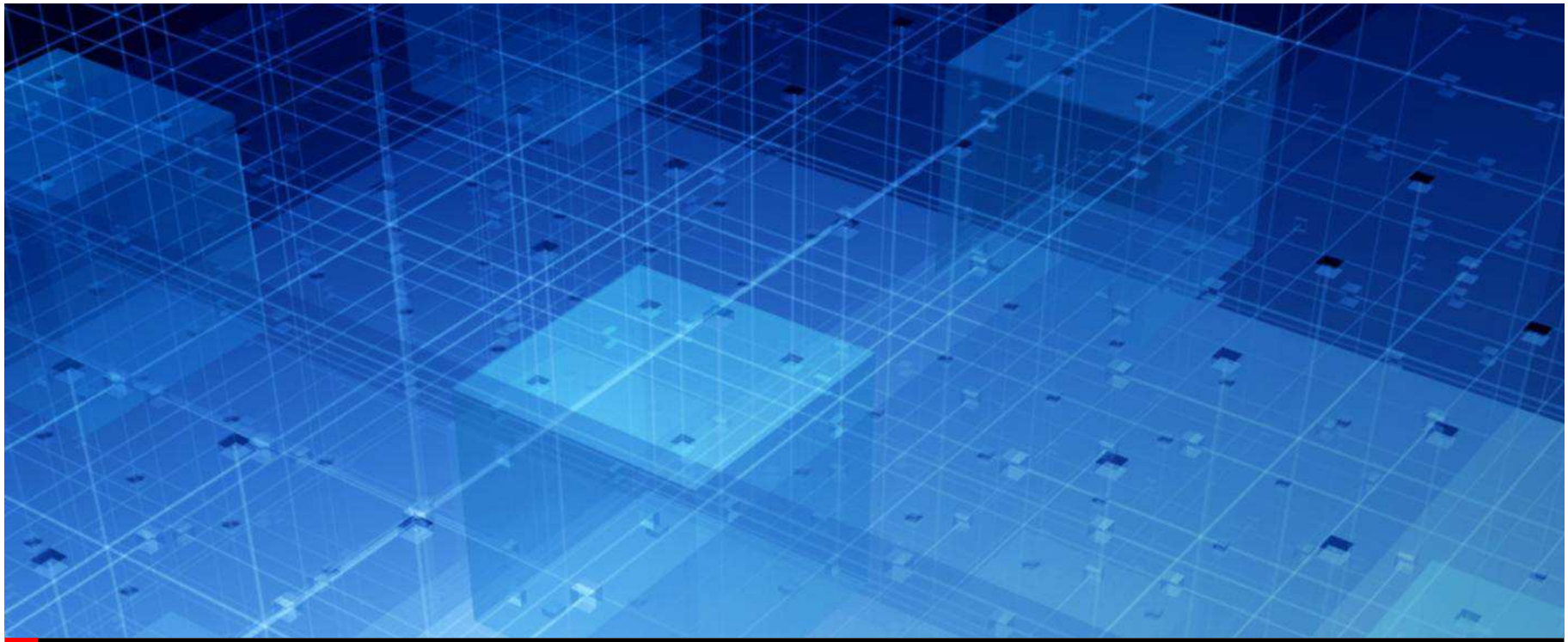


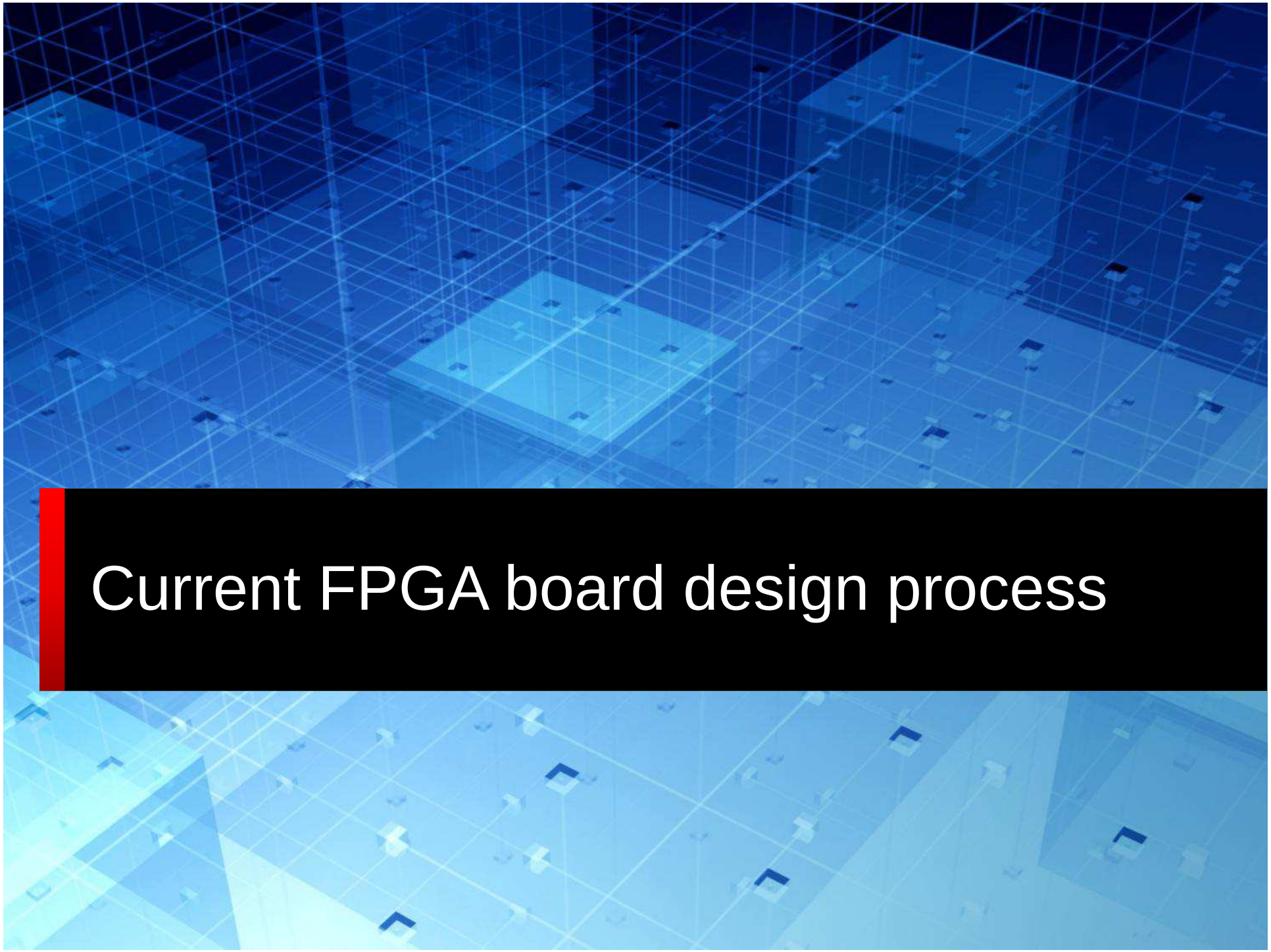
Speed-up FPGA-PCB Co-Design with Cadence FPGA System Planner

Martin Biehl (mbiehl@cadence.com) & Nagesh Gupta
Ecole d'électronique numérique
Fréjus
27.Nov.2012

cadence®

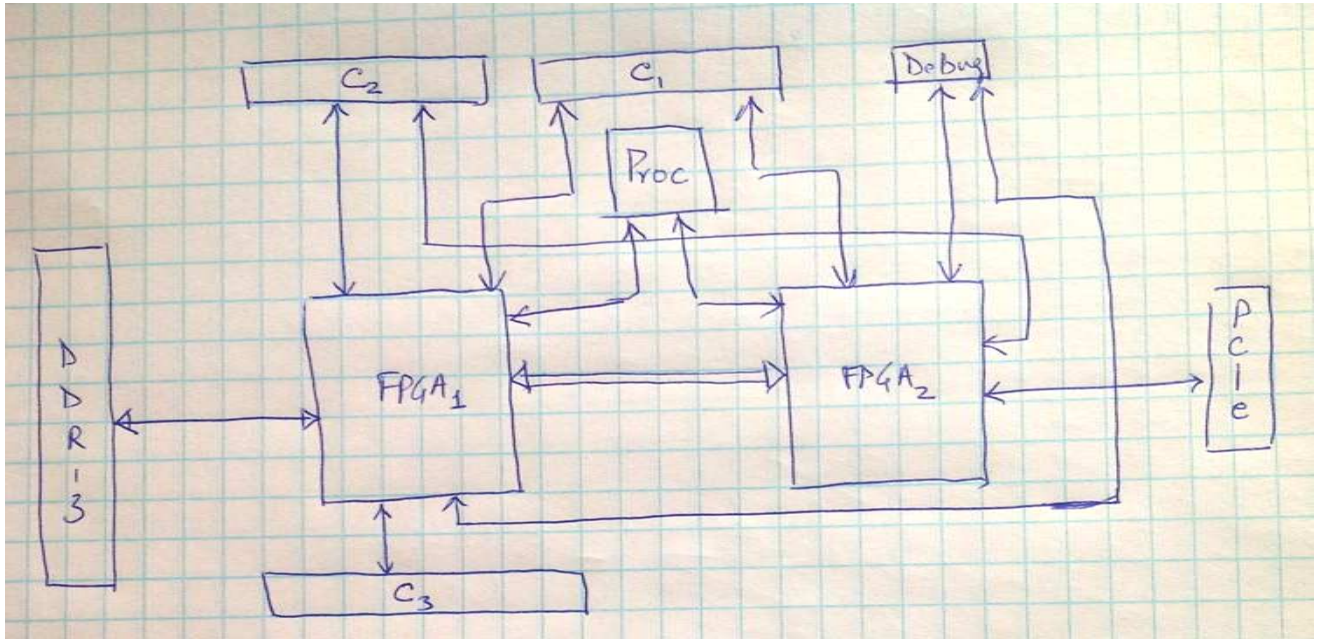
Agenda

1. Current FPGA board design process
2. FPGA design using Cadence FSP
3. Tool flows
4. Value Proposition


Current FPGA board design process

Design your board architecture & placement

- Paper, white board, Visio or…
- Get an idea of part locations, communication between components
  - What's going to be difficult from FPGA perspective?
  - Identify potential board issues
- Is this really do-able?
  - Not sure before taking the next steps



FPGA selection

- Does the FPGA package/pin count suffice?
- How much head room will be available in the FPGA fabric?
- Will Marketing come up with requirements later in the design cycle that may cause change to the selection?
- Is this package/FPGA going to be available in time for my design => or will I need to make changes later in the cycle?

Review, decide & move on!

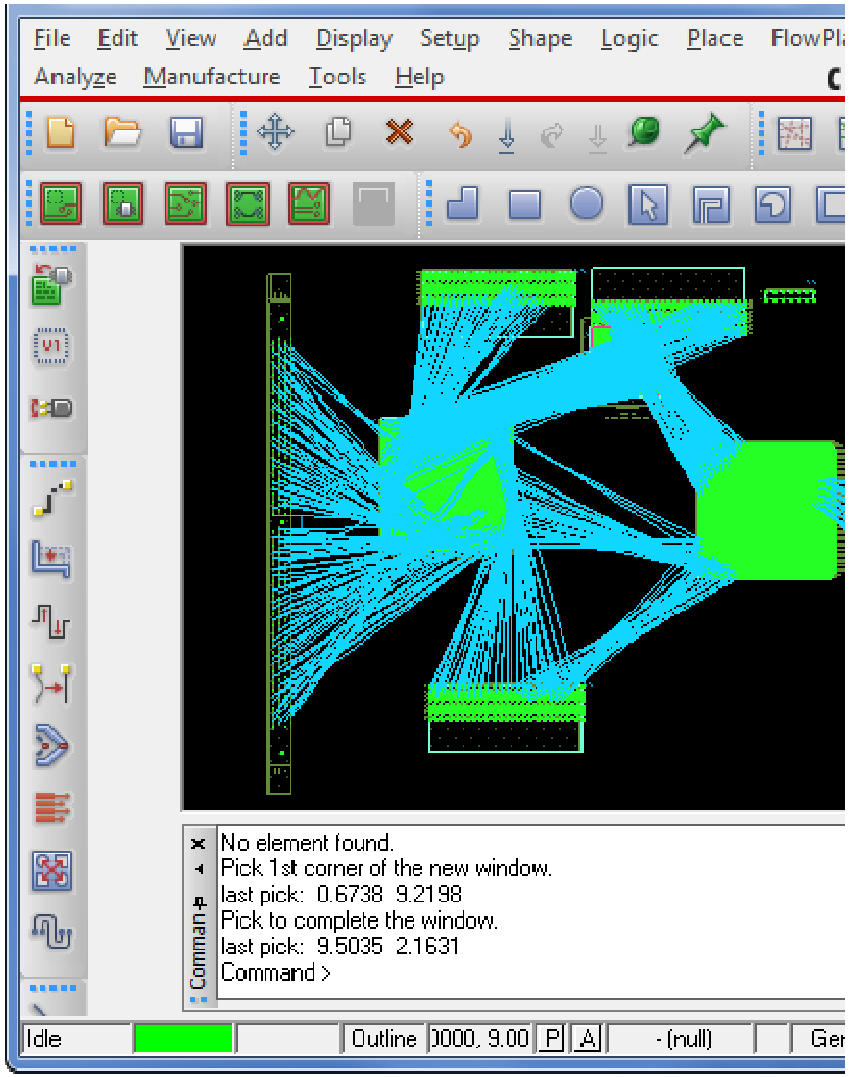
FPGA design & pin allocation

- Excel/FPGA vendor tools, or a combination
- Combined process with FPGA designer & FPGA schematic owner
- Identify FPGA banks for different voltages – make sure to consider board placement while assigning pins!
- Assign pins manually or semi-automatically using FPGA vendor tools

Provide the FPGA pins in Excel/text to FPGA schematic designer

FPGA Schematics & Layout

- Create design specific FPGA symbols or use generic FPGA symbols created by library group
- Draw schematics to make connections as per the pin allocation
- Package the design & bring it to PCB layout tools
- For the first time, you get to see the layout of the parts on the board, and the design rats-nest!
  - Now how do you make any changes to the pin assignments?
  - Go through the process of suggesting changes to the FPGA designers, or give up any optimization?



What if…

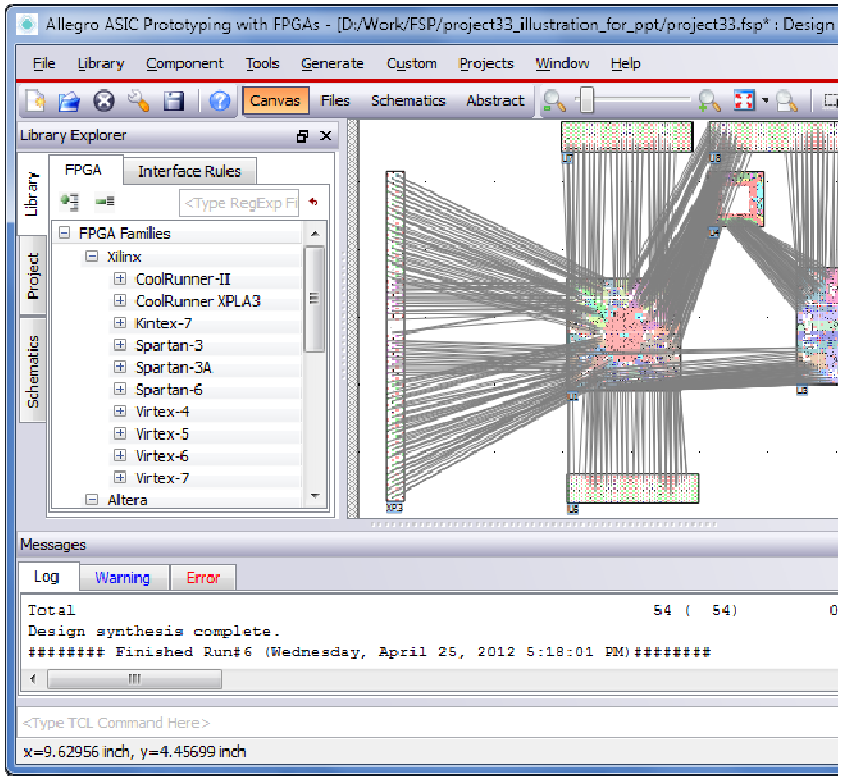
- FPGA logic requires you to change the FPGA used?
- Board mechanical & thermal team requires moving some parts to the bottom of the board
- FPGA or other component availability requires you to change the part used?
- Marketing has new requirements?

• FPGA board is more difficult to change than FPGA front-end
• FPGA board changes will become the critical path in the project

FPGA board using Allegro FSP

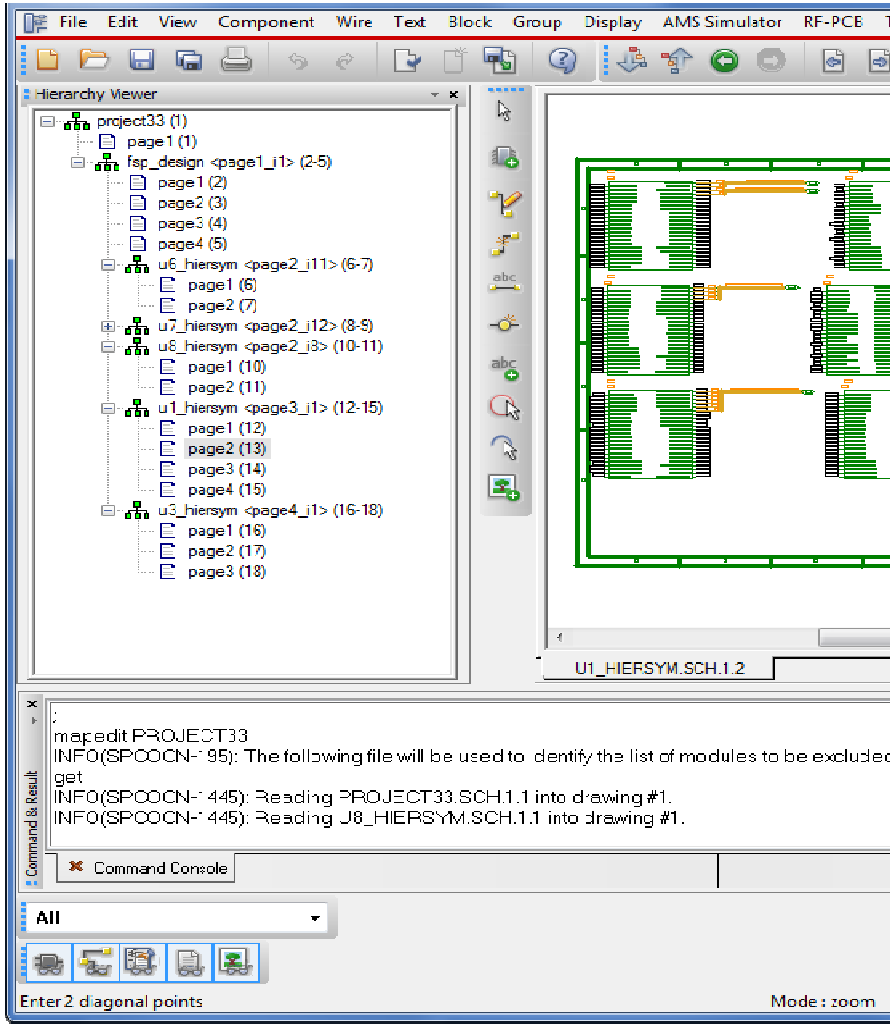
Board Architecture

- FSP provides a canvas that represents the actual board
  - Place your parts from your library on the FSP canvas
- FSP uses a patented, rules based I/O synthesis engine to automatically determine the best connections
- With these two key provisions, you can try different architectures before locking the placement



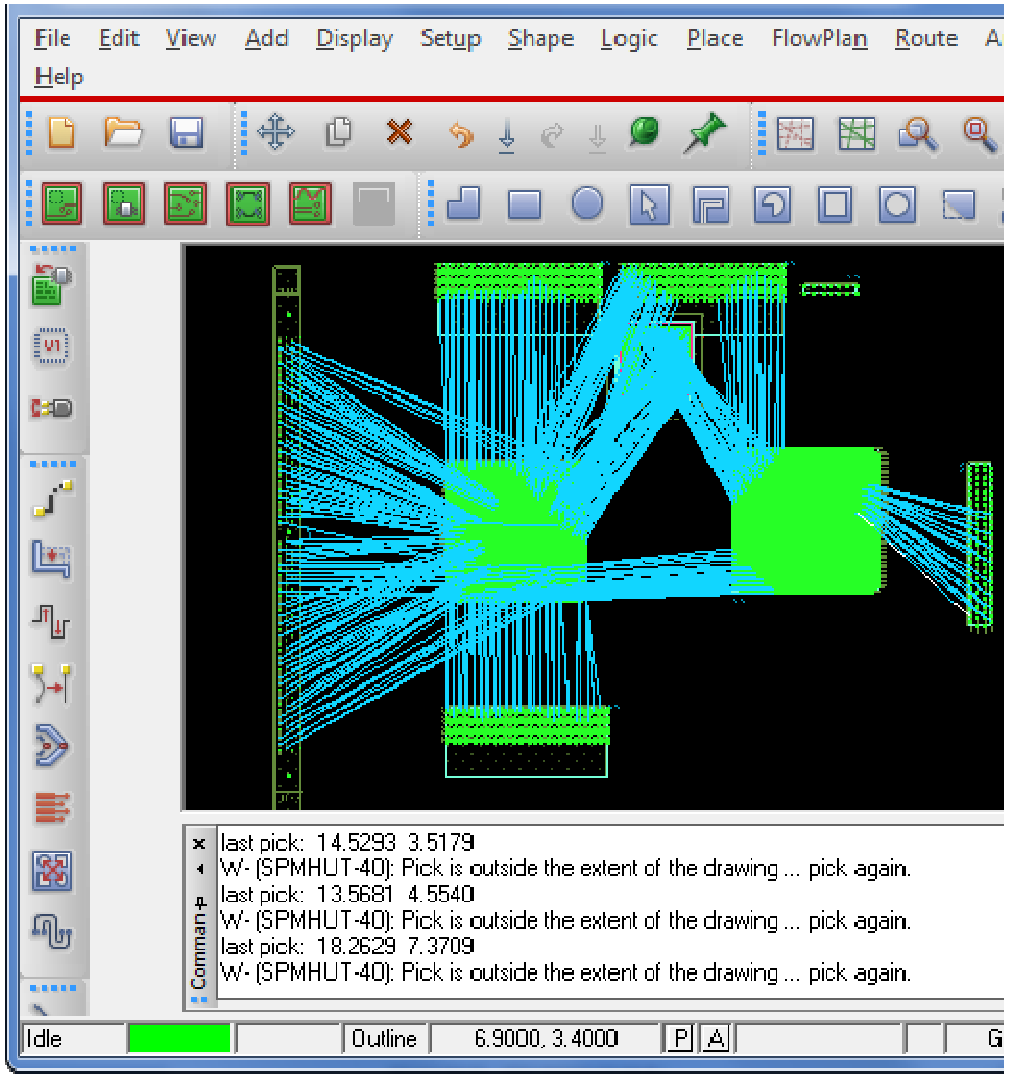
Generating schematics & symbols

- Schematics are auto-generated by FSP
  - Either use your symbol library and let FSP generate the connectivity, or let FSP generate symbols & connectivity
- Schematics for the FPGA is integrated with the rest of the schematics through hierarchy
- These two features enable design changes at a significantly reduced cost



Optimizing the design in Allegro PCB (ECO)

- PCB designer can perform final optimization using the FSP engine to guide the pin swapping
  - Changes are fully FPGA compliant
  - PCB designer is restricted to make only valid changes
- Enables FPGA & PCB designs to converge to a system optimized solution quickly

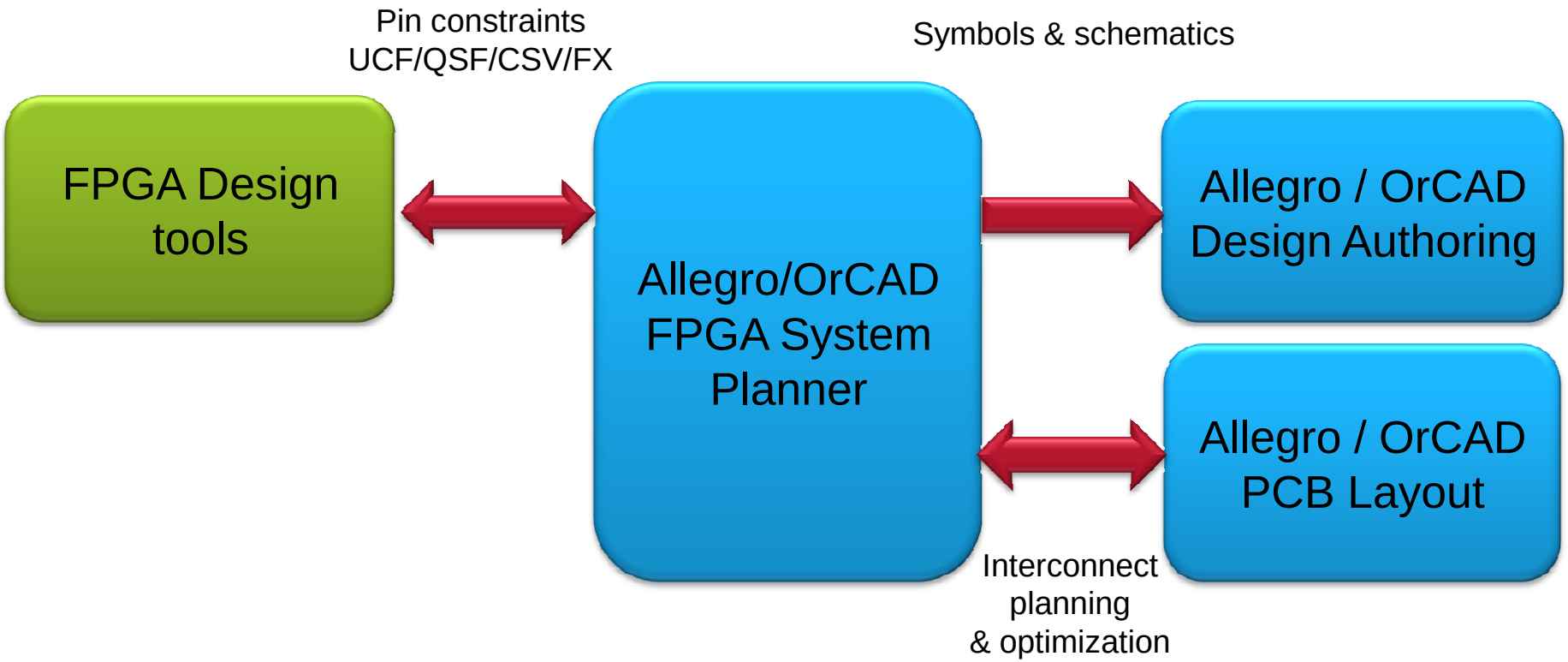


Making late stage changes to the design

- Changes are easy
  - Change the FPGA to another FPGA in the family
  - Change and replace any parts interfacing with the FPGA
  - Flip the FPGA to the bottom/top etc.
- Once the changes are made in FSP, they are propagated to the rest of the design easily
  - Completing the changes in the PCB design flow can be done within a few hours as opposed to weeks!

Tool flow using Cadence FSP

Allegro FSP – interface with tools



Value proposition

Value Proposition
For the project team, company

- Reduces the design cost
  - Reduces the need for design iterations by selecting optimal pin locations for both FPGA & PCB
  - Enables design changes at a much reduced cost during all stages of the project
  - Eliminates PCB design data thrashing by automating FPGA design-in process
- Reduces the end product manufacturing cost
  - Reduces PCB layer count or enables designing within the planned layers through placement aware pin assignment and optimization
- Eliminates physical prototype iterations due to FPGA pin assignment errors


cadence®