



XILINX

ALL PROGRAMMABLE™

Xilinx 7 Series FPGAs Transceiver Technical Module

Gregory Donzel, FAE SILICA XILINX

Ecole d'Electronique IN2P3, 27 Novembre 2012



ACCESS
GRANTED

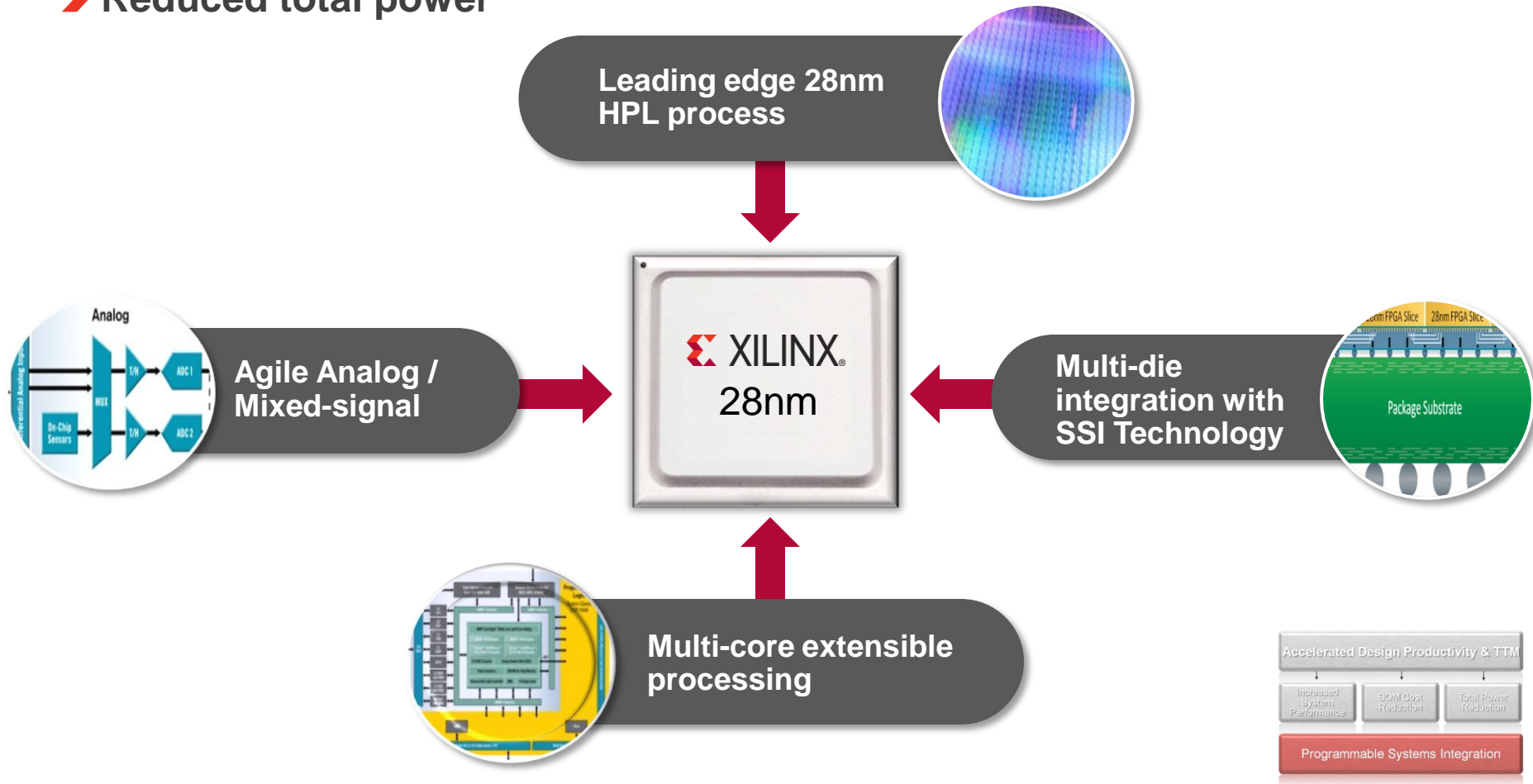
Expanding Programmable Technology Leadership

- Committed to be First to Process Nodes
- Pioneering 3-D IC Technology
- Leading Edge Transceiver Technologies
- Programmable Analog/Mixed Signal
- System to IC Tools & IP to Enable Silicon

**From Programmable Logic to
Programmable System Integration**

Four Unique Systems Integration Technologies

- Increased system-level performance
- Reduced BOM cost
- Reduced total power



Agenda

- **7 Series Transceiver Quick Take**
- **7 Series Transceiver Performance Delivered**
 - 7 series GTZ performance
 - 7 series GTX performance
- **Xilinx Transceiver History and Roadmap**
- **Design with 7 Series Transceiver**
 - Architecture Block Diagrams
 - Backplane and Equalization
 - Optics Support
 - Power Advantage
 - Modeling and Simulation
 - Power Integrity
- **Tools : Transceiver Wizard And ChipScope Pro SIOTK (IBERT)**
 - Demos
- **7 Series Product Table**
- **Summary**



XILINX

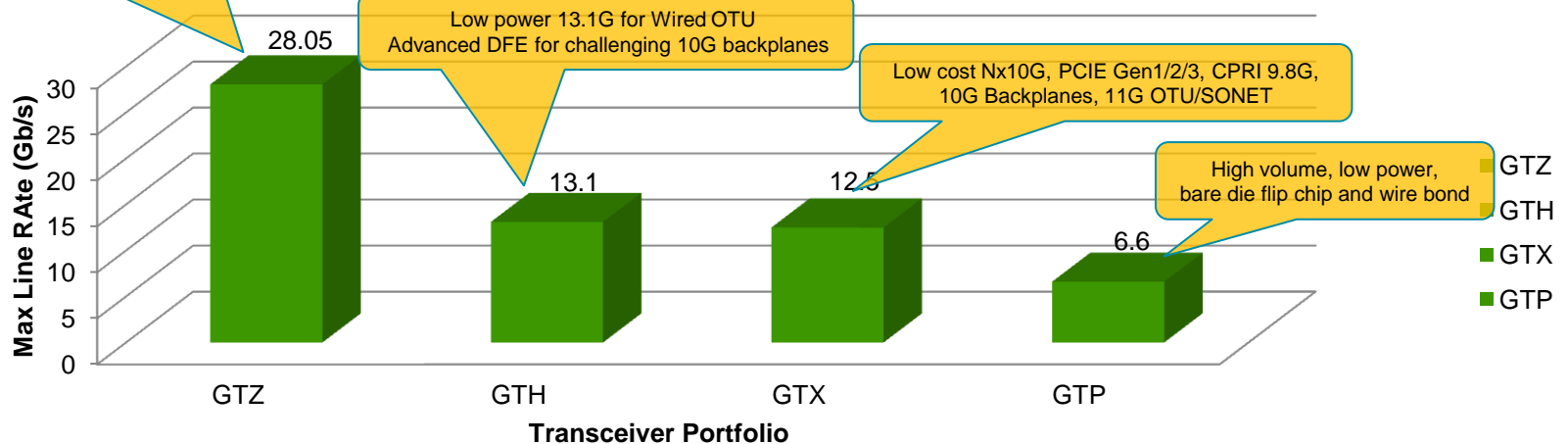
ALL PROGRAMMABLE™

Xilinx 7 Series Transceiver Quick Take

Xilinx 7 Series Transceiver - Portfolio and Bandwidth

Industry leading 28G with SSI for 100G/400G data path
100GE, SONET/OTU, FC, Aurora, CPRI 19.6G

7 Series Transceiver Max Line Rate



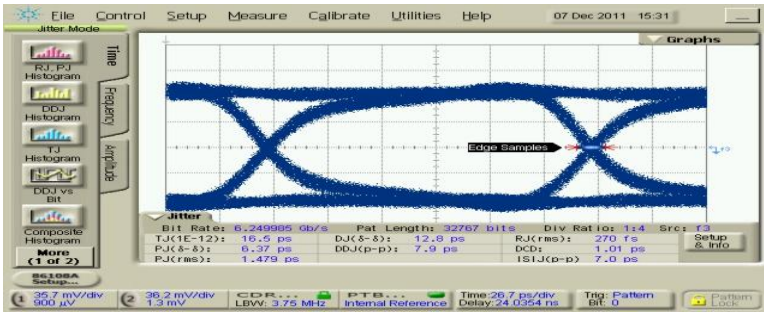
- 7 series offers a full transceiver portfolio for variant customer needs
 - Ultra-high performance GTZ: **28.05Gb/s X 16**
 - High-end Low-power GTH: **13.1Gb/s X 96**
 - Mid-Range GTX: **12.5Gb/s X 32**
 - High-Volume Low-Power GTP: **6.6Gb/s X 16**
- Virtex-7 HT has up to **2.802Tbps** total transceiver bandwidth
 - 16 GTZ and 72 GTH transceivers



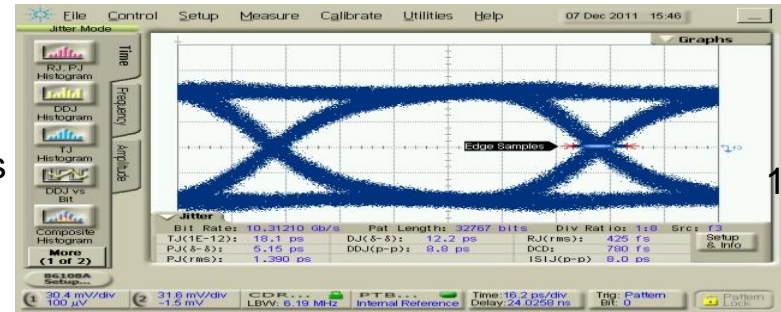
Increased System Performance

High Line Rate and High Count Boost System Throughput

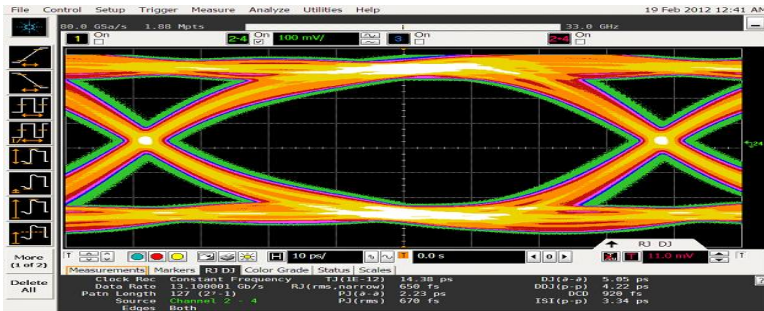
Xilinx 7 Series Transceivers Jitter Performance



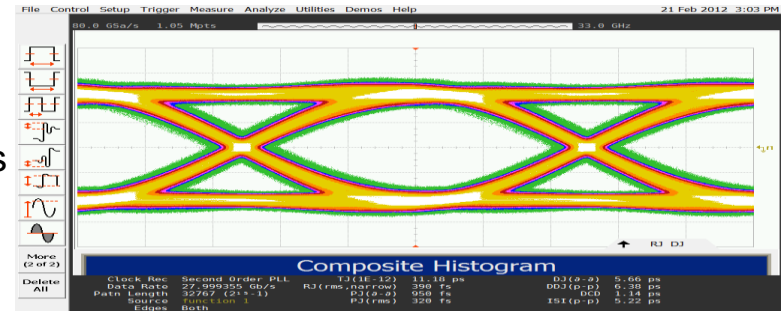
6.25Gb/s



10.3125Gb/s



13.1Gb/s



28Gb/s

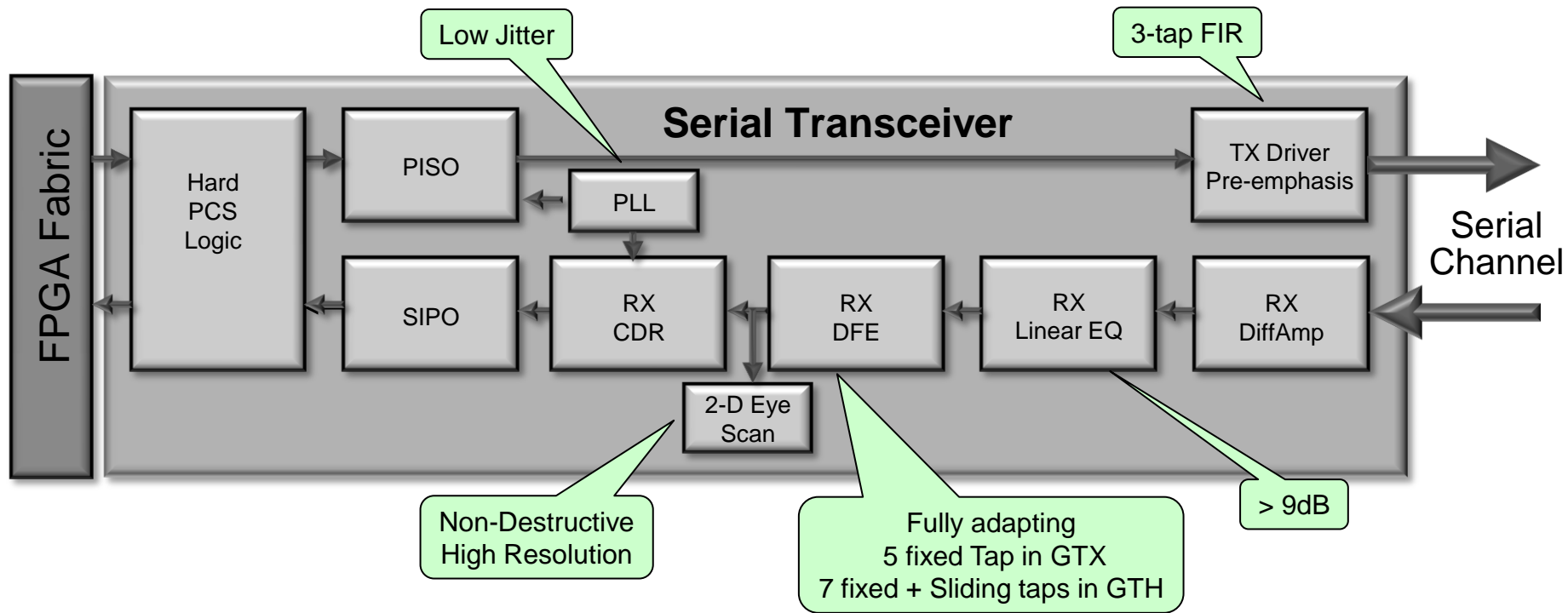
- Note: The eye diagrams and jitter are measured with PRBS15 or PRBS7 data pattern on early sample devices at nominal conditions
- 7 series transceivers offer the best jitter performance at 6Gb/s, 10Gb/s+ and 28Gb/s in FPGA industry
 - Both transmitter and receiver use the high performance PLL



Increased System Performance

Low Jitter is the First Guarantee of an HSSI System Performance

Xilinx 7 Series Transceiver Signal Integrity



- 7-GTH will have the best equalization capability in FPGA industry
 - Compensate **reflection** in **long** channels thus support tough 10G backplanes
- 7-GTX equalization is only second to 7-GTH in FPGA industry
 - Fully auto-adaptive DFE for easy link tuning



Increased System Performance

Best in Class Signal Integrity and Fully Adaptive Link Tuning



XILINX

ALL PROGRAMMABLE™

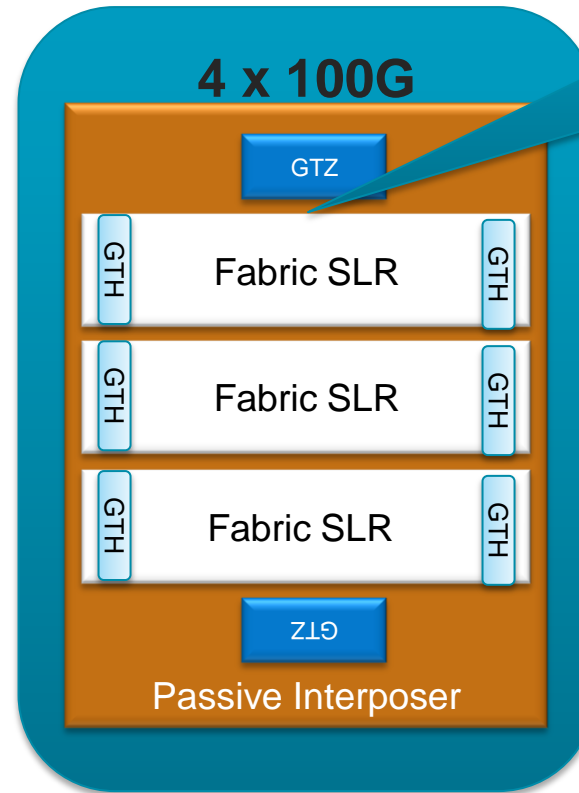
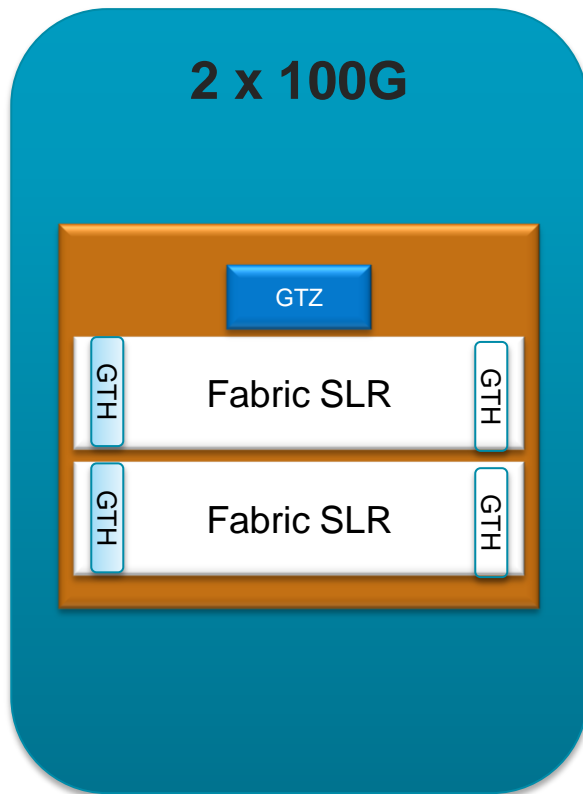
Xilinx 7 Series Transceiver Performance Delivered

7 series HT Devices Overview

Supports up to four 100G CFP2 optical modules

GTZ 8 lanes / 28G
12 lanes / 13G

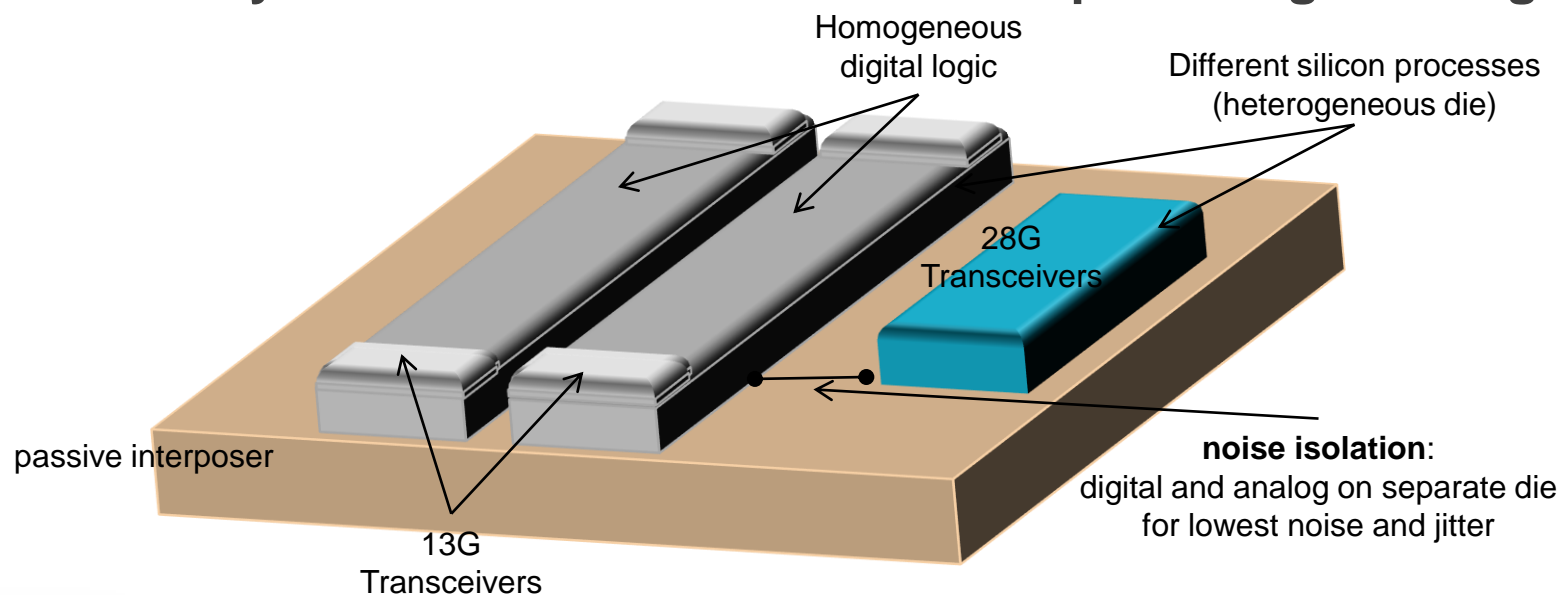
Virtex-7 HT = SLR +GTZ



Total Transceiver Bandwidth Each Direction > 1Tbps

Benefits of Heterogeneous Integration

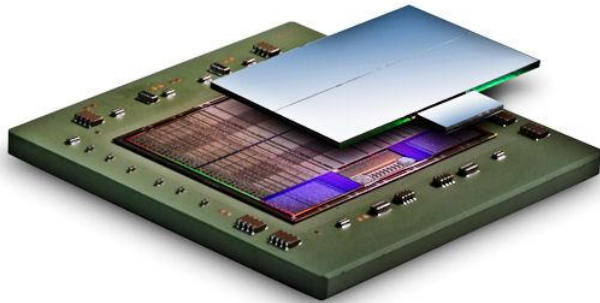
- Highest levels of integration
- Form-fit-function die for varying design requirements
- Electrically isolated 28G transceivers for optimal signal integrity



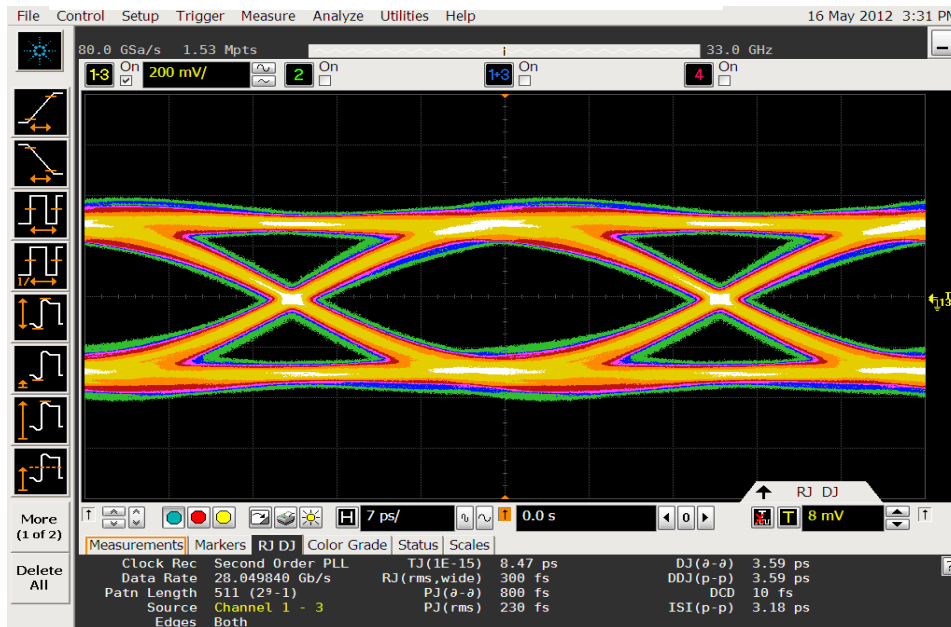
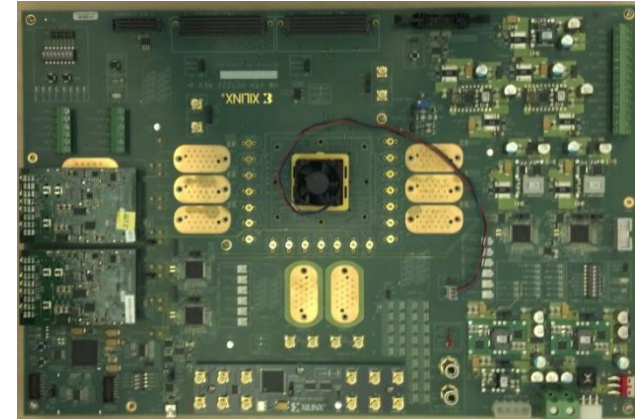
BOM Cost Reduction

Eliminate Multiple FPGAs and Transceiver Costs

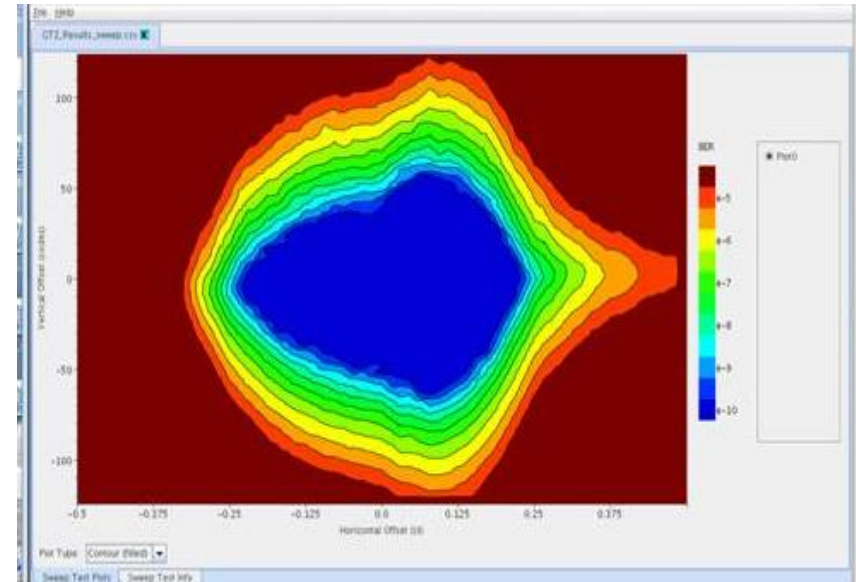
28nm FPGA with GTZ XCVR 7VH580T



Heterogeneous
VH580T



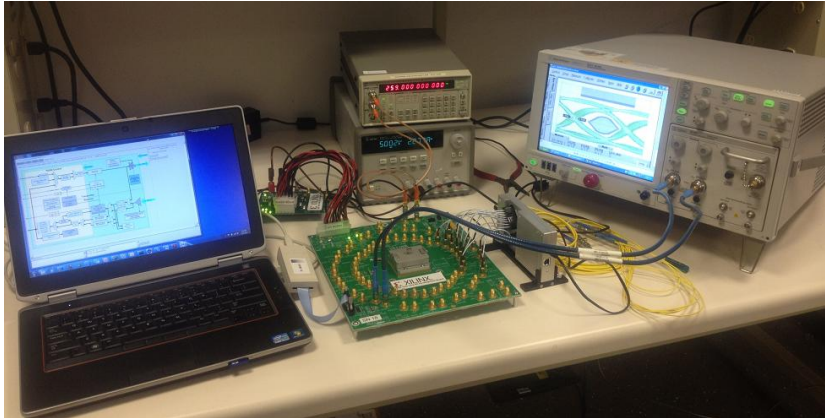
VH580T GTZ TX
Eye Diagram: 28.05Gb/s



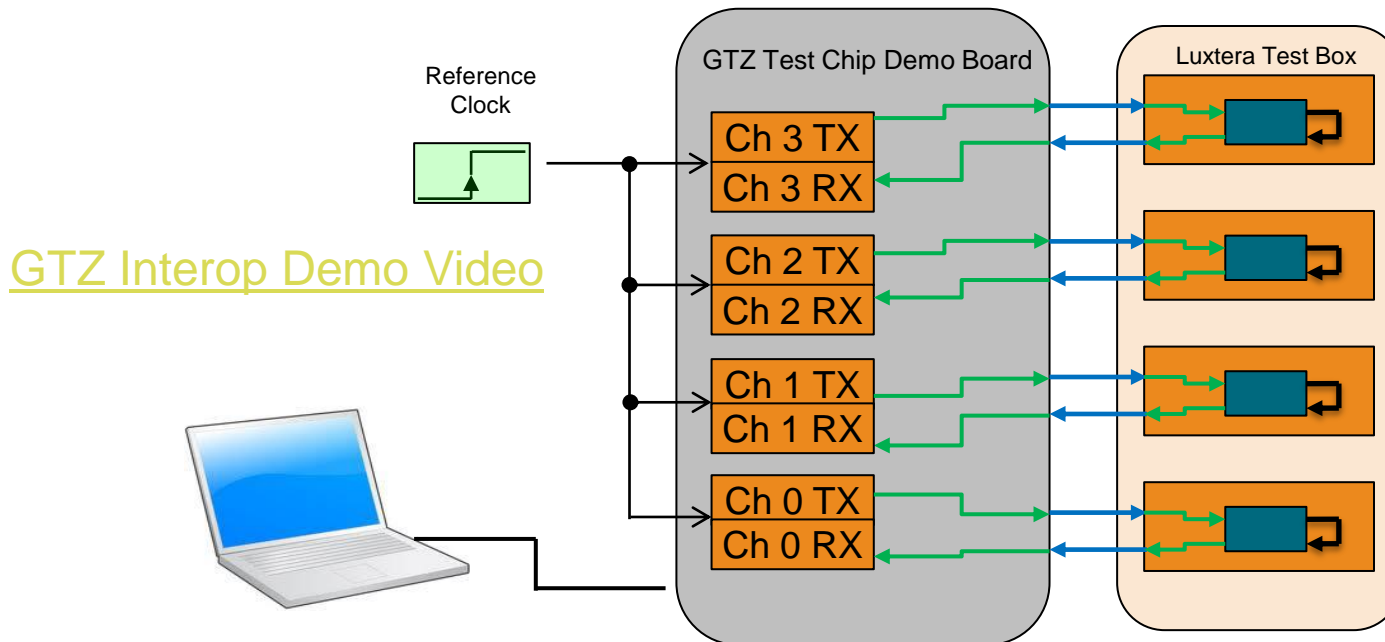
VH580T GTZ
RX Eye Scan: 28.05Gb/s:
Thru 12.5dB Trace

[7VH580T Demo Video](#)

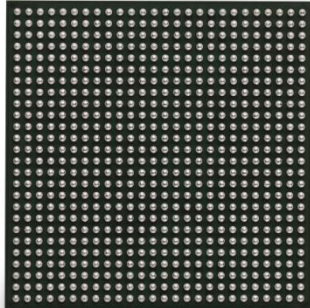
Virtex-7 GTZ Test Chip – 100G Interop with Luxtera Optical Module



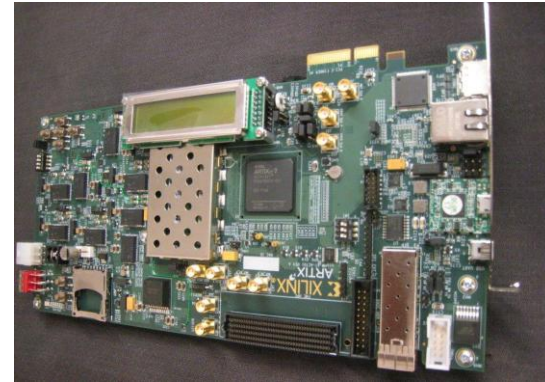
- 4x26G running a PRBS31 data pattern
- Un-retimed optical module
 - Save on power budget
 - Board space and BOM cost
- Up to 16 GTZ transceivers
 - Can support 400G applications



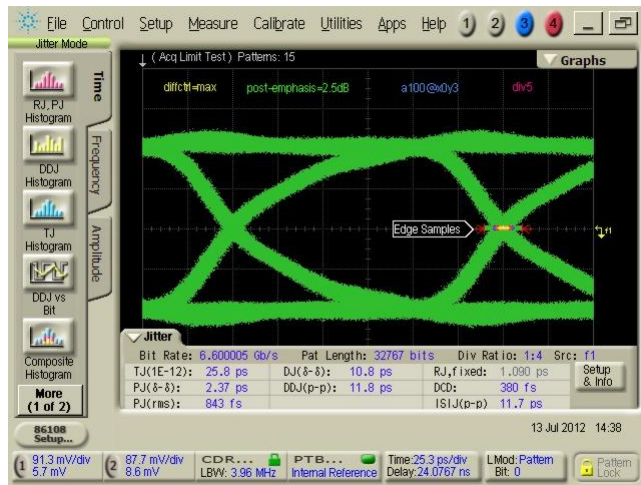
28nm FPGA with GTP XCVR 7A100T/200T



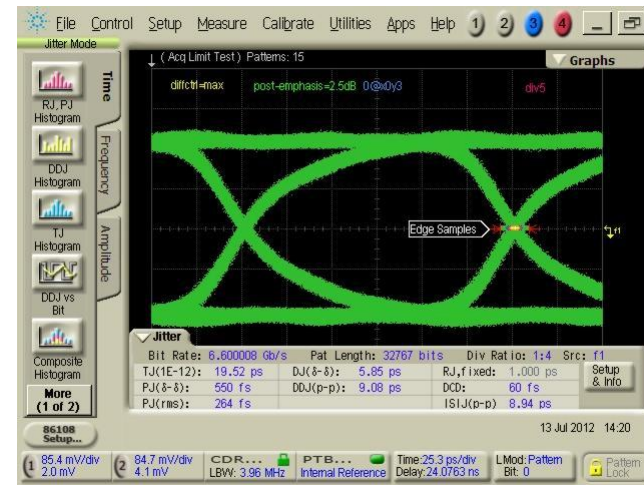
7A100T Part



AC701 Board



7A100T TX Eye Diagram:
6.6Gb/s

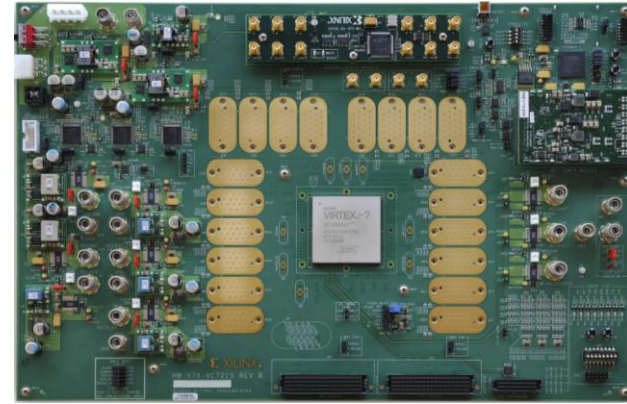


7A200T TX Eye Diagram:
6.6Gb/s

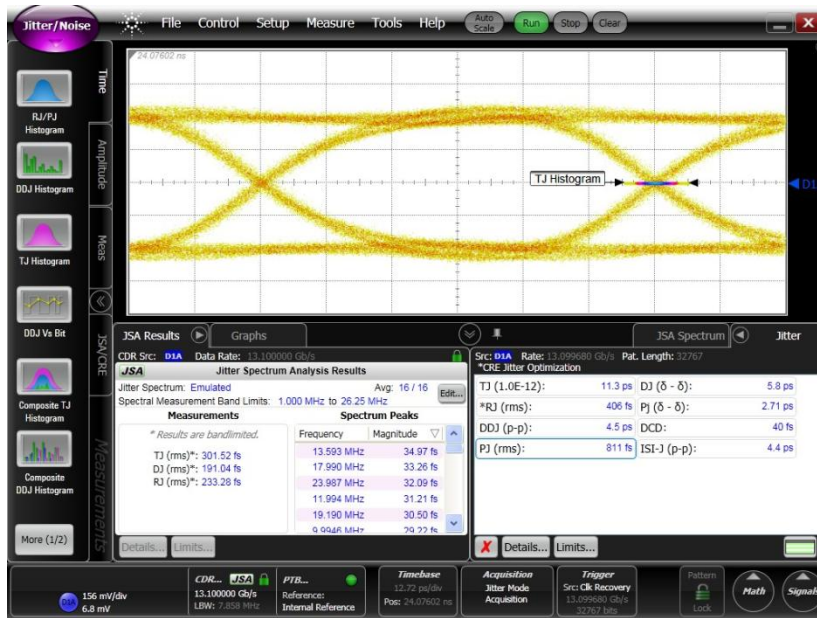
28nm FPGA with GTH XCVR 7VX690T



7VX690T Part

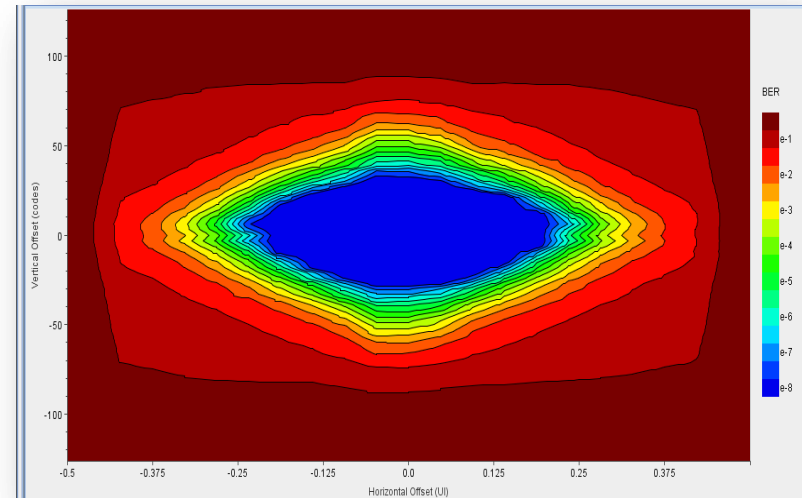


VC7215 Char Board



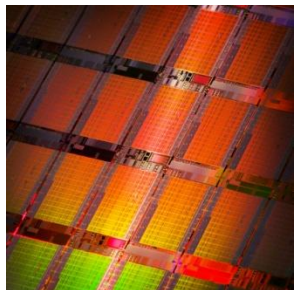
7VX690T TX Eye Diagram:
13.1Gb/s

[7VX690T Demo Video](#)



7VX690T GTH RX Eye Scan:
13.1Gb/s: 33dB
16 inch Tyco Backplane + Line cards
+ Char Board

Industry First 28nm FPGA – 7K325T

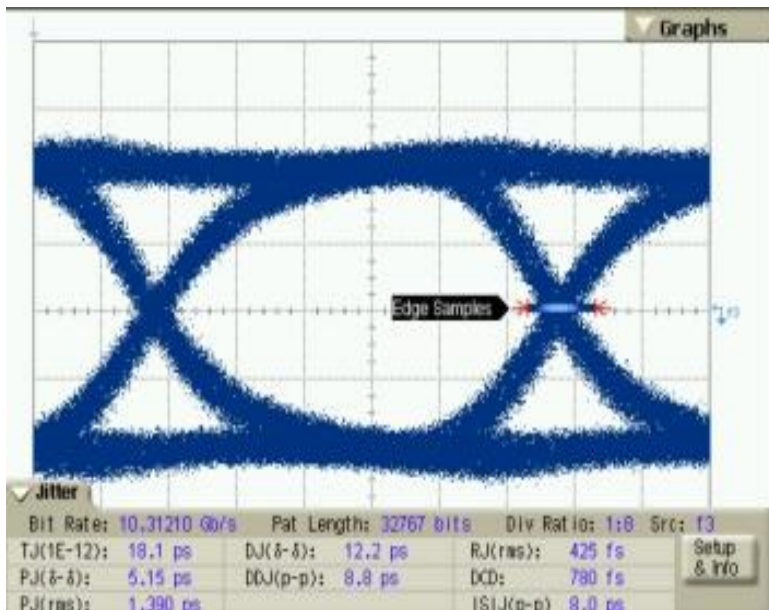
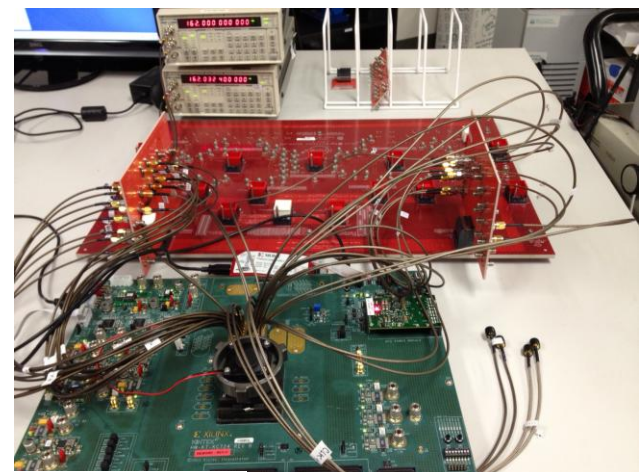


K325T
silicon wafer
March 5th, 2011

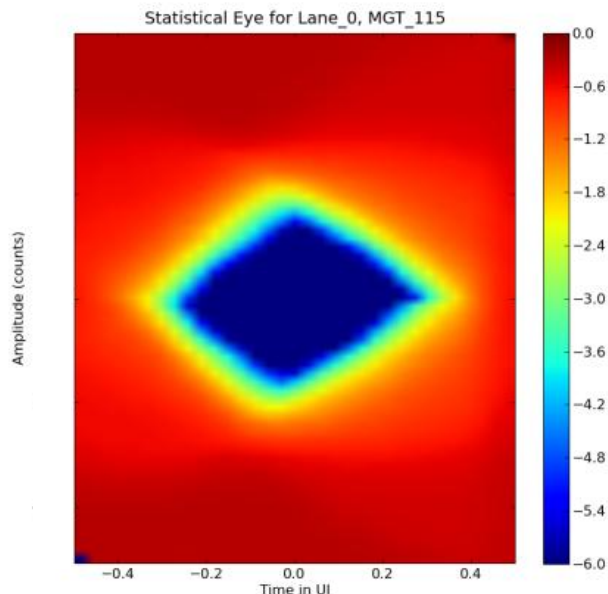


K325T
First Package Parts
March 15th, 2011

KC724 Char Board

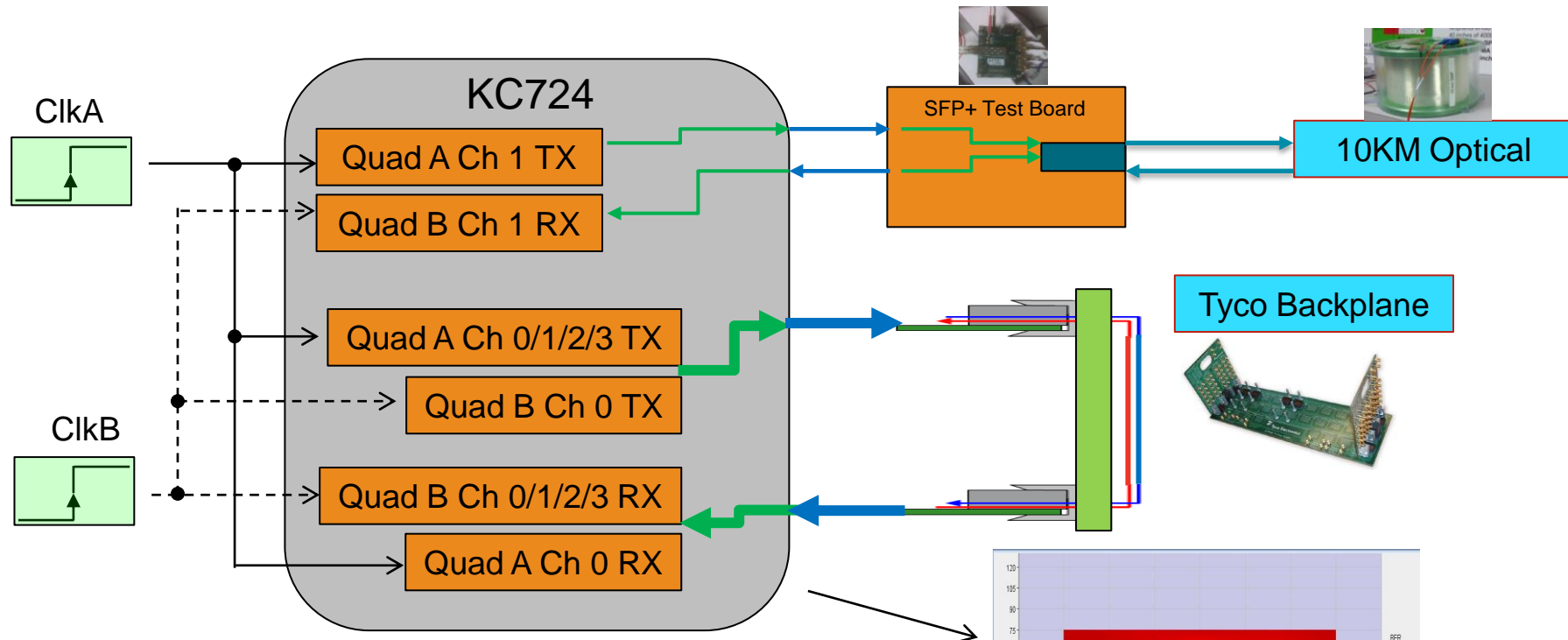


Kintex-7 GTX Eye Diagram:
10.3125Gb/s

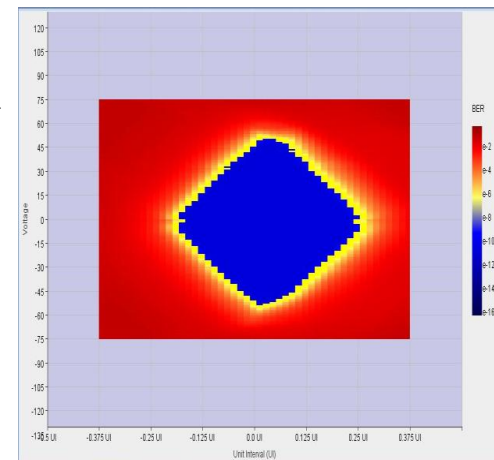


Kintex-7 GTX
RX Eye Scan: 10.3125Gb/s:
25dB Molex BP
+ Line cards
+ Char Board

Kintex-7 GTX – Tyco Backplane



- 6 links between Quad A (115) and B (116)
 - 5 links Q115 ↔ Q116 through 24" Tyco BP
 - 28 dB loss at Nyquist
 - 1 link through un-retimed limiting SFP+ optics
 - Asynchronous links @ 10.3125Gbps with PRBS31
 - Different ref clock for quad A & B, 200ppm difference
 - Error free for >2hrs. BER ~ 1e-14



[7K325T Demo Video](#)



XILINX

ALL PROGRAMMABLE™

Xilinx Transceiver History and Roadmap

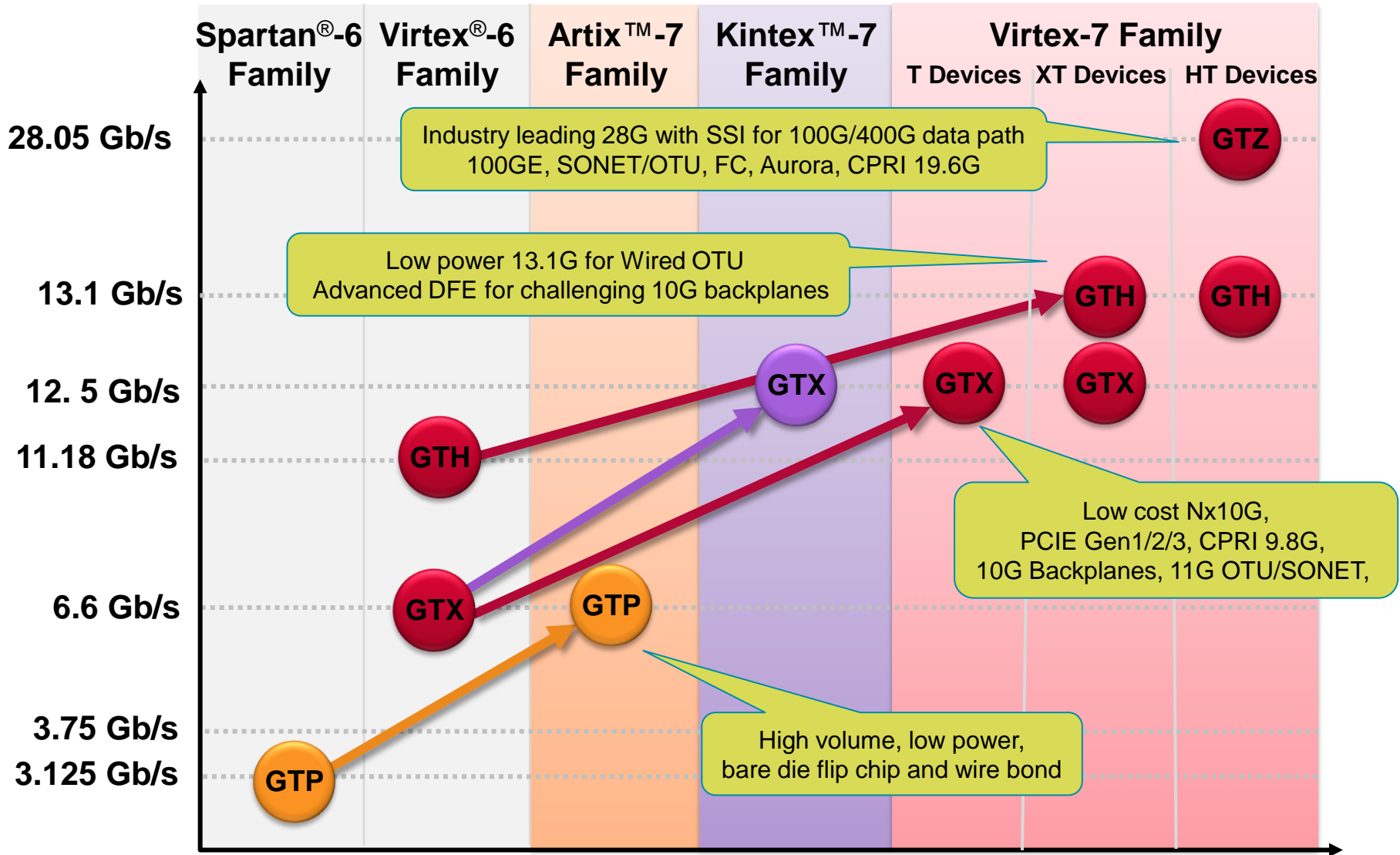
History of Xilinx Transceivers

Product family	Data Rate Low End	Data Rate Mid Class	Data Rate High End
Virtex-2 Pro			3.125G
Virtex-4			6G
Virtex-5		3.125G	6.6G
6-Series	3.75G	6.6G	11.18G



Xilinx has 80% cumulative revenue share of Transceiver FPGAs!

7 Series Transceiver Roadmap - 40nm => 28nm



7 Series Min/Max Performance by Package/Speed Grade

Speed Grade	Virtex GTZ (Gb/s)	
	min*	max
-1C/E	2.45	25.78
-2C/-2L(1V)	2.45	25.78
- 2G	2.45	28.05

Speed Grade	Virtex GTH (Gb/s)	
	min	max
-1C/I, -2LE(0.9V)	0.5	8.5
- 2I	0.5	10.3125
-2C/-2LE (1V)	0.5	11.3
-3E/-2GE	0.5	13.1

Speed Grade	Virtex GTX (Gb/s)	
	min	max
-1/-2L(0.9V)	0.5	6.6
-2/-2L(1V)	0.5	10.3125
-3/-2G	0.5	12.5

Speed Grade	Kintex GTX (Gb/s)		
	min	max (FB)	max (FF)
-1/-2L (0.9v)	0.5	6.6	6.6
-2/-2L (1V)	0.5	6.6	10.3125
-3	0.5	6.6	12.5

Speed Grade	Artix GTP (Gb/s)		
	min	max (CS)	max (FB,FF)
-1/-2L(0.9V)	0.5	3.75	3.75
-2/-2L(1V)	0.5	5.4	6.6
-3	0.5	5.4	6.6

Notes:

- 10G+ performance in K7 requires FF Pkg
- G temp grade has -2 fabric with -3 transceivers and 0°C – 100°C temp
 - Available 7V2000, 7VX1140, and 7VH parts
- GTZ frequency range is 19.6G to max with /2, /4 and /8 dividers
- 0~500Mbps can be supported with XAP875
- At 0.9V, -2L transceivers will run up to -1 rates



Increased System Performance

Serial I/O Bandwidth

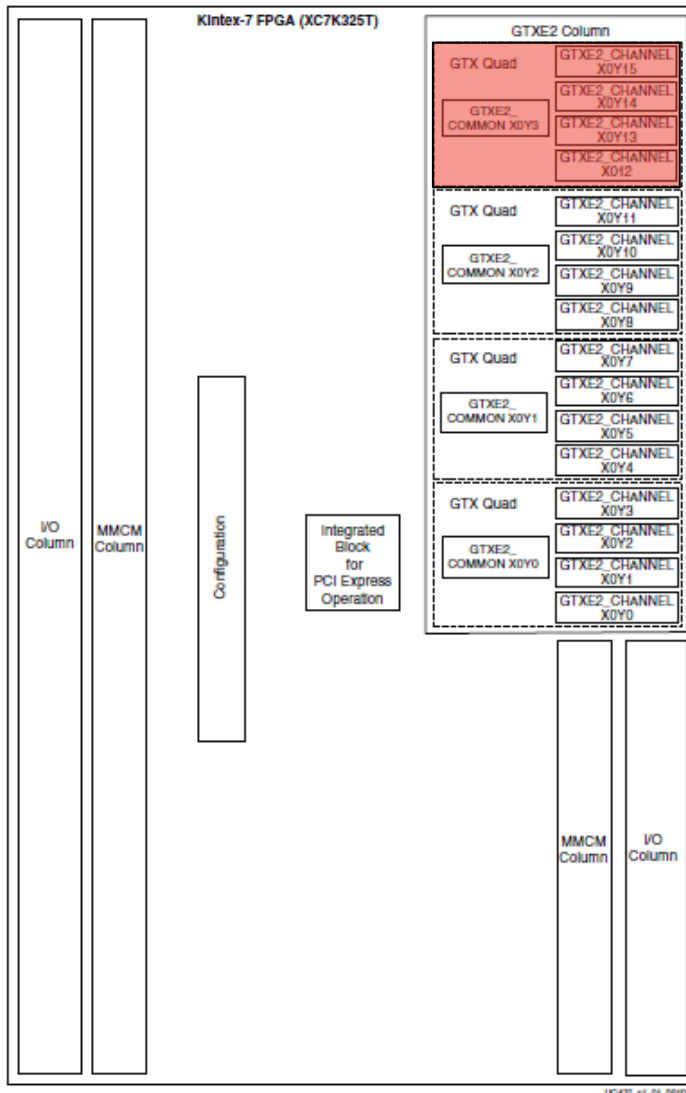


XILINX

ALL PROGRAMMABLE™

Xilinx 7 Series Transceiver Architecture

7 Series Architecture Device Layout



➤ Transceivers in Quads

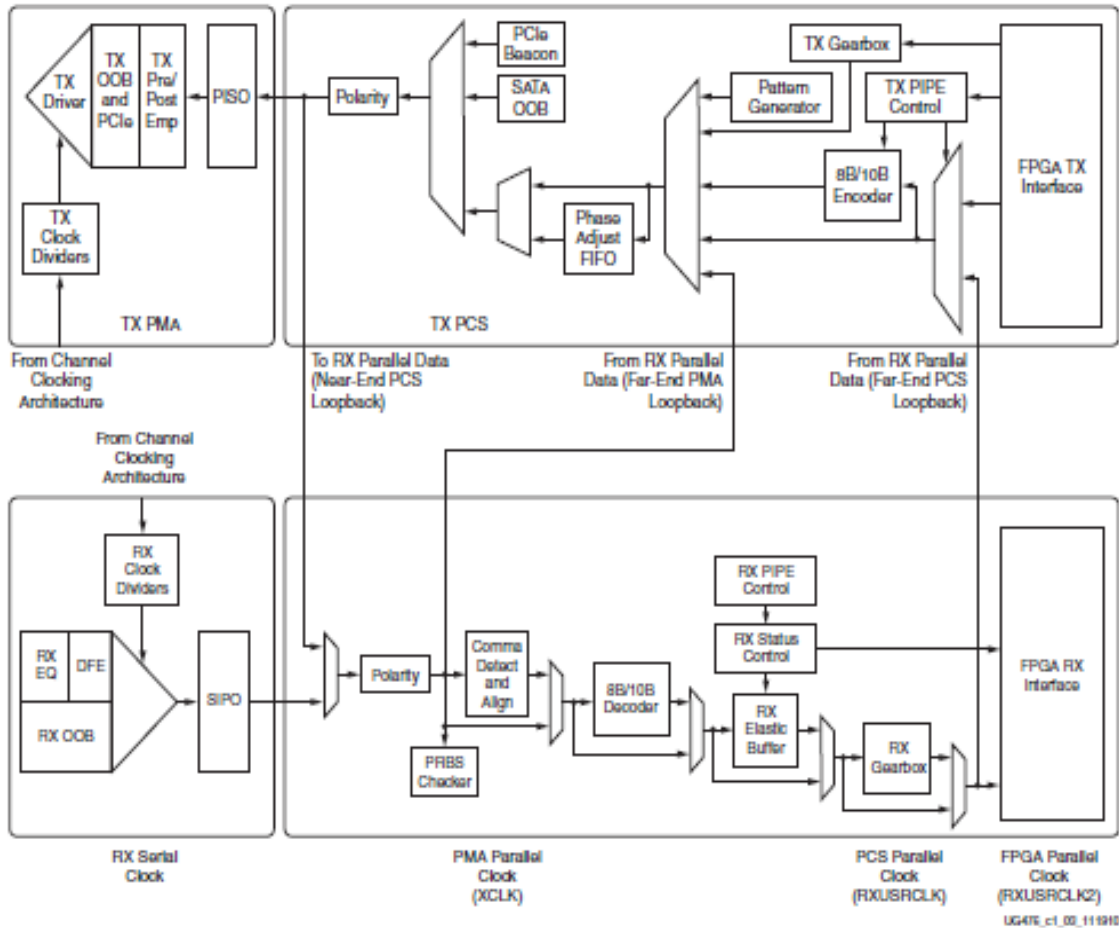
- 4 TX / 4 RX
- PLLs in shielded transceiver quads
- QPLL modelled as a separate block

➤ Layout

- Arranged in columns on one or both sides of the chip.
- Virtex-7: full transceiver columns
- Kintex-7: mix Transceivers and IOs in the same column
- Artix-7: transceivers at top and bottom (wire bond chip)

7 Series Architecture

Block Diagram of a Single Channel (GTX)



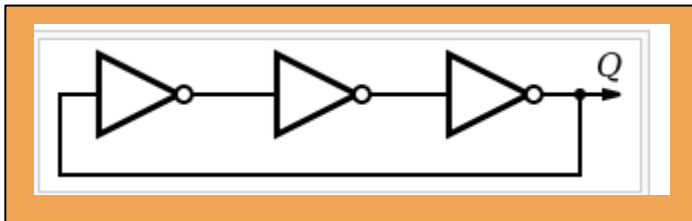
➤ Key Features:

- Data paths:
 - 0G~12.5G* for GTX
- Equalization:
 - TX Pre/Post Emphasis
 - RX AGC
 - RX CTLE
 - RX DFE
- Debug/Test
 - Hard Logic PRBS gen/check
 - 2D Eye-Scan

* 0G – 0.499G requires XAPP 875

Oscillator Topology – The Right Choice

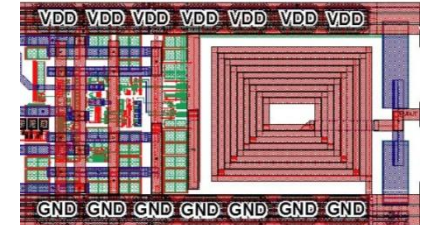
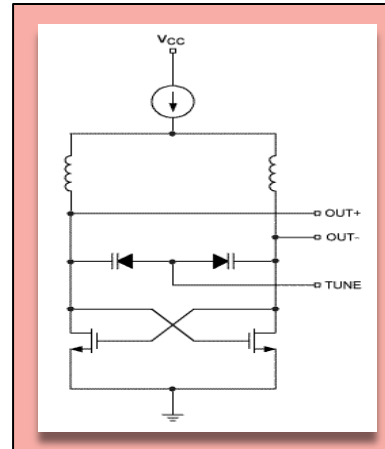
➤ Ring Oscillator



$$freq = \frac{1}{n * (BuffDelay)}$$

- Wide frequency tuning Range
- Area & integration
- Poor Random jitter @ high rates
 - 1ps-3ps rms RJ @ 10G

➤ LC Tank Oscillator



LC Tank circuit layout (example)

$$freq = \frac{1}{\sqrt{LC}}$$

- Excellent phase noise / Jitter
 - 300fs-600fs rms RJ @10G
- Narrow tuning range
- Area and integration

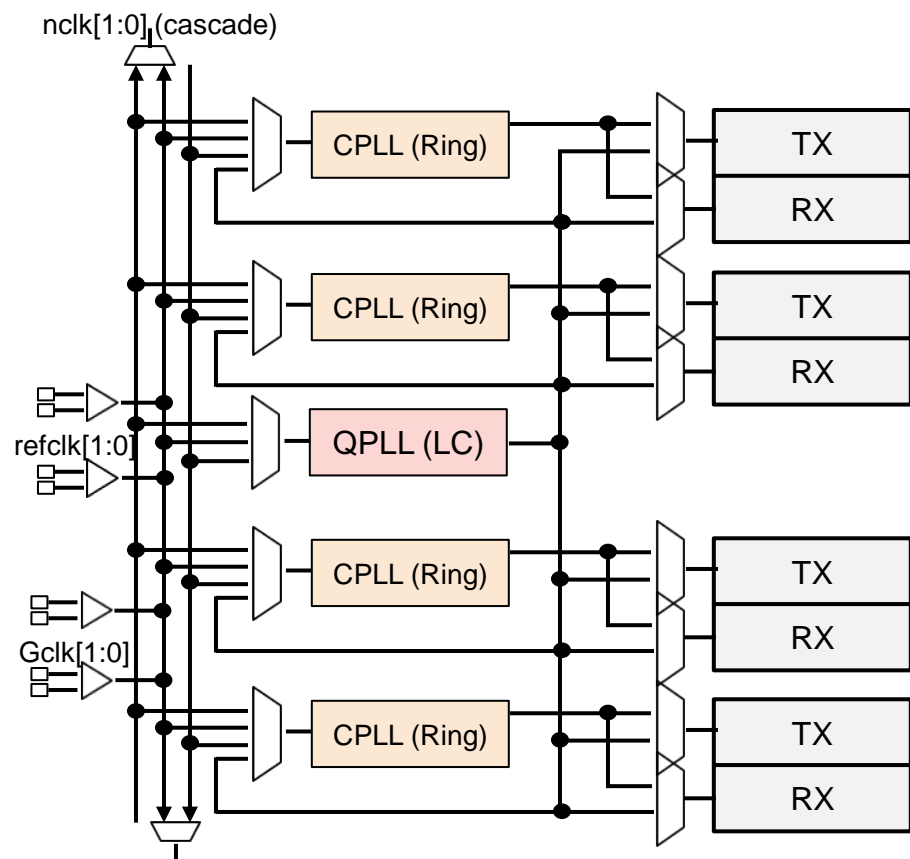
PLL Type	GTP	GTX	GTH	GTZ
LC (Performance)		✓	✓	✓
Ring (Flexibility)	✓	✓	✓	

PLL Structure: 7-GTX/GTH

➤ Virtex-7/Kintex-7

- One dedicated Ring PLL per channel, local TX/RX only
- Shared LC Tank PLL per Quad, drive ANY TX/RX

- + High Flexibility
- + Low Power
- + High Line Rates



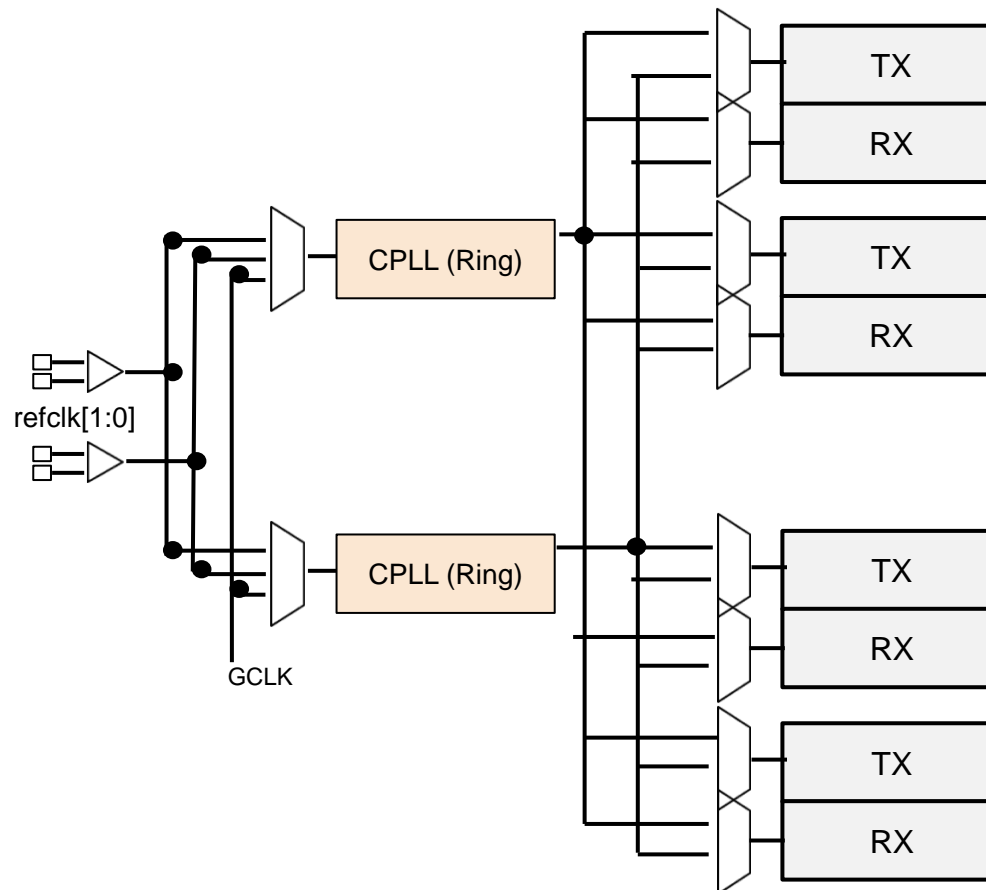
PLL Structure: 7-GTP

➤ Artix-7 Transceivers:

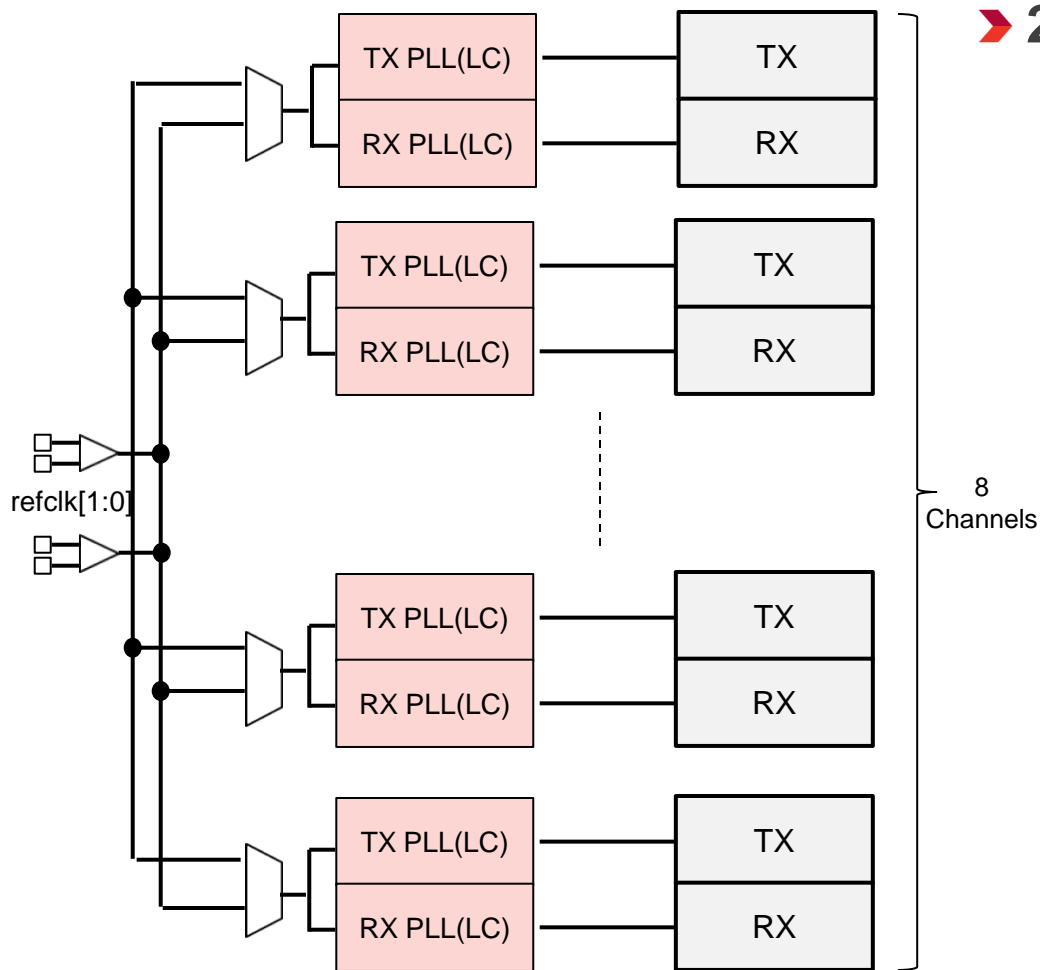
- 2 Ring PLLs per Quad, can drive ANY TX/RX
- No LC Tank PLLs

+ Moderate Flexibility

+ Low Power



PLL Structure: 7-GTZ



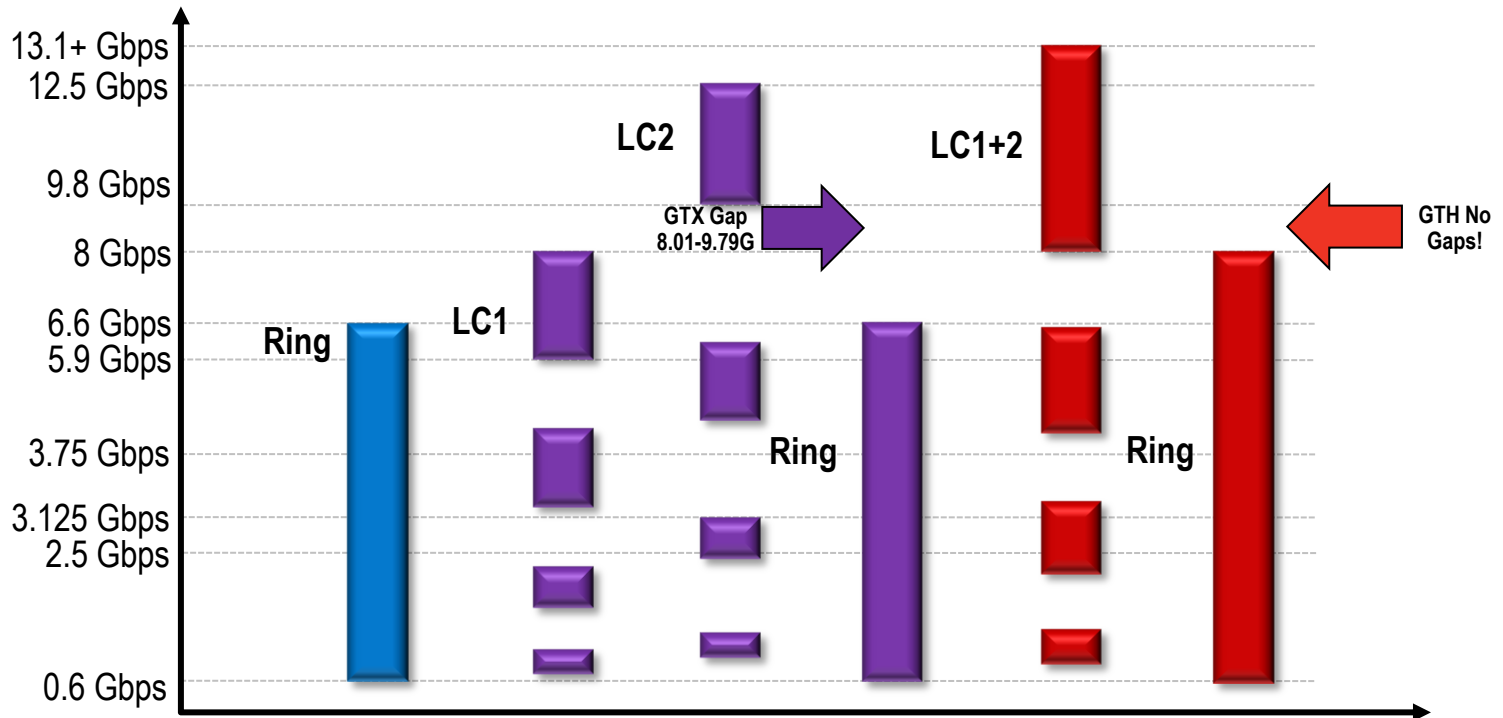
➤ 28G-focused PLL Architecture

- Dedicated LC tank PLL for TX/RX
- 2 Ref clocks per 8 channels
- No high speed muxing
- SFI-S skew alignment up to 8 channels

Divider	7 Series GTZ	
	Line Rate Range	
/1	19.6 - 28.05	
/2	9.8 - 14.025	
/4	4.9 - 7.0	
/8	2.4 - 3.5	

7 Series Transceiver Architecture

Line Rate Coverage (-3E speed grade)



Divider	Artix7 GTP		Kintex7/Virtex7 GTX			Virtex7 GTH	
	LC	Ring	LC1	LC2	Ring	LC1+2	Ring
/1	N/A		5.9-8.0	9.8-12.5		8.0-13.1	
/2	N/A		2.9-4.0	4.9-6.25		4.0-6.55	
/4	N/A		1.45-2.0	2.4-3.125		2.0-3.25	
/8	N/A		0.7-1.26	1.2-1.56		1.0-1.6	
		0.6-6.6			0.6-6.6		0.6-8.0

7 Series Transceiver Architecture

Major Supported Protocols

Market	Protocol	Artix-7 GTP	Kintex-7/Virtex-7 GTX	Virtex-7 GTH	Virtex-7 GTZ
General	PCI Express	Gen1, 2	Gen1, 2, 3	Gen1, 2, 3	(supported on GTH)
Wired	Ethernet	1GE, 2.5GE, XAUI, RXAUI	1GE, 2.5GE, XAUI, RXAUI, 10GBase-R, 10G-KR*, 40GE, 100GE	1GE, 2.5GE, XAUI, RXAUI, 10GBase-R, 10G-KR (enhanced), 40GE, 100GE	100GE (25.7G)
	SONET/OTU	OC-3/12/48	OC-3/12/48/192, OTU1/2/3/4	OC-3/12/48/192, OTU1/2/3/4	OTU4 w 7% FEC (27.95G) SFI-S, OTL4.4
	Interlaken	<= 6.6G	<=6.5G, 10.3125G 12.5G	<=6.5G, 10.3125G, 12.5G	20.625G (2x10.3125), 25G (2x12.5G)
	Custom Backplane	<= 3.125G	<=6.5G, CEI-11-LR*	<= 6.5G, CEI-11LR (enhanced)	(supported on GTH)
	PON	BPON, GPON, GEAPON (up to 1.25 BCDR)	BPON, GPON, GEAPON, 10GEAPON, 10GGPON (up to 2.5G BCDR)	BPON, GPON, GEAPON, 10GEAPON, 10GGPON	(supported on GTH)
Wireless	CPRI/OBSAI	0.614, 1.2, 2.4, 3.0, 4.9, 6.6	0.614, 1.2, 2.4, 3.0, 4.9, 6.14, 9.8, 12	0.614, 1.2, 2.4, 3.0, 4.9, 6.14, 9.8, 12	2.4, 3.0, 4.9, 6.0, 9.8, 19.6, 24
	Serial Rapid IO	Gen1, 2	Gen1, 2	Gen1, 2	(supported on GTH)
Audio Video ²	SDI	SD/HD/3G-SDI	SD/HD/3G-SDI/10G-SDI	SD/HD/3G/10G-SDI	(supported on GTH)
	DisplayPort*	1.6, 2.7, 5.4	1.6, 2.7, 5.4	1.6, 2.7, 5.4	(supported on GTH)
Other	QPI	x	4.8, 6.4*	4.8, 6.4, 8.0, 9.6	(supported on GTH)
	Fiber Channel	1G, 2G	1G, 2G, 4G, 10G	1G, 2G, 4G, 8G, 10G	FC32 (28.05G), FC20, FC16, FC10
	SATA/SAS	1.5G, 3G, 6G	1.5G, 3G, 6G	1.5G, 3G, 6G	(supported on GTH)
	Aurora	Up to 6.6G	Up to 12.5G	Up to 13.1G	Up to 28.05G

PCS Details

Fabric Width vs. Line Rate

Line Rate	Transceiver Min Fabric Width (bytes)		
	GTP	GTX	GTH
≤ 3.75G	2	2	2
≤ 5.4G	4 (-2 wirebond)	2	2
≤ 6.6G	4 (-2 flipchip)	2	2
≤ 10.3125		4 (-2)	4 (-2)
≤ 11.3		4 (-3E)	4 (-2E)
≤ 12.5		4 (-3E)	4 (-2GE)
≤ 13.1G			4 (-2GE)

► Decoder Ring

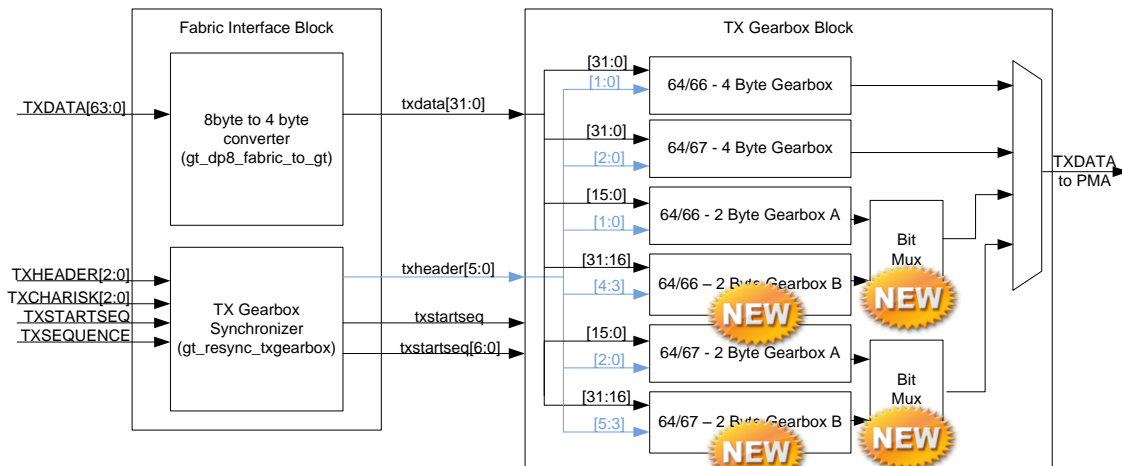
- * = run length limited (see datasheet)
- ** = Gearbox and bit muxing (Interlaken, 10GE, 40GE and 100GE (GTH only) modes)
- *** = Different functionality from ** for 25G+ applications

PCS Details

GTH PCS upgrades

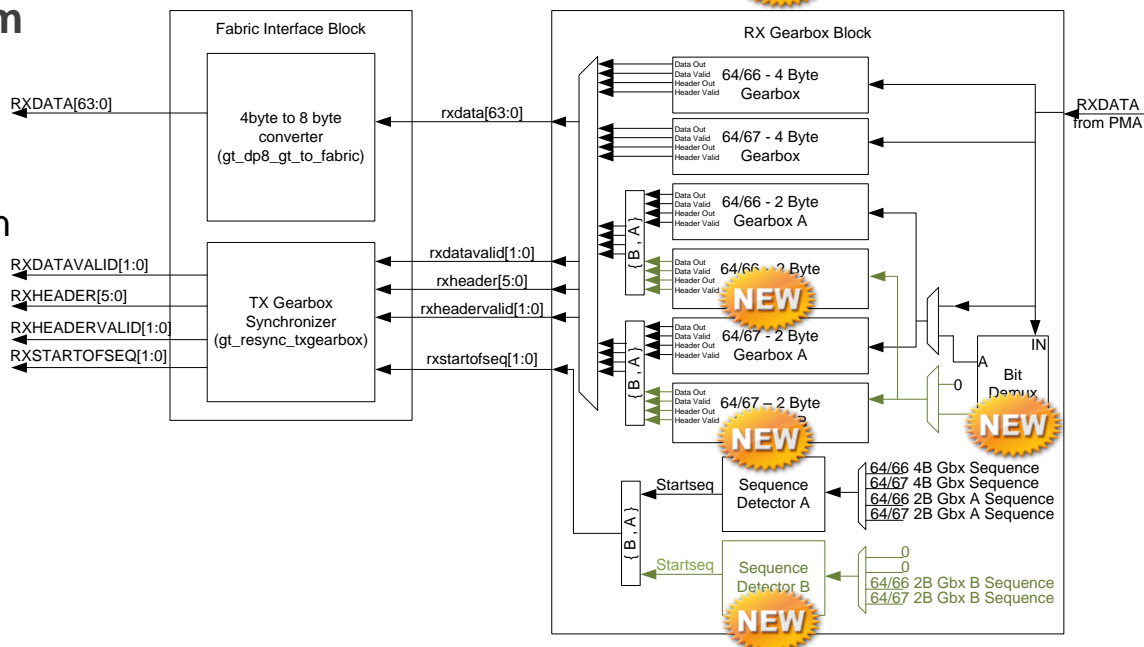
▶ GTX PCS Features

- PRBS gen/check hard logic
- 8b/10b hard logic
- 64/66 and 64/67 gearboxing hard logic
- Pass-through support for SONET/OTU and user-defined datapatterns



▶ GTH PCS Enhancements in 28nm

- Native CAUI support for 100GE
 - 2x 5G PCS Lane inputs
 - PCS Lane Bit muxing
 - Second Sequence Byte checker on RX
- (128/130b support is in PCIe Gen3 hard block)



PCS Details

Encoding/Decoding Support

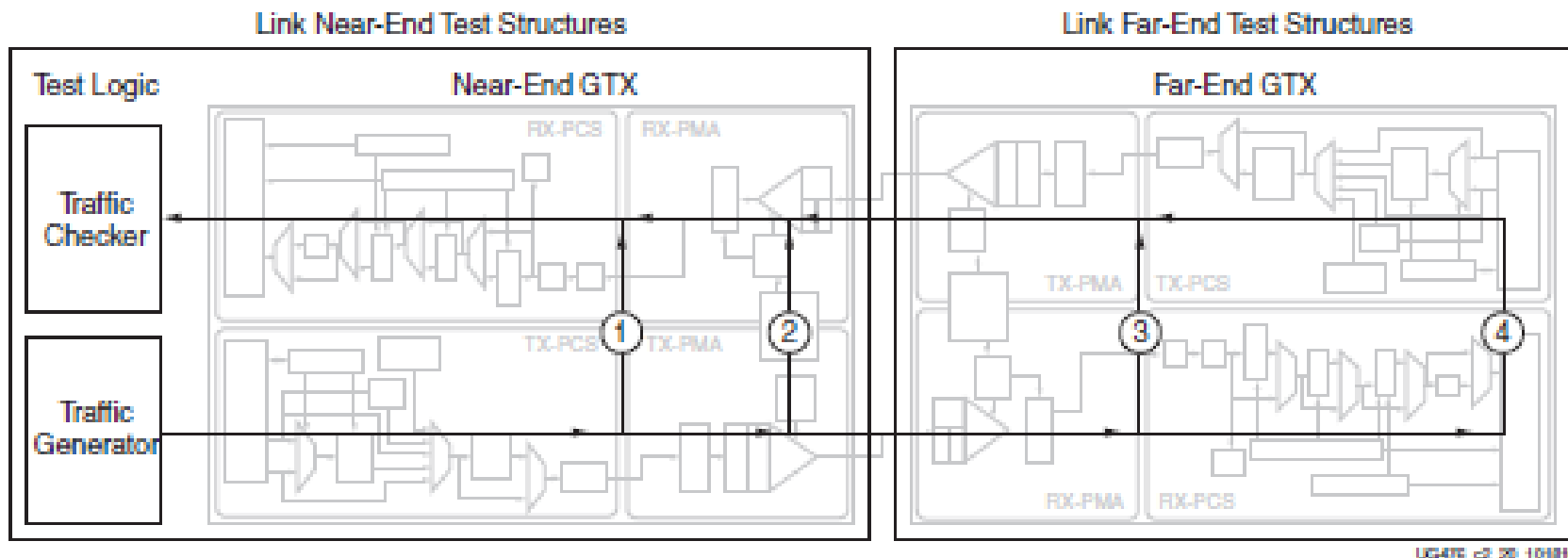
Fabric DIY	Hard GT Logic	Hard PCIe Logic	GTP	GTX	GTH	GTZ
8b/10b			Yes	Yes	Yes	Yes
64/66b			Yes	Yes	Yes	Yes
64/67b			Yes	Yes	Yes	Yes
128/130b			No	Yes	Yes	TBD
SONET			Yes	Yes	Yes	Yes
Custom			Yes*	Yes*	Yes*	Yes*
	8b/10b		Yes	Yes	Yes	Yes
	64/66b		Yes**	Yes**	Yes**	Yes***
	64/67b		Yes**	Yes**	Yes**	No
	128/130b		No	No	No	No
		128/130b	No	No	Yes	No

➤ Decoder Ring

- * = run length limited (see datasheet)
- ** = Gearbox and bit muxing (Interlaken, 10GE, 40GE and 100GE (GTH only) modes)
- *** = Different functionality from ** for 25G+ applications

PCS Details

Loopback (PCS and PMA)



► 7 Series Transceivers (GTP, GTX and GTH) Loopback

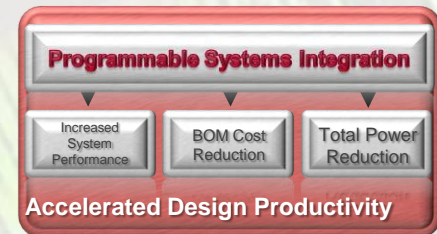
- Both PCS and PMA loopbacks for near-end and far-end test cases
 - 1 --- Near-End PCS loopback
 - 2 --- Near-End PMA loopback
 - 3 --- Far-End PMA loopback
 - 4 --- Far-End PCS loopback



XILINX

ALL PROGRAMMABLE™

Xilinx 7 Series Transceiver Optical Support



Optical Interfaces

Optics Basics

➤ Types of Optics

– Retimed

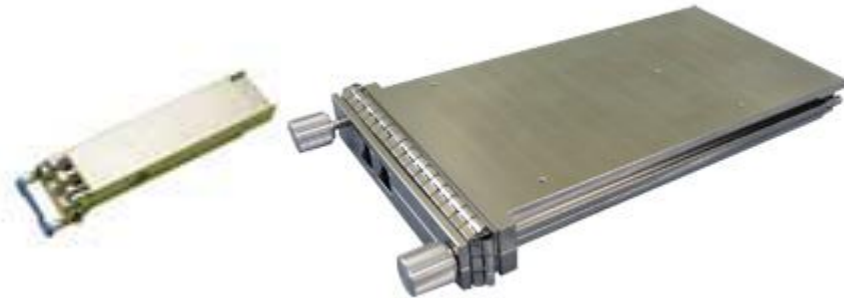
- (e.g. XFP)
- More margin for system (e.g. FPGA)
- Higher cost
- Follow “Limiting” specifications

– Unretimed

- (e.g. SFP+)
- System must be higher performance
- Lower cost/smaller/lower power
- 2 Types: Limiting or Linear

➤ Transceiver Parameters Needed for Optical Interfaces

- Low Transmit Jitter (frequently $< 0.28UI$)
- Good Jitter Tolerance (to work around optical dispersion)



10GE XFP
(retimed)

100GE CFP
(retimed)



10GE SFP+
(unretimed)



100GE CXP
(unretimed)

SFP+ Dominating Optical Questions

- SFP+ is becoming the default standard for a single 10Gb/s+ optical lane
- Single duplex lane: 1 RX, 1 TX
- Electrical defined in SFF-8431 (SFI)
- Protocol Applications
 - 10G-Base R: SR, LR, LRM, ER, ZR
 - **Commonly used as reference!**
 - CPRI: 9.8Gb/s
 - FibreChannel
 - 10G-SDI
- Non-protocol specific...



Available Data

➤ Characterization:

- 7 series GTX SFP+/XFP Characterization Report
 - Tests to the SFF-8431 specification for limiting interfaces
 - Final Internal characterization report available upon request
- 7 series GTH SFP+/XFP Characterization Report
 - Tests to the SFF-8431 specification for limiting interfaces
 - Full Schedule published on Monthly Update



➤ Interoperation:

- 7 series GTX Interoperation with Finisar 40km/80km Limiting Optics
 - Contact Technical Marketing

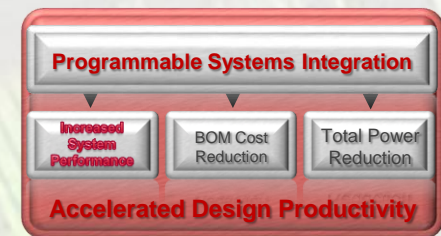




XILINX

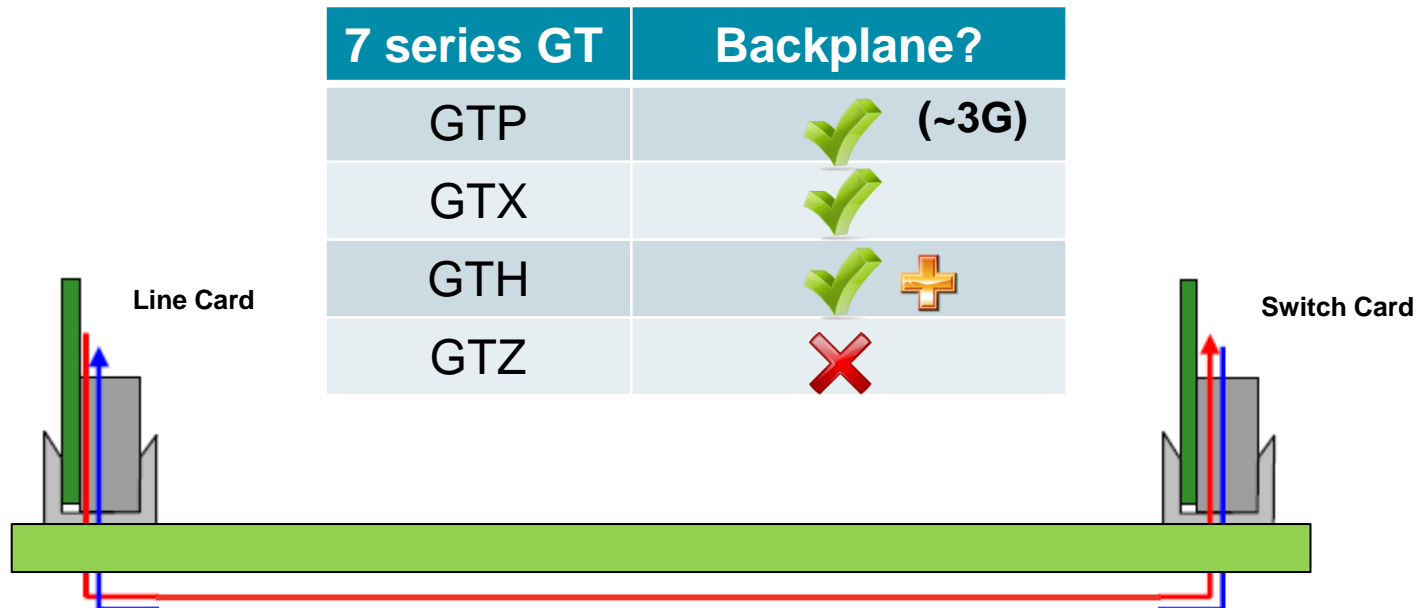
ALL PROGRAMMABLE™

Xilinx 7 Series Transceiver Backplane & Equalization

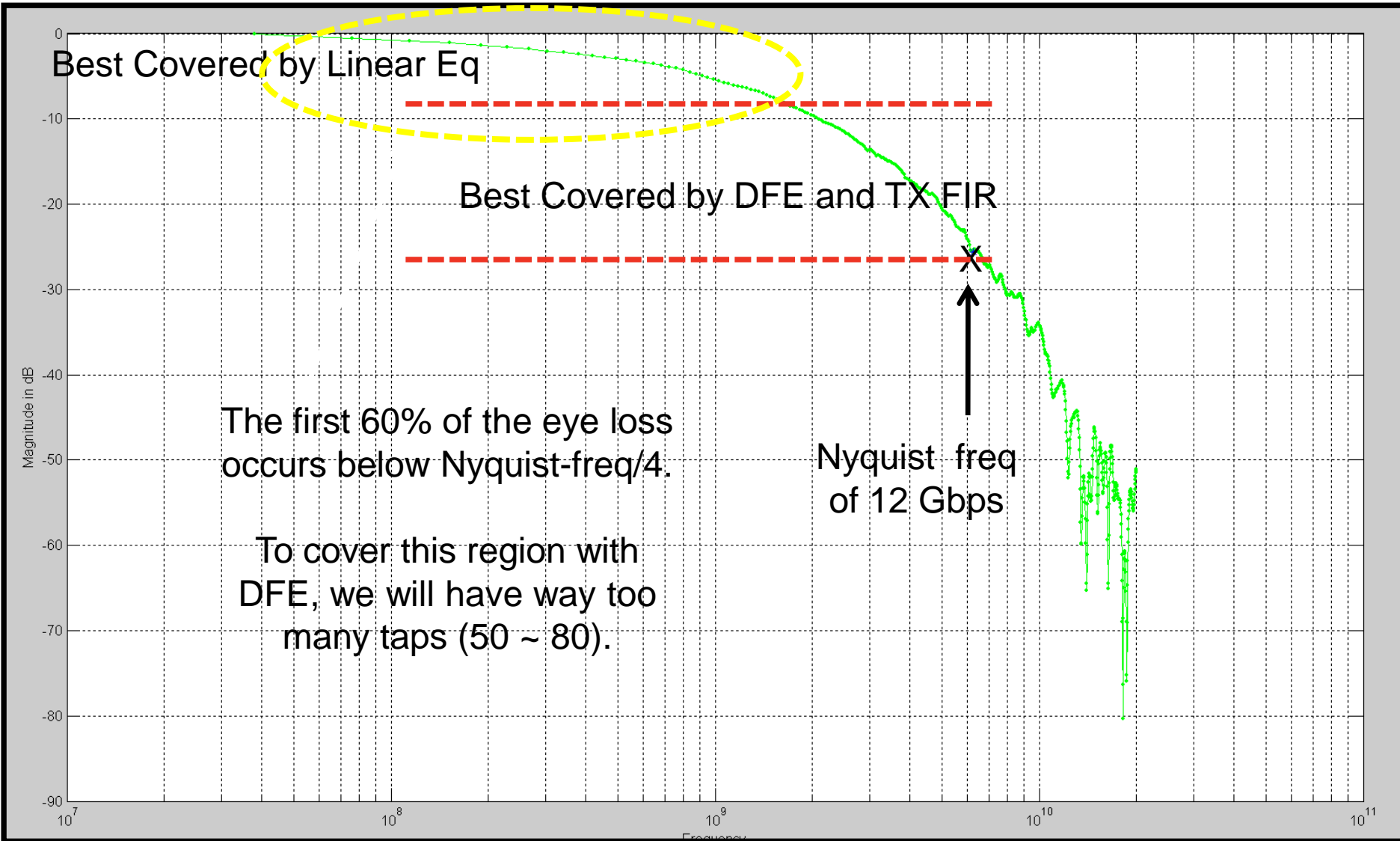


Backplanes Support with 7 Series Transceiver

- 7-GTX is designed to support 10GBase-KR (well-designed high confidence channels)
- 7-GTH will provide enhanced 10GBase-KR support
- 7-GTP will support custom backplane up to 3.125Gbps
- 7-GTZ will support CEI-28G VSR but not backplane applications



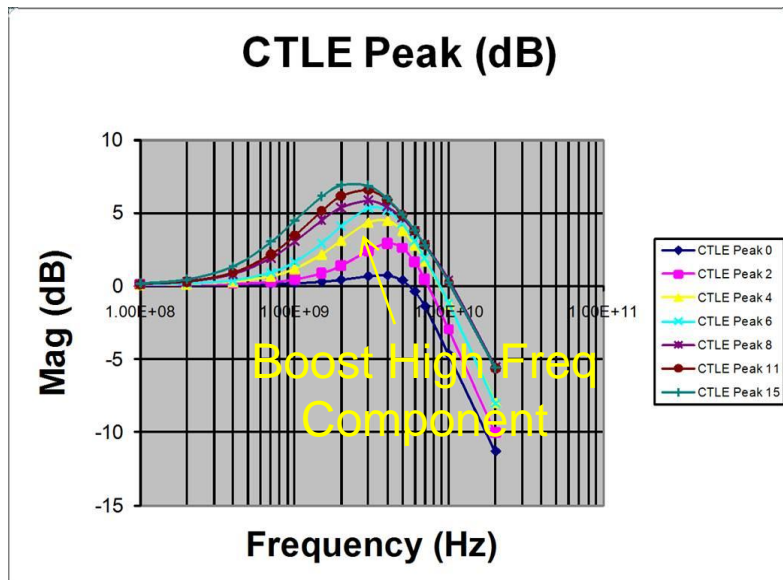
Why We Use Both Linear and DFE in 7 Series?



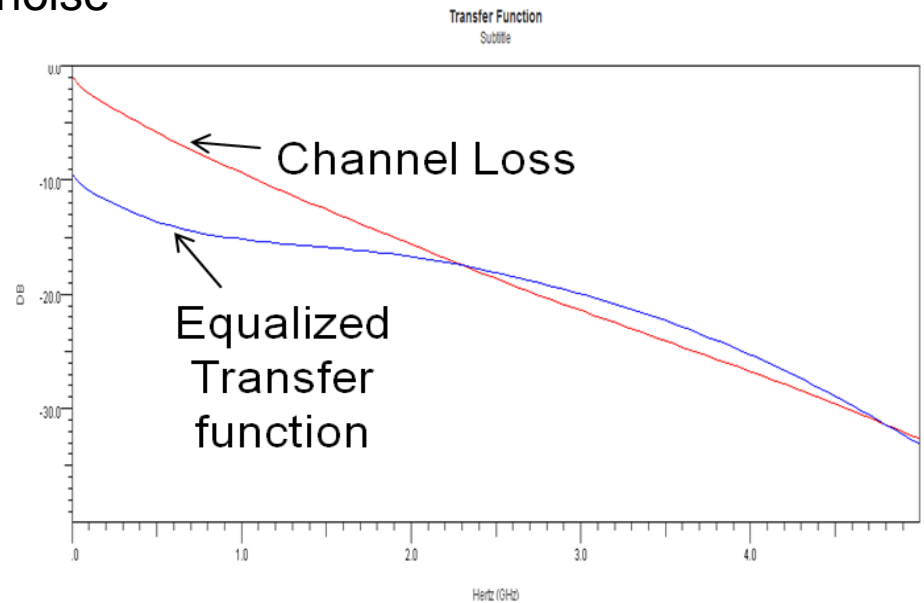
Technique #1: Linear Equalization

➤ Linear Equalization

- Transmitter: Attenuate low frequency and/or boost high frequency
- Receiver: Boost high frequency
- Compensate insertion loss
- Limitation: Boost high frequency noise

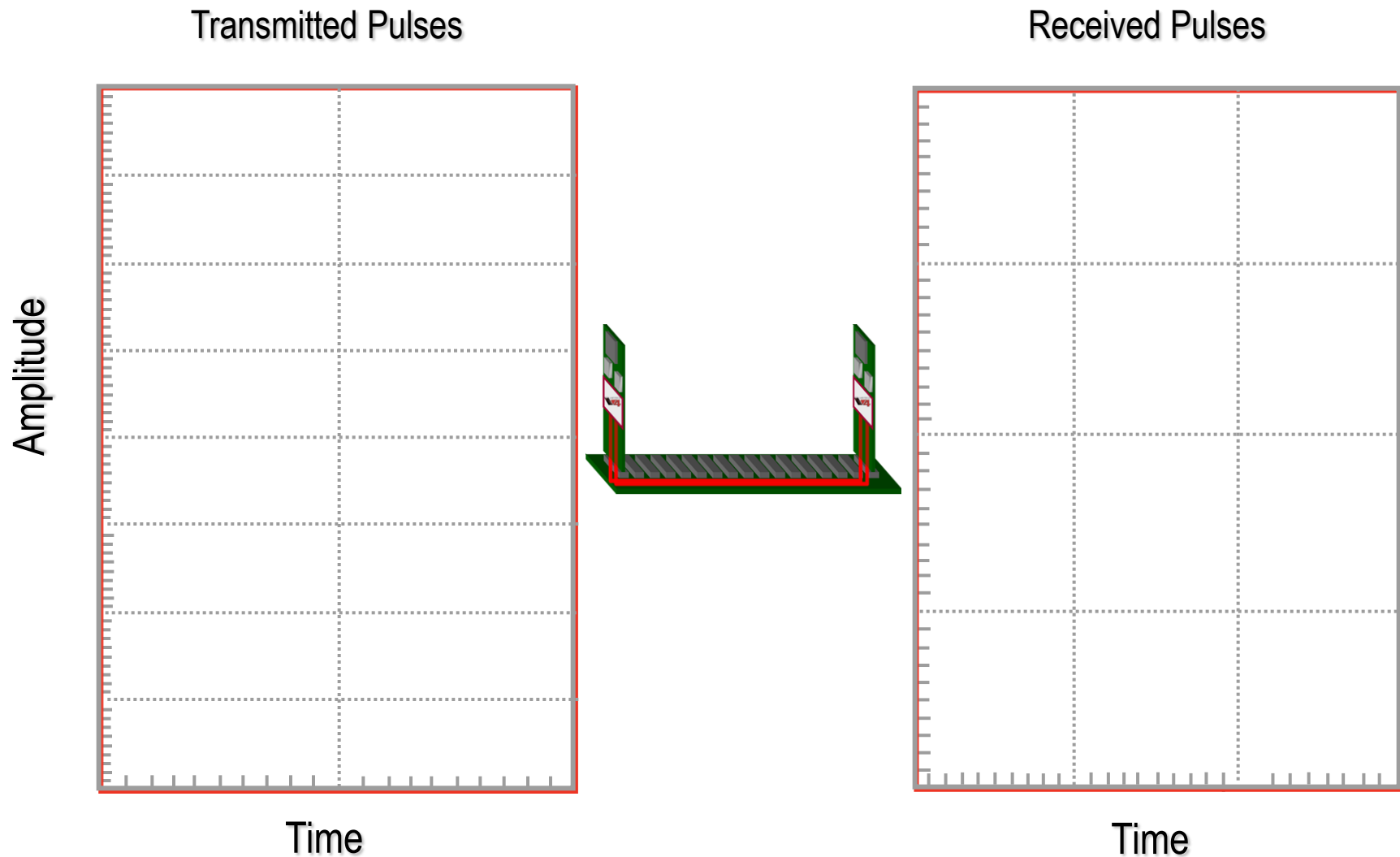


RX linear equalizer frequency response



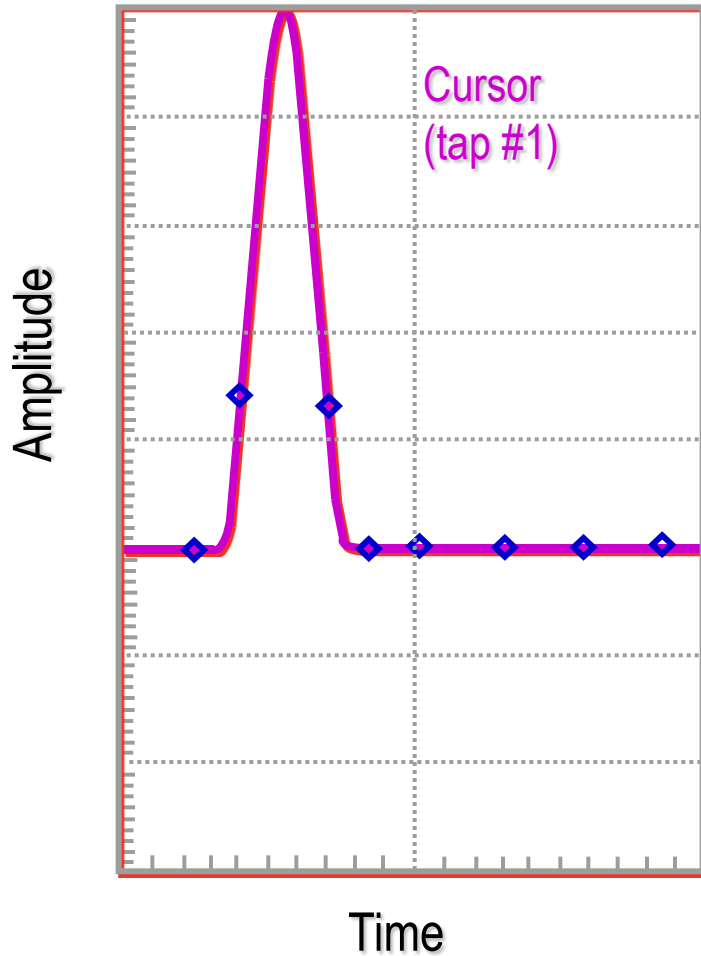
TX pre-emphasis attenuate low frequency & boost high frequency

TX Emphasis To Reduce Loss

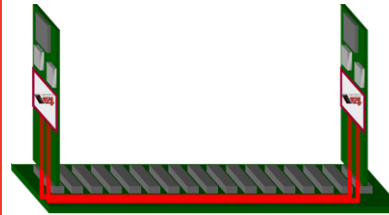
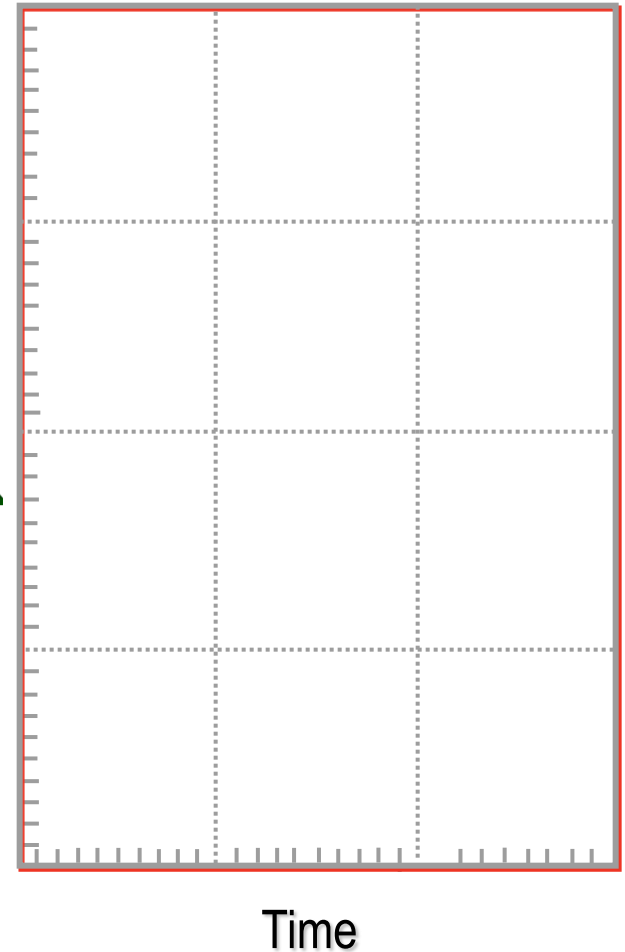


TX Emphasis To Reduce Loss

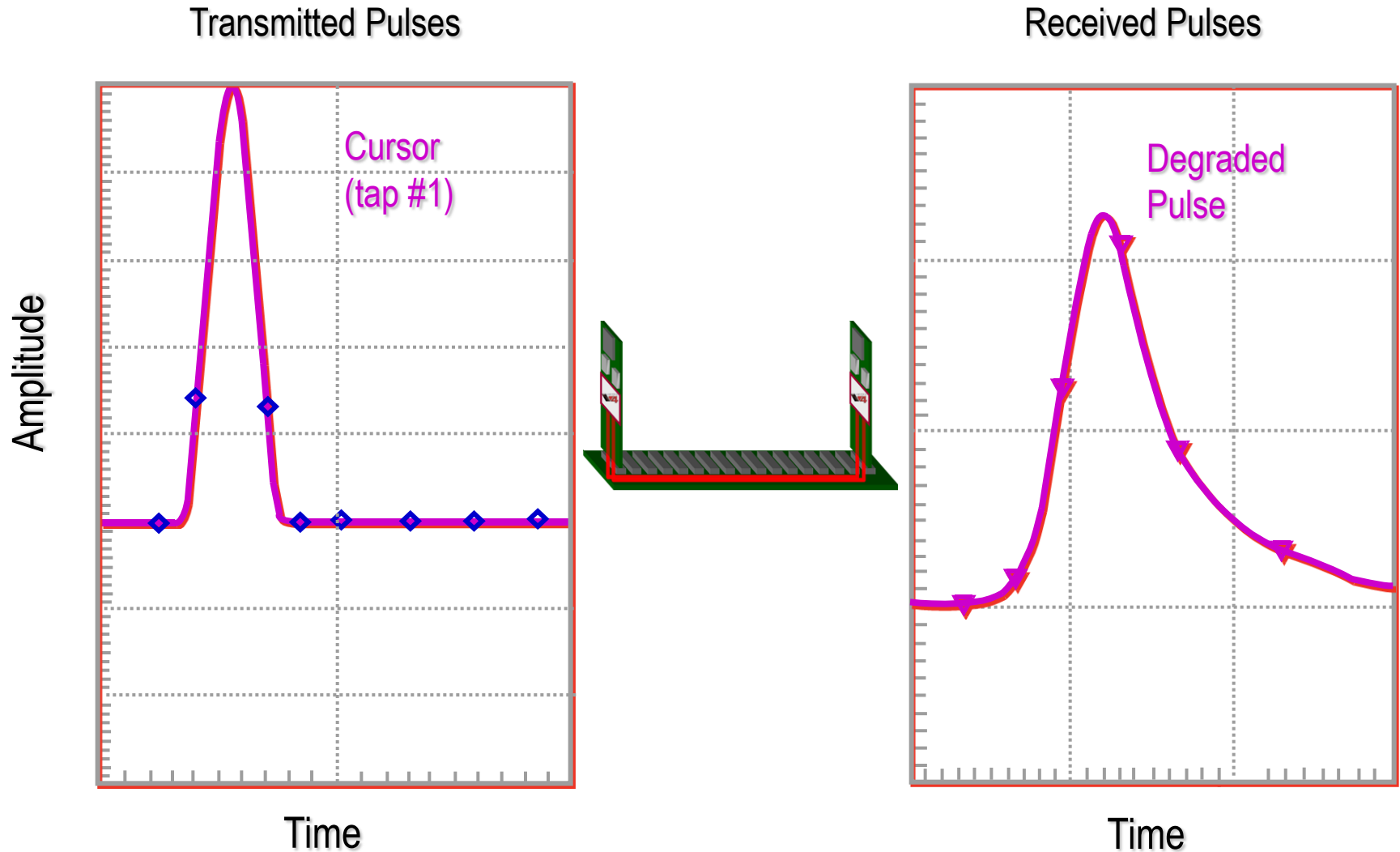
Transmitted Pulses



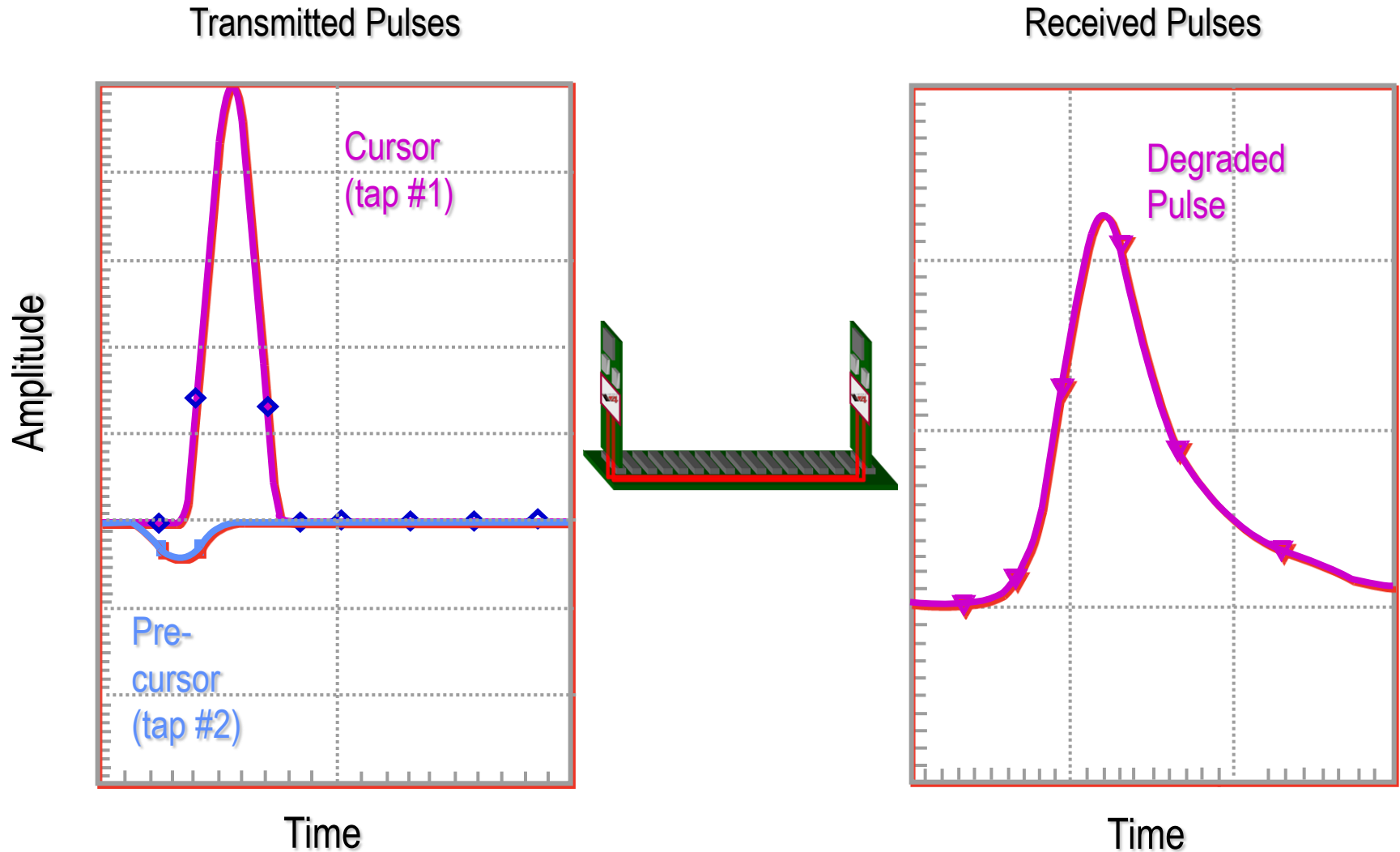
Received Pulses



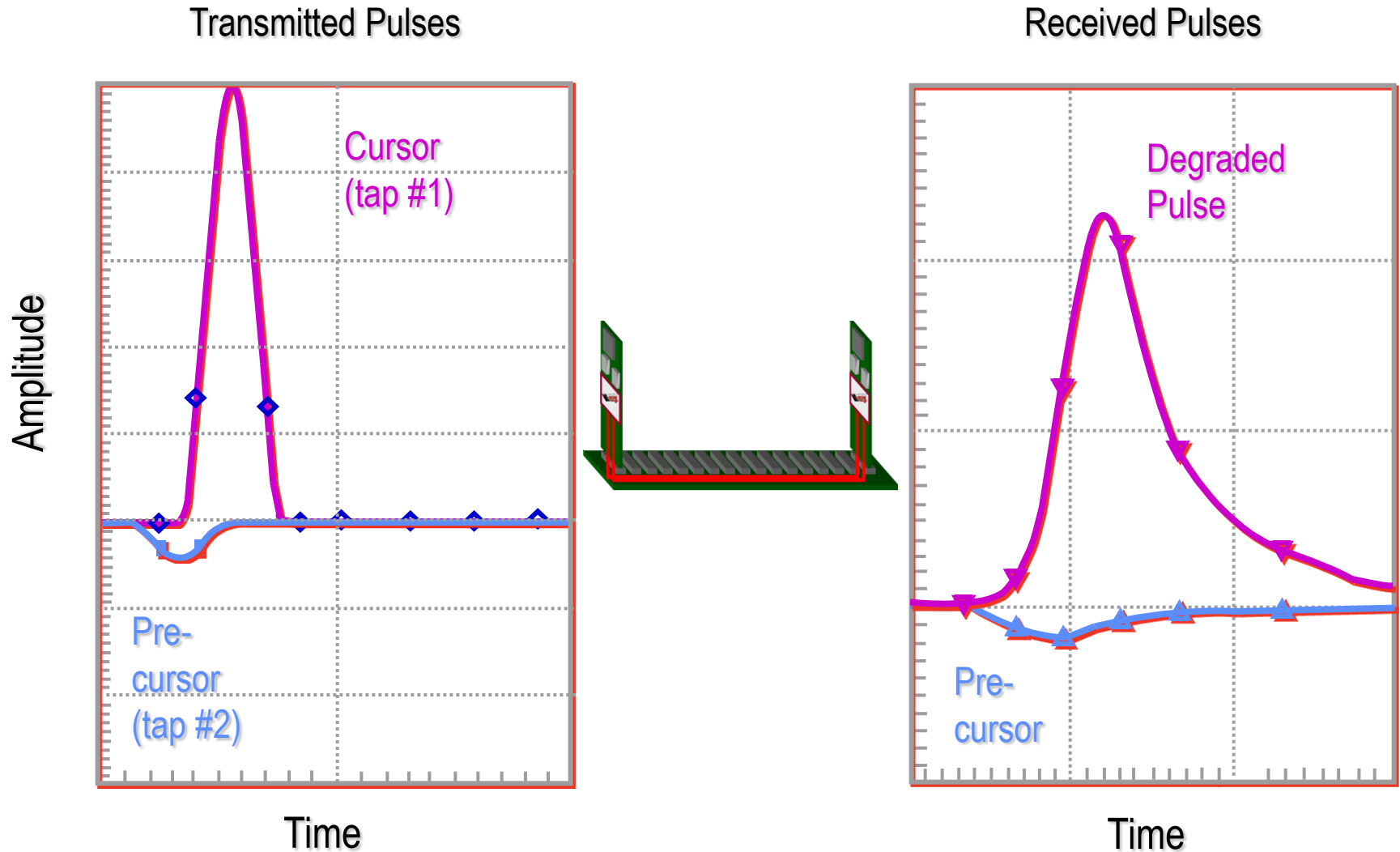
TX Emphasis To Reduce Loss



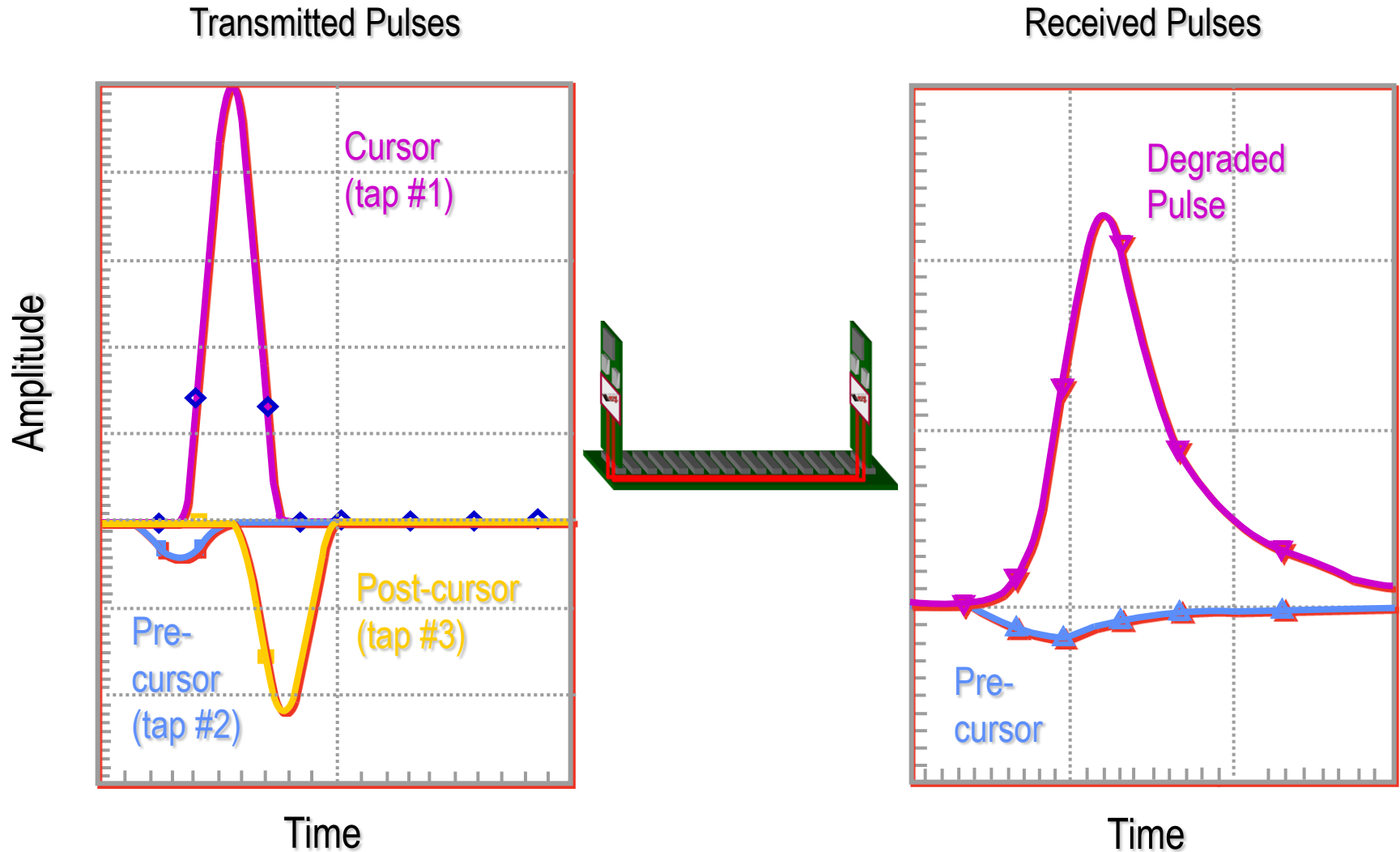
TX Emphasis To Reduce Loss



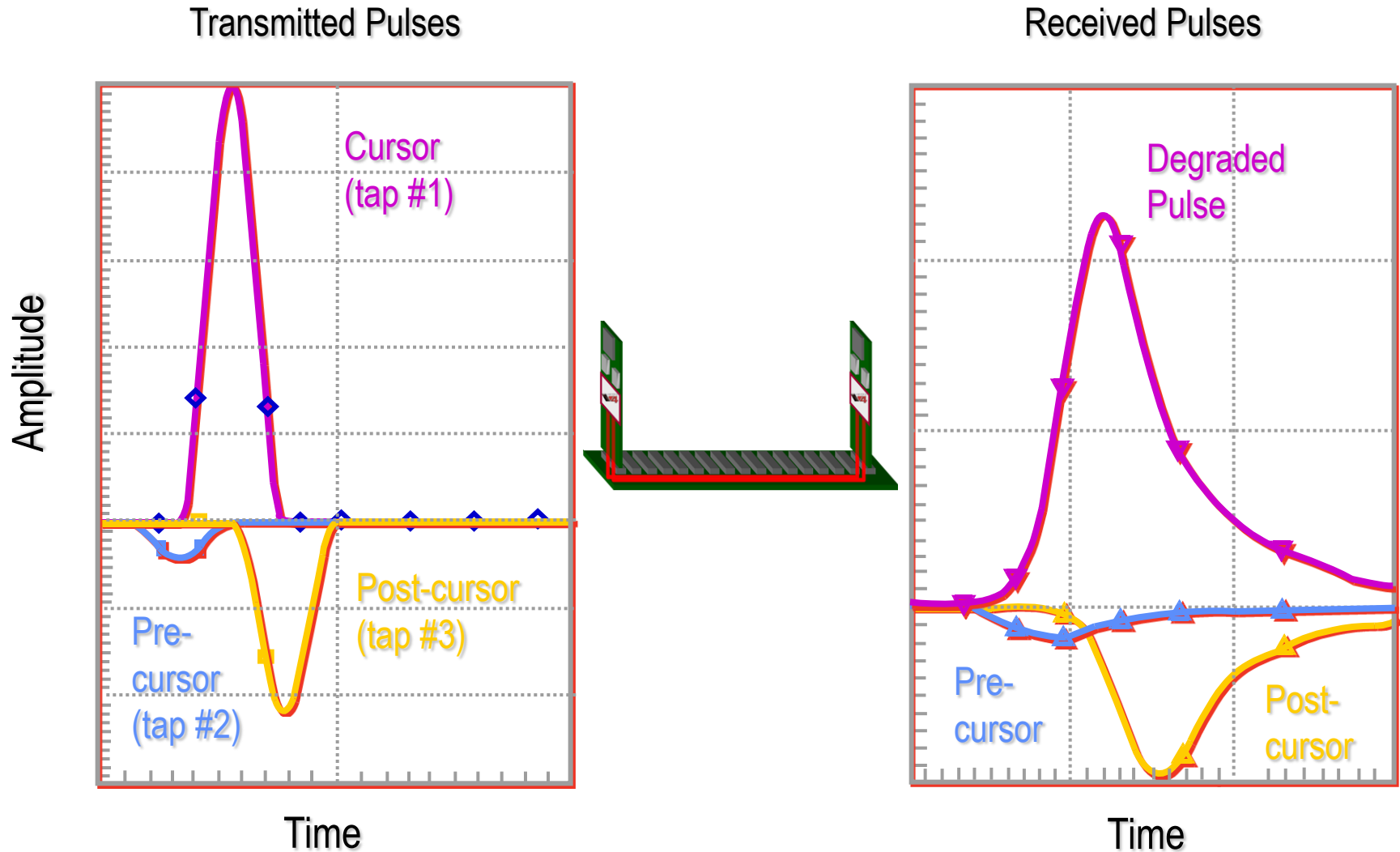
TX Emphasis To Reduce Loss



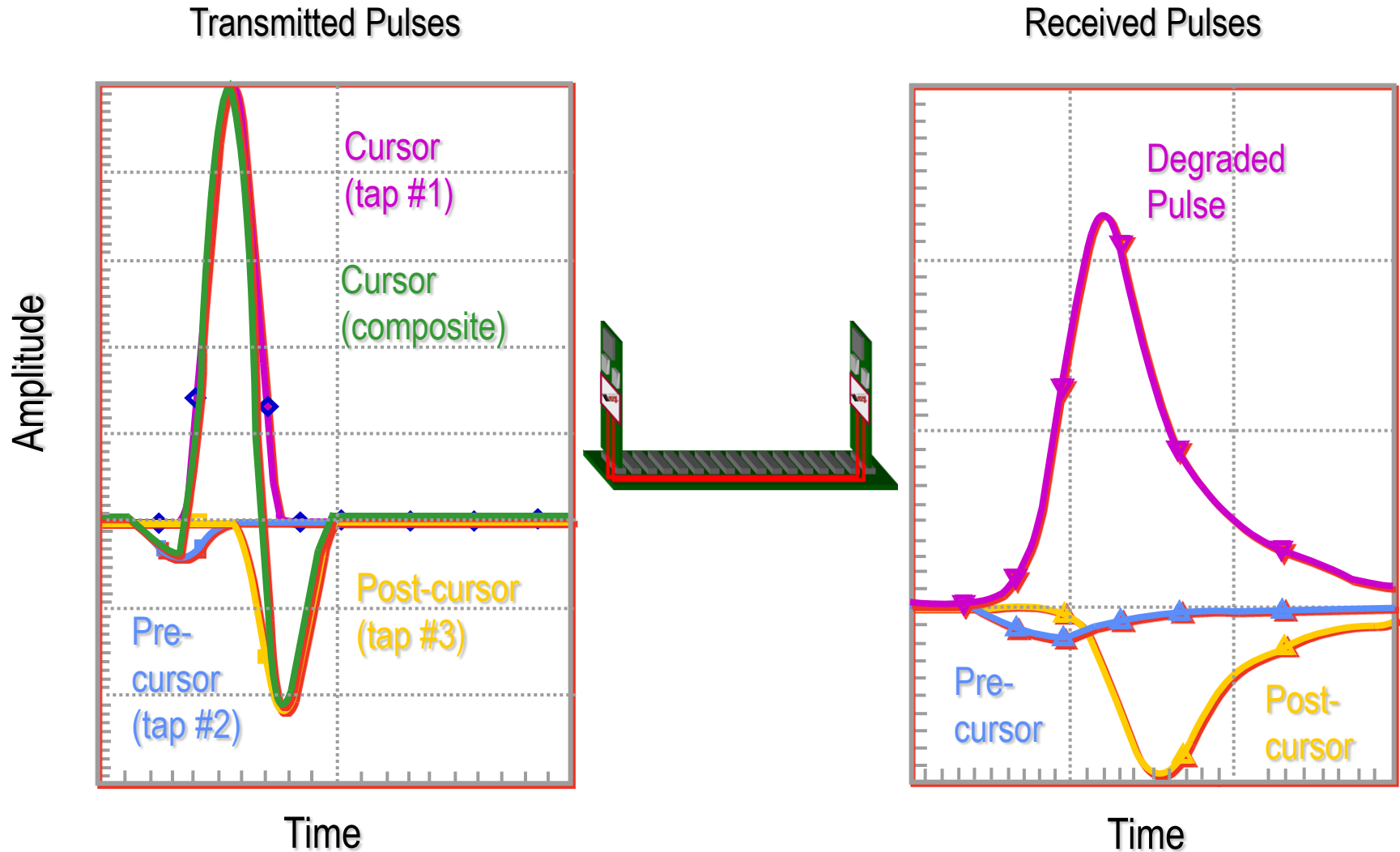
TX Emphasis To Reduce Loss



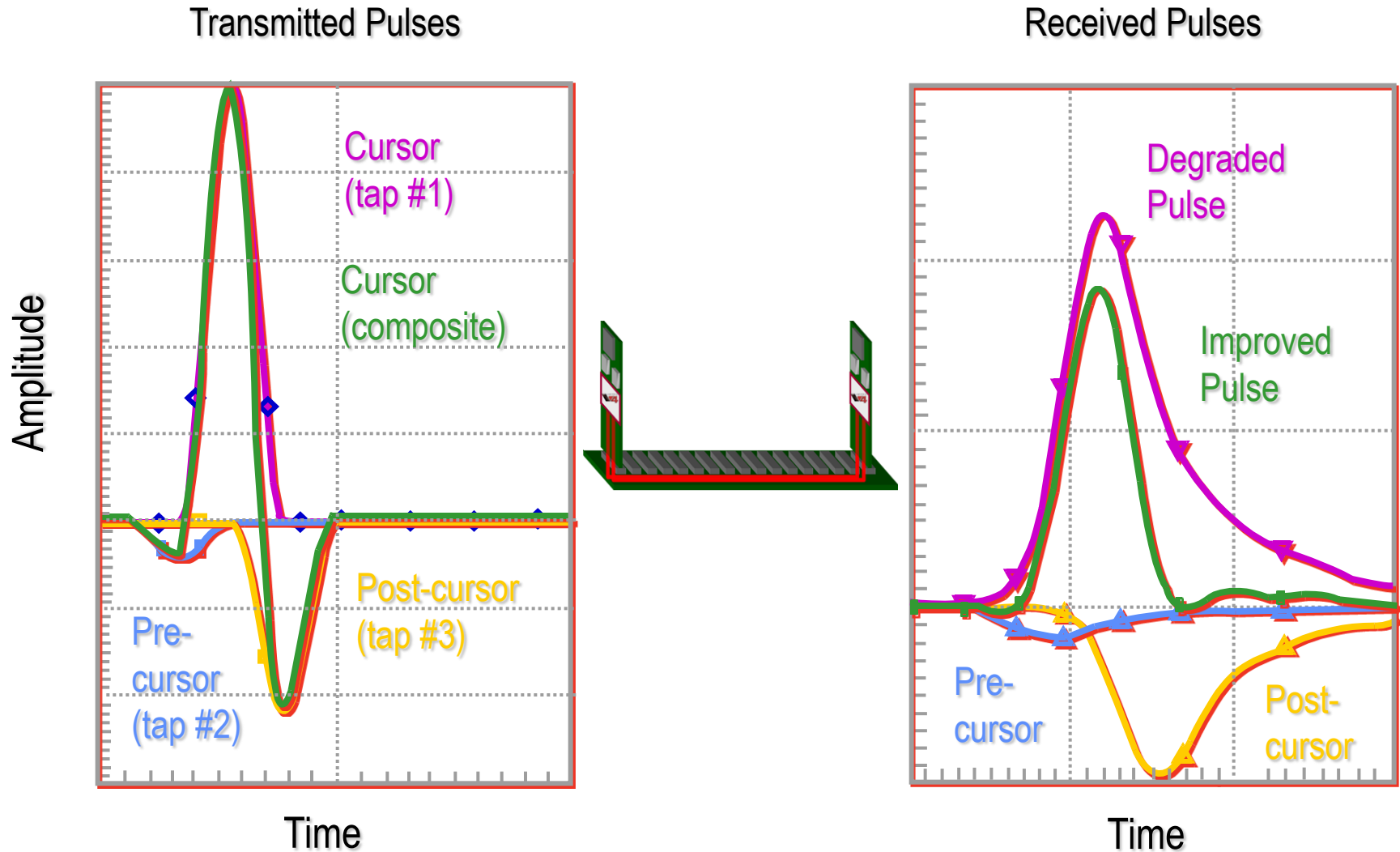
TX Emphasis To Reduce Loss



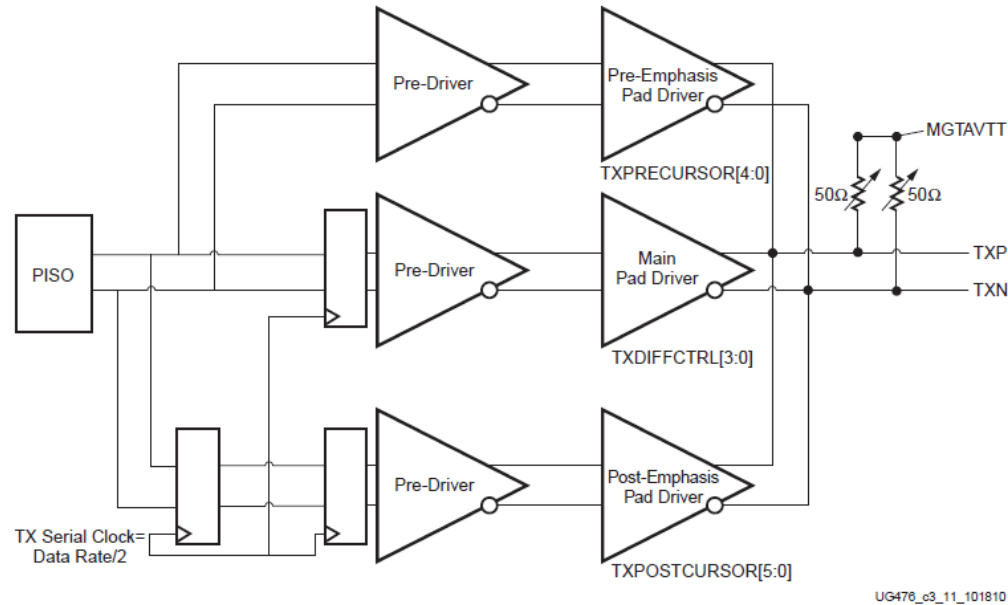
TX Emphasis To Reduce Loss



TX Emphasis To Reduce Loss



7 Series TX Driver Structure With 3 Tap Emphasis



UG476_c3_11_101810

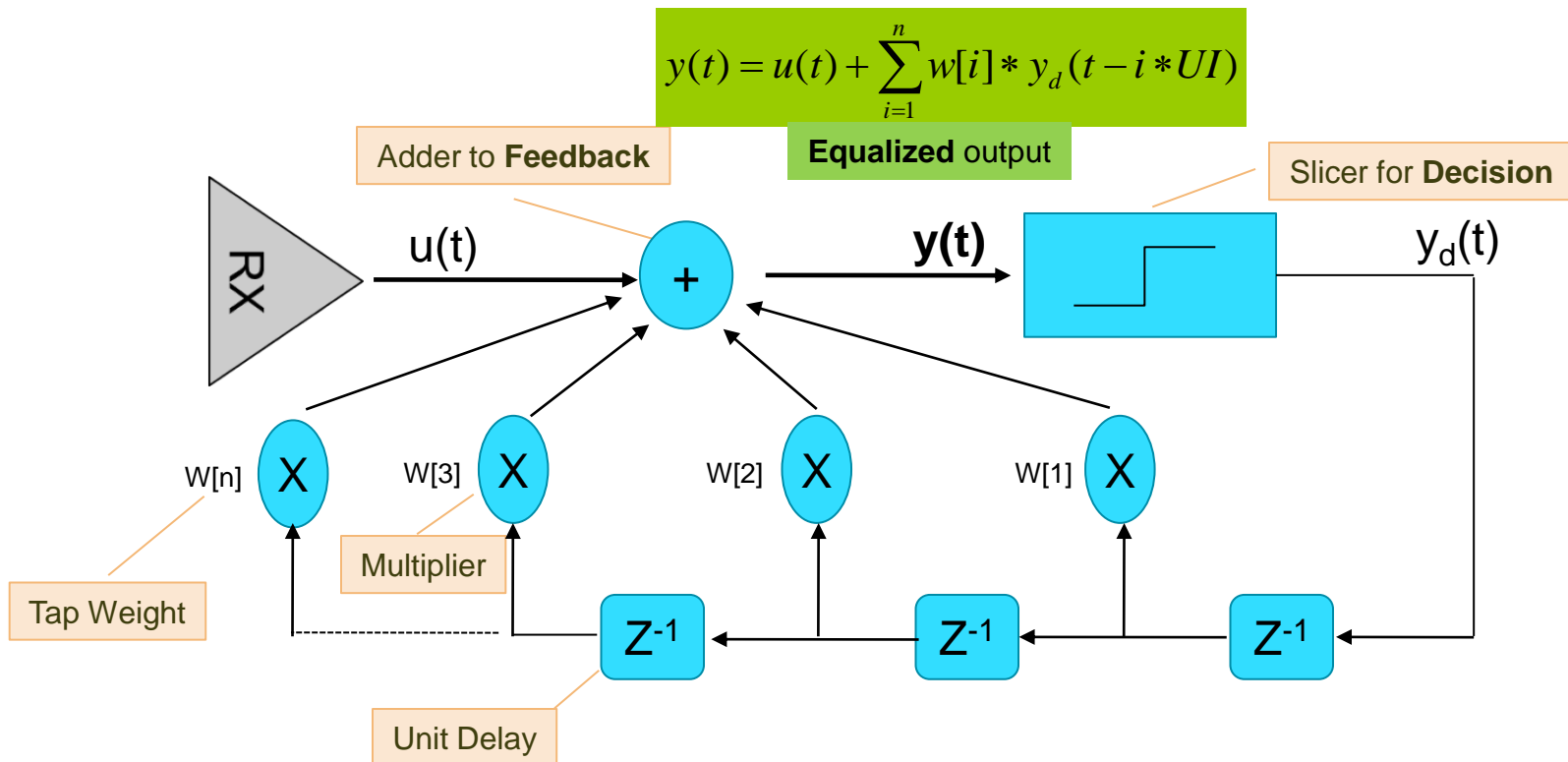
Figure 3-11: TX Configurable Driver Block Diagram

7 Series Serdes	GTP	GTX	GTH	GTZ
Main Cursor	Yes	Yes	Yes	Yes
Post Cursor De-Emphasis	Yes	Yes	Yes	NDA
Pre Cursor De-Emphasis	Yes	Yes	Yes	NDA
10G-KR Backplane TX	NA	Yes	Yes	No

Technique #2: Decision Feedback Equalization

► Decision Feedback Equalization (DFE)

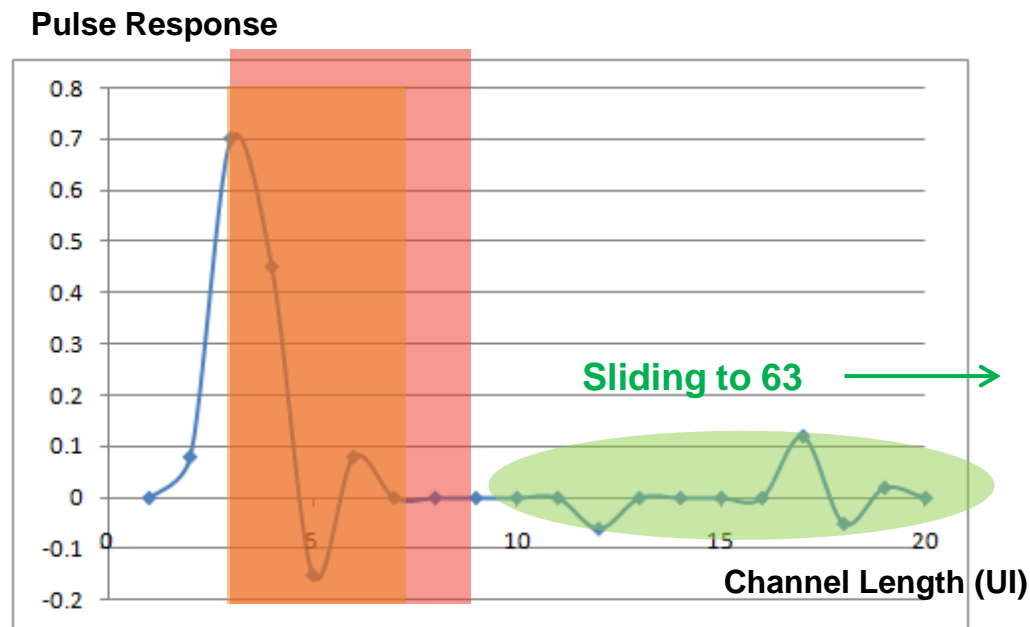
- A nonlinear equalizer that uses previous symbols to eliminate the Inter-Symbol-Interference (ISI) on current symbol.
 - The ISI on current symbol, caused by previous symbols, is subtracted by DFE.



Backplane and Equalization

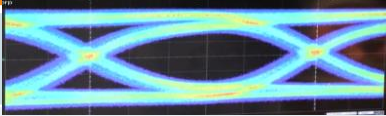
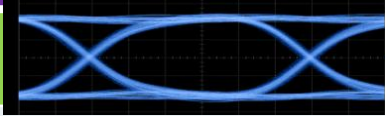
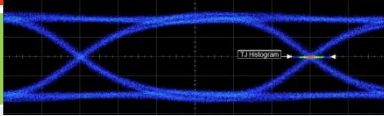



7 Series GTH: Advanced DFE

- Several DFE taps compensate reflections in short distance
 - 5 tap @ 10Gbps => ~1.5 inch
- Virtex-7 GTH DFE
 - 7 fixed taps + 4 sliding taps (up to 63)
 - Compensates 10x distance of reflection with auto adaptation



Xilinx 7-GTX & Xilinx 7-GTH
Best Competition 7 fixed + 4 sliding

10G Backplane Support with 7 Series Competitive Position

Parameter	Best 28nm FPGA Competitor	7-GTX	7-GTH
Jitter @ 10Gb/s+			
TX FIR	Yes	Yes	Yes
RX Linear EQ (CTLE)	16dB	Up to 20dB	Up to 20dB
RX DFE #taps	5 fixed	5 fixed	7 fixed + 4 sliding -> tap 63
RX DFE Adaptation	Adaptive 	Fully Adaptive (proven)	Fully Adaptive(proven)
2-D EyeScan	Yes 	Yes(proven)	Yes (proven)
10G Backplane	Well-designed high confidence channel 	Well-designed high confidence channel	Enhanced KR support for tough backplanes

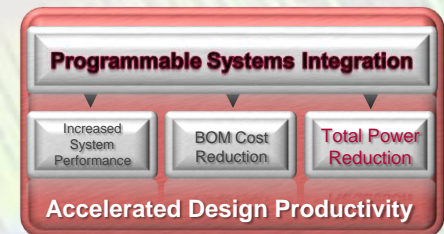
- Low cost 7-GTX has superior jitter performance and better equalization capability as best competitor
- 7-GTH has the BEST KR support in FPGA industry



XILINX

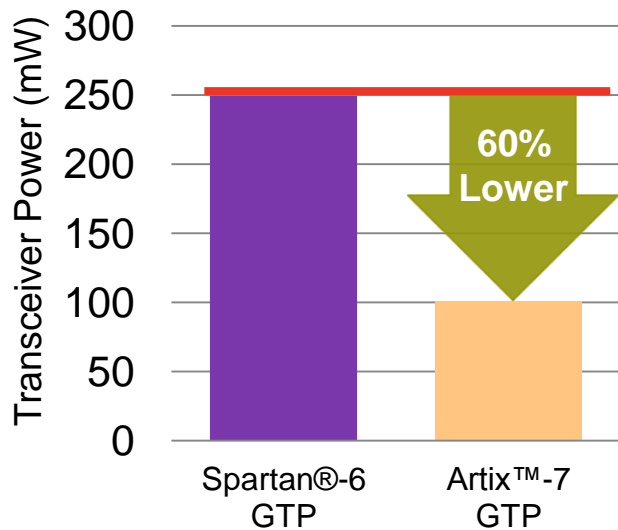
ALL PROGRAMMABLE™

Xilinx 7 Series Transceiver Power Advantage

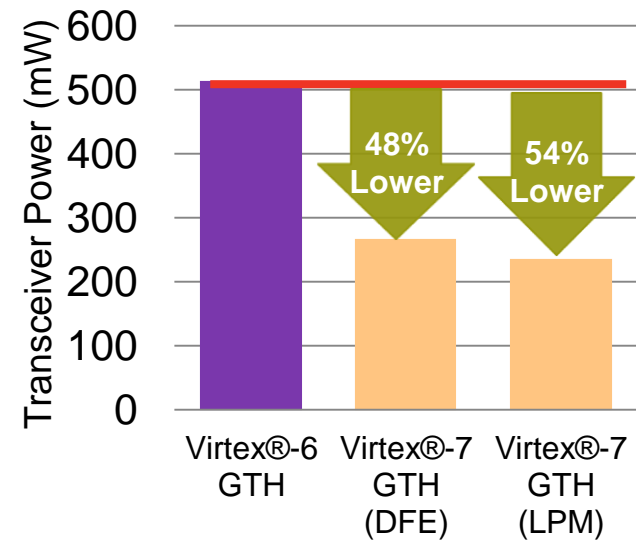


7 Series Re-Architected Transceivers

Power Per Channel* at 3.2 Gbps
(PCS+PMA)



Power Per Channel* at 11.18 Gbps
(PCS+PMA)



* Based on four transceivers and low power modes in XPE 14.1 for Virtex-7 & Artix-7 and XPE13.1 for Virtex-6 and Spartan-6

Artix-7 GTP

- Focus: absolute lowest power / cost
- Up to 6.6 Gbps

Virtex-7 XT GTH

- Focus: high-bandwidth
- Up to 96 channels
- Up to 13.1 Gbps, advanced features (10G KR, etc.)

Saving Power with 7 Series Transceivers Overview

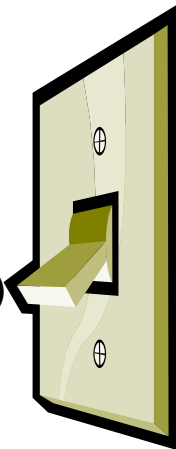
- In addition to our choice of TSMC's HPL process to offer 50% lower power FPGA logic than previous generation, we offer 2 programmable power-saving options for GTX/GTH transceivers.

(1) Power Efficient Mode

Asymmetric Mode
(TX/RX independence)

High Flexibility
(per lane independence)

Power Efficient Mode
(4 lanes @ same freq.)

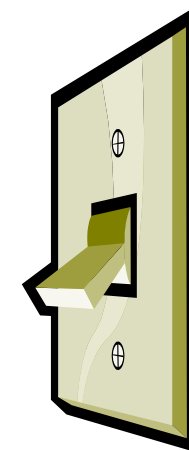


Trade off Flexibility for Power

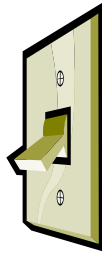
(2) Low Power Mode

Long Channels (40''+)

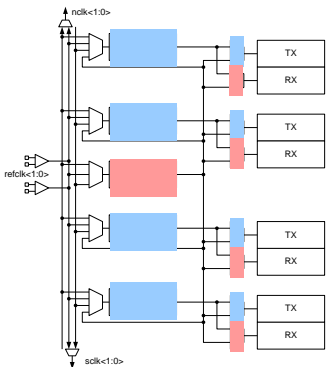
Short Channels (< 7'')



Trade off Trace Length for Power

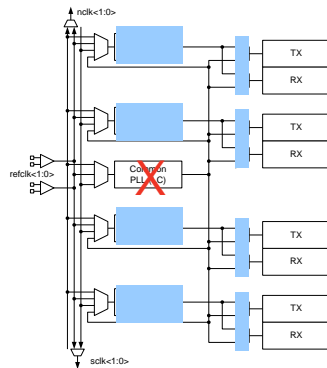


Saving Power with 7 Series Transceivers Power Efficient Mode



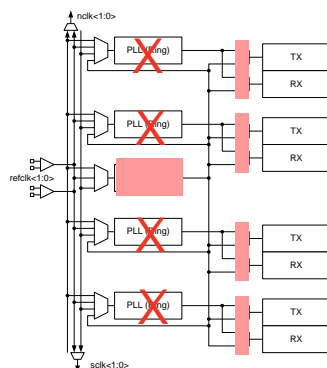
➤ Asymmetric Mode

- Use both LC and Ring Osc.
- TX and RX can operate at a separate speed/protocol (see prev. slide)
- Allows Full Density SDI on FJ2
- => 1.33x higher power for max TX/RX flexibility



➤ High Flexibility Mode

- Each Transceiver on local Ring Oscillator
 - LC Tank powered down
- Each Transceiver can operate at a separate speed/protocol
- => 1.25x higher power for per-channel flexibility



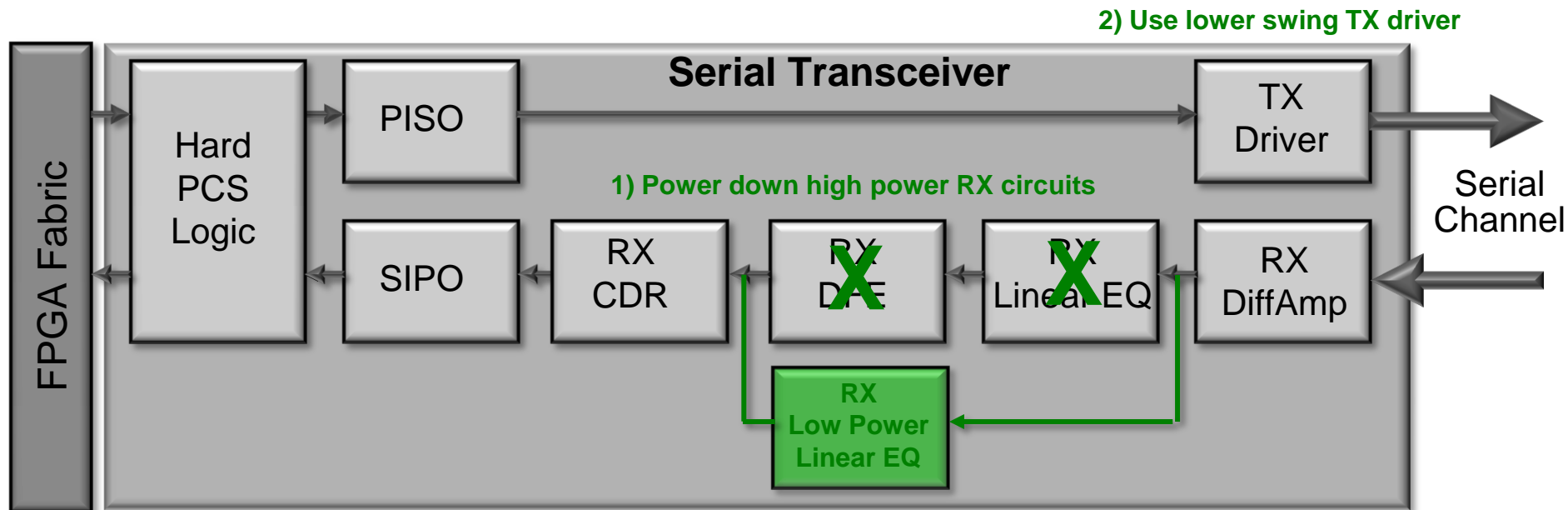
➤ Power Efficient Mode

- Everything on LC Tank (1 PLL/quad)
 - Ring Oscillators Powered Down
- All 4 Transceivers running at the same rate (/1, /2, /4, /8)
 - Most common use case
- CDR can pull in plesiochronous differences
- => 1.0x Lowest power but lowest flexibility



Saving Power with 7 Series Transceivers Low Power Mode (LPM)

- Customer Transceiver Use Models:
 - Chip-to-Optics
 - Chip-to-Chip
 - Backplane
- Increasing # of Chip-to-Chip customers
- Low Power Mode is:
 - Special power-optimized circuitry for “easy” chip-to-chip channels
 - Currently define “easy” as 7” with no connector (feedback welcome)
 - Saves 10%-15% power/lane



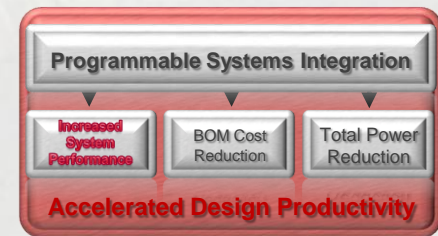
Xilinx 10G Transceiver Feature Evolution:

	V6-GTH	7-GTX	7-GTH
Max Line rate	11.182 (-3)	12.5Gbps (-3)	13.1Gbps (-3)
LC PLL Freq Range	4.96-5.591GHz	5.93-8GHz 9.8-12.5GHz	8-13.1GHz
Ring PLL Freq Range	N/A	1.6-3.3GHz	1.6-4GHz
Total RX DFE taps	3	5	11
RX Channel Loss Compensation	8dB	24dB	24dB
RX DFE Sliding taps (to cancel reflections)	None	None	Last 4 taps can slide up to 63 UIs
Termination Calibration	No	Yes	Yes
Baseline wander cancellation	No	Yes	Yes
Per-slicer offset cancellation	No	No	Yes
RX AGC	Partial	Yes	Yes
TX FIR taps	Pre, Main, Post	Pre, Main, Post	Pre, Main, Post
TX Amplitude control	16 choices	16 choices	16 choices



XILINX

ALL PROGRAMMABLE™



Xilinx 7 Series Transceiver Modelling and Simulation

Transceiver Modeling for Link Budget Analysis

IBIS-AMI instead of HSPICE

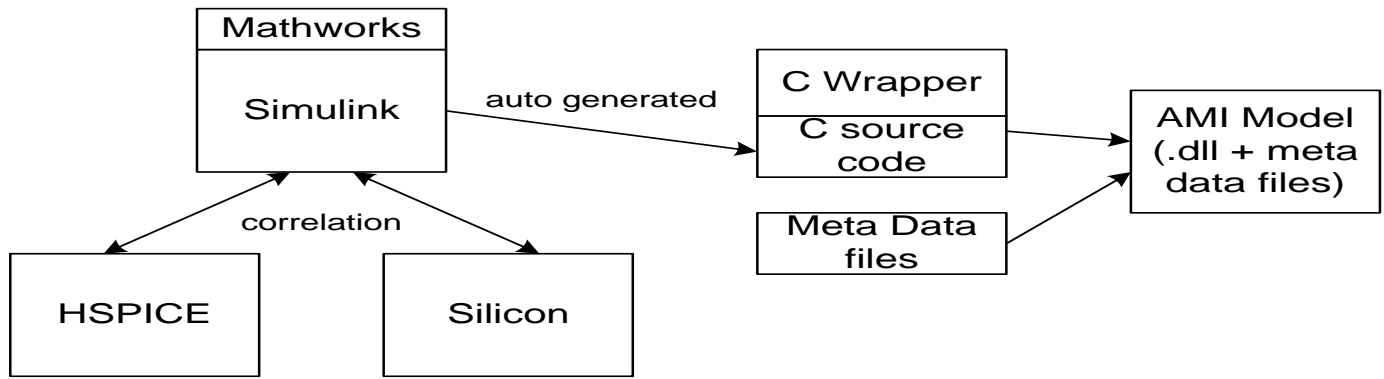
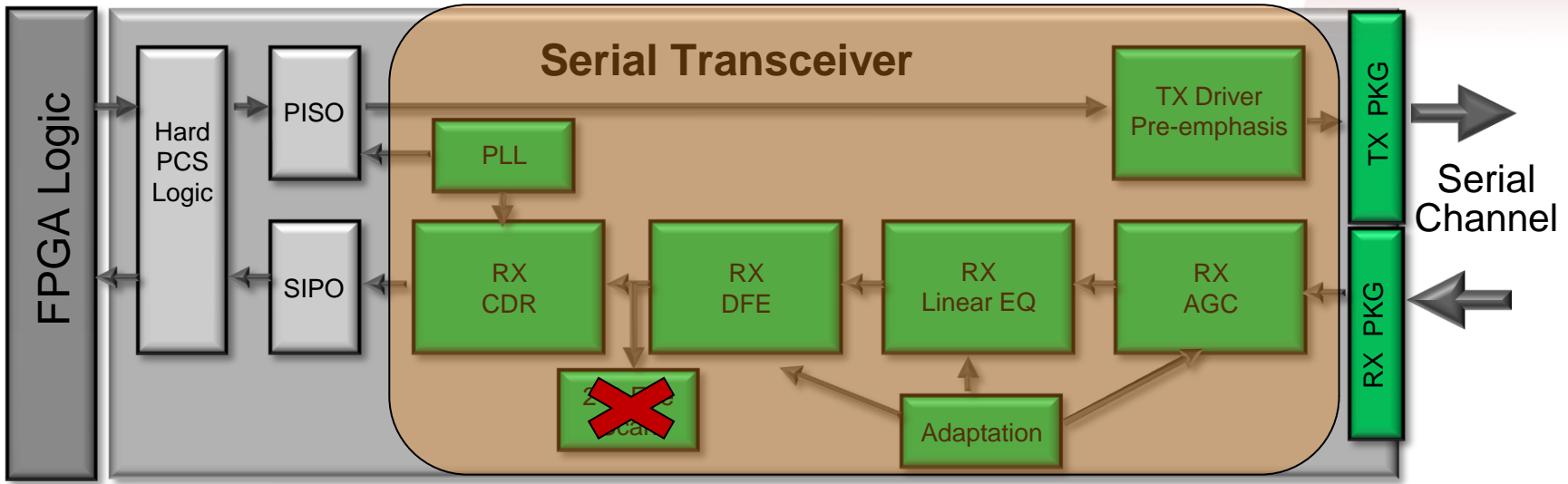
Feature	HSPICE	IBIS-AMI
Model blocks	TX driver with pre-emphasis RX buffer with CTLE & AGC	HSPICE blocks + DFE, CDR & Adaptation (CTLE, DFE & AGC)
Speed	Slow Days/Weeks for 1M bit simulation	Fast Minutes for 1M bit simulation
Accuracy	High Transistor level extraction	Medium-High Behavior model correlated to HSPICE/Hardware

7 Series Transceivers IBIS-AMI modeling

Programmable Systems Integration

Increased System Performance BOM Cost Reduction Total Power Reduction

Accelerated Design Productivity

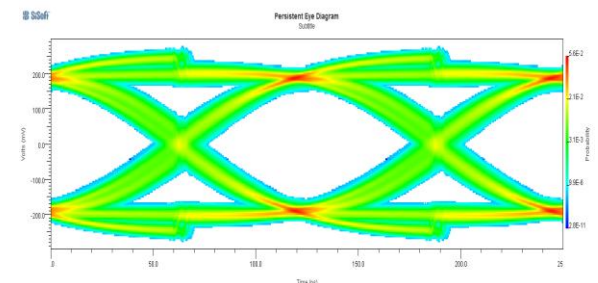
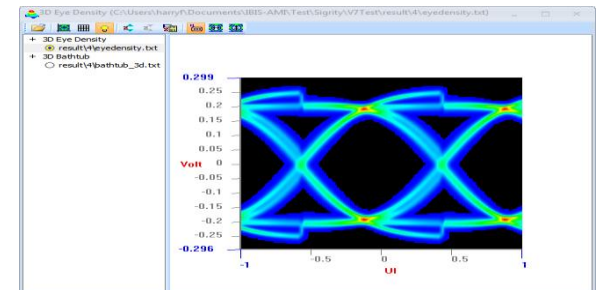
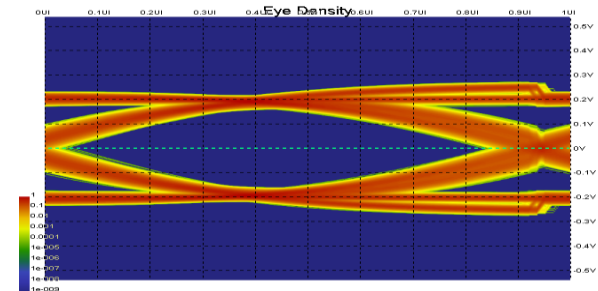
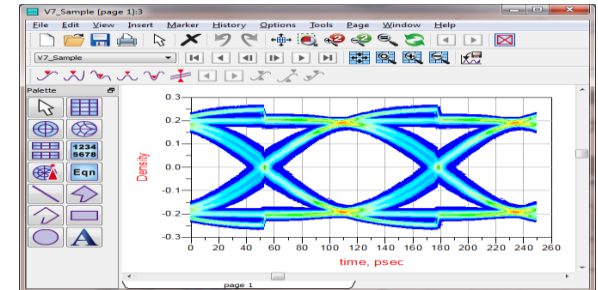


➤ PMA blocks are modeled with the same algorithm as silicon

7 Series Transceiver IBIS-AMI EDA Tool Compatibility

EDA Tool	7 series
Agilent Advanced Design System	Yes
ANSYS Ansoft Designer	Yes
Cadence Allegro PCB SI & PI	Yes
Mentor Graphics HyperLynx	Yes
Sigrity System SI Channel Designer	Yes
SiSoft Quantum Channel Designer	Yes
Synopsys HSPICE	Yes

Note: Listed in Alphabetic order

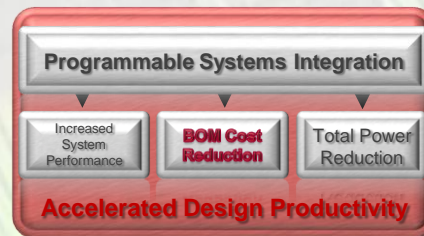




XILINX

ALL PROGRAMMABLE™

Power Integrity 7 Series Transceivers



Power Integrity Simulation

XC7VX485T-FF1761 - Xilinx WP411

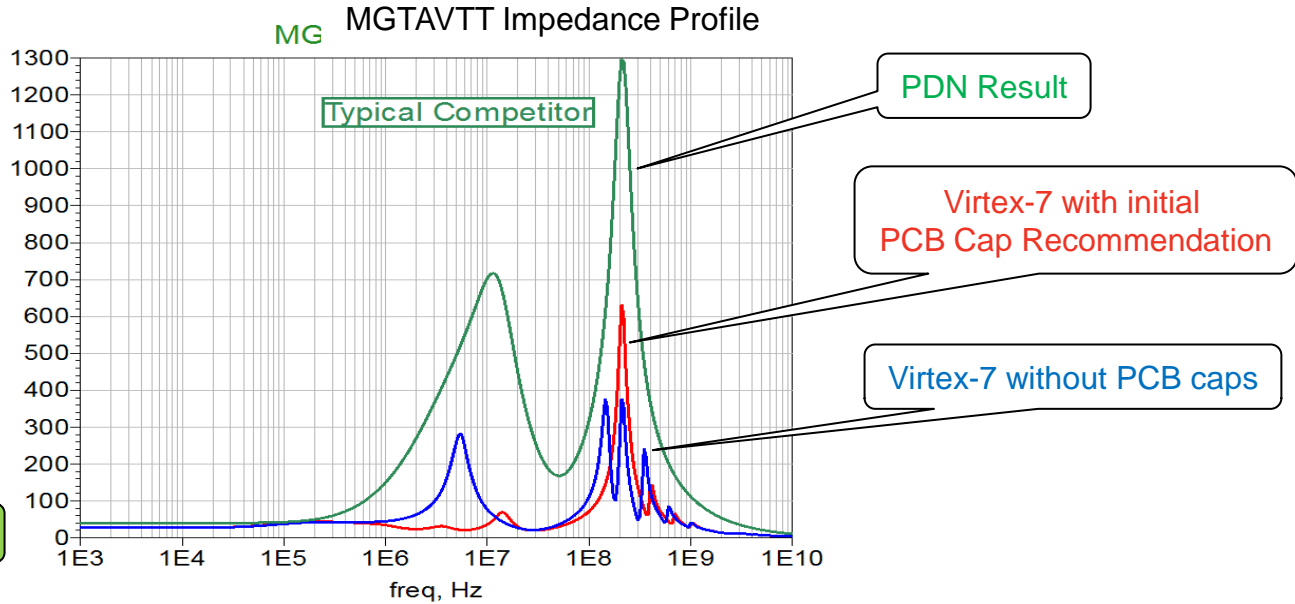


Table 2: Case 1 Capacitors

QTY per Group			Capacitance (µF)
MGTAVCC	MGTAVTT	MGTVCCAUX	
4	4	2	0.022
4	4	0	0.47
2	2	1	1
2	2	1	4.7

Table 3: Case 2 Capacitors

QTY per Group			Capacitance (µF)
MGTAVCC	MGTAVTT	MGTVCCAUX	
0	0	0	0.022
0	0	0	0.47
0	0	0	1
0	0	0	4.7

28 Caps per Group

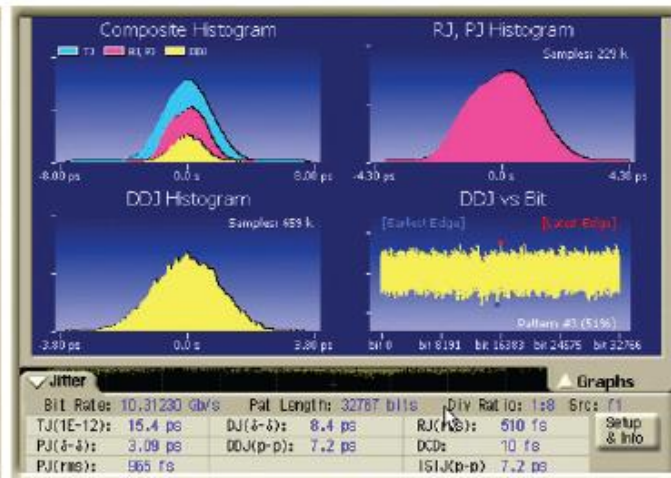
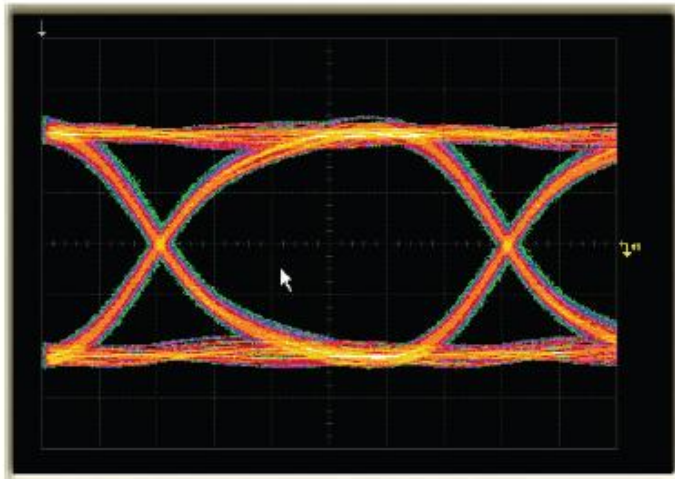


0 Caps

Power Integrity Measurement

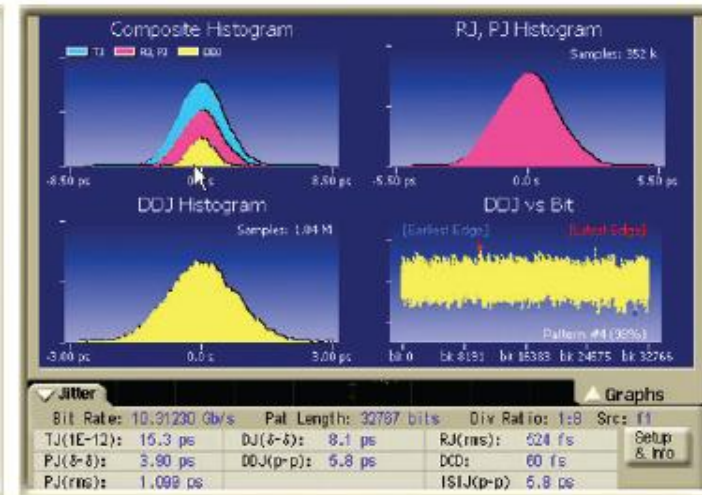
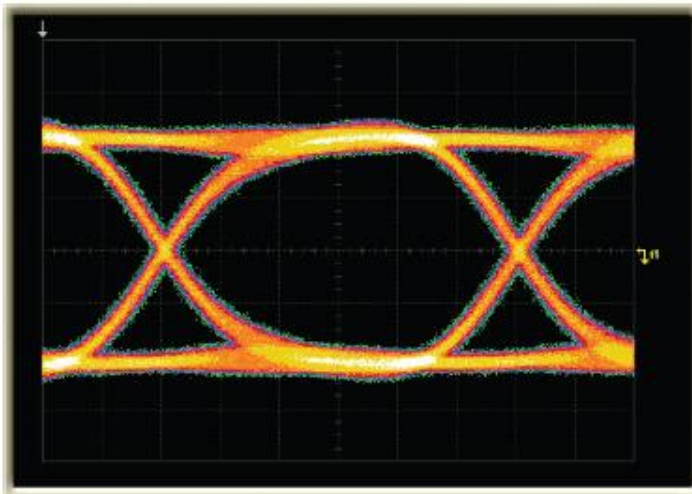
7-GTX TX Eye: PRBS15 @ 10.3125Gb/s

With
PCB
Caps



WP411_17_011612

Without
PCB
Caps



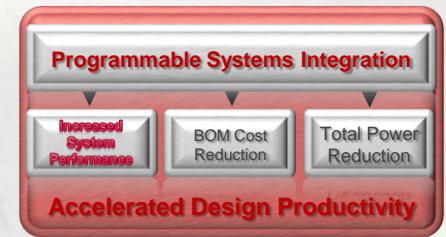
WP411_18_011612



XILINX

ALL PROGRAMMABLE™

Xilinx 7 Series Transceiver Tools



Transceiver Tools

A Note on Tools and Usability

➤ Xilinx IP cores

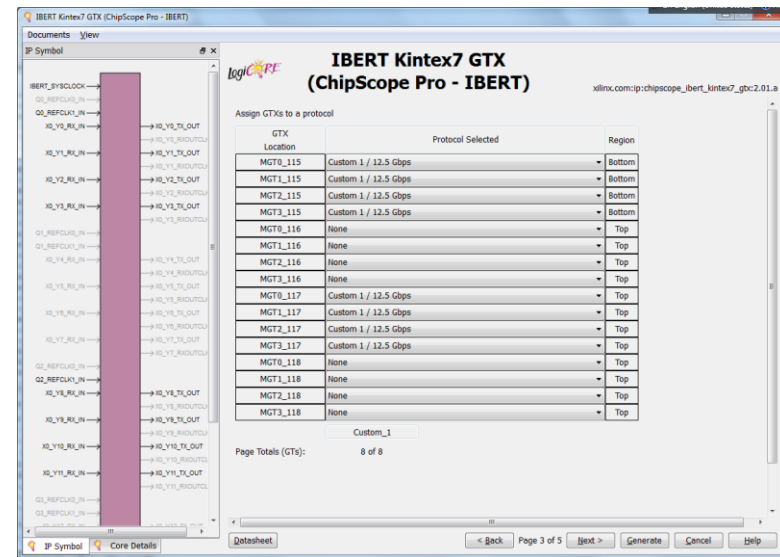
- Encapsulate the transceiver in the IP cores
- Eg: PCIe, 10GE, Interlaken, CPRI, SDI, etc.

➤ Xilinx Transceiver Wizard

- Pre-configured settings for common protocols
- GUI-based customization for customer protocols
- Performs clocking and other transceiver connectivity DRCs

➤ Xilinx ChipScope IBERT

- Integrated Bit Error Rate Tester
- Hardware evaluation of customized channel
- In-system debug to help system bring-up
- IBERT on 2 different FPGAs controlled from one



IBERT Generator GUI



Accelerated Design
Productivity

IP and Tools to Simplify Design Entry and Verification

Transceiver Tools

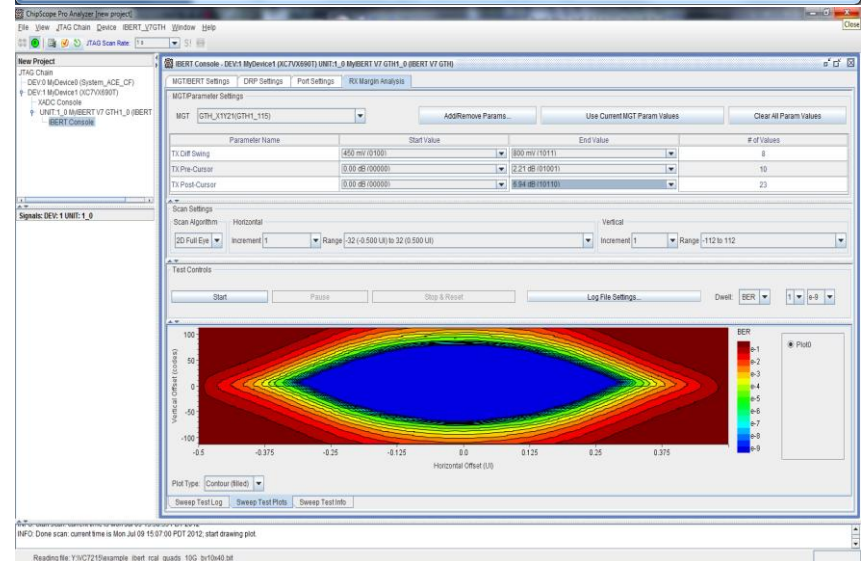
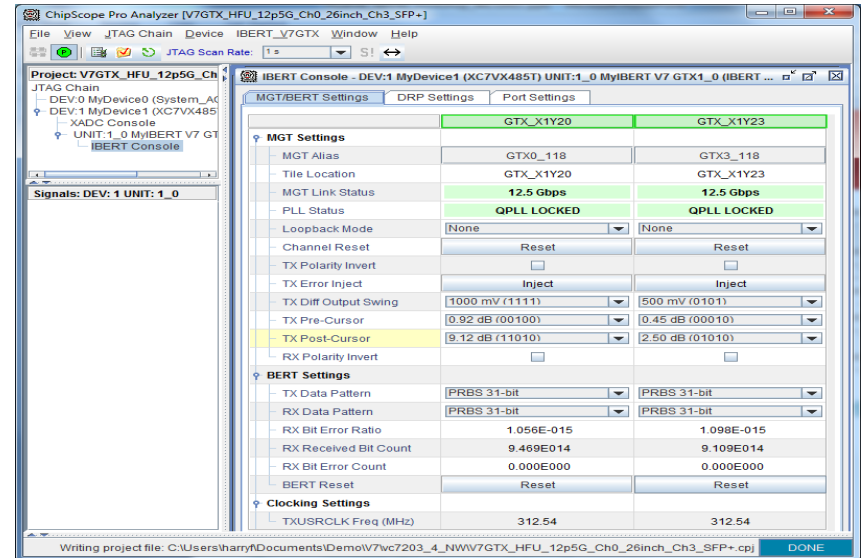
IBERT – Runtime GUI

➤ Key Features

- Link Status
- Hardware PRBS Generator/Checker
- TX Swing and TX Pre-emphasis adjustment
- Attributes and Port setting in advanced tabs

➤ On-chip Margin Analysis

- Choice of 1-D or 2-D
- Choice of resolution
- Choice of target BER
- System tuning made easy with parameter sweeping



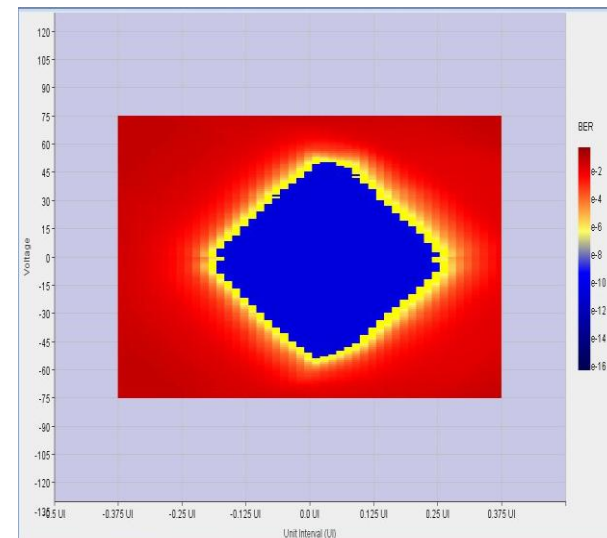
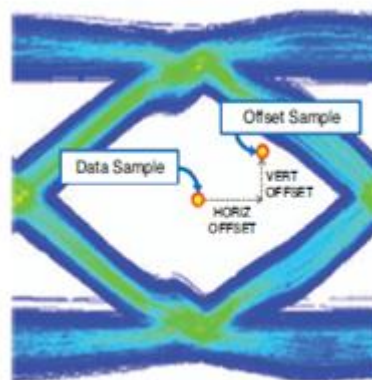
System Analysis with Eye Scan

Non-Destructive On-Chip Debug

- **Internal Scan History in Xilinx**
 - Multi-generations of 1-D BER plot

- **Two Samplers in RX Path**
 - Data Sampler at the eye center
 - Moveable Offset Sampler
 - Compare two samplers
 - 2-D BER Eye built from error location

- **Eye Scan inside receiver on live data**
 - Non-destructive
 - Post equalization
 - BER Measurement
 - 2-D Plot



Features	7 Series Eye Scan
Horizontal Taps	64 at max rate, up to 512
Vertical Taps	256
Diagnostic Tool	IBERT



XILINX

ALL PROGRAMMABLE™

Xilinx 7 Series Product Table

Artix-7 FPGA Family Table

Artix-7 Product Table

Subject to Change

		Artix-7 FPGAs		
		Optimized for Lowest Cost and Power with Small Form-Factor Packaging for Highest Volume Applications (1.0V, 0.9V)		
	Part Number	XC7A100T	XC7A200T	
Logic Resources	Slices	15,850	33,650	
	Logic Cells	101,440	215,360	
	CLB Flip-Flops	126,800	269,200	
Memory Resources	Maximum Distributed RAM (Kbits)	1,188	2,888	
	Block RAM/FIFO w/ ECC (36Kbits each)	135	365	
	Total Block RAM (Kbits)	4,860	13,140	
Clock Resources	CMTs (1 MMCM + 1 PLL)	6	10	
I/O Resources	Maximum Single-Ended I/O ⁽⁴⁾	300	500	
	Maximum Differential I/O Pairs ⁽⁴⁾	144	240	
Embedded Hard IP Resources	DSP48E1 Slices	240	740	
	PCI Express ⁽¹⁾	1	1	
	Agile Mixed Signal (AMS) / XADC	1	1	
	Configuration AES / HMAC Blocks	1	1	
	GTP 5.4 / 6.6 Gb/s Transceivers	8	16	
Speed Grades	Commercial	-1, -2	-1, -2	
	Extended	-2L, -3	-2L, -3	
	Industrial	-1, -2	-1, -2	
Configuration	Configuration Memory (Mbits)	29.3	62.4	
	Package ⁽³⁾	Dimensions (mm)	Available User I/O: 3.3V SelectIO™ Pins (GTP Transceivers)	
	CSG324	15 x 15	210 (0)	
	FTG256	17 x 17	170 (0)	
	SBG484	19 x 19		285 (4)
Footprint Compatible	FGG484 ⁽²⁾	23 x 23	285 (4)	
	FBG484 ⁽²⁾	23 x 23		285 (4)
Footprint Compatible	FGG676 ⁽²⁾	27 x 27	300 (8)	
	FBG676 ⁽²⁾	27 x 27		400 (8)
	FFG1156 ⁽²⁾	35 x 35		500 (16)

5.4G ↑
0.6G ↓

Up to 16 GTP Transceivers

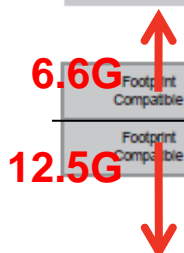
Kintex-7 FPGA Family Table

Subject to Change

Kintex-7 Product Table

Kintex-7 FPGAs
Optimized for Best Price-Performance
(1.0V, 0.9V)

Part Number		XC7K70T	XC7K160T	XC7K325T	XC7K355T	XC7K410T	XC7K420T	XC7K480T	
EasyPath™ Cost Reduction Solutions ⁽¹⁾		—	—	—	XCE7K355T	XCE7K410T	XCE7K420T	XCE7K480T	
Logic Resources	Slices	10,250	25,350	50,950	55,650	63,550	65,150	74,650	
	Logic Cells	65,600	162,240	326,080	356,160	406,720	416,960	477,760	
	CLB Flip-Flops	82,000	202,800	407,600	445,200	508,400	521,200	597,200	
Memory Resources	Maximum Distributed RAM (Kbits)	836	2,188	4,000	5,088	5,663	5,936	6,788	
	Block RAM/FIFO w/ ECC (36Kbits each)	135	325	445	715	795	835	955	
	Total Block RAM (Kbits)	4,860	11,700	16,020	25,740	28,620	30,060	34,380	
Clock Resources	CMTs (1 MMCM + 1 PLL)	6	8	10	6	10	8	8	
I/O Resources	Maximum Single-Ended I/O	300	400	500	300	500	400	400	
	Maximum Differential I/O Pairs	144	192	240	144	240	192	192	
Embedded Hard IP Resources	DSP48E1 Slices	240	600	840	1,440	1,540	1,680	1,920	
	PCI Express ⁽²⁾	1	1	1	1	1	1	1	
	Agile Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1	
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	
	GTX 12.5 Gb/s Transceivers	8	8	16	24	16	32	32	
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	
	Extended	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	
	Industrial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	
Package ⁽⁴⁾	Dimensions (mm)	Available User I/O: 3.3V SelectIO™ Pins, 1.8V SelectIO Pins (GTX Transceivers)							
Footprint Compatible	FBG484	23 x 23	185, 100 (4)	185, 100 (4)					
	FBG675	27 x 27	200, 100 (8)	250, 150 (8)	250, 150 (8)	250, 150 (8)			
	FFG675	27 x 27		250, 150 (8)	250, 150 (8)	250, 150 (8)			
Footprint Compatible	FBG900	31 x 31		350, 150 (16)		350, 150 (16)			
	FFG900	31 x 31		350, 150 (16)		350, 150 (16)			
	FFG901	31 x 31			300, 0 (24)		380, 0 (28)	380, 0 (28)	
	FFG1156	35 x 35					400, 0 (32)	400, 0 (32)	



FBG 1.0mm Leadless flip-chip; FFG: 1.0mm Flip-chip fine-pitch

XMP085 (v3.5)

- Notes: 1. EasyPath™ solutions provide a fast and conversion-free path for cost reduction.
 2. Hard block supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.
 3. Leadless package options ("FBxxx" or "FFxxx") available for the following Kintex-7 devices: XC7K160T, XC7K325T, XC7K355T, XC7K410T, XC7K420T, XC7K480T
 4. Preliminary product information, subject to change. Please contact your Xilinx representative for the latest information.

4~32 GTX Transceivers

Virtex-7T and XT FPGAs

Subject to Change

Virtex-7 Product Table

		Virtex-7 FPGAs										
		Optimized for Highest System Performance and Capacity (1.0V, 0.9V)					(1.0V, 0.9V)					
		Part Number	XC7V585T	XC7V2000T	XC7VX330T	XC7VX415T	XC7VX485T	XC7VX550T	XC7VX690T	XC7VX980T	XC7VX1140T	
		EasyPath™ Cost Reduction Solutions ⁽¹⁾	XC7V585T	XC7V2000T	XC7VX330T	XC7VX415T	XC7VX485T	XC7VX550T	XC7VX690T	XC7VX980T	XC7VX1140T	
Logic Resources	Slices	91,050	305,400	51,000	64,400	75,900	86,600	108,300	153,000	178,000		
	Logic Cells	582,720	1,954,560	326,400	412,160	485,760	554,240	693,120	979,200	1,139,200		
	CLB Flip-Flops	728,400	2,443,200	408,000	515,200	607,200	692,800	866,400	1,224,000	1,424,000		
Memory Resources	Maximum Distributed RAM (Kbits)	6,938	21,550	4,388	6,525	8,175	8,725	10,888	13,838	17,700		
	Block RAM/FIFO w/ ECC (36Kbits each)	795	1,292	750	880	1,030	1,180	1,470	1,500	1,880		
	Total Block RAM (Kbits)	28,620	46,512	27,000	31,680	37,080	42,480	52,920	54,000	67,680		
Clocking	CMTs (1 MMCM + 1 PLL)	18	24	14	12	14	20	20	18	24		
I/O Resources	Maximum Single-Ended I/O	850	1,200	700	600	700	600	1,000	900	1100		
	Maximum Differential I/O Pairs	408	576	336	288	336	288	480	432	528		
	DSP48E1 Slices	1,260	2,160	1,120	2,160	2,800	2,880	3,600	3,600	3,360		
Embedded Hard IP Resources	Gen2 PCI Express Interface Blocks	3	4	—	—	4	—	—	—	—		
	Gen3 PCI Express Interface Blocks	—	—	2	2	—	2	3	3	4		
	Agile Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1	1	1		
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1	1		
	GTX 12.5Gb/s Transceivers ⁽²⁾	36	36	—	—	56	—	—	—	—		
	GTH 13.1Gb/s Transceivers ⁽³⁾	—	—	28	48	—	80	80	72	96		
	GTZ 28.05Gb/s Transceivers	—	—	—	—	—	—	—	—	—		
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2		
	Extended ⁽⁴⁾	-2L, -3	-2L, -2G	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -2G		
	Industrial	-1, -2	-1	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1		
Configuration	Configuration Memory (Mbits)	153.9	426.6	106.1	131.5	154.7	219.2	219.2	269.4	367.2		
		Package ⁽⁵⁾	Area	Available User I/O: 3.3V SelectIO™ Pins, 1.8V SelectIO Pins (GTX, GTH Transceivers)								
		Flip chip, fine pitch BGA (1.0 mm ball spacing)										
Footprint Compatible	FFG1157	35 x 35 mm	0, 600 (20, 0)		0, 600 (0, 20)	0, 600 (0, 20)	0, 600 (20, 0)		0, 600 (0, 20)			
	FFG1761	42.5 x 42.5 mm	100, 750 (36, 0)		50, 650 (0, 28)		0, 700 (28, 0)		0, 850 (0, 36)			
	FLG1761	42.5 x 42.5 mm										
	FHG1761	45 x 45 mm	0, 850 (36, 0)									
	FLG1925	45 x 45 mm	0, 1200 (45, 0)									
Footprint Compatible	FFG1158	35 x 35 mm			0, 350 (0, 48)	0, 350 (48, 0)	0, 350 (0, 48)	0, 350 (0, 48)				
	FFG1926	45 x 45 mm						0, 720 (0, 64)	0, 720 (0, 64)			
	FLG1926	45 x 45 mm								0, 720 (0, 64)		
Footprint Compatible	FFG1927	45 x 45 mm			0, 600 (0, 48)	0, 600 (56, 0)	0, 600 (0, 80)	0, 600 (0, 80)				
	FFG1928	45 x 45 mm							0, 480 (0, 72)			
Footprint Compatible	FLG1928	45 x 45 mm								0, 480 (0, 96)		
	FFG1930	45 x 45 mm				0, 700 (24, 0)		0, 1000 (0, 24)	0, 900 (0, 24)			
Footprint Compatible	FLG1930	45 x 45 mm								0, 1100 (0, 24)		

20~96 GTX/GTH transceivers

16~36 GTX transceivers

Virtex-7HT FPGAs

Virtex-7 Product Table

		(1.0V)			
		Part Number	XC7VH290T	XC7VH580T	XC7VH870T
		EasyPath™ Cost Reduction Solutions ⁽¹⁾	—	—	—
Logic Resources	Slices	44,375	90,700	138,900	
	Logic Cells	284,000	580,480	876,160	
	CLB Flip-Flops	355,000	725,600	1,095,200	
Memory Resources	Maximum Distributed RAM (Kbits)	4,425	8,850	13,275	
	Block RAM/FIFO w/ ECC (36Kbits each)	470	940	1,410	
	Total Block RAM (Kbits)	16,920	33,840	50,760	
Clocking	CMTs (1 MMCM + 1 PLL)	6	12	18	
I/O Resources	Maximum Single-Ended I/O	300	600	650	
	Maximum Differential I/O Pairs	144	288	312	
Embedded Hard IP Resources	DSP48E1 Slices	840	1,680	2,520	
	Gen2 PCI Express Interface Blocks	—	—	—	
	Gen3 PCI Express Interface Blocks	1	2	3	
	Agile Mixed Signal (AMS) / XADC	1	1	1	
	Configuration AES / HMAC Blocks	1	1	1	
	GTX 12.5Gb/s Transceivers ⁽²⁾	—	—	—	
	GTH 13.1Gb/s Transceivers ⁽³⁾	24	48	72	
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	
	Extended ⁽⁴⁾	-2L, -2G	-2L, -2G	-2L, -2G	
	Industrial	—	—	—	
Configuration	Configuration Memory (Mbits)	91.8	183.6	275.4	
Package ⁽⁵⁾		Area	1.8V SelectIO Pins (GTH, GTZ)		
Ceramic flip chip, fine pitch BGA (1.0 mm ball s					
HCG1155	35 x 35 mm	300 (24, 8)	400 (24, 8)		
HCG1931	45 x 45 mm		600 (48, 8)	650 (48, 8)	
HCG1932	45 x 45 mm		300 (48, 8)	300 (72, 16)	

24~72 GTH transceivers
8~16 GTZ transceivers

XMP084 (v4.4)



XILINX

ALL PROGRAMMABLE™

Summary

Summary

➤ New for 7 Series:

- Common Transceiver Architecture
 - IP portability
- Different Rates for different platforms
- Low Power Mode
 - 30% lower power for chip-to-chip channels

➤ 7 Series FPGAs Have the Most Comprehensive Transceiver Family

- Virtex-7 GTZ : 28Gb/s Transceivers for 100G and 400G datapaths
- Virtex-7 GTH : Highest Performance/Count Transceiver Family
- Virtex-7 GTX : 12.5Gb/s with more SelectIO for wider memory interfaces
- Kintex-7 GTX : 12.5Gb/s to the masses
- Artix-7 GTP : Ultra-High Volume Transceivers



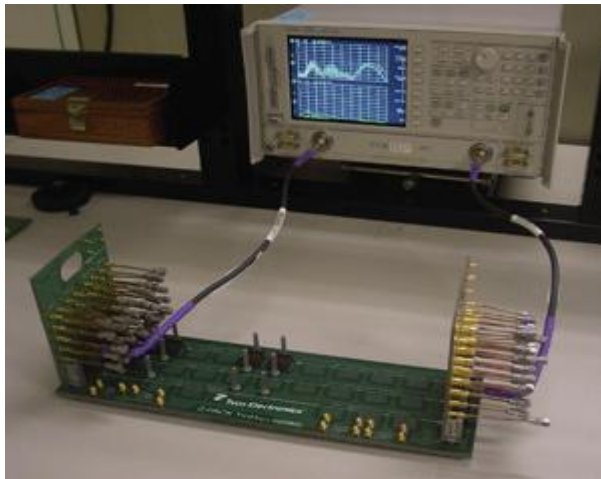
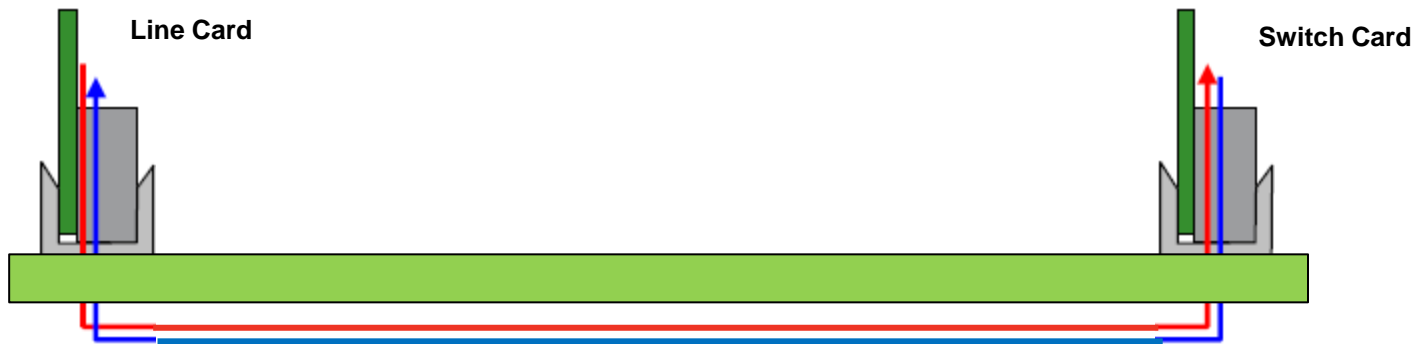
XILINX

ALL PROGRAMMABLE™

Appendix A: Backplane

Backplane Basics

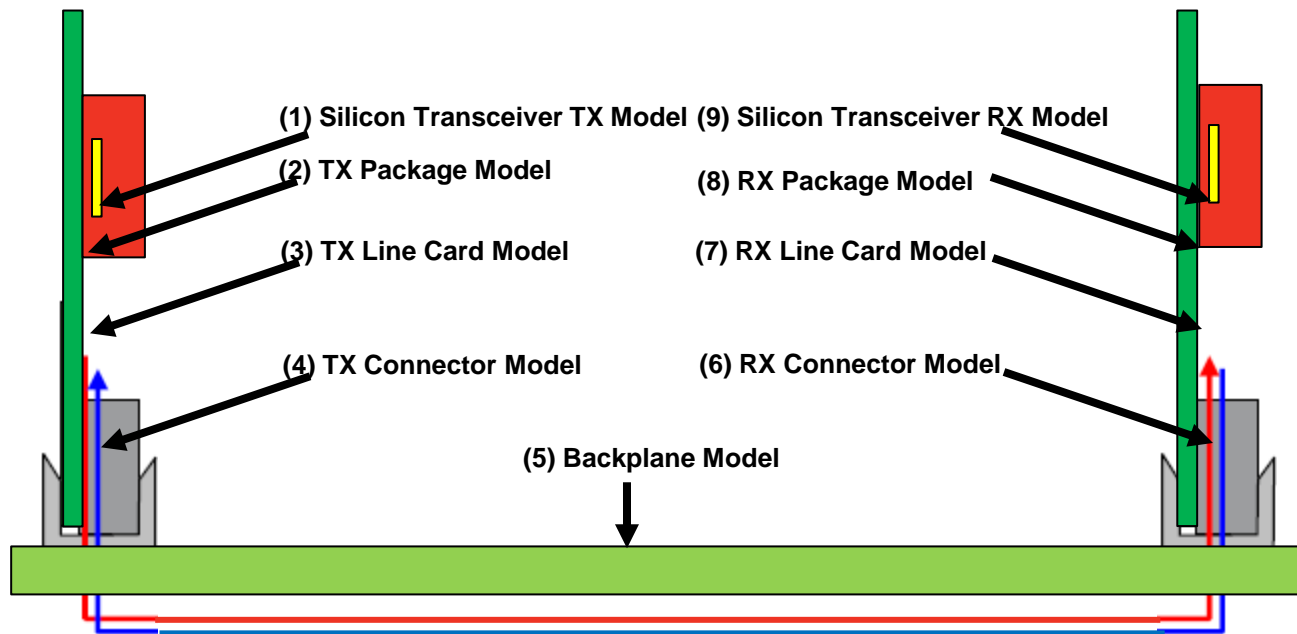
- A backplane is a **PCB board** that connects **connectors** so that each pin on each connector is linked to the same relative pin on the other connector(s) forming a data bus.



Example: Tyco Electronics' Z-Pack TinMan backplane for 10G-KR

7 series GT	Backplane?
GTP	✓ (~3G)
GTX	✓
GTH	✓ +
GTZ	✗

Backplane System Modeling



- Components to properly design and model a backplane system
- Xilinx provides Silicon IBIS-AMI Models and Package S-parameter files
 - 1000x faster simulation time than HSPICE
 - Correlated with HSPICE before silicon
 - Correlated to HW at Production
 - Xilinx was the first in the industry to offer IBIS-AMI models (Virtex-5)

Signal Integrity Challenge and Mitigation in Backplane System

➤ Signal Integrity Challenge

- Insertion Loss
- Reflection
- Crosstalk

➤ Factors

- Channel length
- Board material selection
- Trace width & spacing
- Board thickness & Via
- Signal intensity

➤ Mitigation

- TX Jitter
 - Improve jitter performance to increase system margin
- TX FIR
 - Pre and Post tap
- RX CTLE
 - Compensate Insertion Loss
 - Adaptation significantly reduces the time identify
- RX DFE
 - Compensate insertion loss at high frequency
 - Compensate reflection within tap limitation

▪ IEEE 802.3 10GBase-KR Channel Parameters

- Fitted Attenuation
- Insertion Loss
- Insertion Loss Deviation
- Return Loss
- Insertion Loss to Crosstalk Ratio

Backplane

802.3 10GBase-KR Channel Parameters

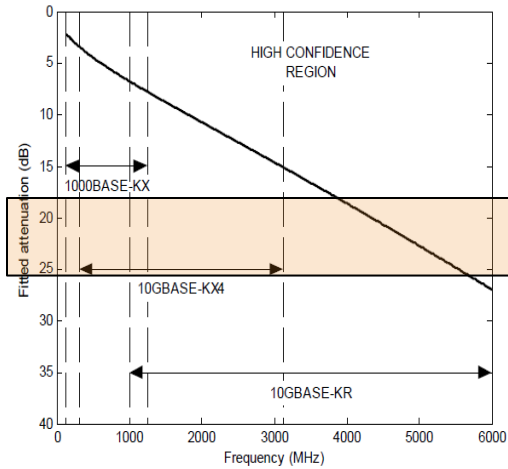


Figure 69B-2—Fitted attenuation limit

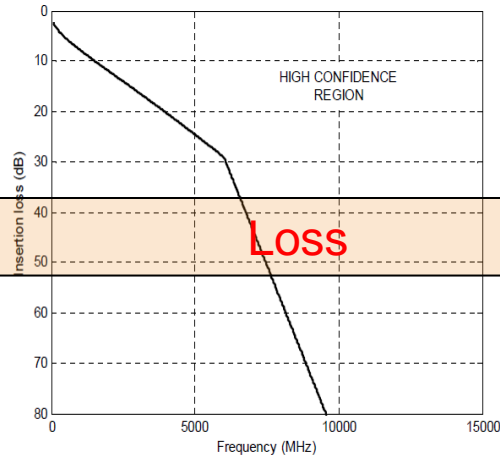


Figure 69B-5—Insertion loss limit for 10GBASE-KR

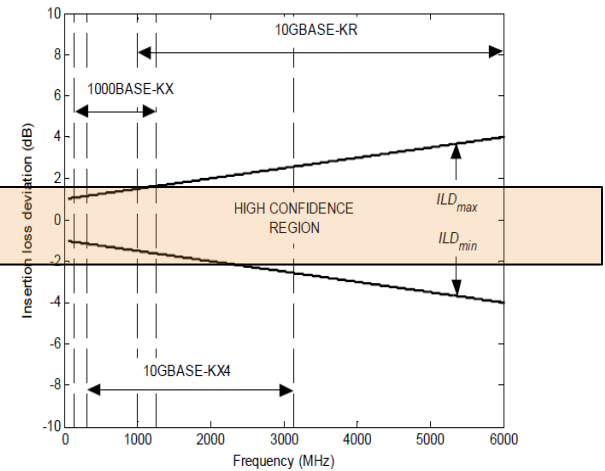


Figure 69B-6—Insertion loss deviation limits

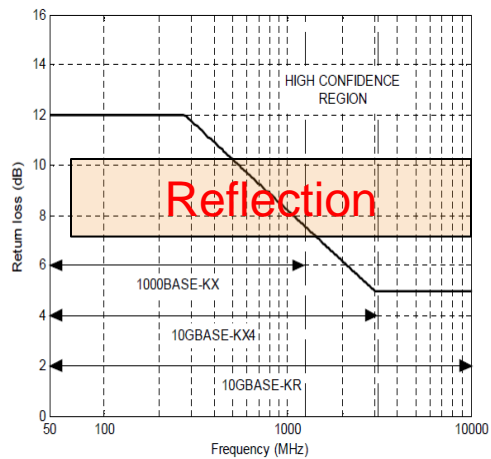


Figure 69B-7—Return loss limit

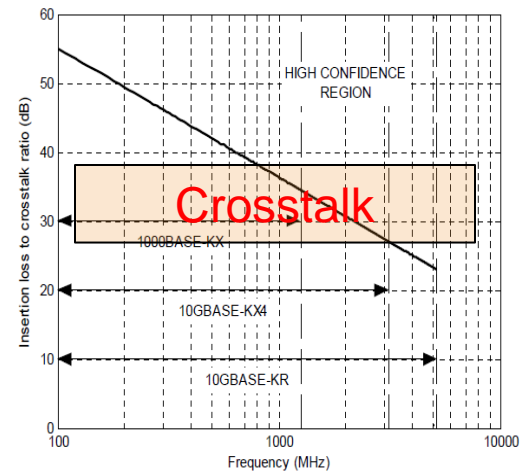


Figure 69B-8—Insertion loss to crosstalk ratio limit



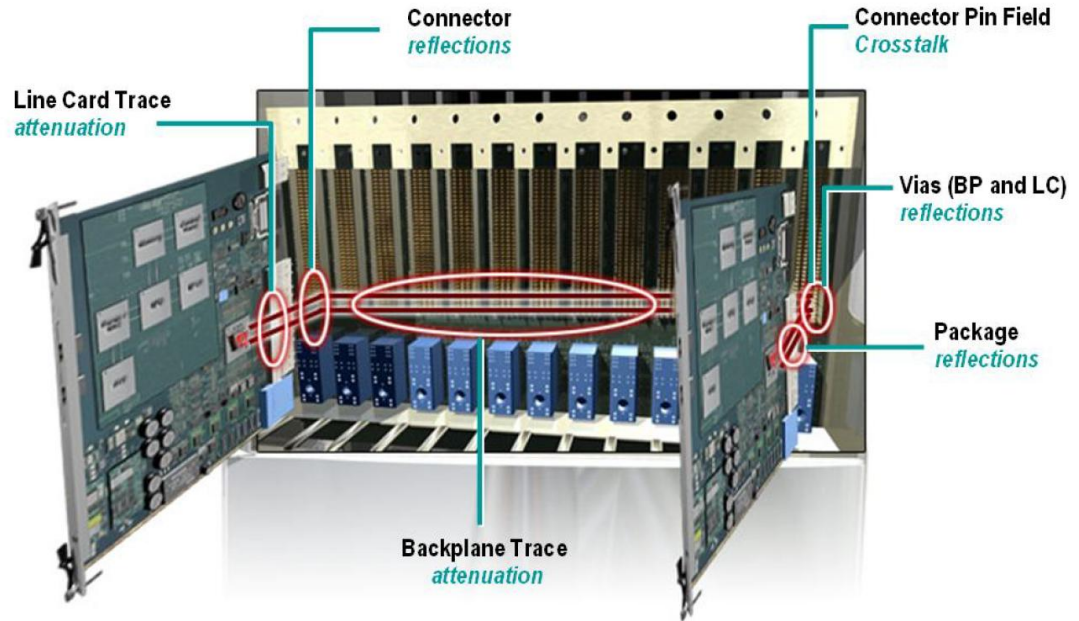
XILINX

ALL PROGRAMMABLE™

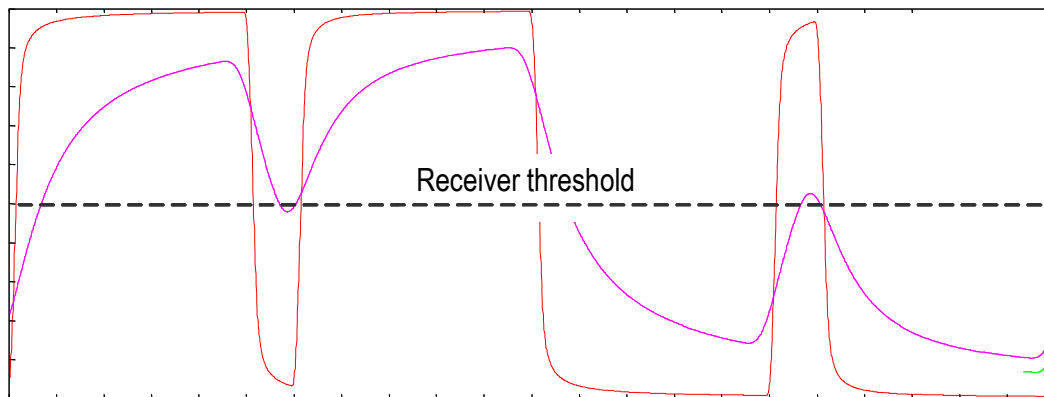
Appendix B: Equalization

The Channel – What to do about it?

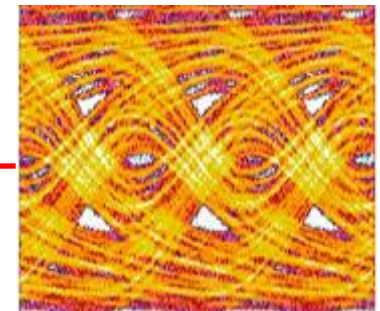
- Traditionally we worry about ISI – see below
- Today we also need to worry about reflections, noise and crosstalk



Signal amplitude at receiver



Time (1 bit per tick = 400 ps)



Received Signal (Distorted)

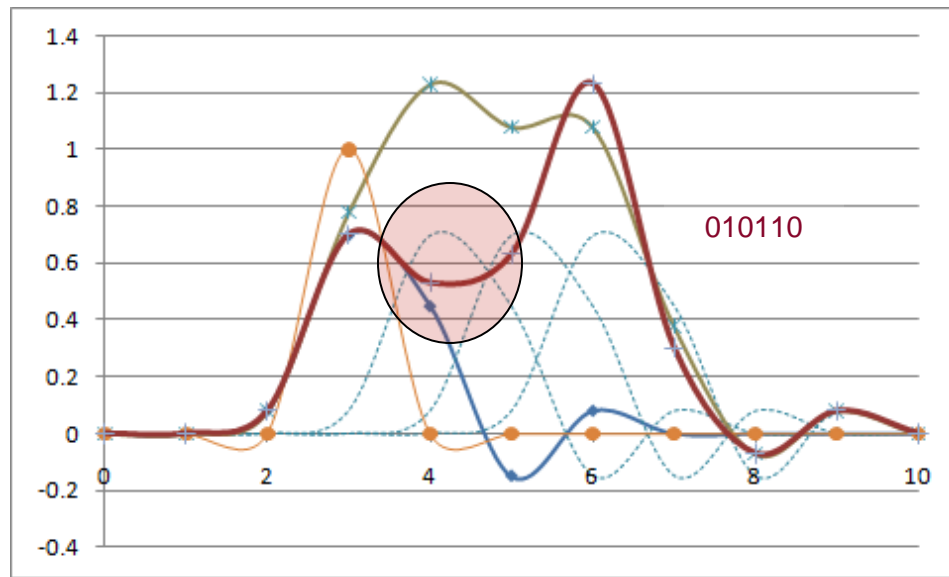
Inter-Symbol-Interference and Equalization

➤ Inter-Symbol-Interference (ISI)

- An impulse response through a channel can expand to other symbols hence impact the waveforms at other symbols

➤ Equalization - Mitigate ISI to ensure correct data sampling

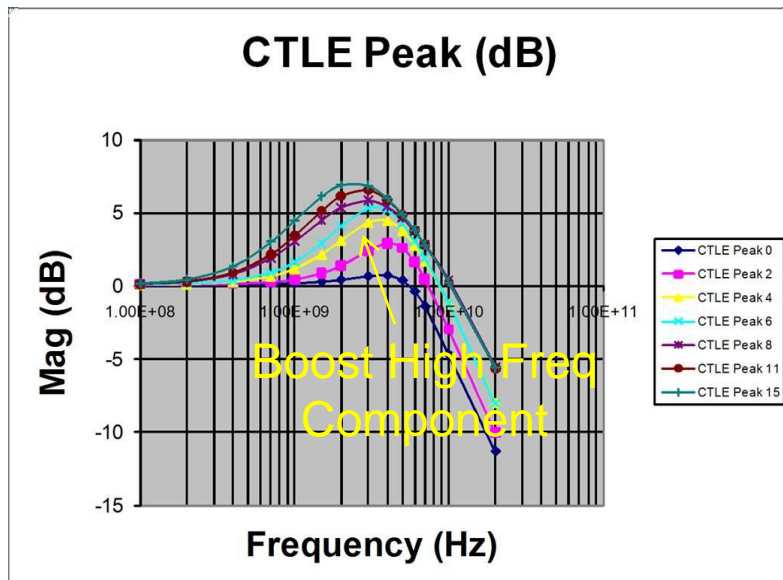
- Linear Equalization
- Non-linear Equalization



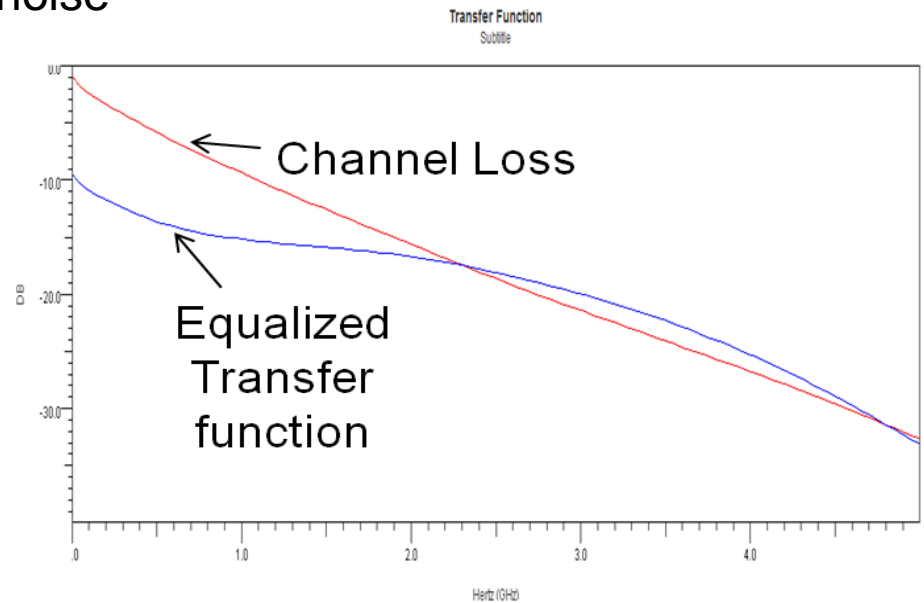
Technique #1: Linear Equalization

➤ Linear Equalization

- Transmitter: Attenuate low frequency and/or boost high frequency
- Receiver: Boost high frequency
- Compensate insertion loss
- Limitation: Boost high frequency noise

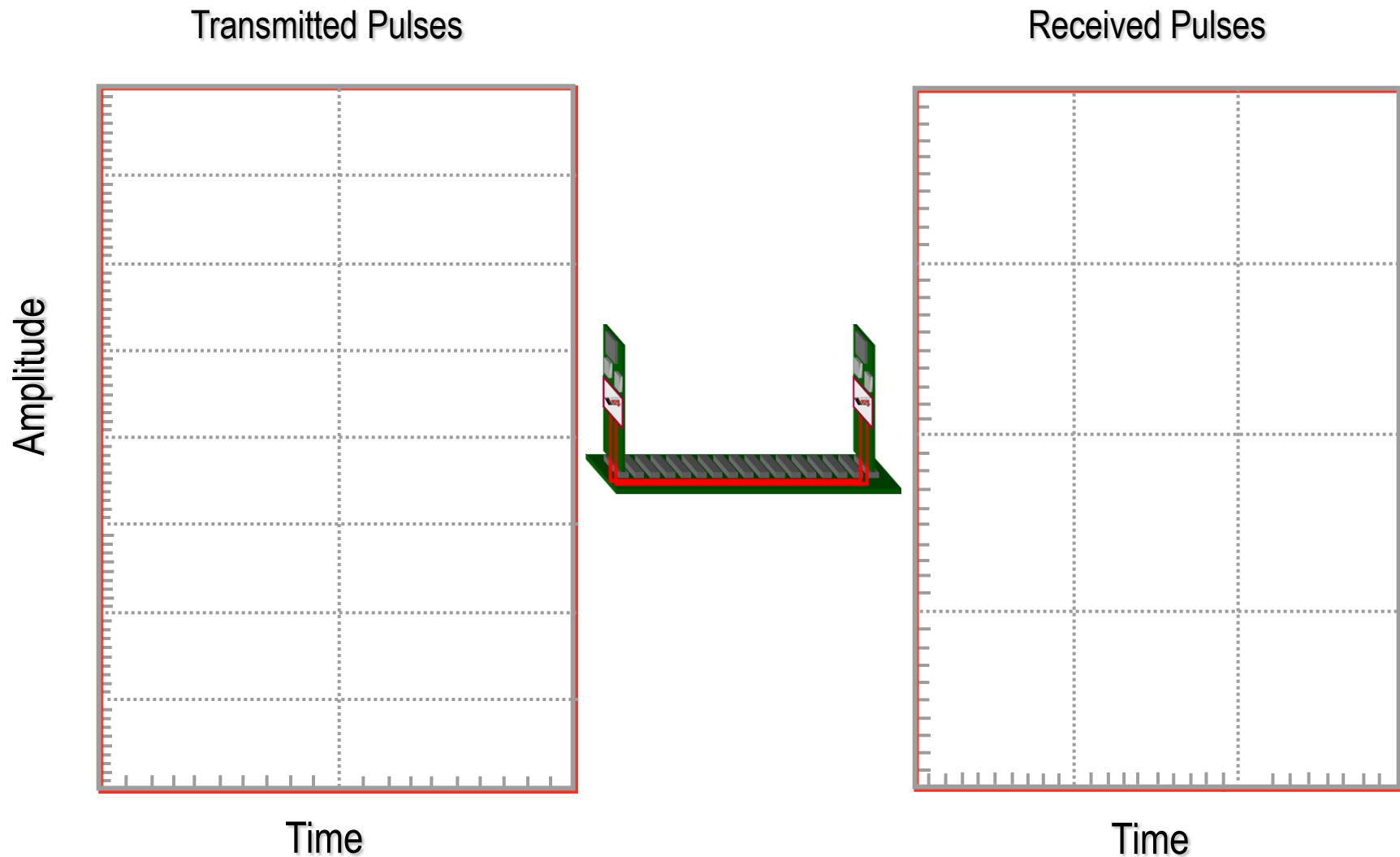


RX linear equalizer frequency response



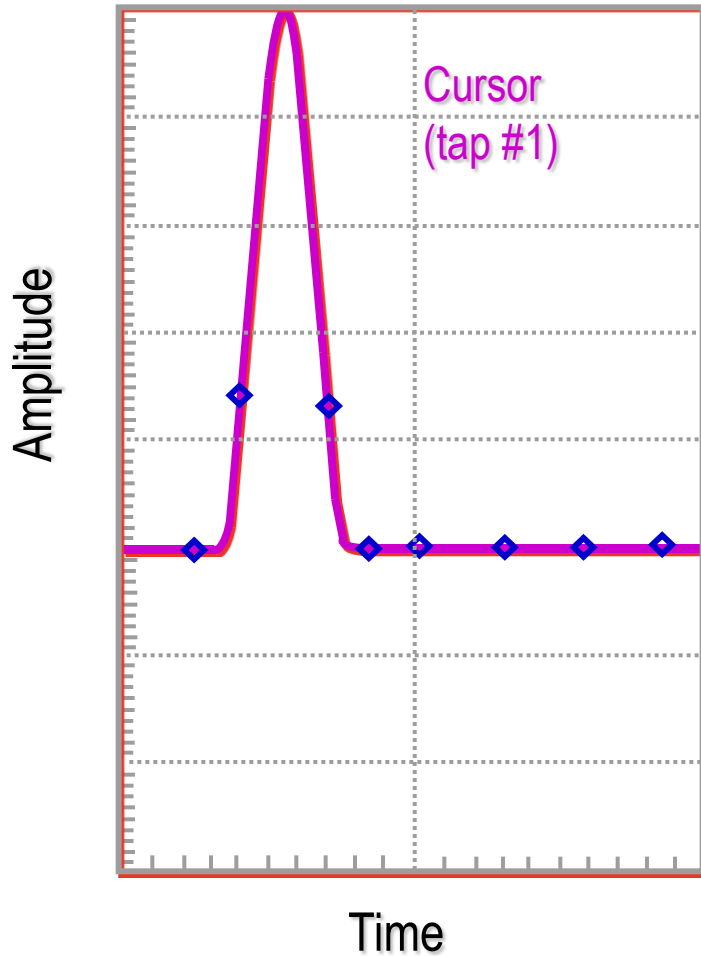
TX pre-emphasis attenuate low frequency & boost high frequency

TX Emphasis To Reduce Loss

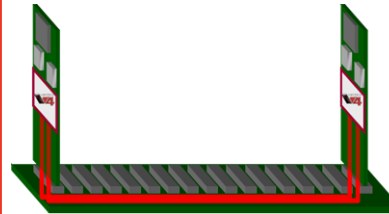
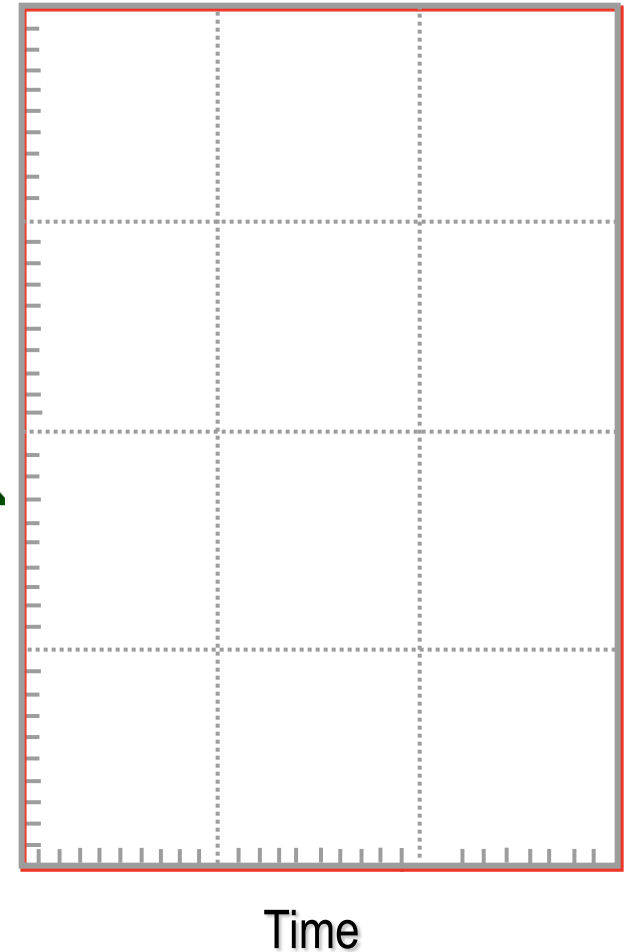


TX Emphasis To Reduce Loss

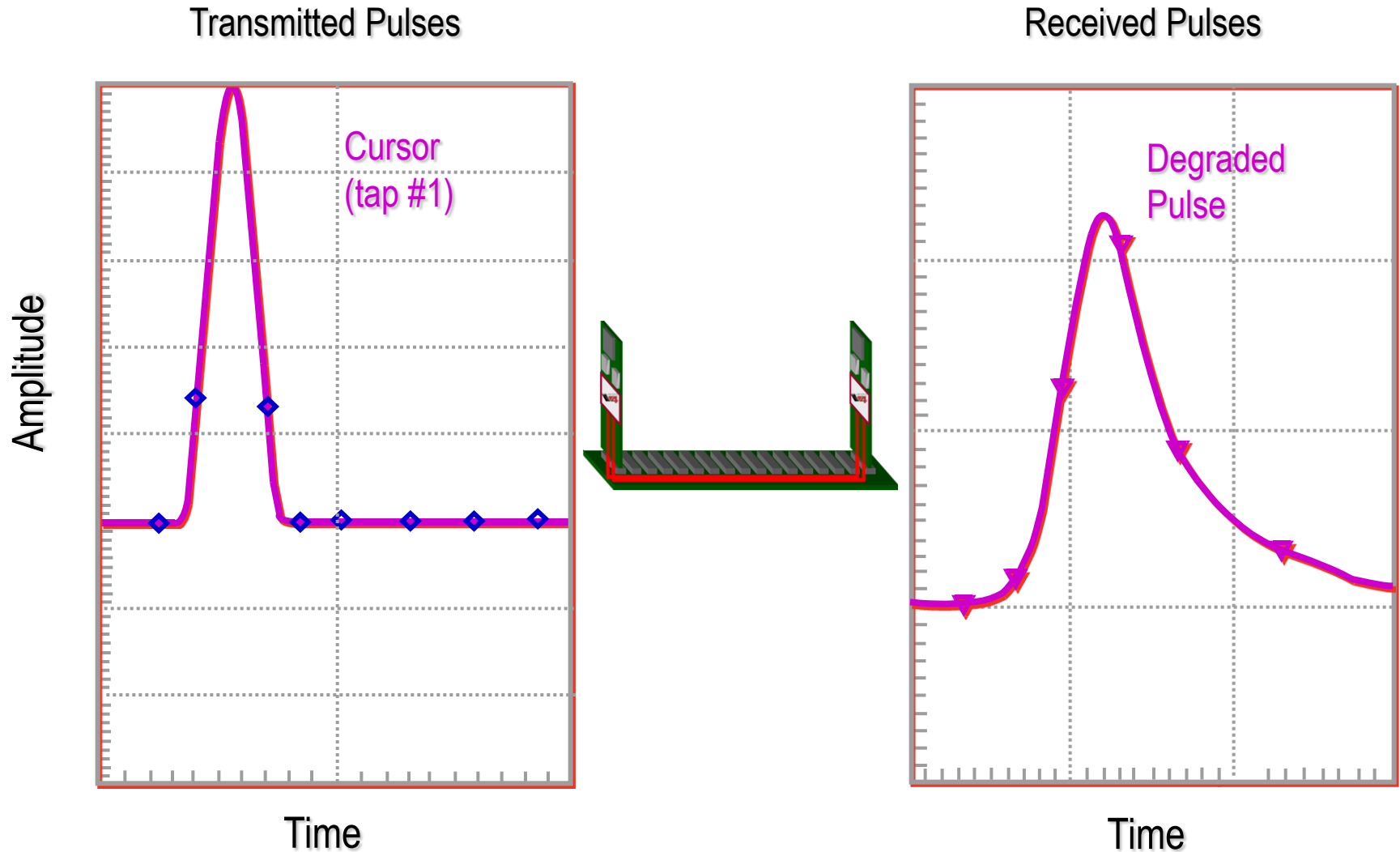
Transmitted Pulses



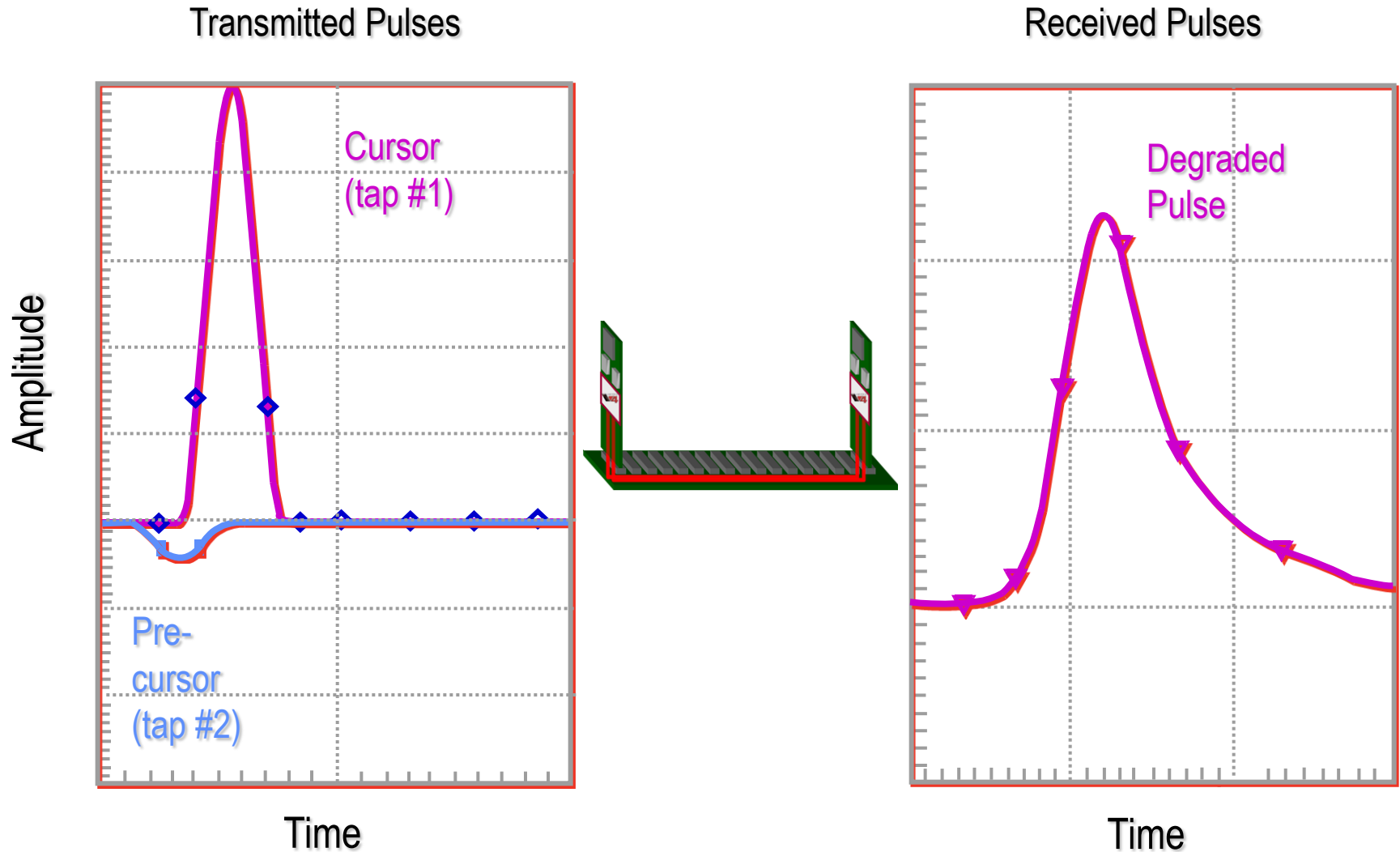
Received Pulses



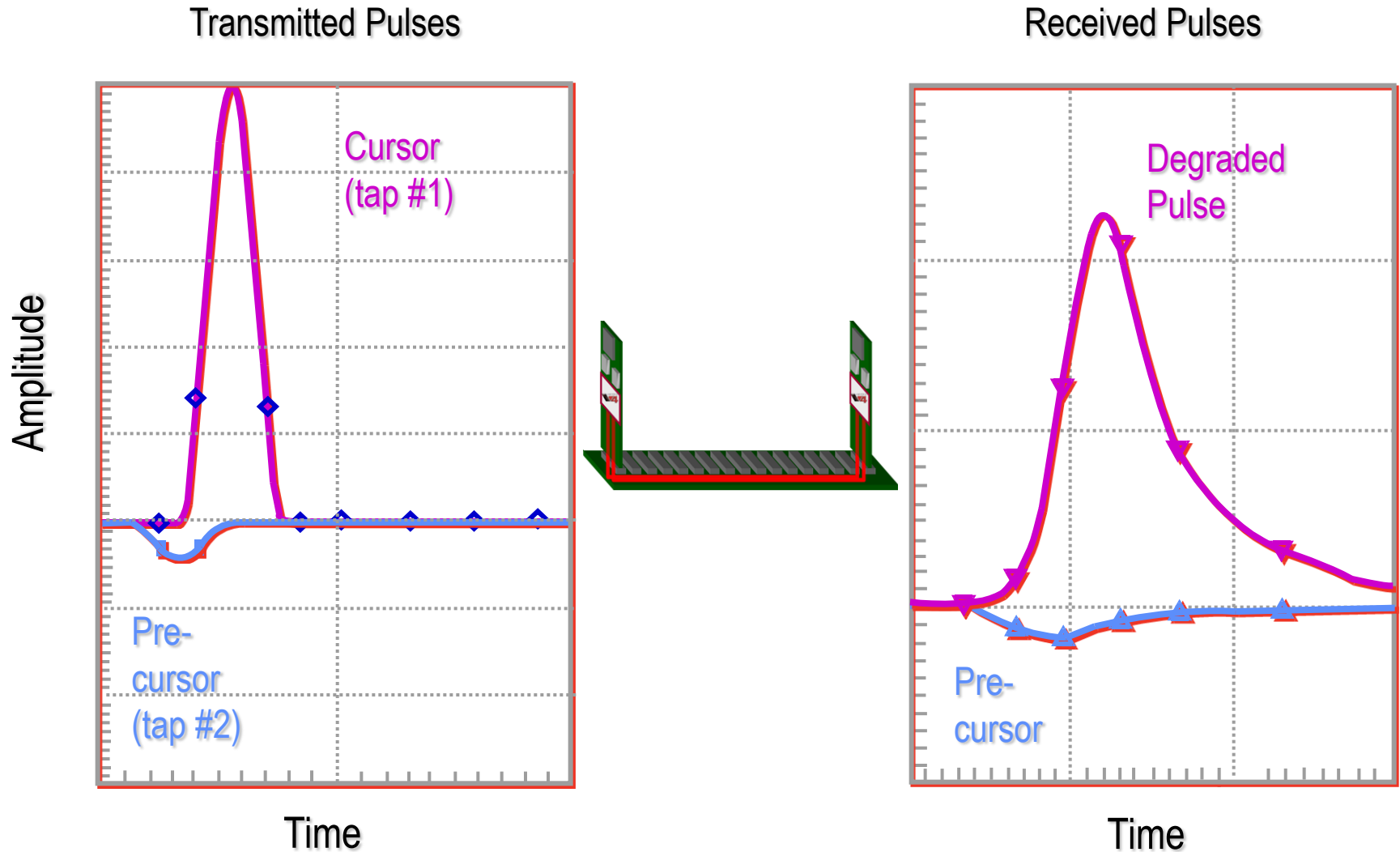
TX Emphasis To Reduce Loss



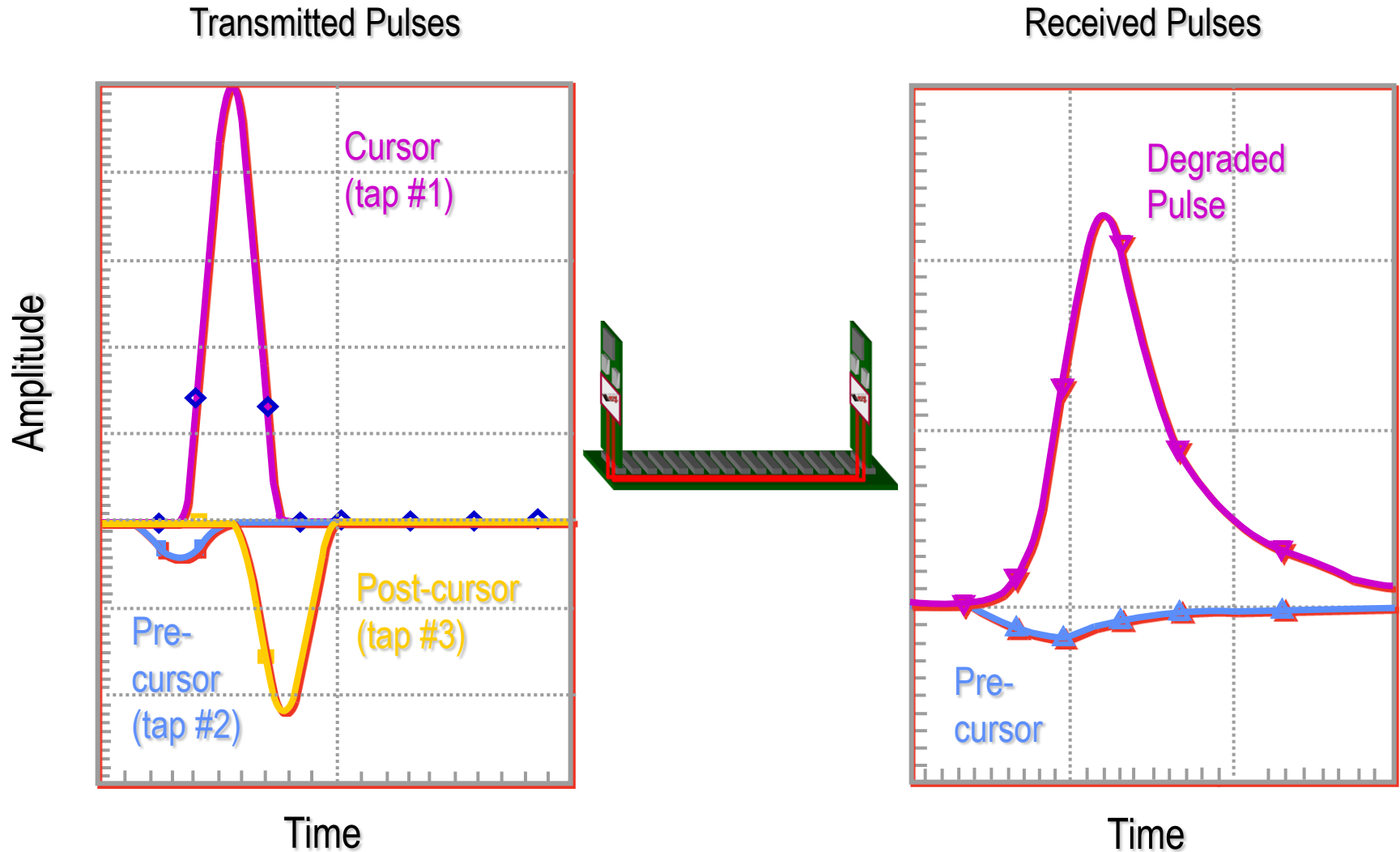
TX Emphasis To Reduce Loss



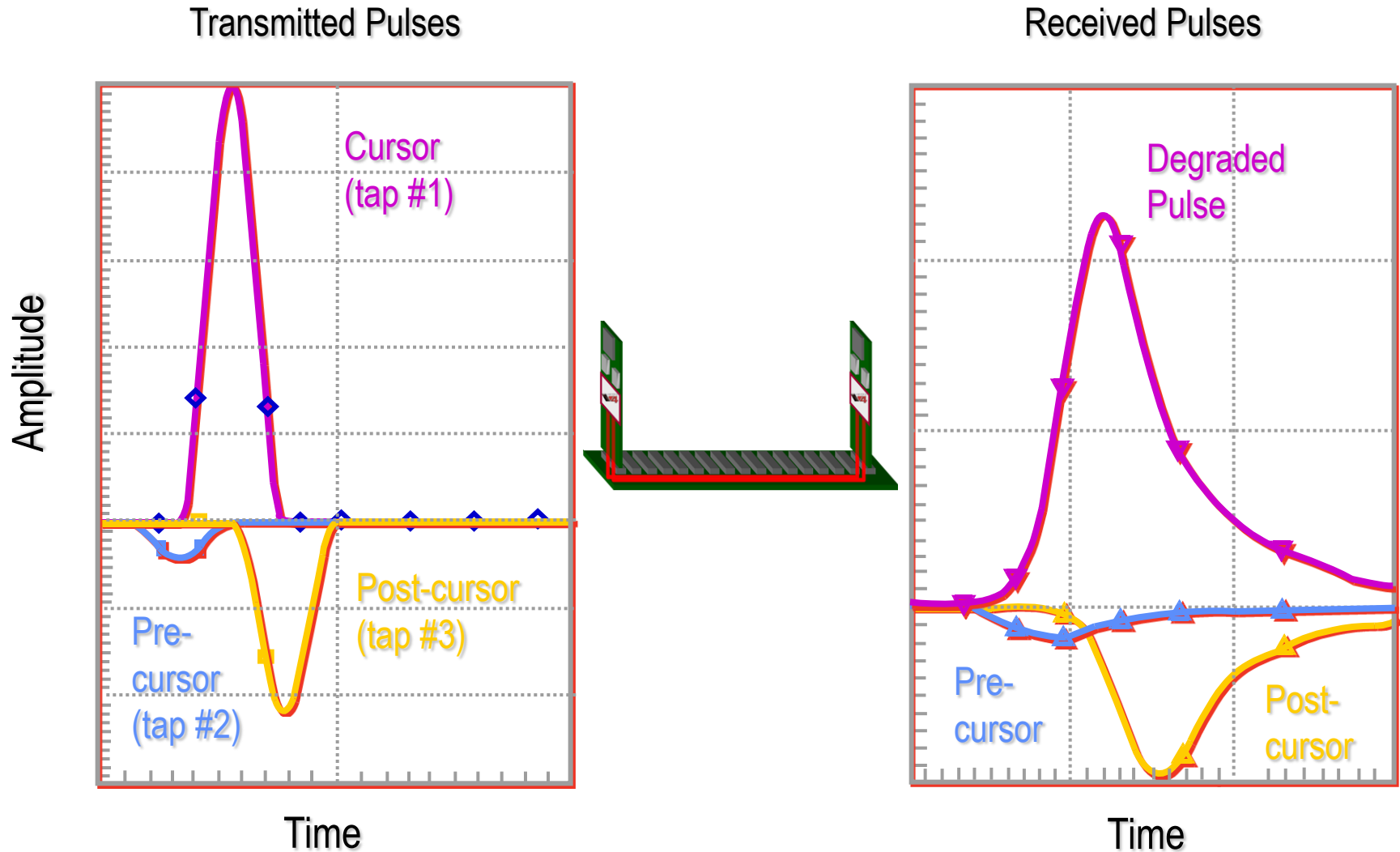
TX Emphasis To Reduce Loss



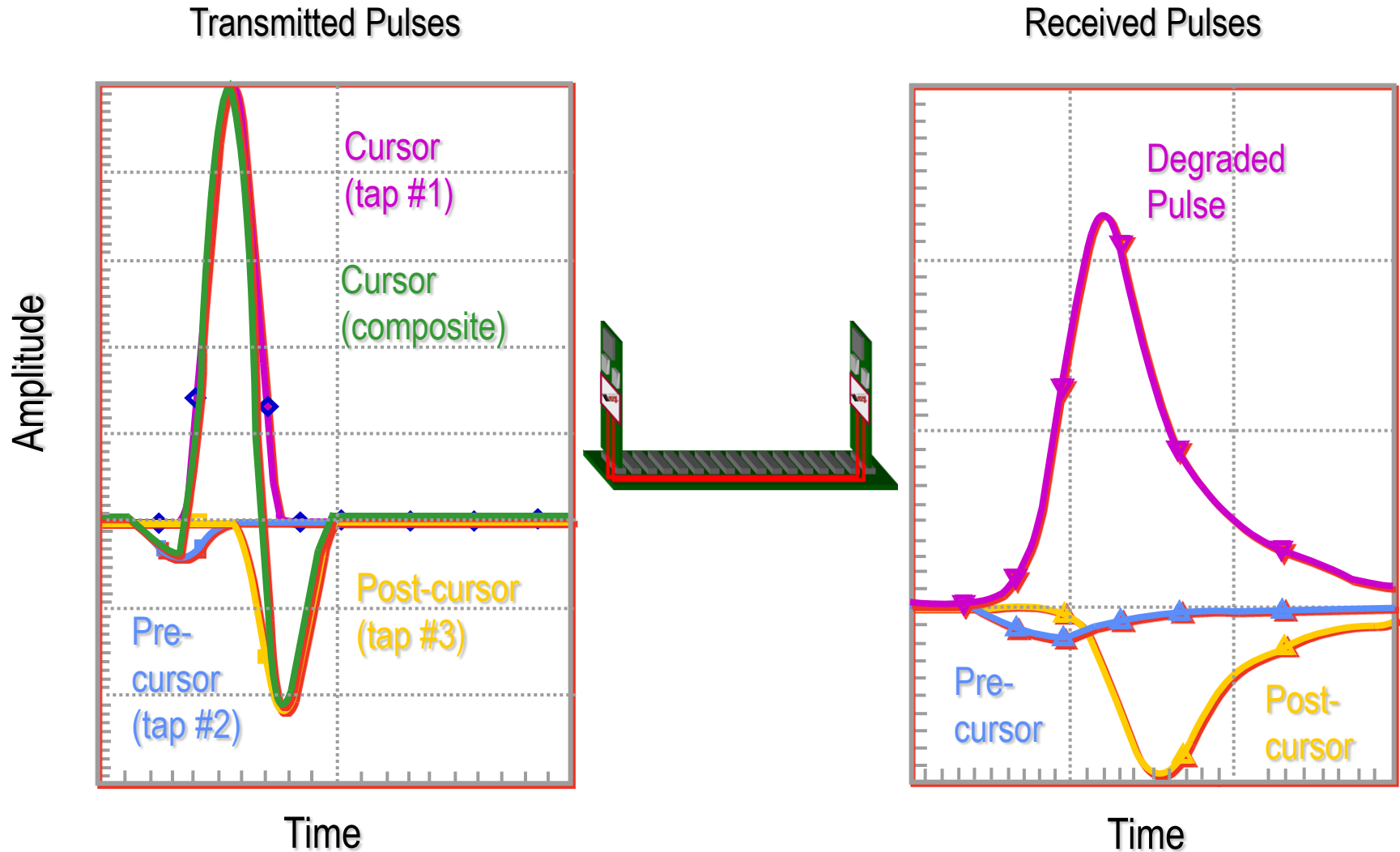
TX Emphasis To Reduce Loss



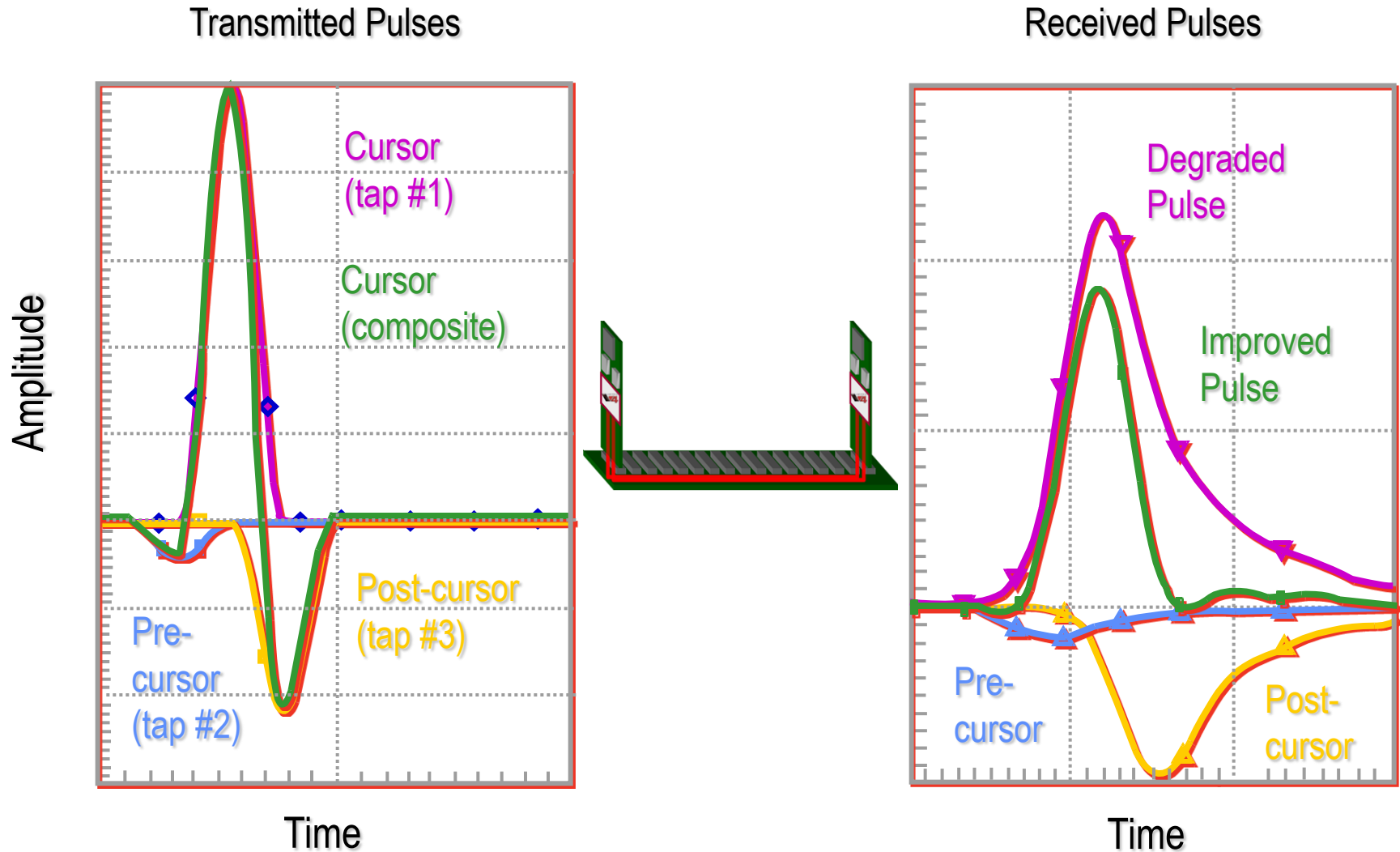
TX Emphasis To Reduce Loss



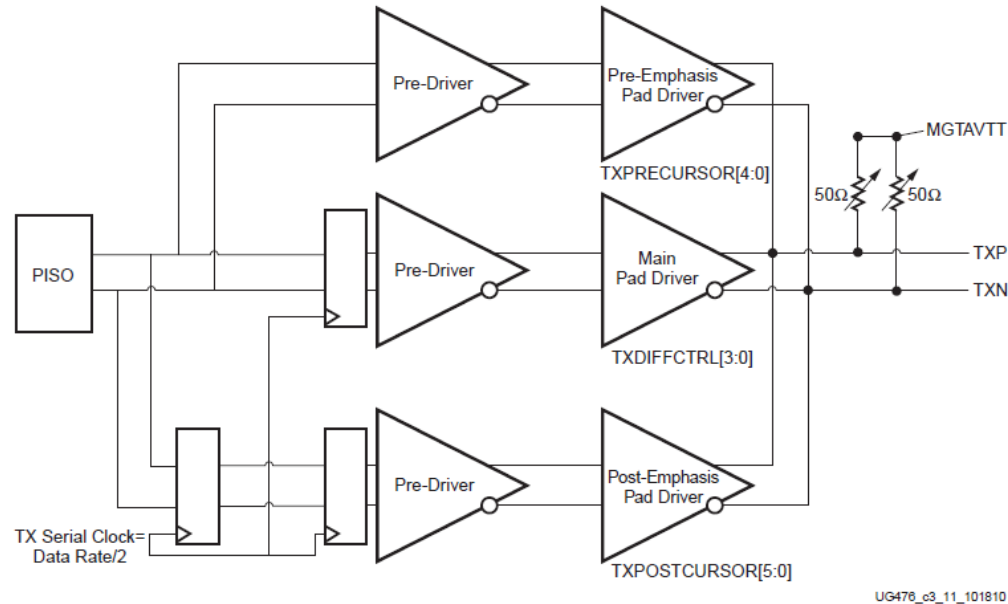
TX Emphasis To Reduce Loss



TX Emphasis To Reduce Loss



7 Series TX Driver Structure With 3 Tap Emphasis



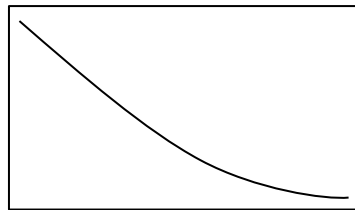
UG476_c3_11_101810

Figure 3-11: TX Configurable Driver Block Diagram

7 Series Serdes	GTP	GTX	GTH	GTZ
Main Cursor	Yes	Yes	Yes	Yes
Post Cursor De-Emphasis	Yes	Yes	Yes	NDA
Pre Cursor De-Emphasis	Yes	Yes	Yes	NDA
10G-KR Backplane TX	NA	Yes	Yes	No

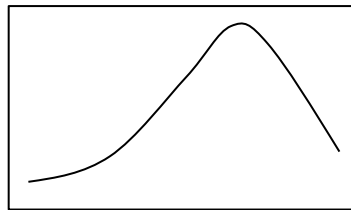
RX Linear Equalization – Loss Compensation

Channel Loss



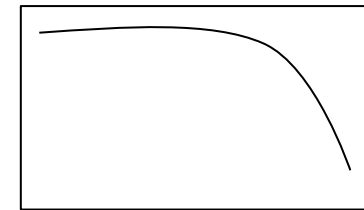
+

CTLE

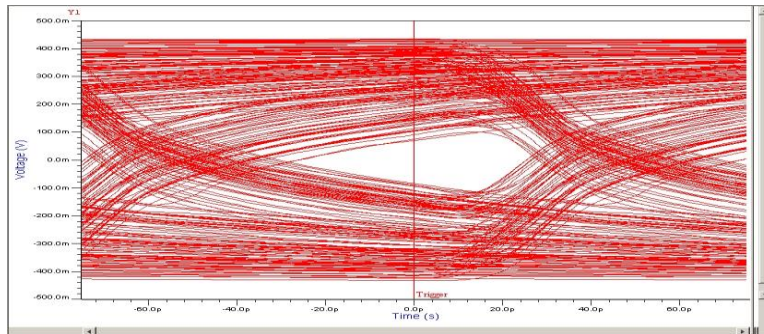


=>

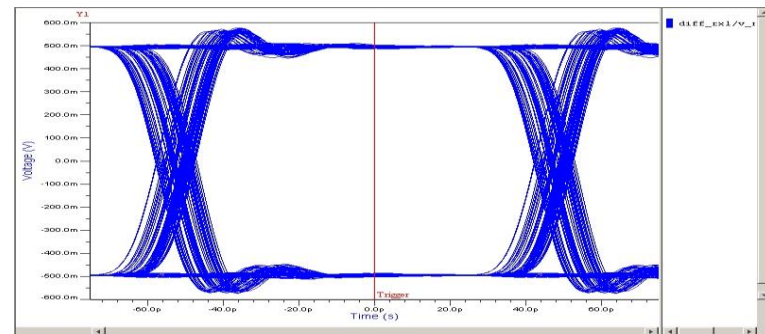
Combined Frequency response



No equalization



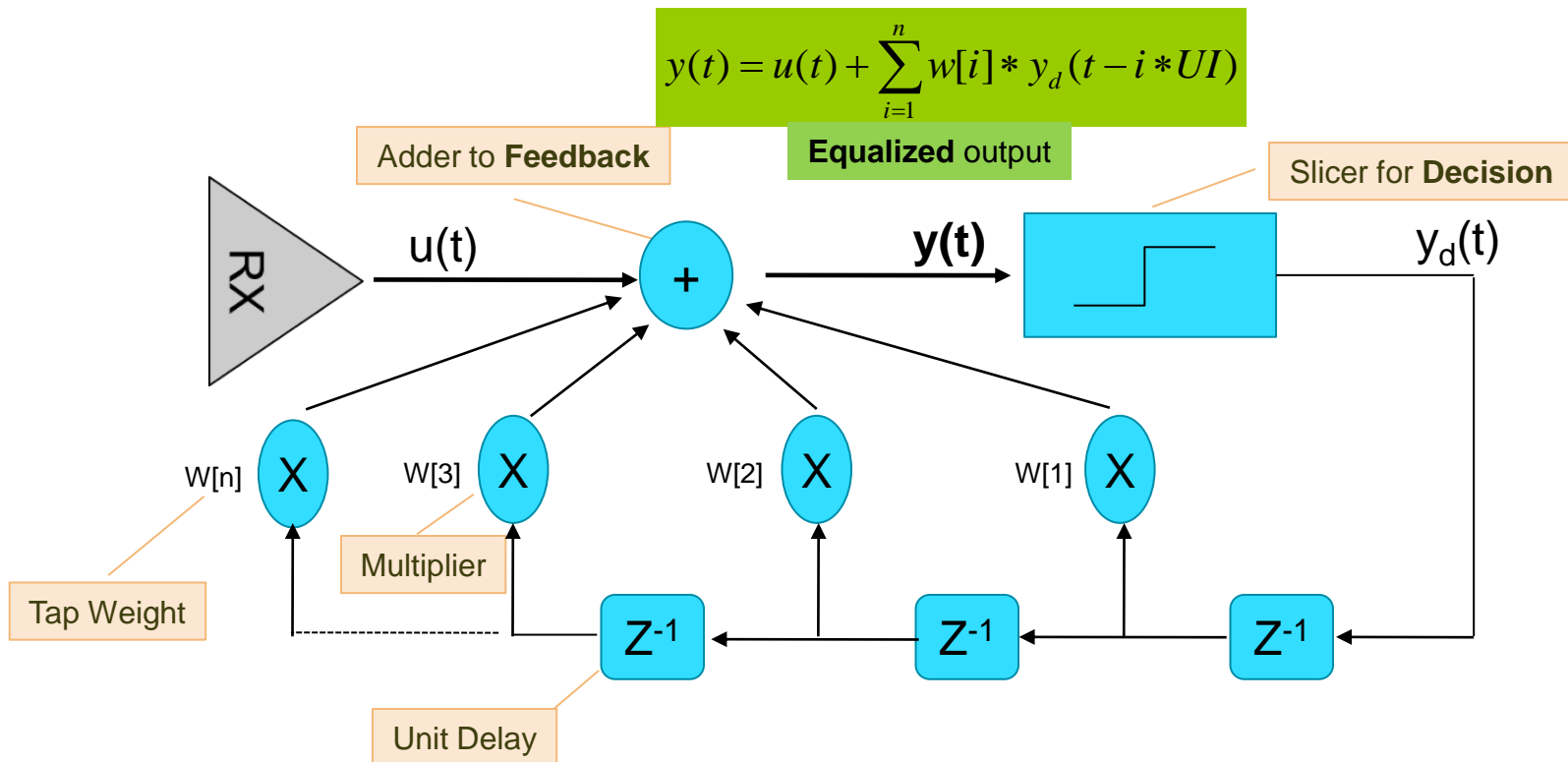
Full equalization



Technique #2: Decision Feedback Equalization

► Decision Feedback Equalization (DFE)

- A nonlinear equalizer that uses previous symbols to eliminate the Inter-Symbol-Interference (ISI) on current symbol.
 - The ISI on current symbol, caused by previous symbols, is subtracted by DFE.



DFE Challenge and Limitation

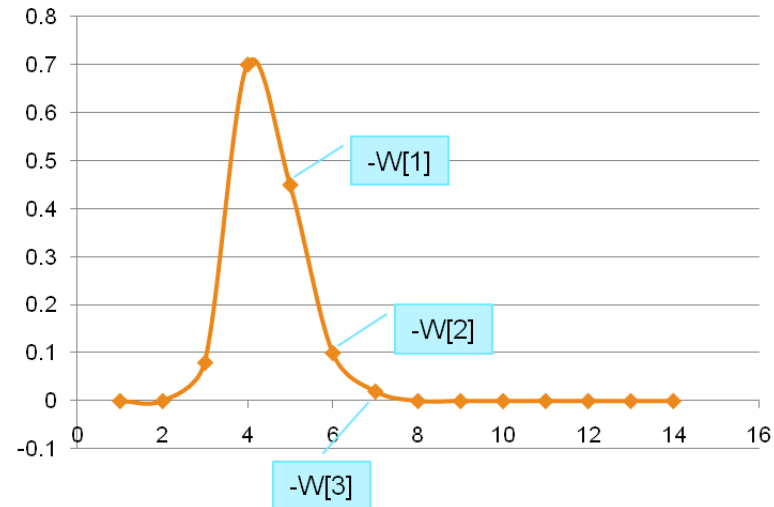
➤ Tap weight

- Ideal tap weights
- LMS Adaptation

➤ Error propagation

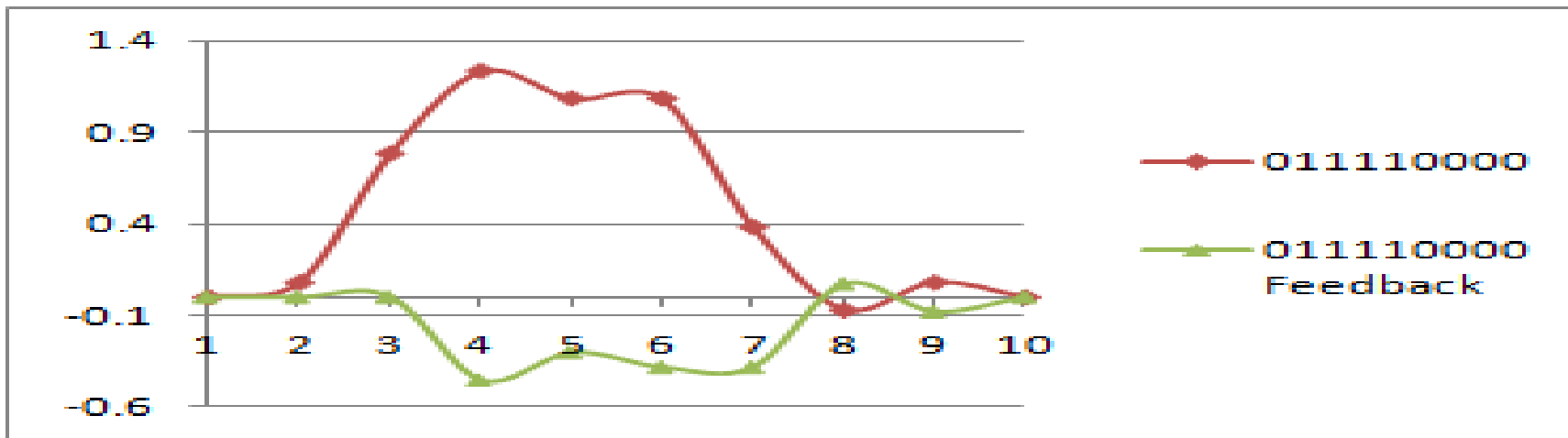
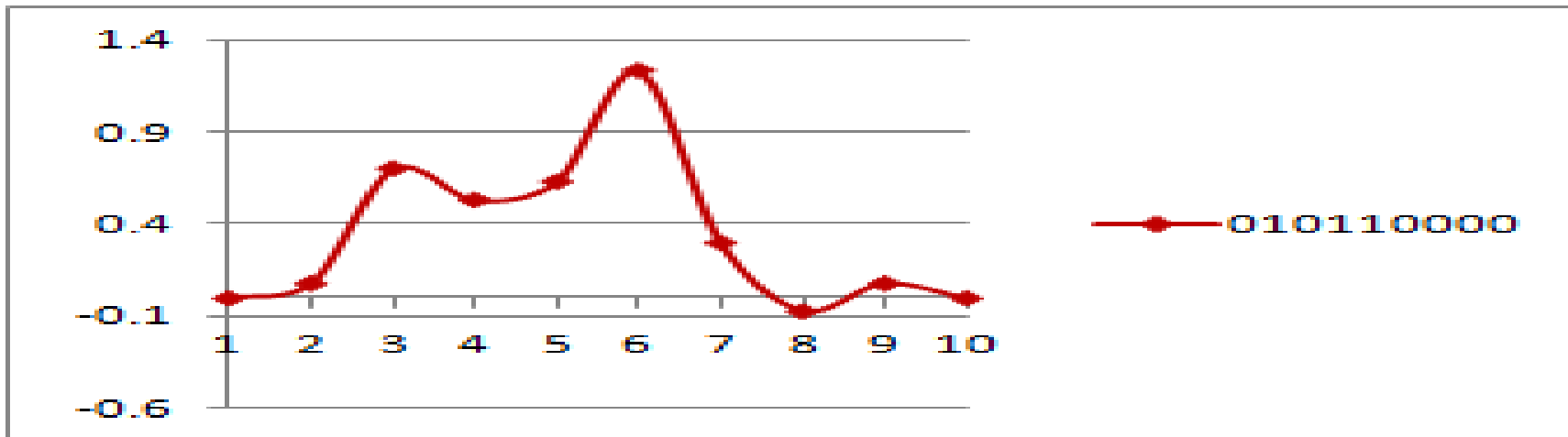
➤ Speed requirement

➤ Post Tap only



Tap weight based on ISI

DFE Effect





XILINX

ALL PROGRAMMABLE™

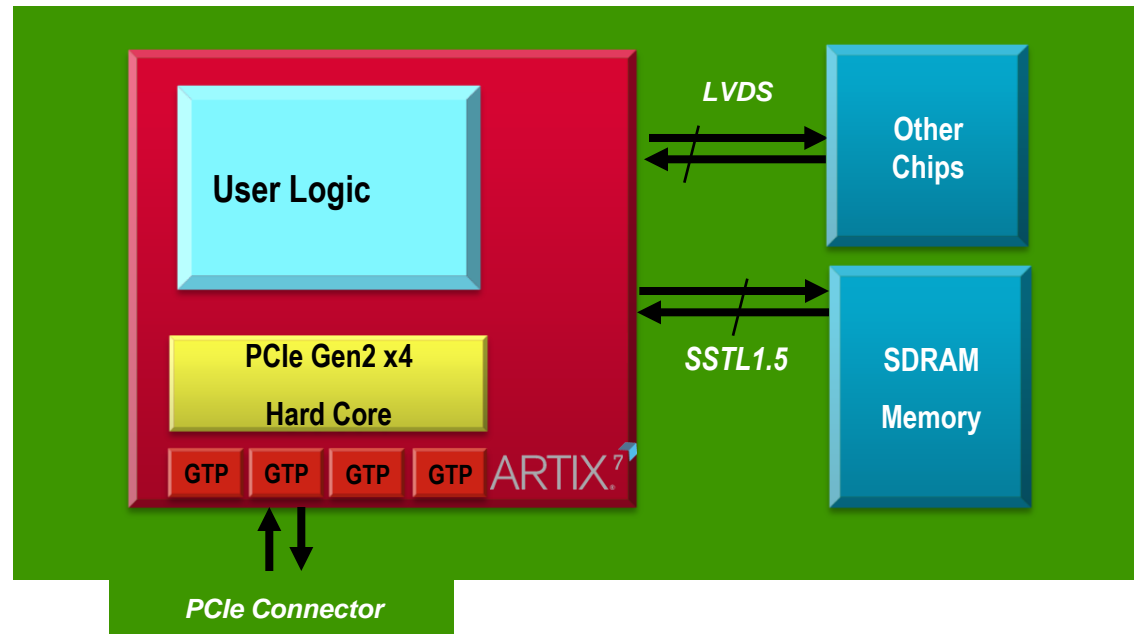
Xilinx 7 Series Transceivers Use Cases

Use Cases for 7 Series FPGAs (with Transceivers)

- **Artix-7 FPGA GTP:**
 - PCIe Gen1 plug-in card
 - Glue Logic w. PCIe
- **Kintex-7 FPGA GTX:**
 - Low-cost CPRI radiohead/base station
 - Low-cost SDI switch
 - PCIe Gen2 plug-in card
 - 40G OTU3 Muxponder
- **Virtex-7 FPGA GTX:**
 - 10G CPRI radiohead/base station
 - Cost-reduced 120G Line Card (Packet Processing)
 - Cost-reduced 120G Line Card (Traffic Management)
- **Virtex-7 FPGA GTH:**
 - 100G OTU4 Transponder with 25% overhead FEC
 - 10G-KR Backplane Switch
 - High Count SDI switch
- **Virtex-7 FPGA GTZ:**
 - 2x100G “Double Smart Gearbox”
 - 100G Line Card
 - 100G OTU4 Muxponder
 - 200G with CFP2 optics
 - 400G Single Chip

Artix-7 FPGA Use Case #1

Lowest Cost PCIe Card



➤ Lowest Cost PCIe Plug-in Card

- Up to x4 Gen2 PCIe

➤ Difference from 40nm:

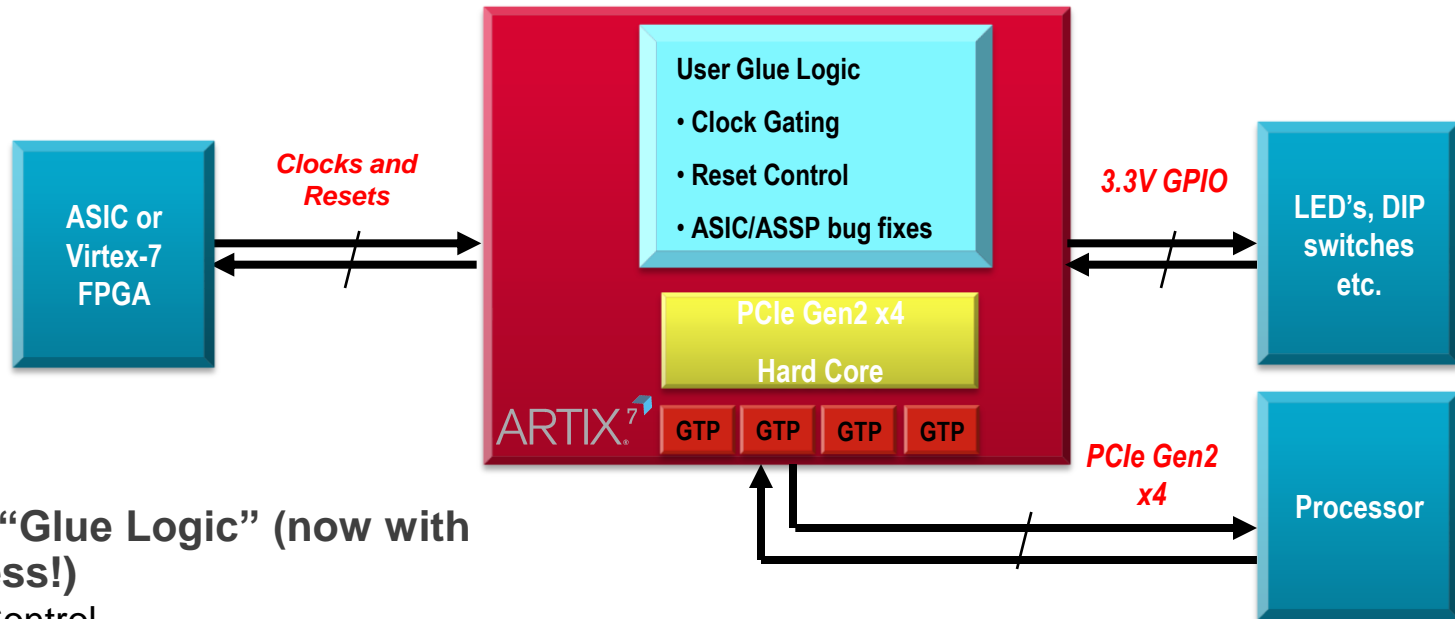
- Improved PCIe (x4)
 - Advanced PCIe features
- More Logic
- Lower Power

➤ Why?

- Lowest Cost per feature

Artix-7 FPGA Use Case #2

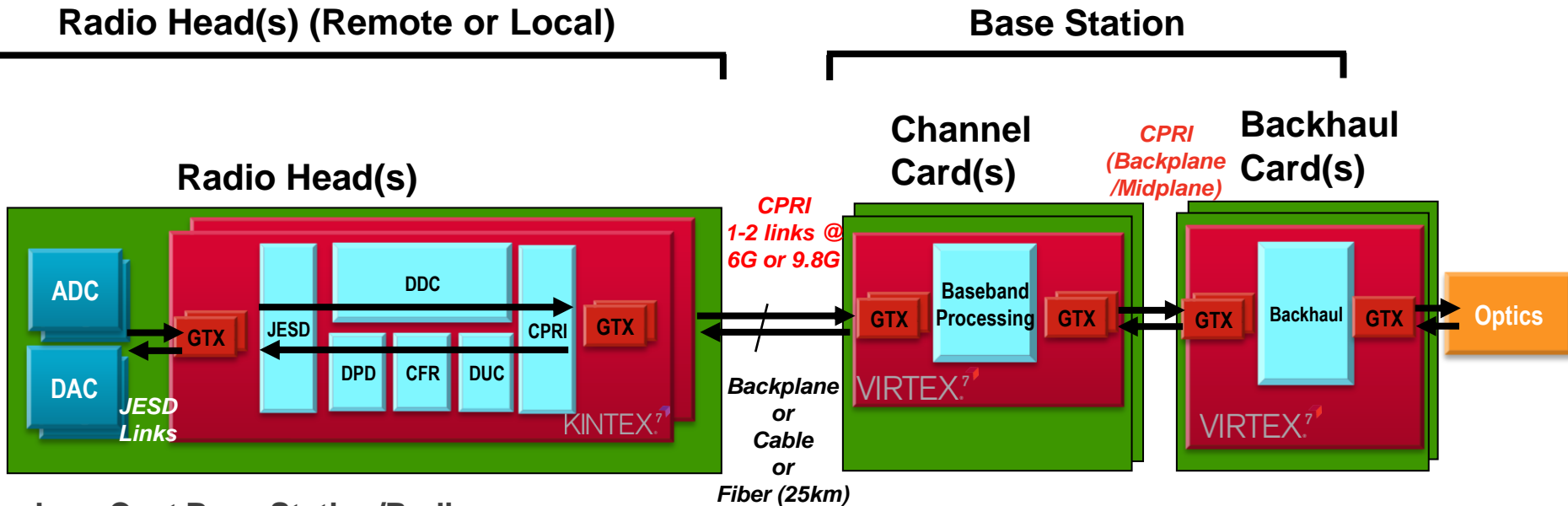
Glue Logic w. PCIe



- **Common “Glue Logic” (now with PCI Express!)**
 - Clock Control
 - Reset Control
 - ASIC/ASSP fixes
 - Misc Glue Logic
- **Difference from 40nm**
 - Cheaper
 - PCIe x4
- **Why?**
 - Historical FPGA function at lowest cost

Kintex-7 FPGA Use Case #1

Low Cost CPRI Radio Head Implementation



➤ Low-Cost Base Station/Radio Implementation

- High CPRI bandwidth
- High DSP Usage
- Low IO Usage
- Extreme Cost Pressure (very high volume)

➤ Difference from 40nm?

- Datarates rising **4x** from generation 1 to generation 2
 - Much faster than Wired Datarates
 - Surprising to all involved (inc. market leading customers)
- Extreme cost pressure (volume ramp)

➤ Why?

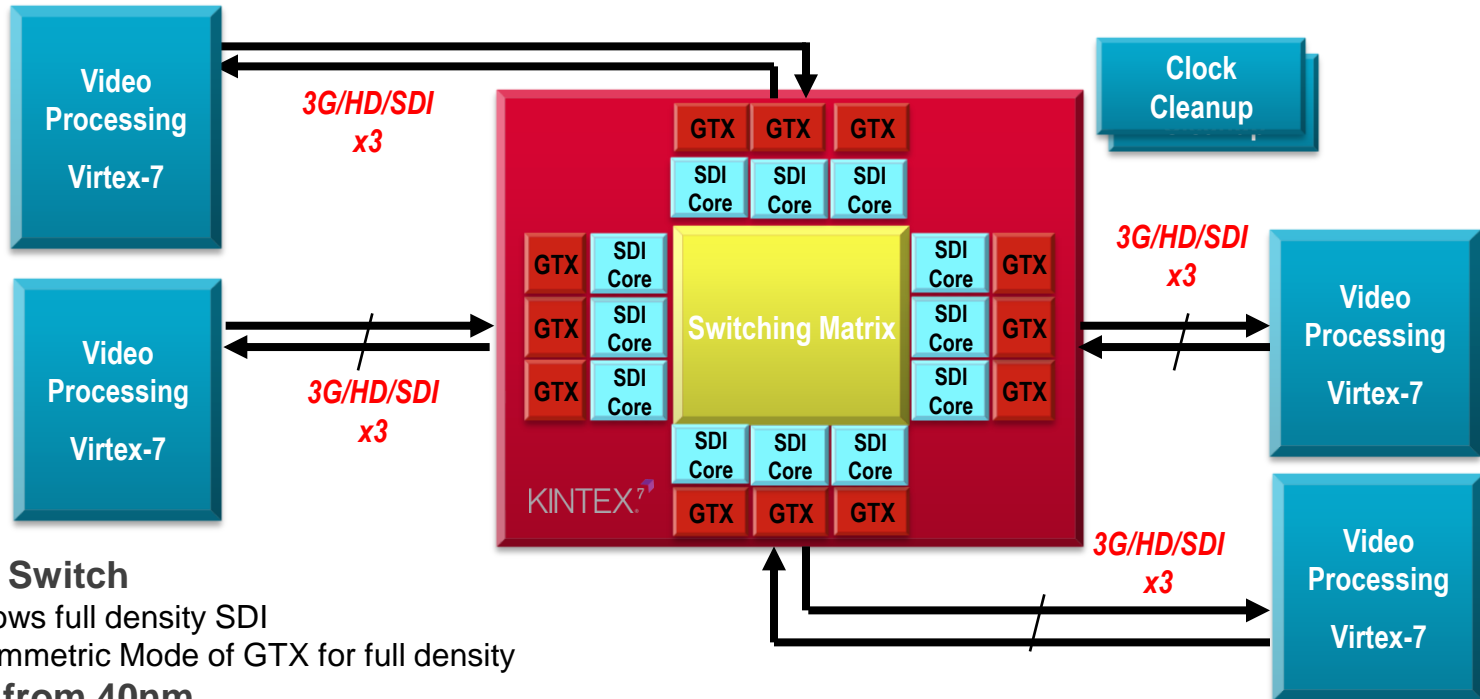
- Cell sites getting smaller due to higher datarates
- Cost pressure due to smaller cell cost points and volume

➤ Other Notes

- # cables is inflexible after installation
- Strong pressure to go faster (not wider) to get to higher datarates to prevent re-install

Kintex-7 FPGA Use Case #2

Low Cost 3G/HD/SDI Switch



➤ 3G/HD/SDI Switch

- GTX allows full density SDI
- use Asymmetric Mode of GTX for full density

➤ Difference from 40nm

- Virtex-6 LXT => Kintex-7

➤ Why?

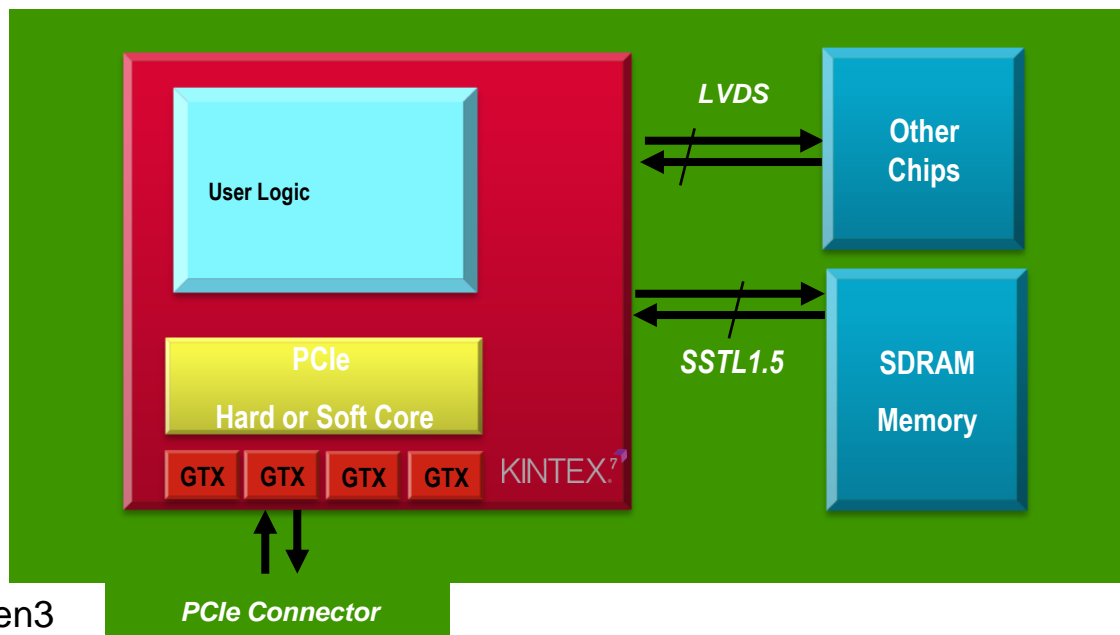
- Low cost switching
- Can add customer processing logic

➤ Note:

- Requires external clock cleanup
 - (internal clock cleanup under investigation - TBD)
 - No cleanup needed for GenLock implementations
- Internal switch implementation limited by Clock Domains

Kintex-7 FPGA Use Case #3

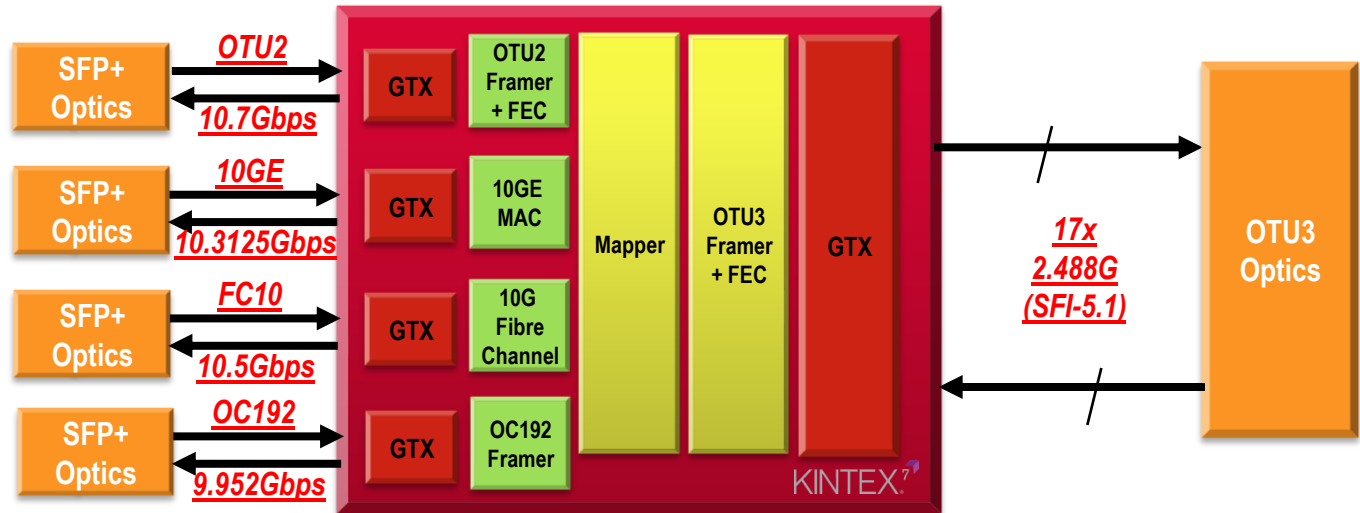
PCIe Gen3 Plug-In Card



- **Lowest Cost PCIe Plug-in Card**
 - Up to x8 Gen3 PCIe
 - Current POR requires soft core for Gen3 in Kintex/Virtex 7 T devices
- **Difference from 40nm:**
 - Improved PCIe Gen3 (x8)
 - Advanced PCIe features
 - More Logic
 - Lower cost than V6 LXT
 - Higher Performance than S6
- **Why?**
 - Allows Xilinx into the low cost Gen3 market and migration of S6 designs to higher bandwidth

Kintex-7 FPGA GTX Use Case #4

40G OTU3 Muxponder



➤ 40G OTU3 Muxponder

- Up to 480k Logic Cells for the largest EFEC implementations
- Up to 20% overhead FEC with 12.5Gbps
- Only mid-range 28nm FPGA that supports OTU speeds

➤ 4th generation Partial Reconfiguration

- 10G tributaries can be individually reconfigured without affecting traffic
- Partial Reconfiguration regions shown in green boxes

➤ Difference from 40nm

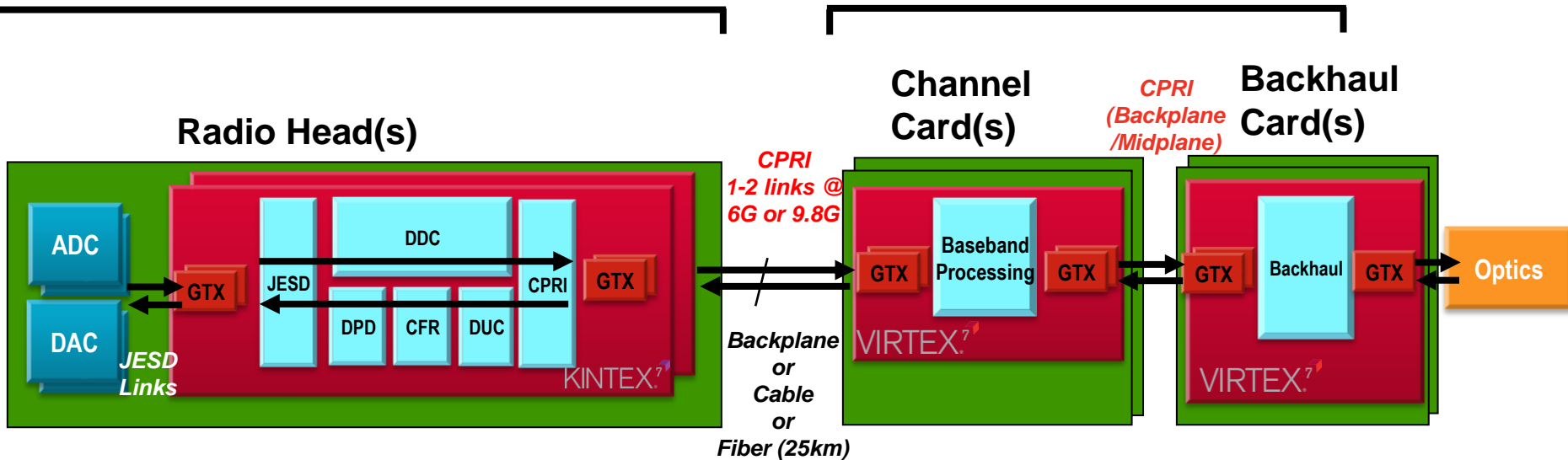
- Virtex-6HXT application supported in Kintex! (significant cost reduction)

Virtex-7 FPGA GTX Use Case #1

10G CPRI Radio Head/Base Station

Radio Head(s) (Remote or Local)

Base Station



➤ Higher Speed Base Station/Radio Implementation

- High CPRI bandwidth
- High DSP Usage
- Low IO Usage

➤ Difference from 40nm?

- Datarates rising **4x** from generation 1 to generation 2
 - Much faster than Wired Datarates
 - Surprising to all involved (inc. market leading customers)

➤ Why?

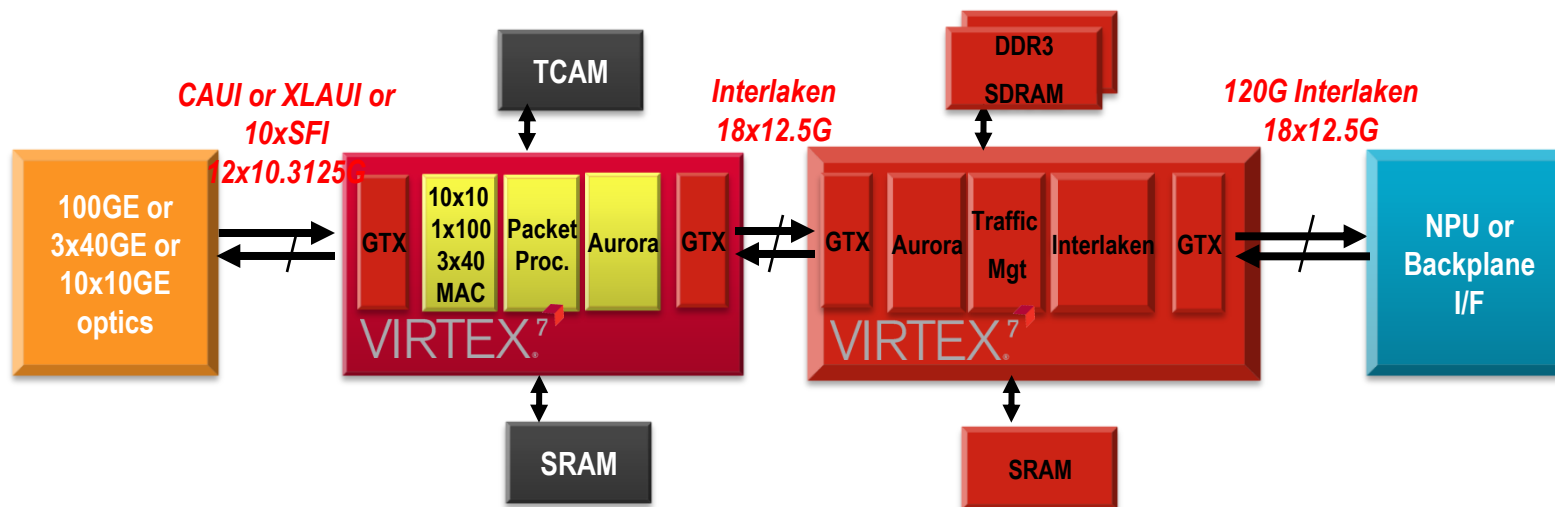
- Remote Radio heads to support smaller cells in larger monolithic base station

➤ Other Notes

- # cables is inflexible after installation
- Strong pressure to go faster (not wider) to get to higher datarates to prevent re-install

Virtex-7 FPGA GTX Use Case #2

Cost Reduced 120G Line Card (Packet Processing)



➤ 100G Packet Processing Implementation

- WRED
- Packet Tagging and Selective Drop (various algorithms)

➤ Difference from 40nm?

- Datarates rising from previous generations

➤ Why?

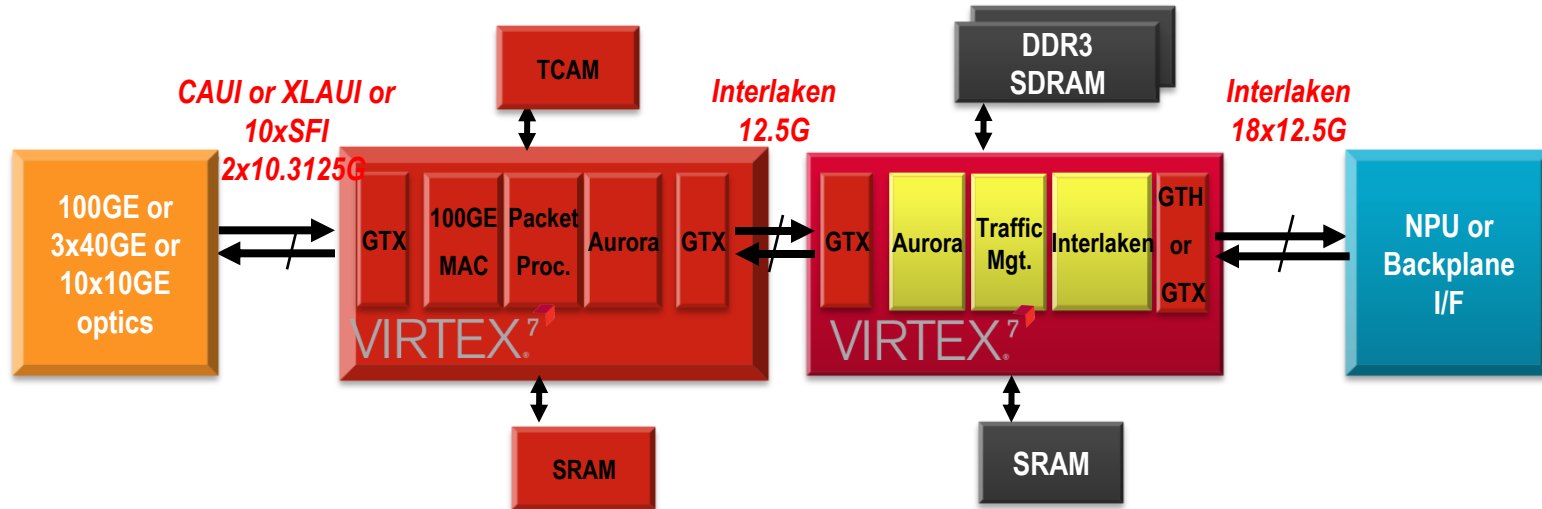
- 100G becomes mainstream in 7 series timeframe
- Increasing need for advanced packet processing

➤ Other Notes

- Trie-based CAM architecture possible with external RAM

Virtex-7 FPGA GTX Use Case #3

Cost Reduced 120G Line Card (Traffic Management)



➤ Industry trend and requirement

- 100G has become mainstream in 7 series timeframe
- Increasing need for granular traffic management

➤ 100G Traffic Management Implementation

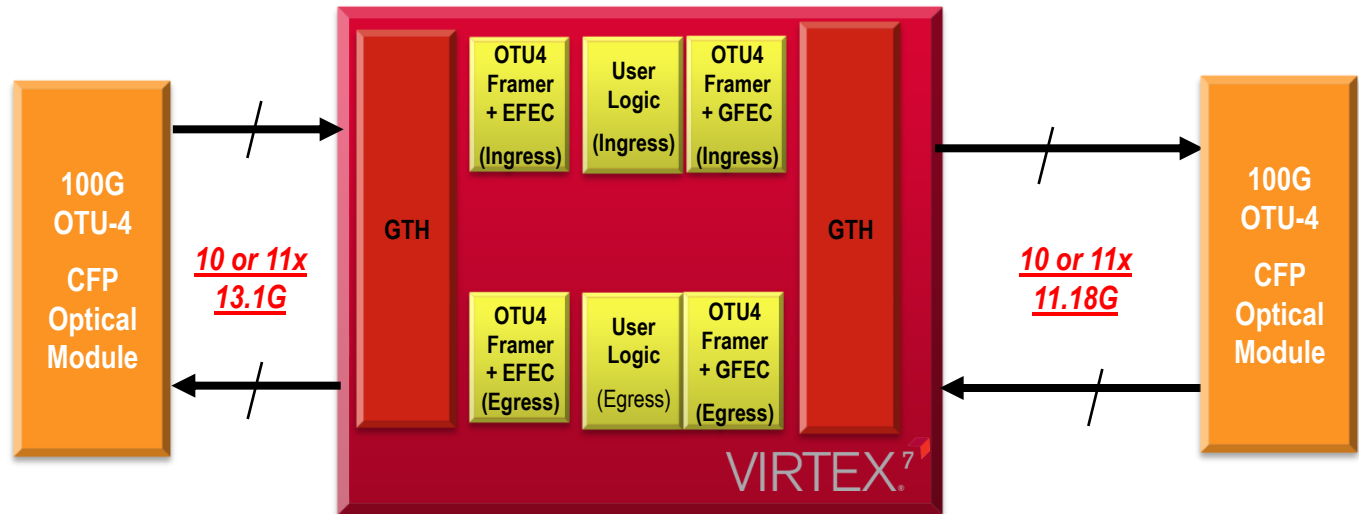
- 400Gbps of packet buffering bandwidth to external DDR3 SDRAM to support unidirectional 100G stream

➤ Difference from 40nm

- 1866Mbps DDR3 SDRAM interface allows lower power implementation
- Data rates rising from previous generations

Virtex-7 FPGA GTH Use Case #1

100G OTU4 Transponder



➤ 100G OTU4 Transponder

- Up to 870k Logic Cells for the largest EFEC implementations
- Up to 25% overhead FEC with 13.1Gbps
- Over 40% larger than competition 28nm FPGAs

➤ 100G Muxponder

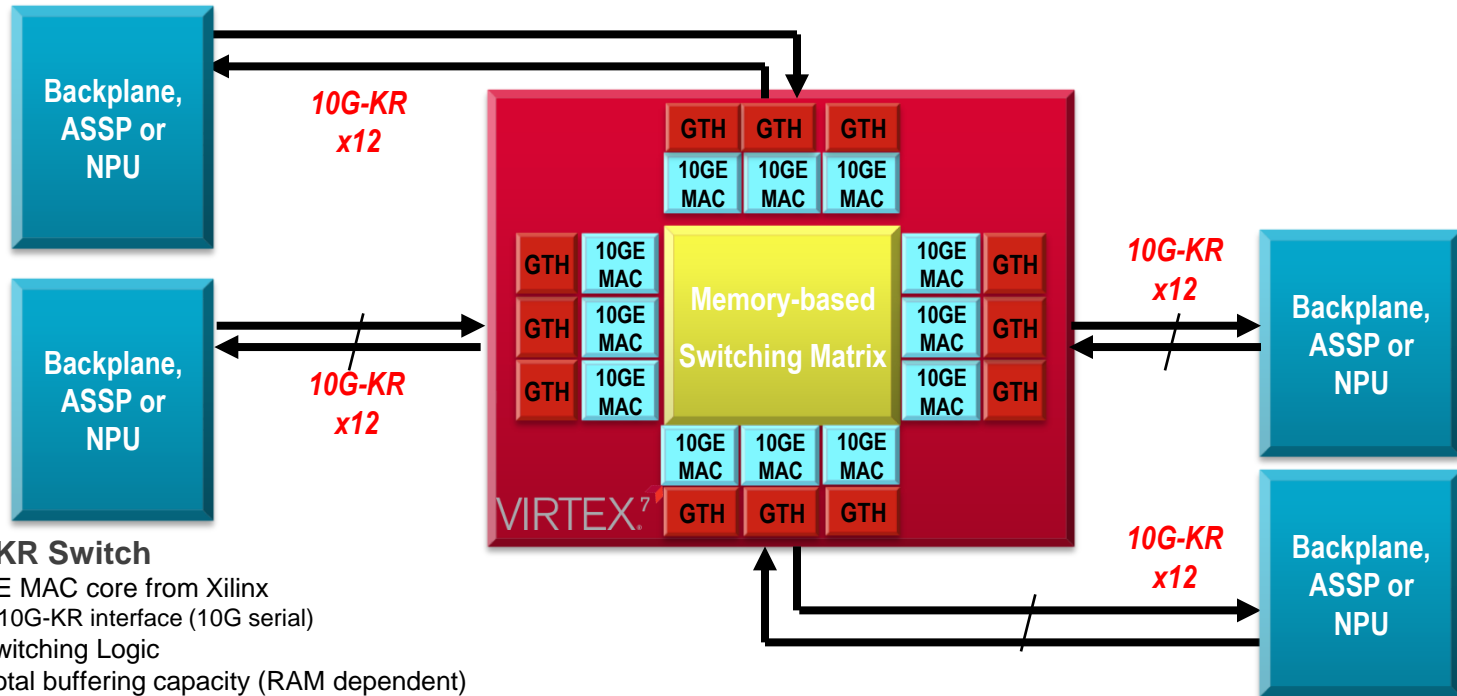
- 10x10G independent tributary to 1x100G trunk muxponder also possible in 7VX485T and above

➤ Difference from 40nm

- Higher overhead – to 13.1Gbps @ 25% FEC

Virtex-7 FPGA GTH Use Case #2

10G-KR Backplane Switch



➤ 48 Port 10G-KR Switch

- Uses 10GE MAC core from Xilinx
 - 10G-KR interface (10G serial)
- Custom Switching Logic
- 150us of total buffering capacity (RAM dependent)
- Buffering : 2x 36k BRAM = 1 jumbo frame
- Optional Features
 - External buffering via DDR3 SDRAM or RLDRAM3 (requires larger package)
 - Traffic Management (see later slides for details)
 - Embedded IEEE1588
 - Ethernet AVB

➤ Differences from 40nm

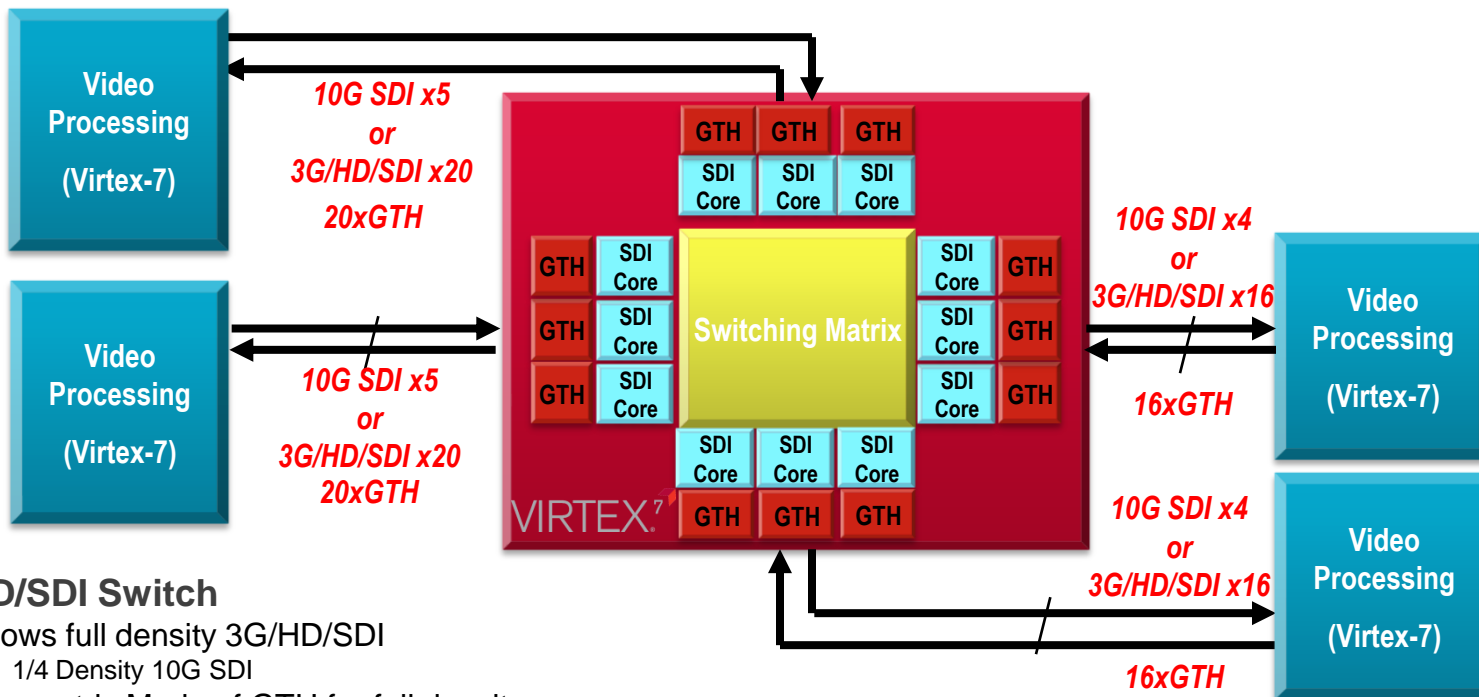
- 48 ports vs. 24 ports in V6
- (possibly larger if more thermal envelope is possible)

➤ Notes:

- Thermal envelope must be tracked carefully

Virtex-7 FPGA GTH Use Case #3

High Density SDI Switch



➤ 10G/3G/HD/SDI Switch

- GTH allows full density 3G/HD/SDI
 - 1/4 Density 10G SDI
- use Asymmetric Mode of GTH for full density

➤ Difference from 40nm

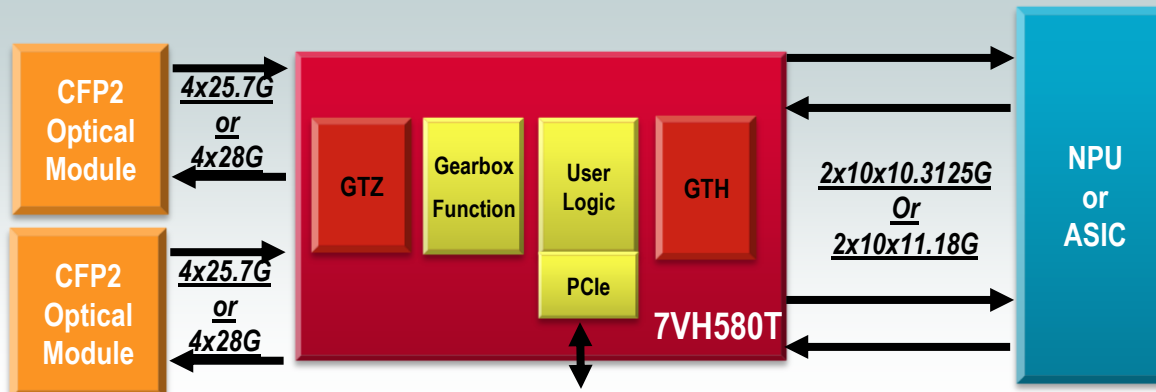
- Size Matters
- 10G SDI Support

➤ Note:

- Requires external clock cleanup
 - (internal clock cleanup under investigation - TBD)
 - No cleanup needed for GenLock implementations
- Internal switch implementation limited by Clock Domains

Virtex-7HT GTZ Use Case #1

2x100G “Double Smart Gearbox”

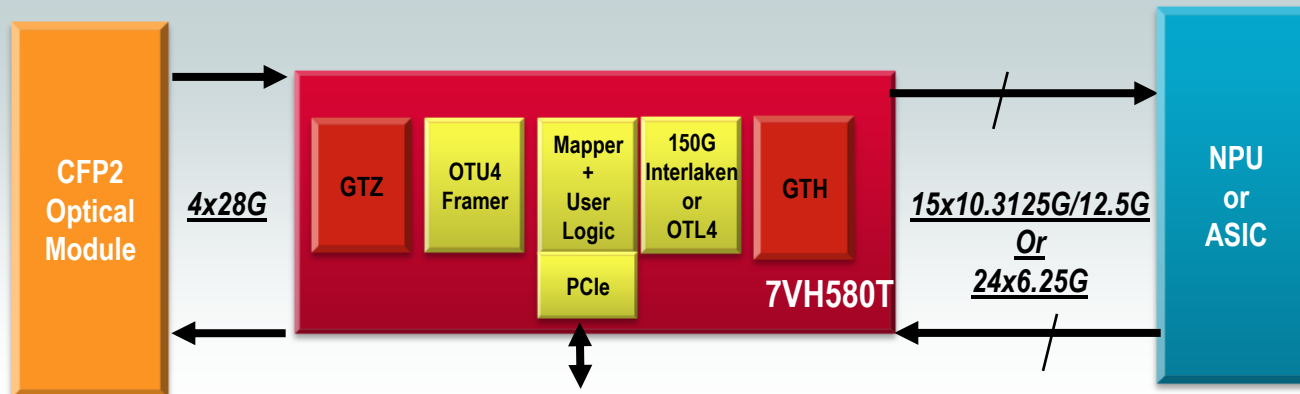


- Allows reuse of legacy ASIC or NPU with new CFP2 optics
- Allows additional functionality in user logic
- Supports 100GE (CAUI), OTU4 (SFI-S or OTL4.10) or custom protocol (e.g. MLD @ 20x5.15G) on system side

Simple Gearbox Function – Achievable Cost-effectively with Virtex-7HT

Virtex-7HT GTZ Use Case #2

100G OTU4 Line Card

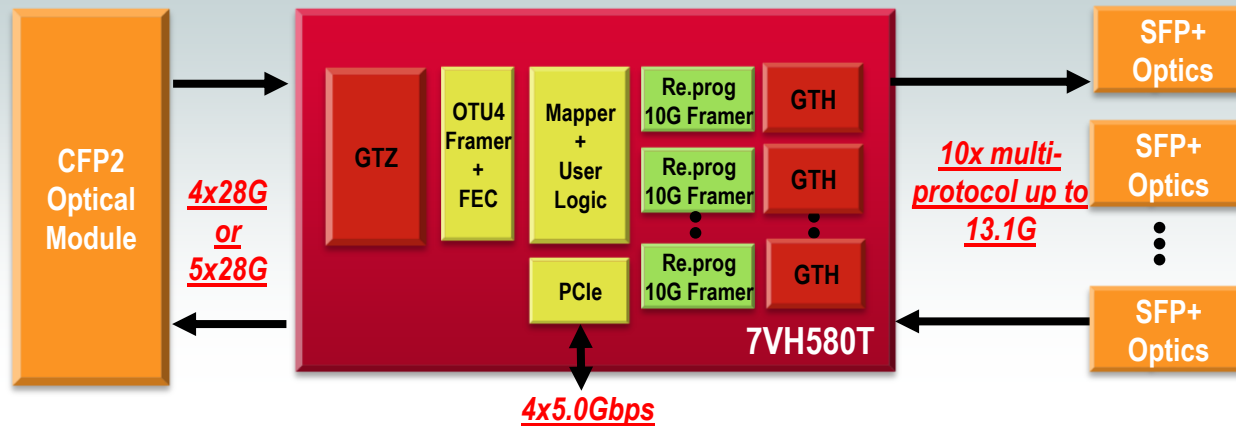


- Allows flexible FEC / EFEC if desired with up to 870,000 logic cells
- Allows connection with legacy ASICs @ 12.5G, 10.3125G and 6.25G

Cost Reduced OTU4 with Next Generation CFP2 Optics

Virtex-7HT GTZ Use Case #3

100G OTU4 Muxponder

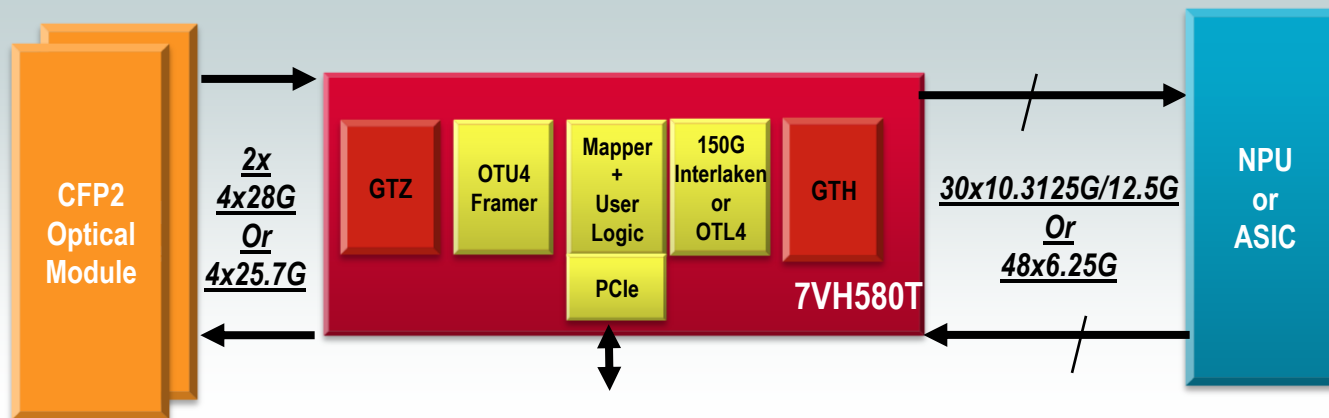


- Allows flexible FEC / EFEC if desired
- OTL4.4 and SFI-S support for 28G
- Up to 18 Independent optically compliant tributaries up to 13.1Gbps
- Partial Reconfiguration on 10G+ Tributary Framers to support 10GE, FC10, OTU2, OC-192 or other protocols. (green boxes)
- Migration path to 870T if more logic is needed (e.g. EFEC)

Single chip 100G Muxponder with EFEC

Virtex-7HT GTZ Use Case #4

2x100G Line Card

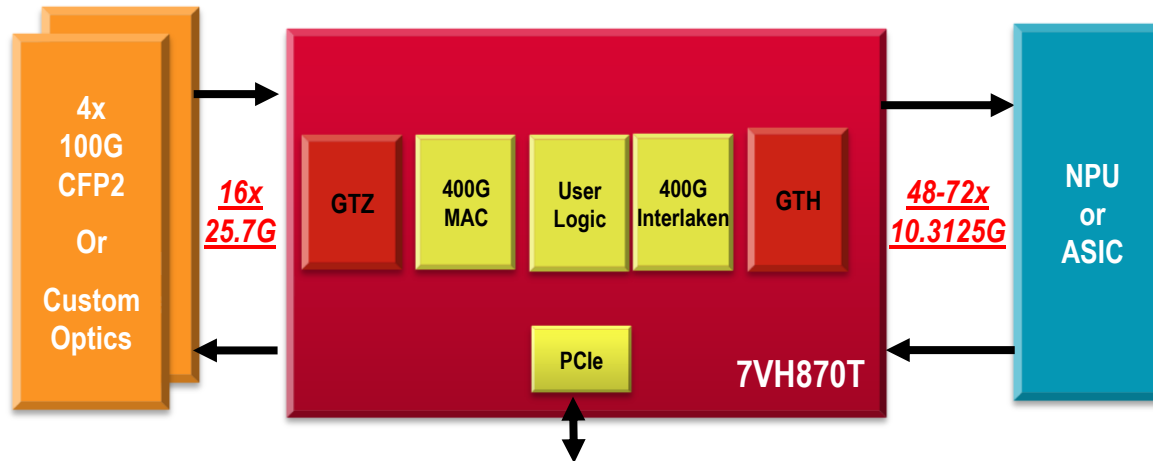


- Allows Density Upgrade from 1x100G solutions
- 2x 100GE or 2xOTU4 (GFEC) possible
- System Side can be 2x Interlaken, 2x CAUI, 2x OTU4 (SFI-S or OTL4.10) or custom

Cost Reduced OTU4 with Next Generation CFP2 Optics

Virtex-7HT GTZ Use Case #5

400GE Line Card



- Allows first-to-market 400GE interface
- No external PHY needed

Only FPGA that Enables a Single Chip 400G Implementation