
# KC705 GTX IBERT Design Creation

**October 2012**

XTP103

# Revision History

| Date | Version | Description |
|---|---|---|
| 10/23/12 | 4.0 | Regenerated for 14.3. |
| 07/25/12 | 3.0 | Regenerated for 14.2. Added AR50886. |
| 05/30/12 | 2.1 | Minor updates. |
| 05/08/12 | 2.0 | Regenerated for 14.1. AR46253 fixed. |
| 04/12/12 | 1.1 | Minor updates. |
| 01/18/11 | 1.0 | Initial version for 13.4. Added AR46253. |

# KC705 IBERT Overview

- Xilinx KC705 Board
- Software Requirements
- Setup for the KC705 IBERT Designs
- KC705 IBERT Design Creation
- References

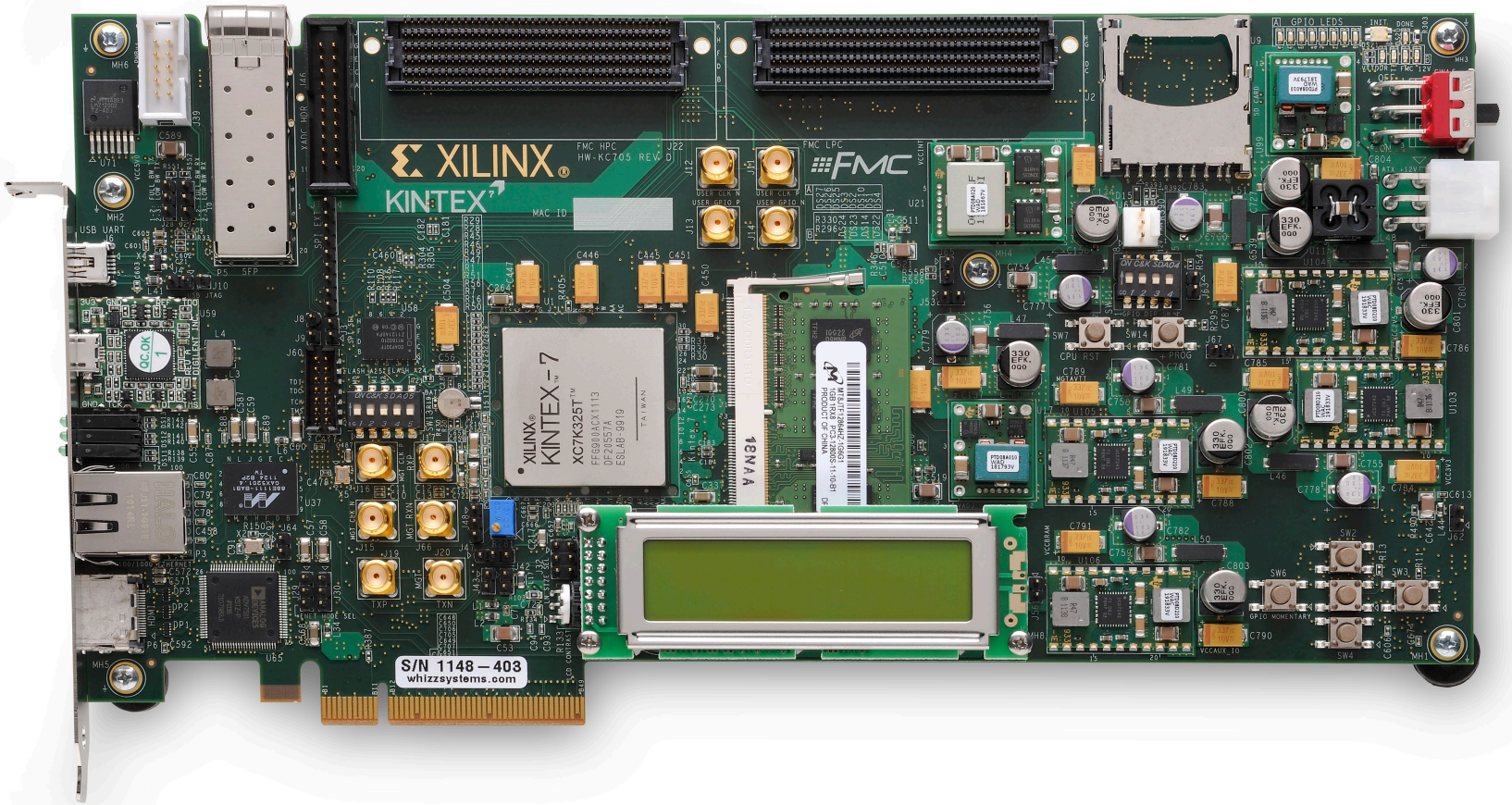
**Note:** This presentation applies to the KC705

# KC705 IBERT Overview

- **Description**
  - The LogiCORE Integrated Bit Error Ratio (IBERT) core is used to create a pattern generation and verification design to exercise the Kintex-7 GTX transceivers. A graphical user interface is provided through the IBERT console window of the ChipScope Pro Analyzer
- **Reference Design IP**
  - LogiCORE IBERT Example Designs
  - ChipScope Pro Analyzer
    - ChipScope Pro Software and Cores User Guide (UG029)

**Note:** Presentation applies to the KC705

# Xilinx KC705 Board



# ISE Software Requirement

- **Xilinx ISE 14.3 software**
  - Apply AR52368


**Note:** Presentation applies to the KC705

# ChipScope Pro Software Requirement

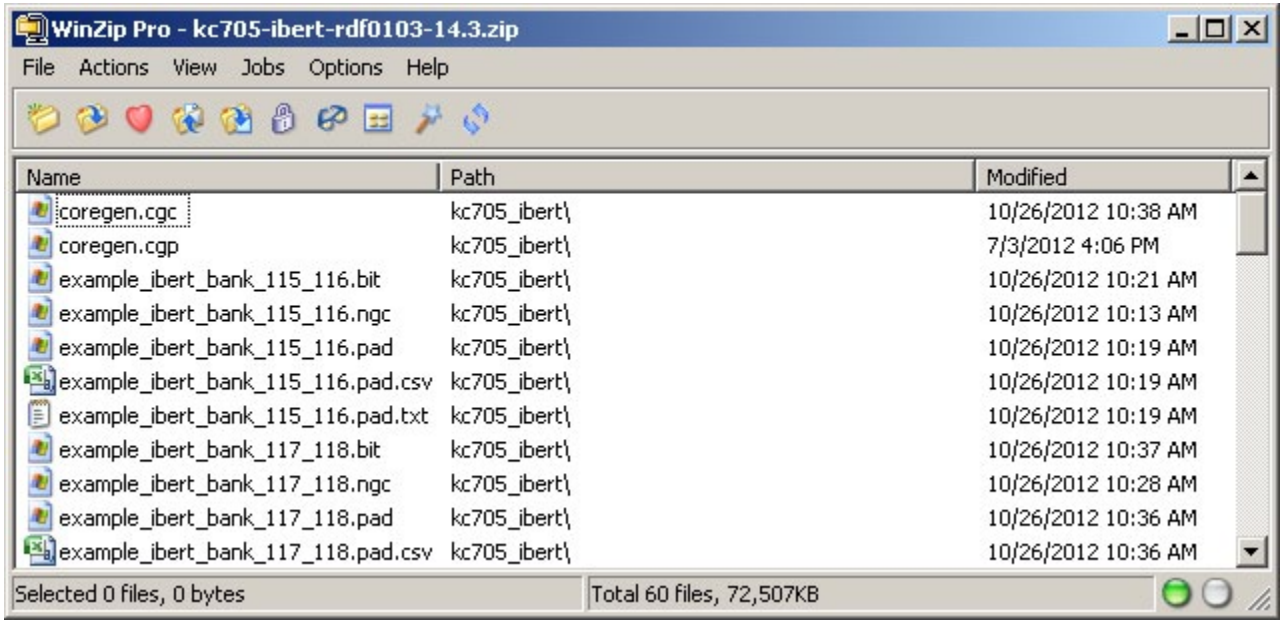
- Xilinx ChipScope Pro 14.3 software


**Note:** Presentation applies to the KC705

# Setup for the KC705 IBERT Designs

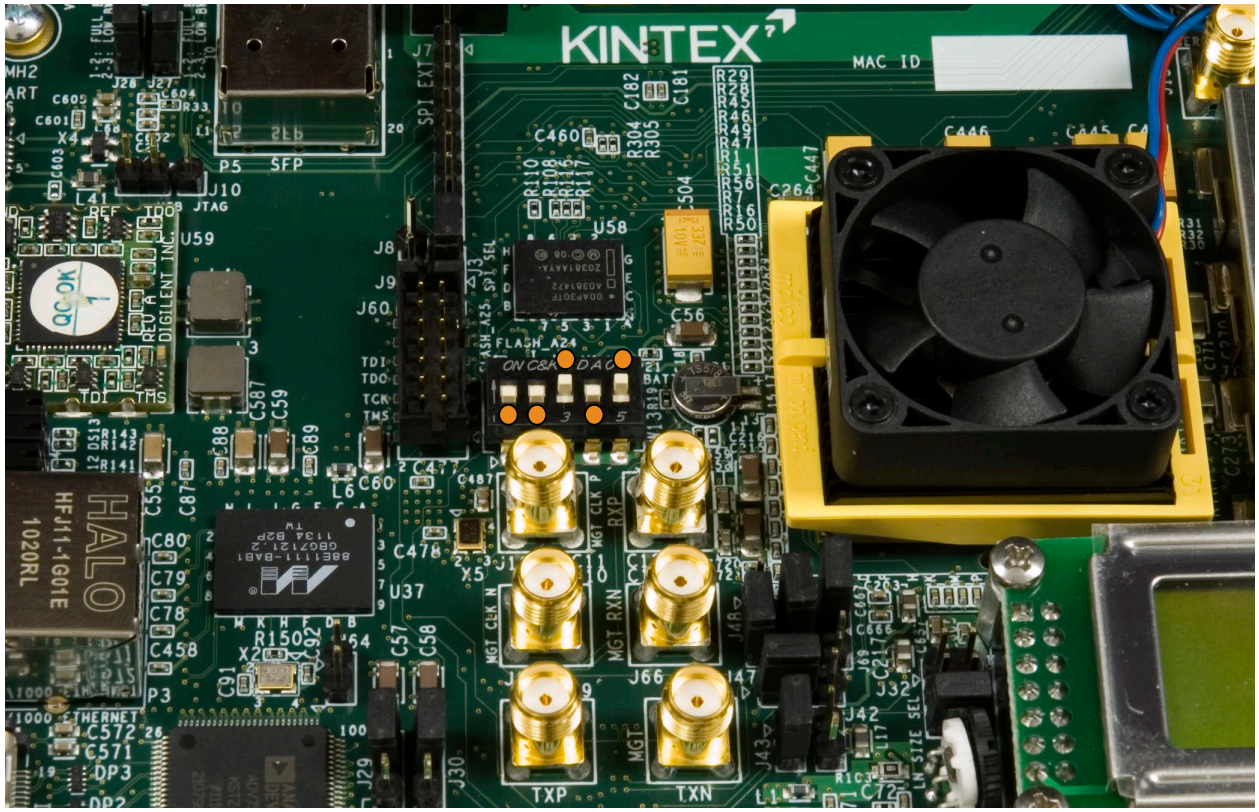
# Setup for the KC705 IBERT Designs

- **Unzip the KC705 GTX IBERT Design Files (14.3 CES) to your C:\ drive**
  - Available through http://www.xilinx.com/kc705



# Hardware Setup

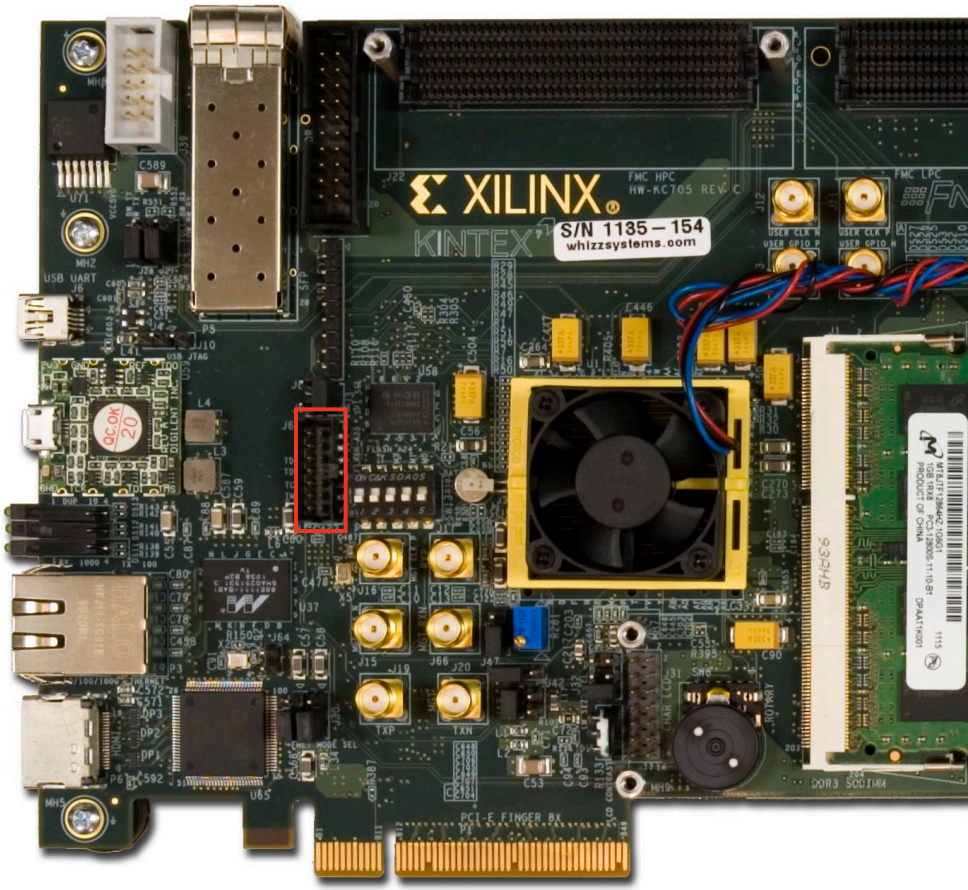
- **Set S13 to 00101 (1 = on, Position 1 → Position 5)**
  - This enables JTAG configuration




**Note:** Presentation applies to the KC705

# Hardware Setup

- **Connect a Platform Cable USB to the KC705**
  - Connect this cable to your PC

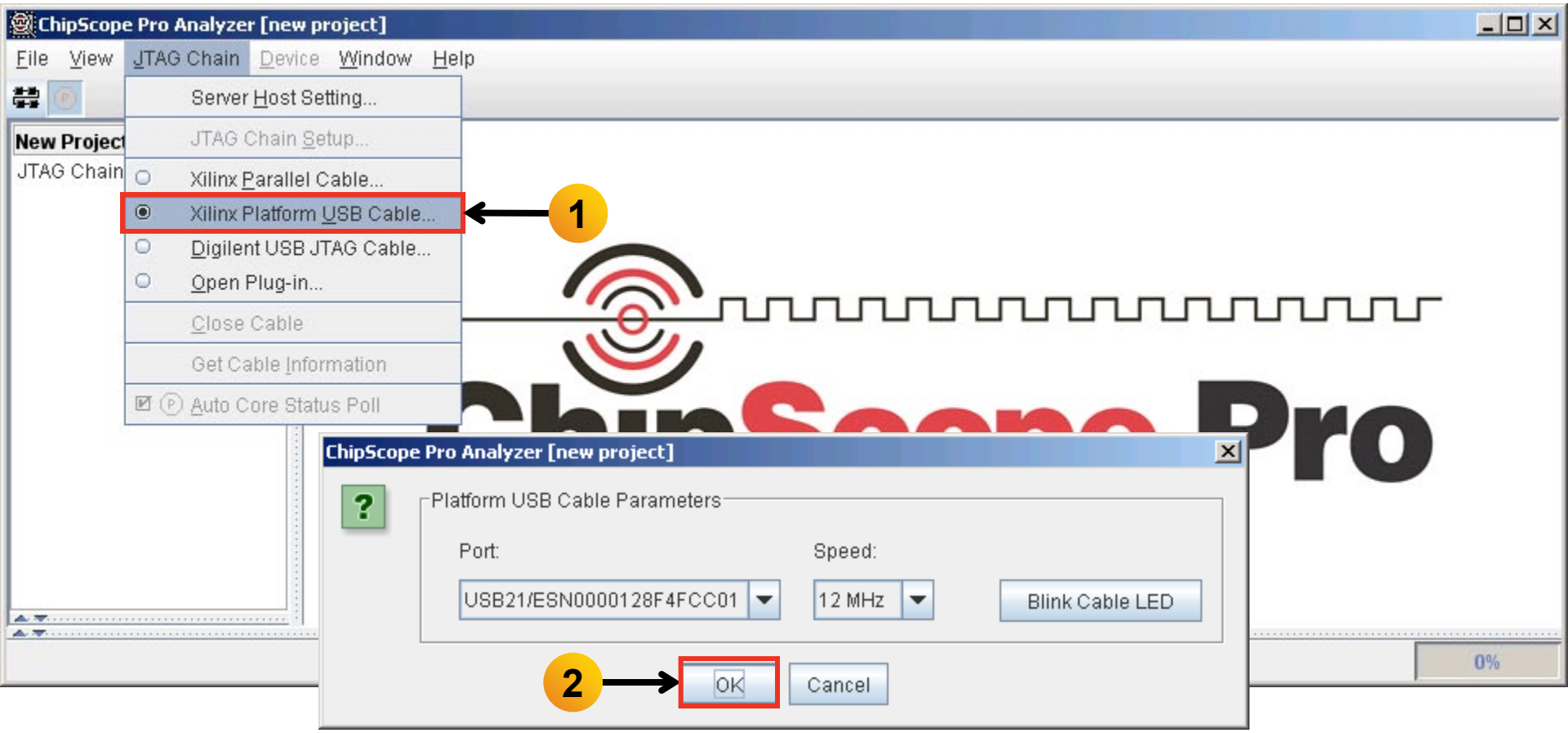



**Note:** Presentation applies to the KC705

# KC705 GTX IBERT Design – Banks 117, 118

# KC705 GTX IBERT Design – Banks 117, 118

- Open ChipScope Pro and select JTAG Chain → USB Cable… (1)
- Click OK (2)

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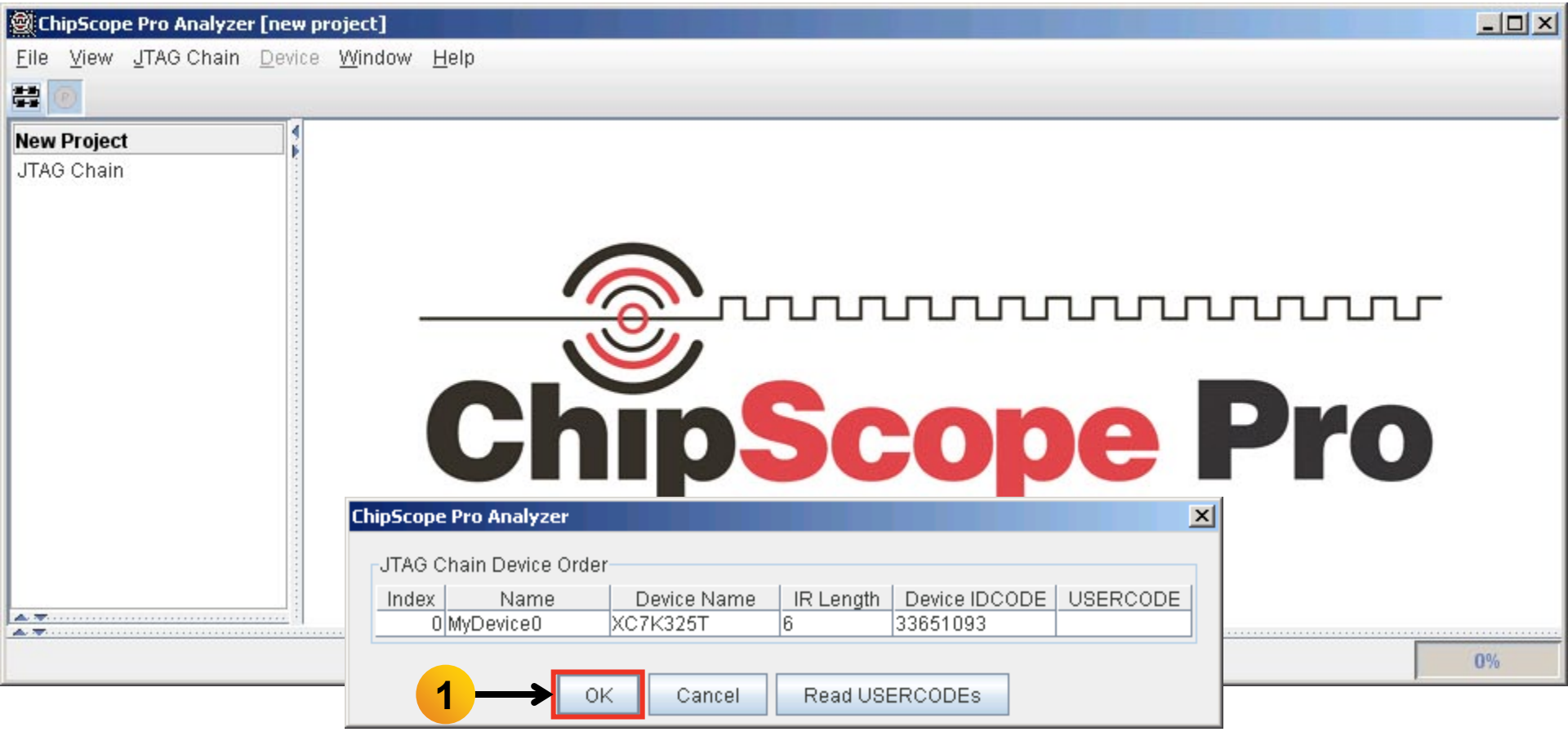
# KC705 GTX IBERT Design – Banks 117, 118

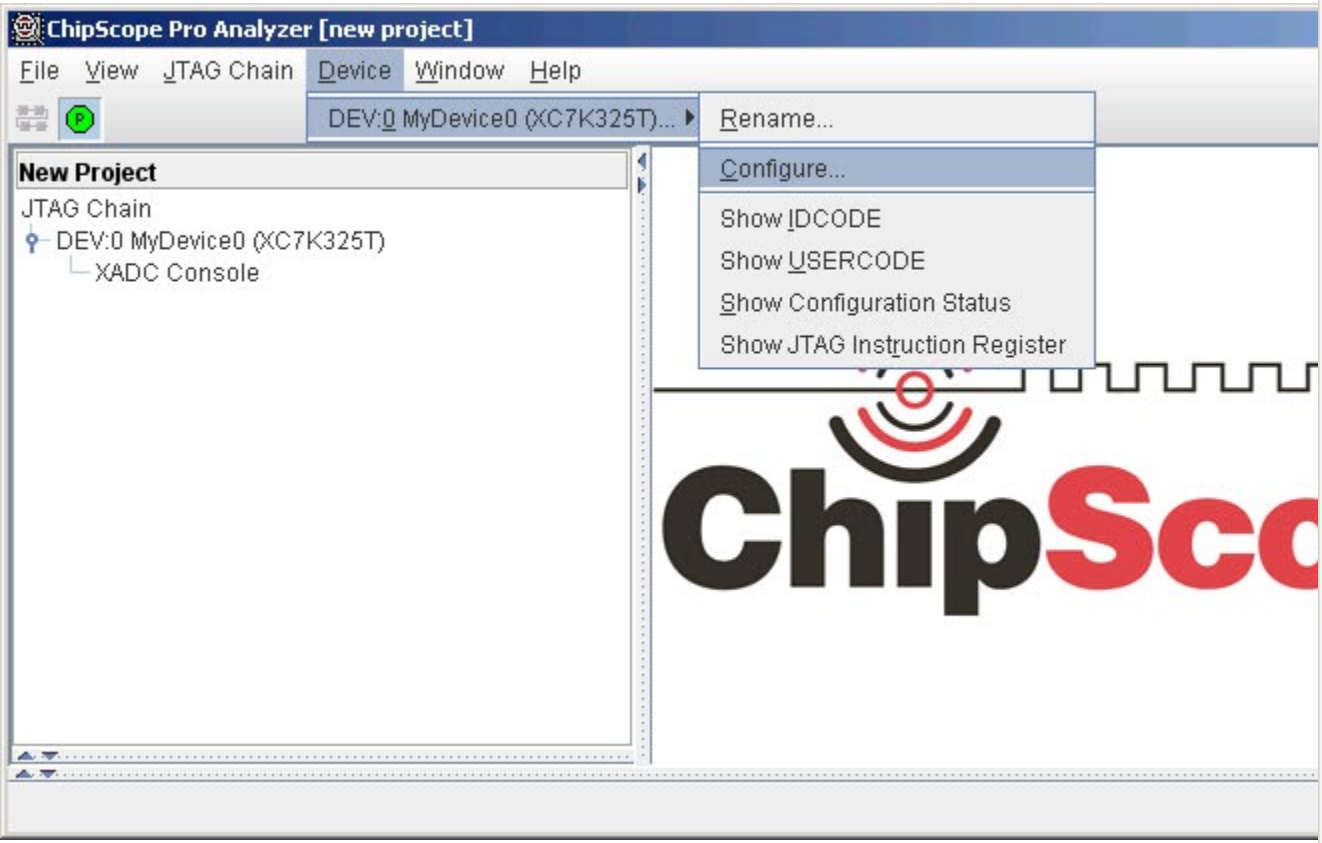
- Click OK (1)

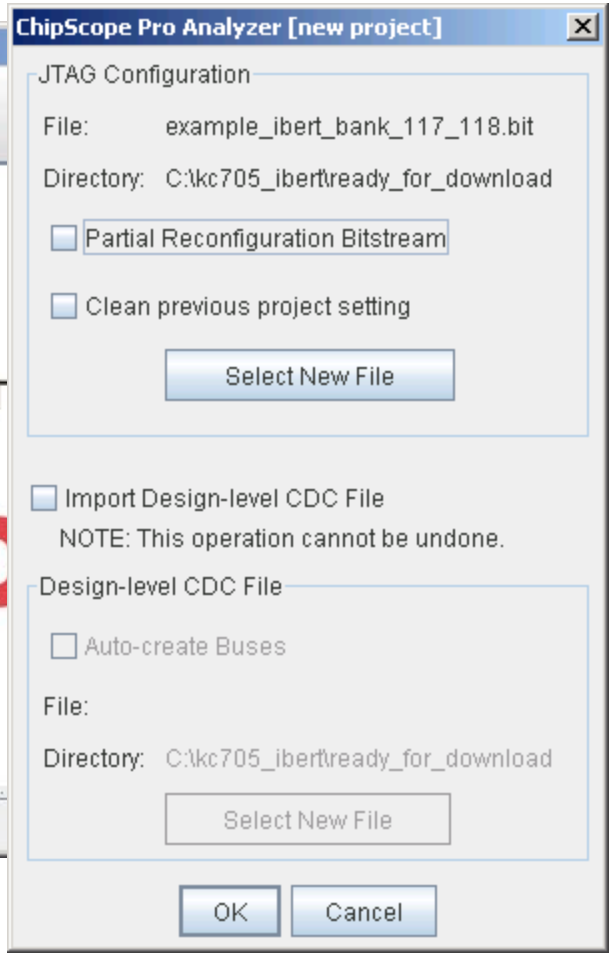



**Note:** Presentation applies to the KC705

# KC705 GTX IBERT Design – Banks 117, 118

- Select Device → DEV:0 MyDevice0 (XC7K325T)… → Configure…
- Select <Design Path>\ready_for_download\ example_ibert_bank_117_118.bit

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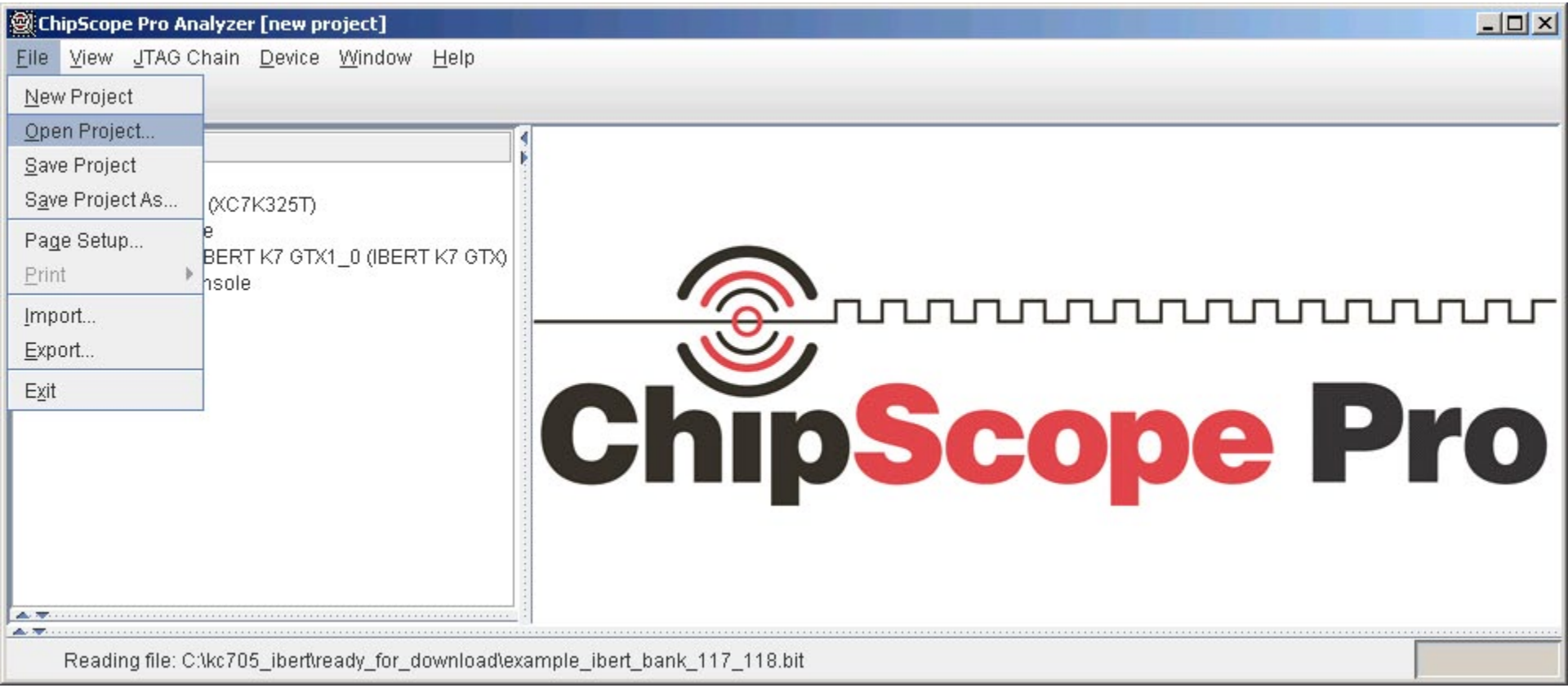
# KC705 GTX IBERT Design – Banks 117, 118

- Select File → Open Project…
- Select <Design Path>\ready_for_download\ibert_bank_117_118.cpj

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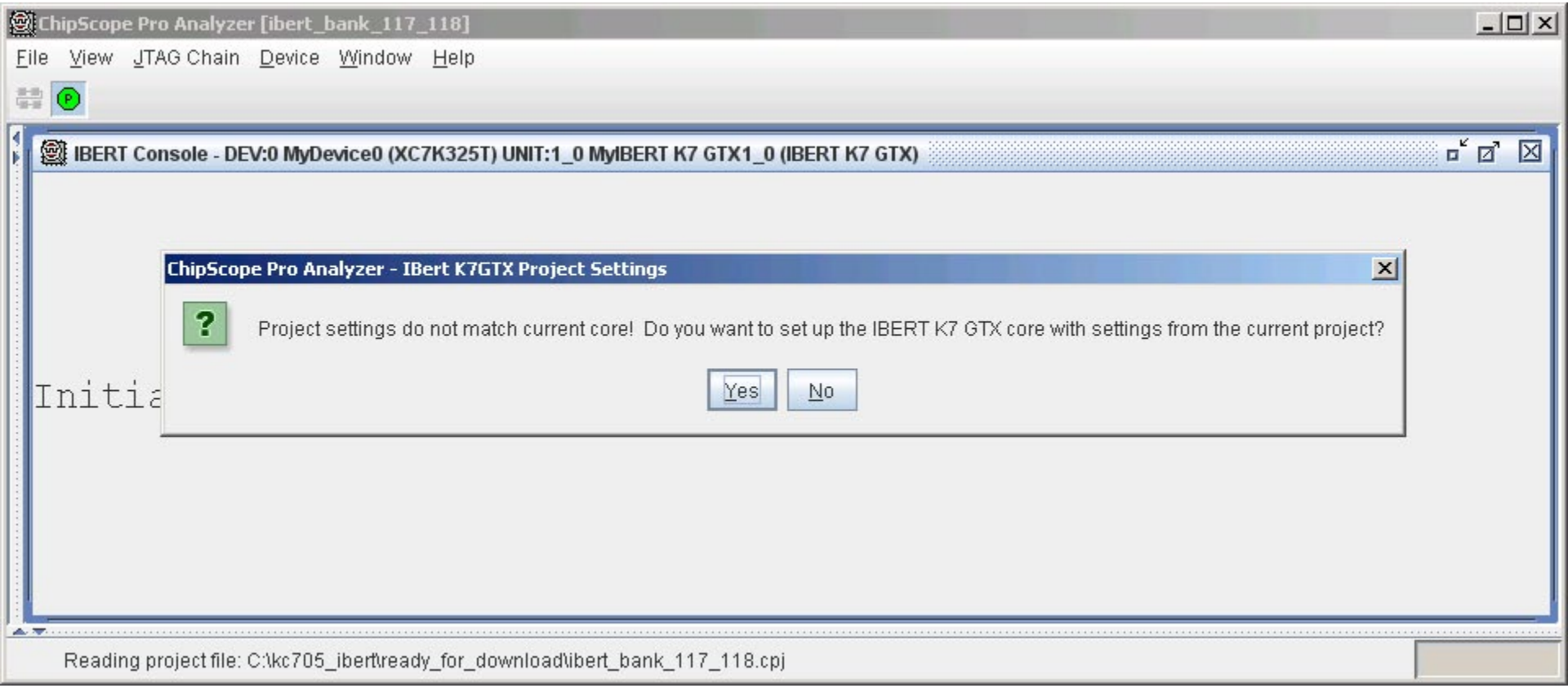
# KC705 GTX IBERT Design – Banks 117, 118

- Click Yes on this Dialog

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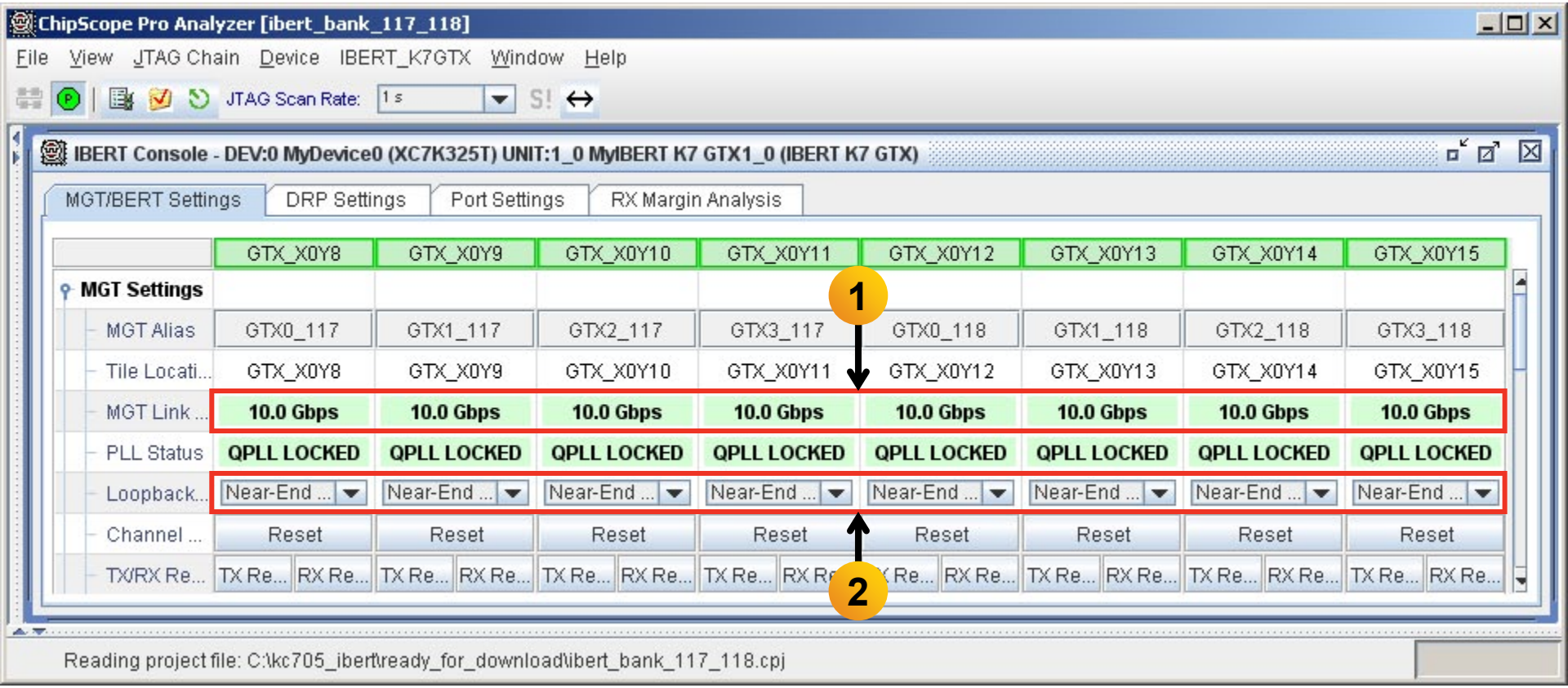
# KC705 GTX IBERT Design – Banks 117, 118

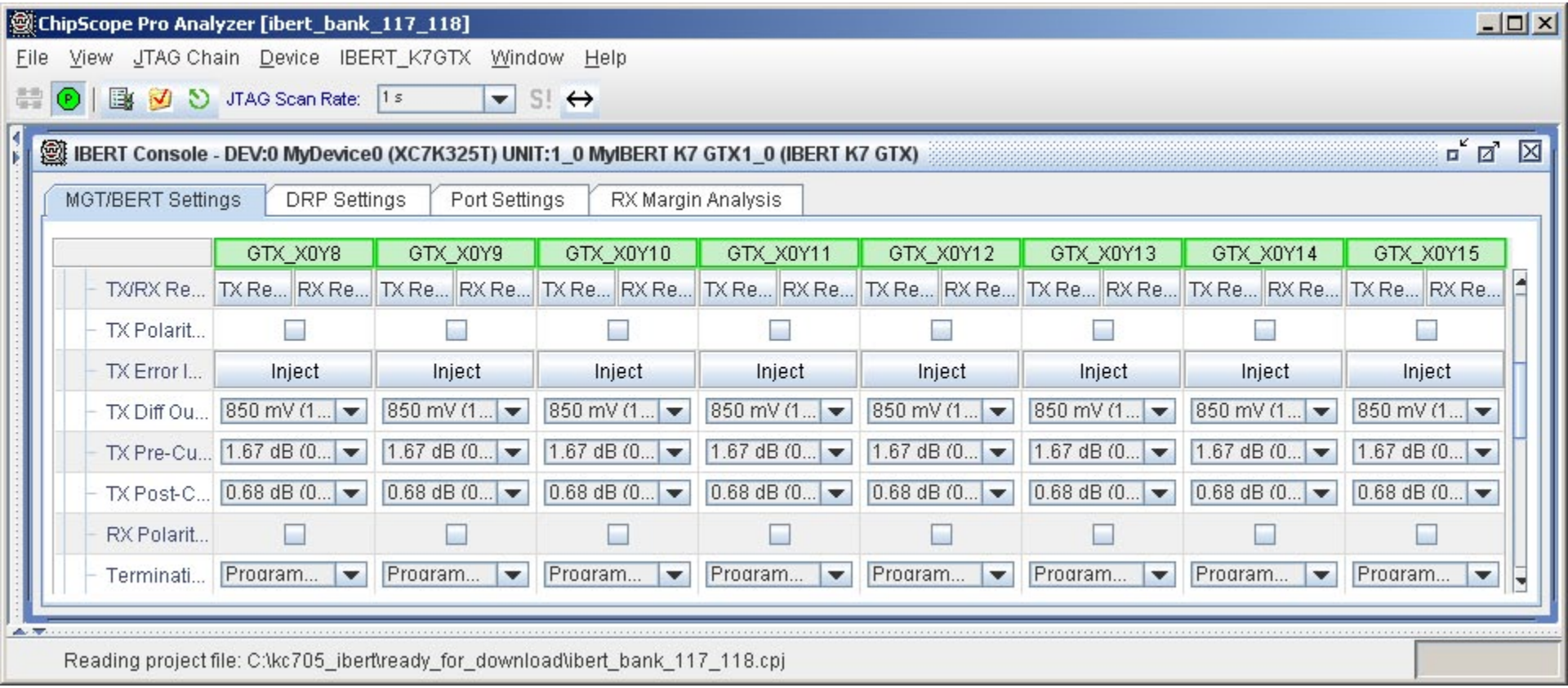
- The line rate is 10.0 Gbps for all GTXs (1)
- All GTXs are in Near-End PCS loopback (2)




**Note:** Bank 117, 118: SMA, SFP+, SGMII, LPC, HPC

# KC705 GTX IBERT Design – Banks 117, 118

- TX Diff Output Swing = 850 mV
- TX Pre-Cursor = 1.67 dB; TX Post-Cursor = 0.68 dB

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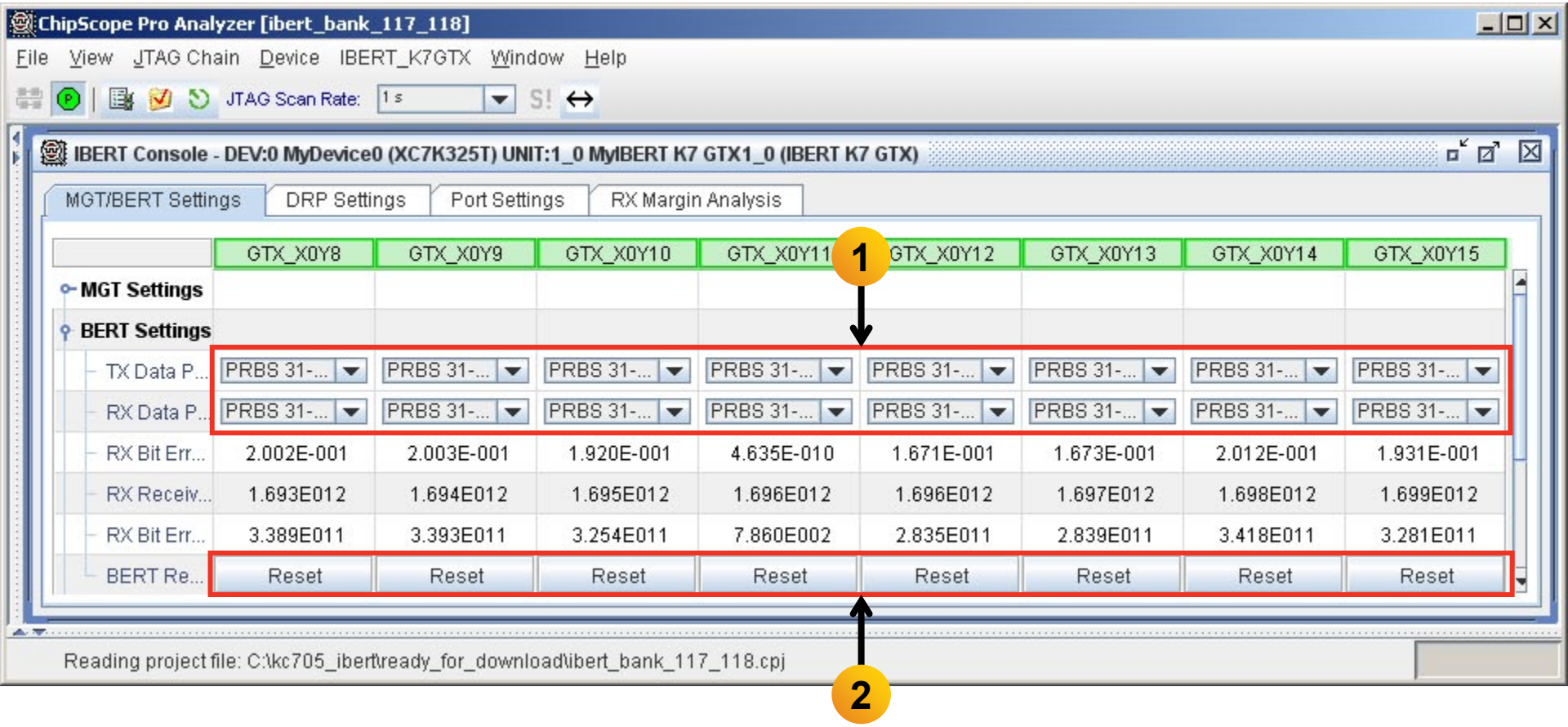
# KC705 GTX IBERT Design – Banks 117, 118

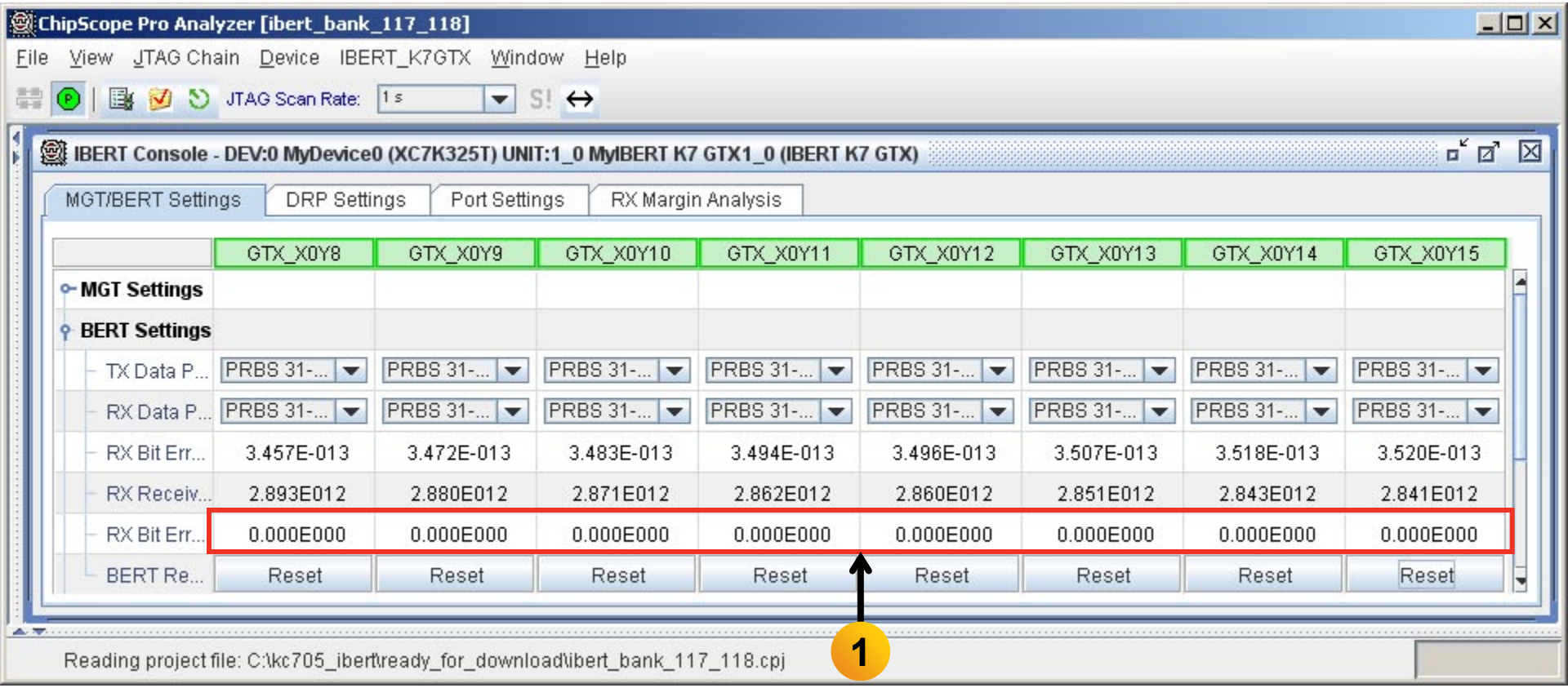
- TX/RX Data Patterns are set to PRBS 31-bit (1)
- Click BERT Reset buttons (2)




**Note:** Presentation applies to the KC705

# KC705 GTX IBERT Design – Banks 117, 118

- View the RX Bit Error Count (1)
- Close ChipScope Pro Analyzer and cycle KC705 board power




**Note:** Presentation applies to the KC705

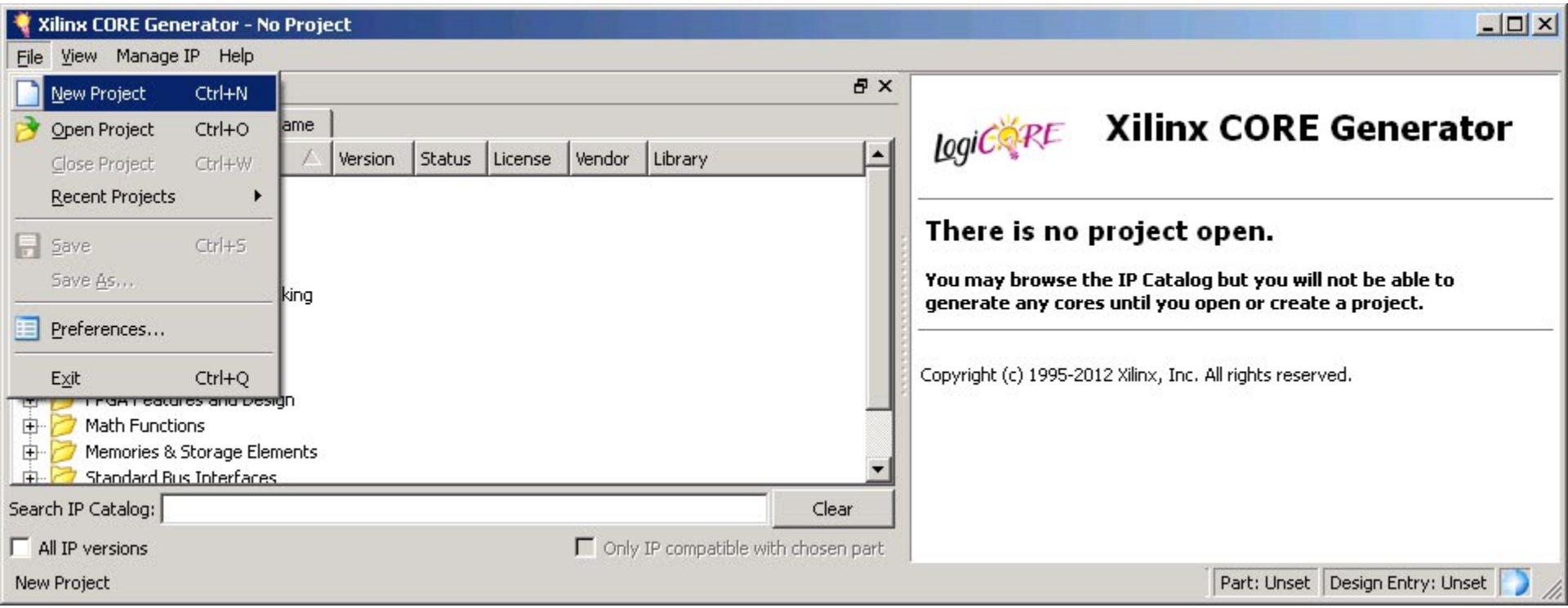
# KC705 IBERT Design Creation

# Create IBERT CORE Generator Project

- Open the CORE Generator

  **Start → All Programs → Xilinx Design Tools → ISE Design Suite 14.3 → ISE Design Tools → 32-bit Tools → CORE Generator**

- Create a new project; select File → New Project

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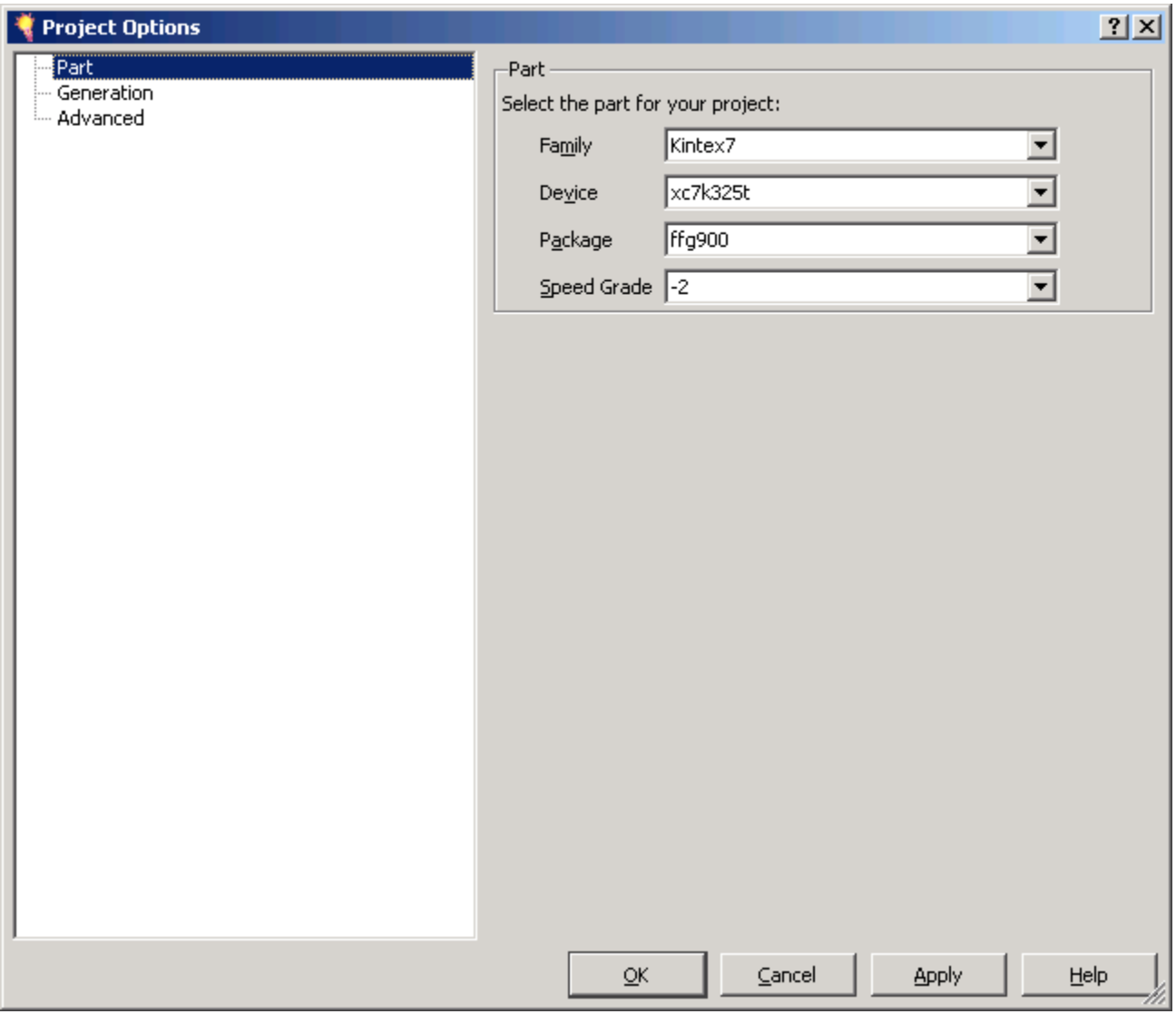
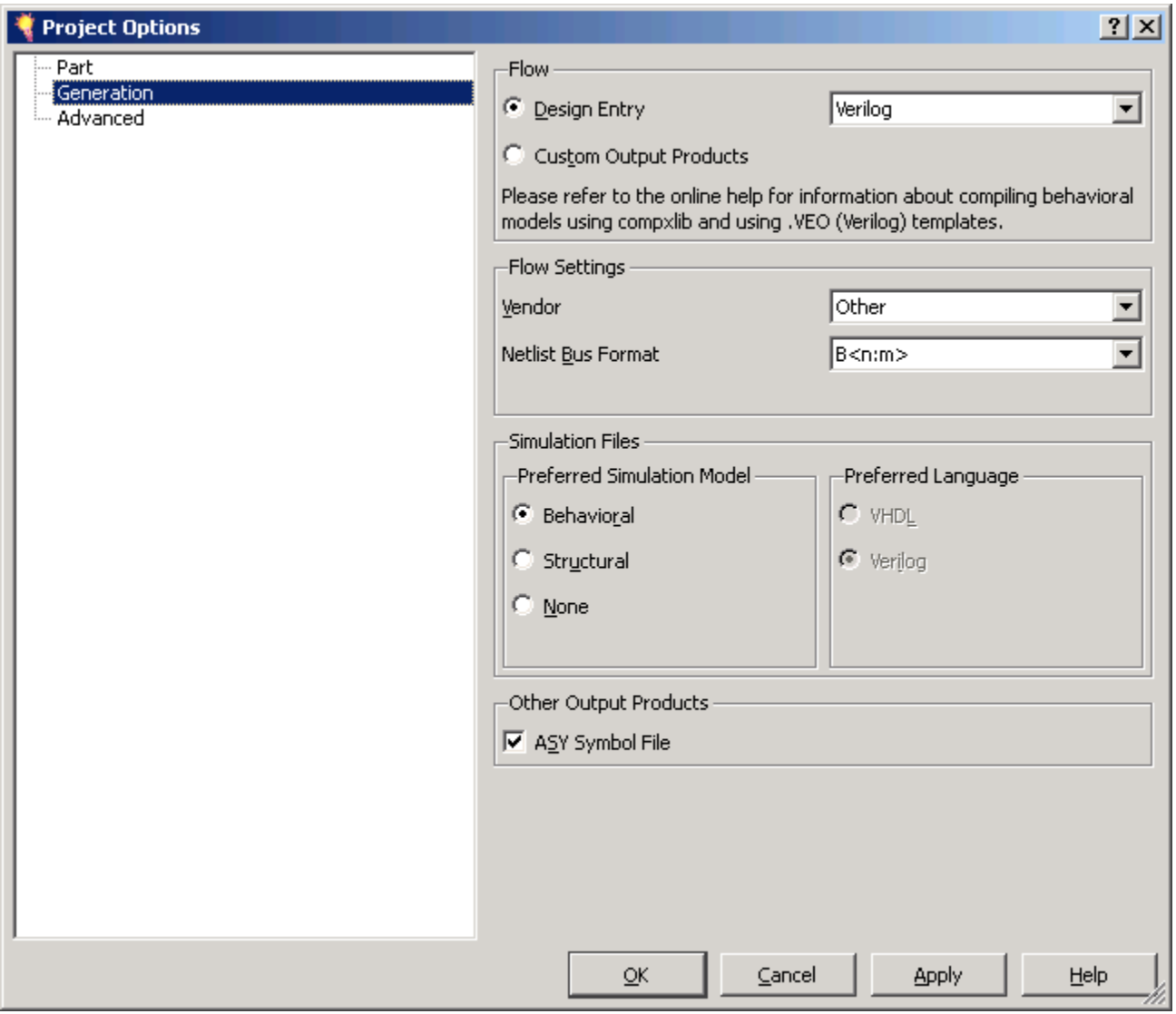
# Create IBERT CORE Generator Project




- **Create a project in a new directory named:**
  - **kc705_ibert**
- **Select Part**
- **Set the Part (as seen here):**
  - Family: Kintex7
  - Device: xc7k325t
  - Package: ffg900
  - Speed Grade: -2
- **Select Generation**

**Note:** Presentation applies to the KC705

# Create IBERT CORE Generator Project



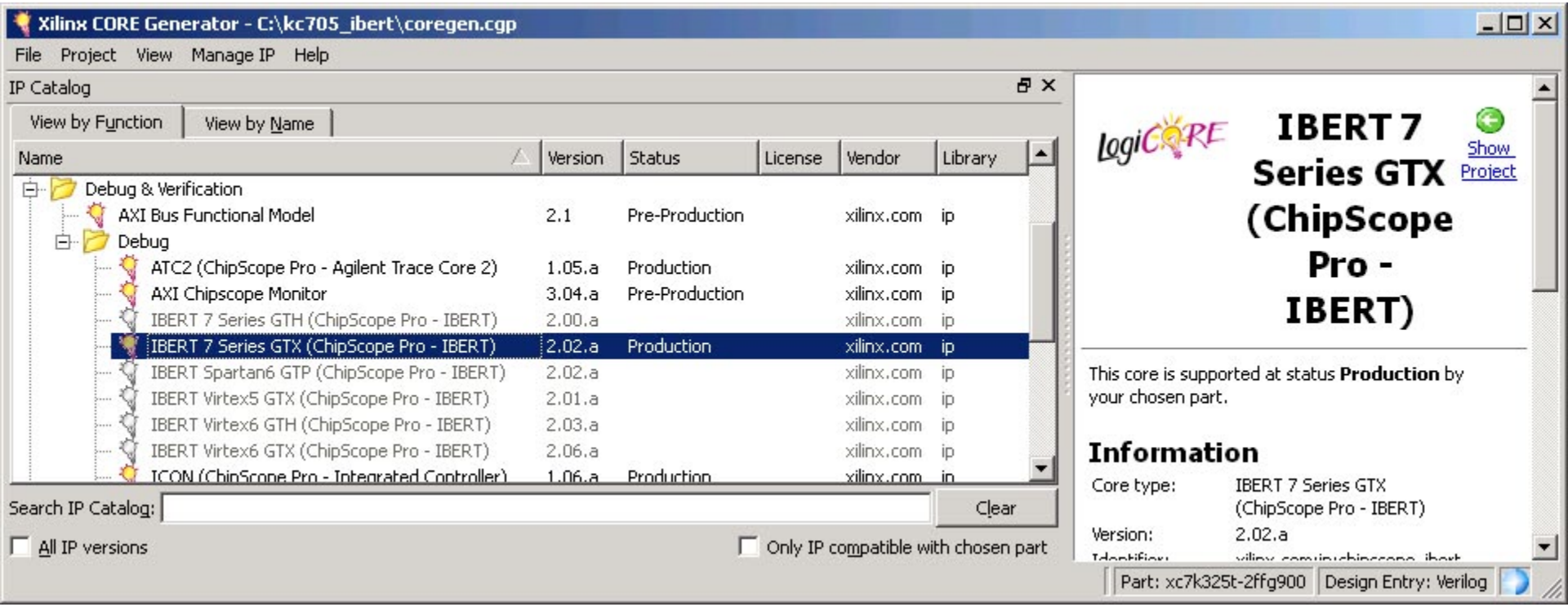

- Select Verilog
- Click OK

**Note:** Presentation applies to the KC705

# Create IBERT Design for Banks 115, 116

# Create IBERT Design for Banks 115, 116

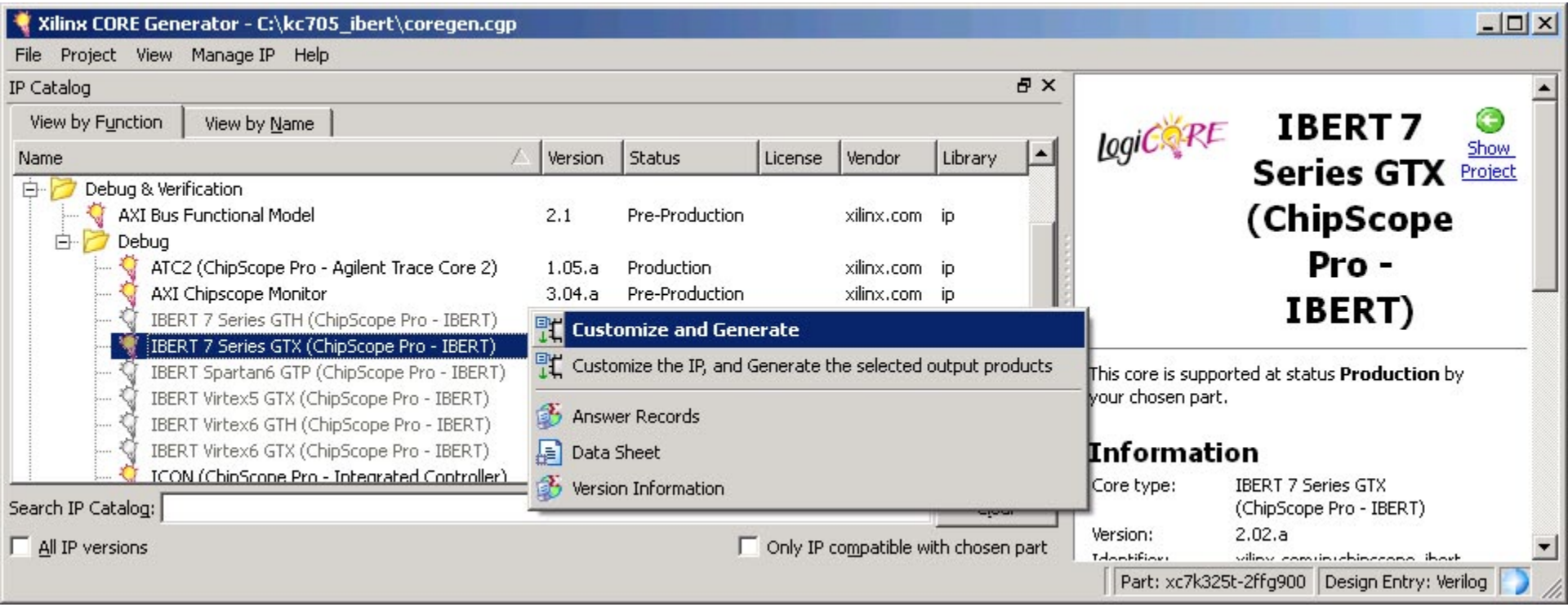
- Select the IBERT 7 Series GTX (ChipScope Pro - IBERT), Version 2.02.a




**Note:** Presentation applies to the KC705

# Create IBERT Design for Banks 115, 116

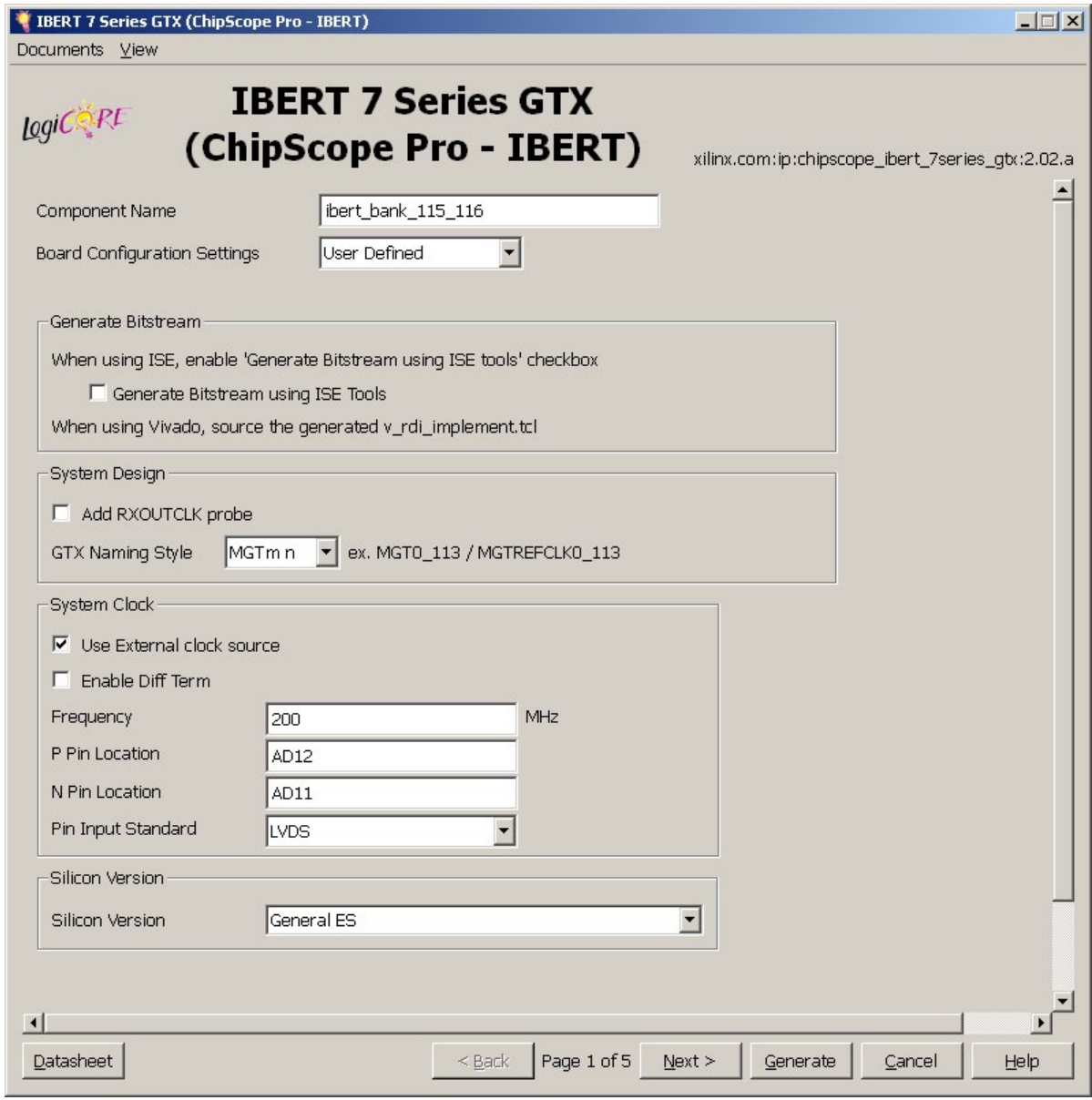
- **Right click on the IBERT Kintex7 GTX (ChipScope Pro - IBERT), Version 2.02.a**
  - Select **Customize and Generate**




**Note:** Presentation applies to the KC705

# Create IBERT Design for Banks 115, 116

- **Make the following settings:**
  - Component name: **ibert_bank_115_116**
  - Set the GTX Naming Style to: MGT m n
  - Set the System Clock
    - Frequency: **200**
    - Pin Input standard: **LVDS**
    - P Pin Location: **AD12**
    - N Pin Location: **AD11**
    - Silicon Version: **General ES**
- **Click Next**

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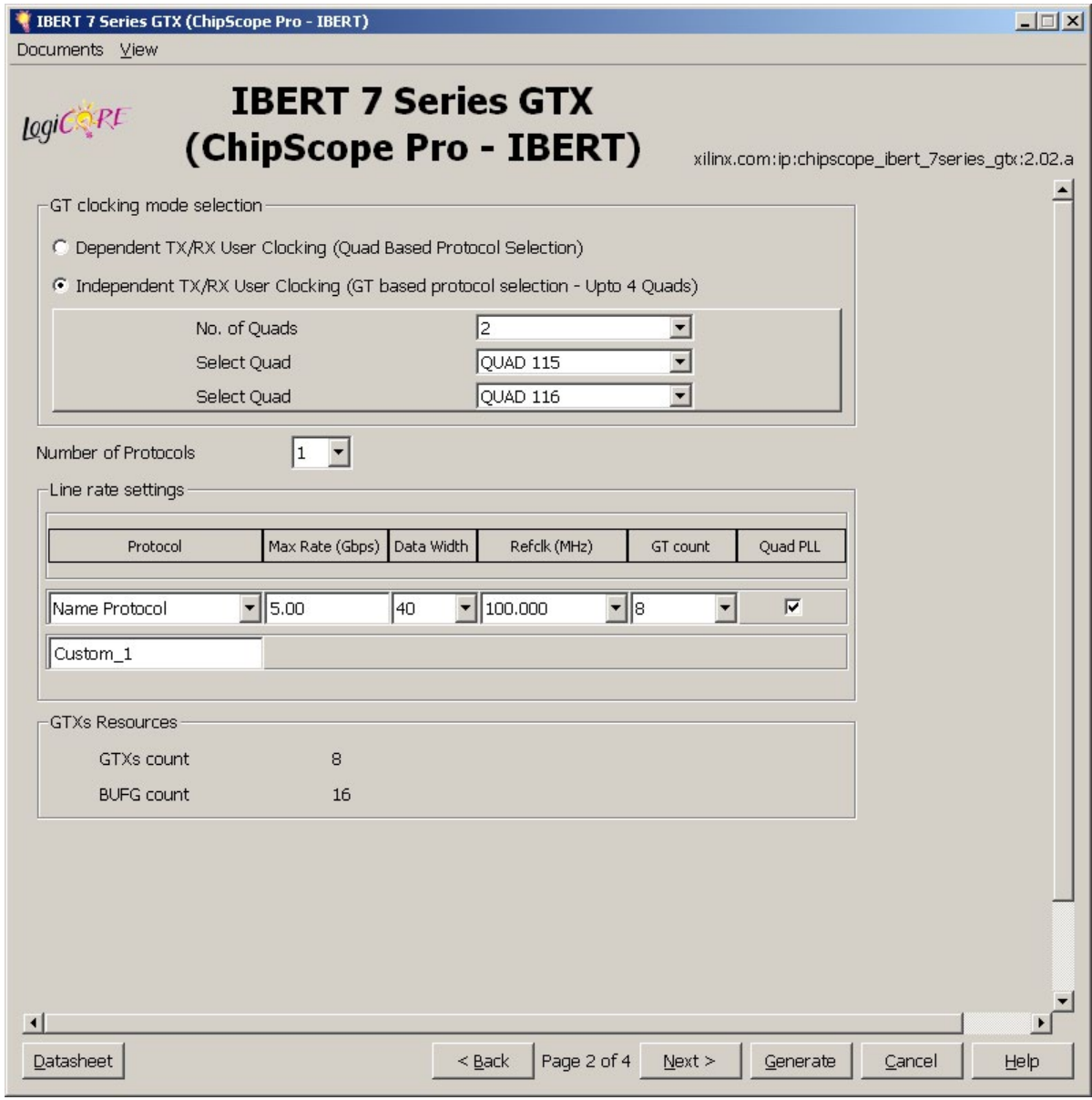
# Create IBERT Design for Banks 115, 116

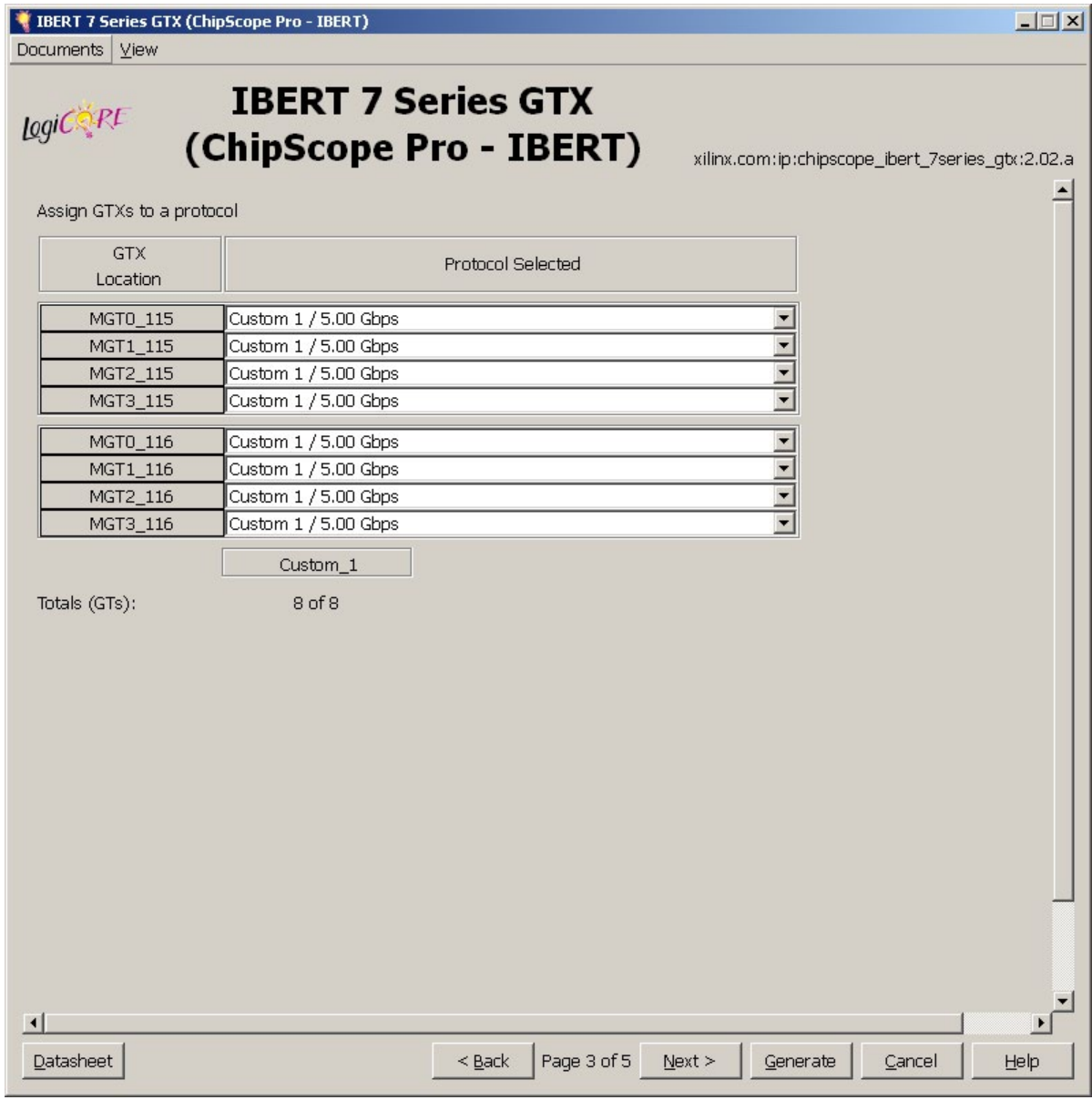
- **Make the following settings:**
  - Select: **Independent TX/RX User Clocking**
  - No. of Quads: **2**
  - Select: **QUAD 115 and QUAD 116**
  - Max Rate (Gbps): **5.00**
  - Refclk (MHz): **100.000**
  - GTX Count: **8**
- **Click Next**




**Note:** Presentation applies to the KC705

# Create IBERT Design for Banks 115, 116

- Set Banks 115 and 116 to:
  - Custom 1 / 5.00 Gbps
- Click Next

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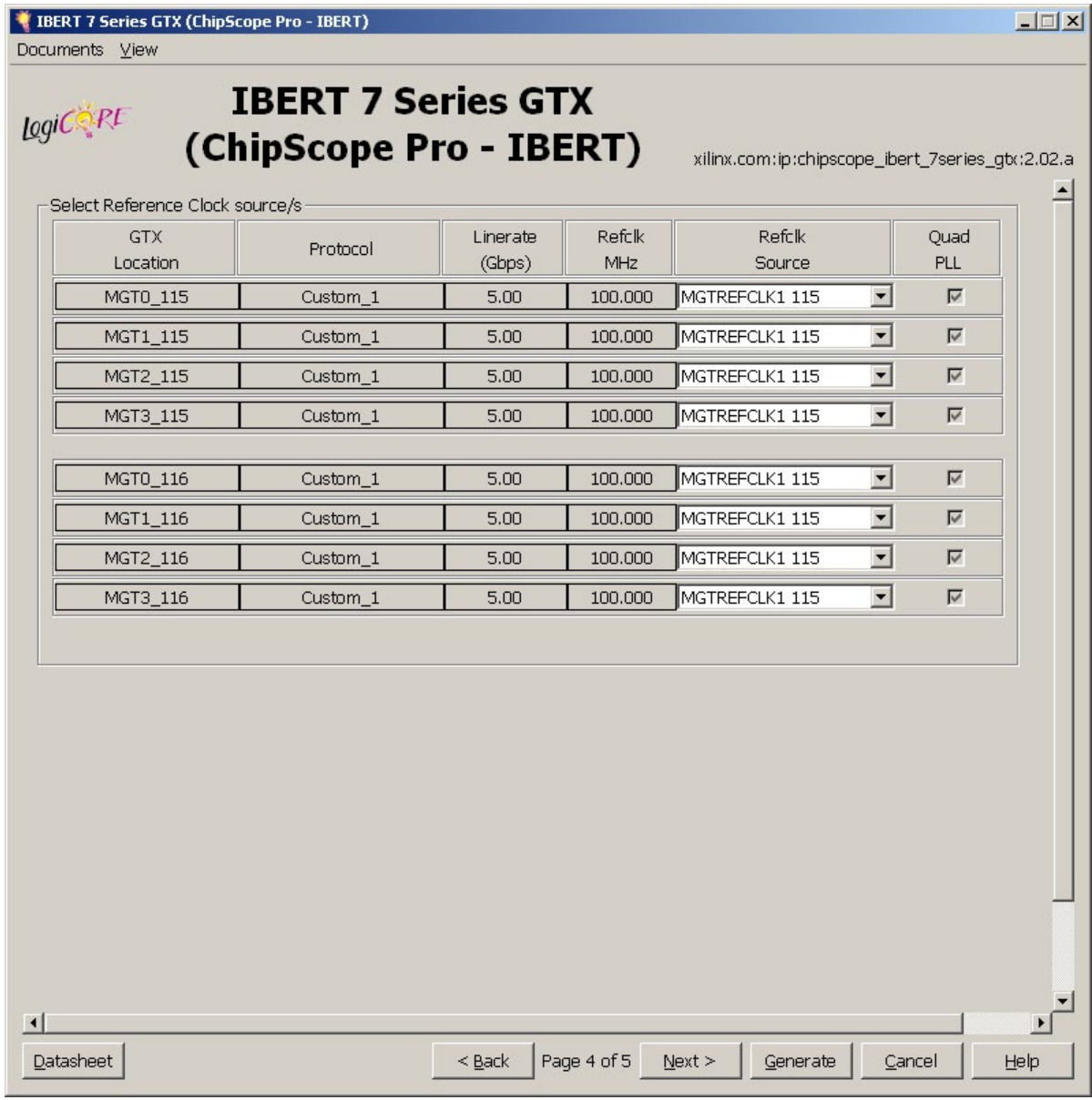
# Create IBERT Design for Banks 115, 116

- Set Banks 115 and 116 Refclk Sources to:
  - MGTREFCLK1 115
- Click Next

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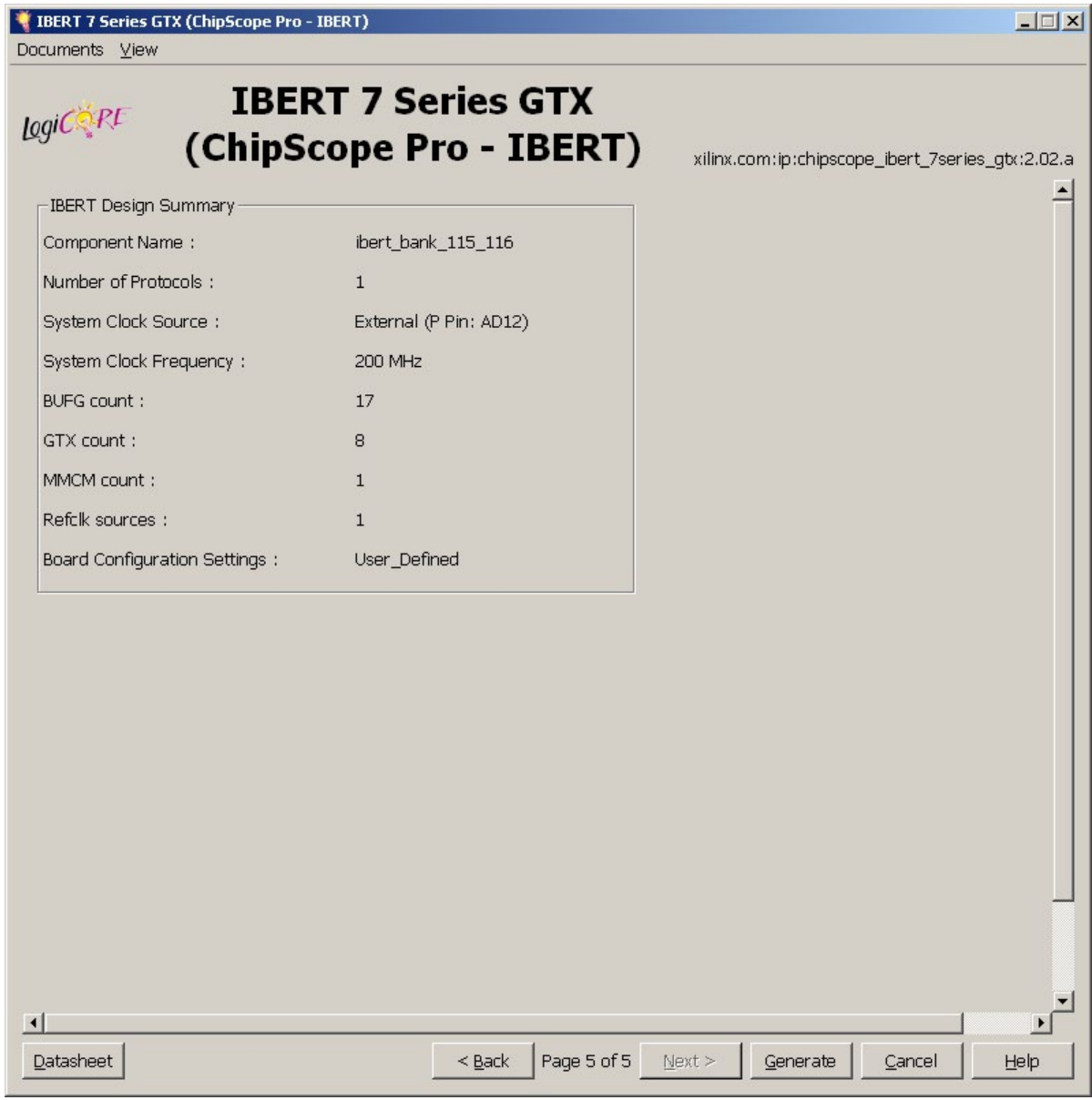
# Create IBERT Design for Banks 115, 116

- Click Generate

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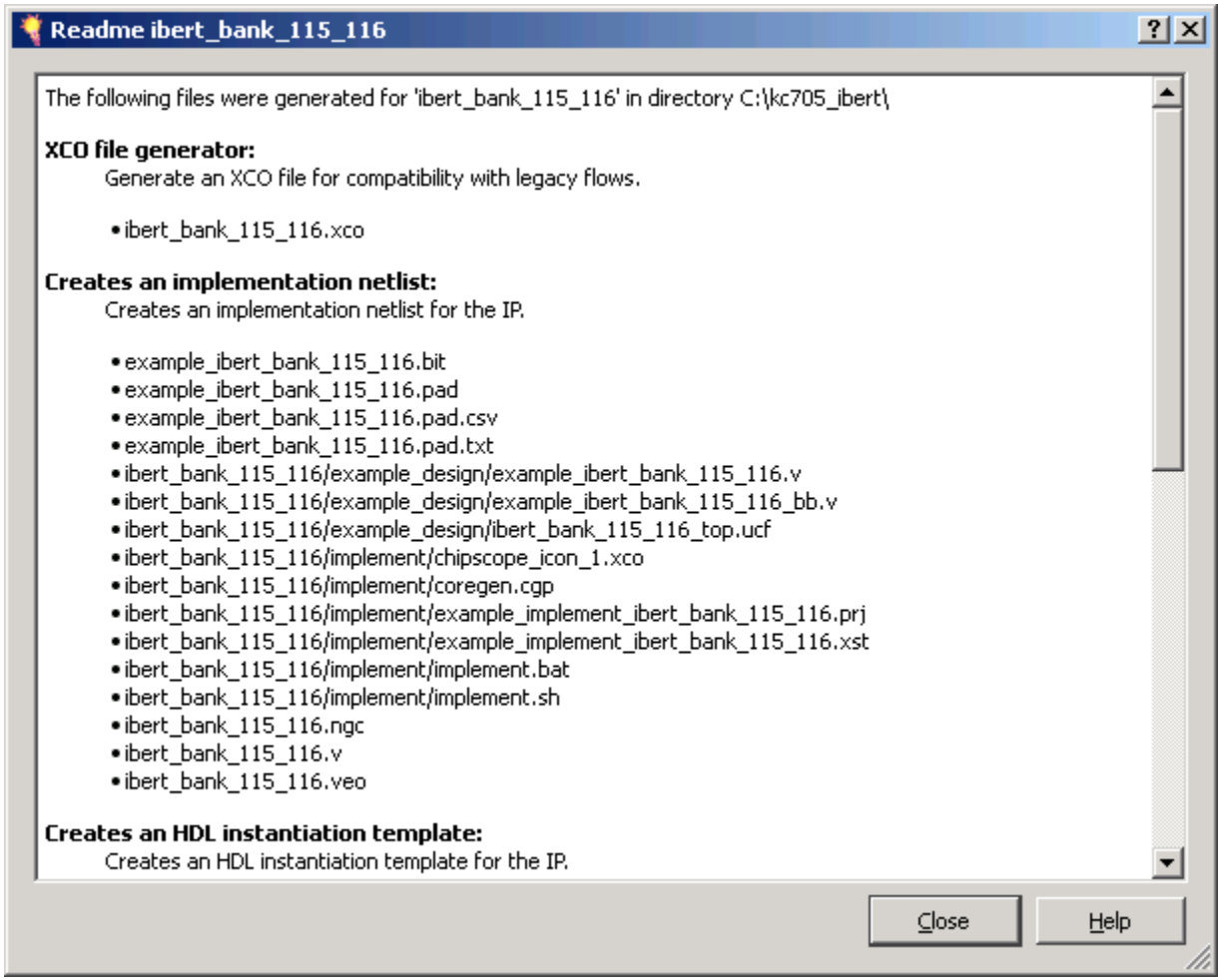
# Create IBERT Design for Banks 115, 116

- After the IBERT core finishes generating, click Close on the Readme File window

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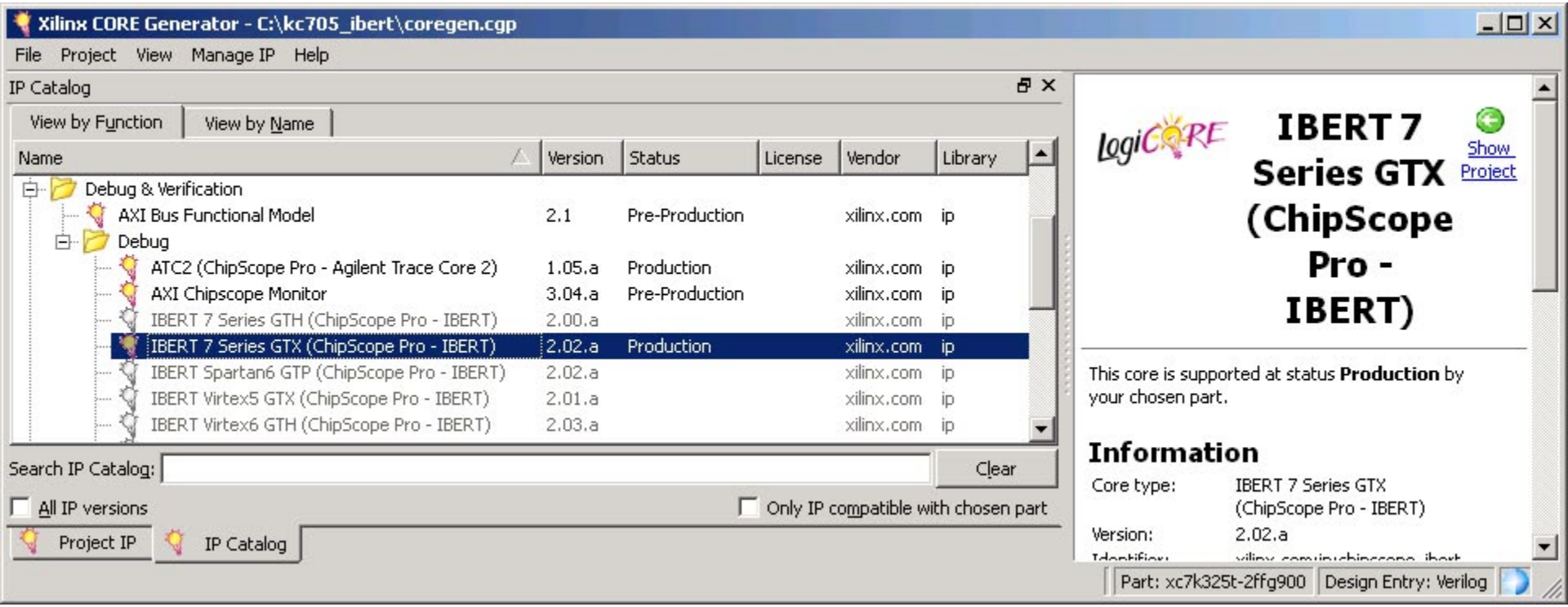
# Create IBERT Design for Banks 117, 118

# Create IBERT Design for Banks 117, 118

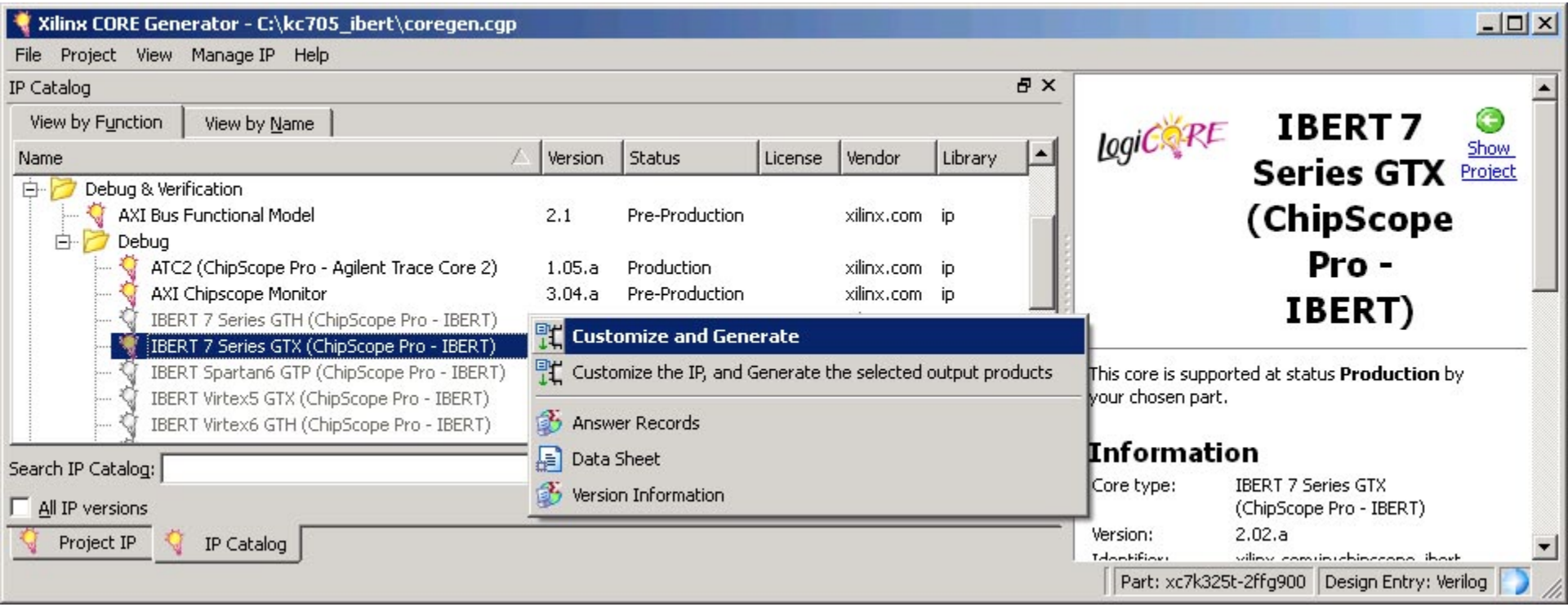
- Select the IBERT 7 Series GTX (ChipScope Pro - IBERT), Version 2.02.a




**Note:** Presentation applies to the KC705

# Create IBERT Design for Banks 117, 118

- **Right click on the IBERT Kintex7 GTX (ChipScope Pro - IBERT), Version 2.02.a**
  - Select Customize and Generate

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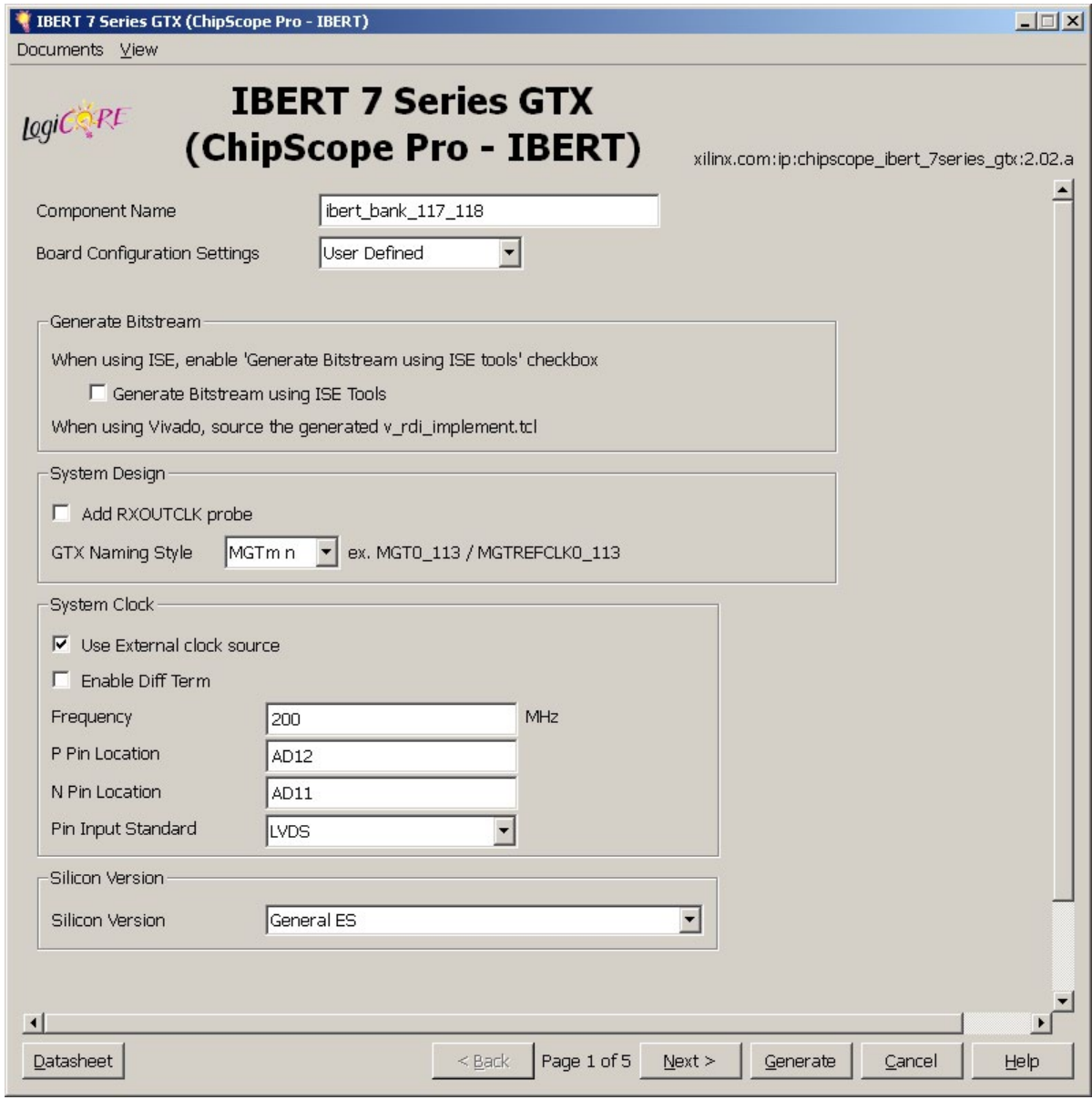
# Create IBERT Design for Banks 117, 118

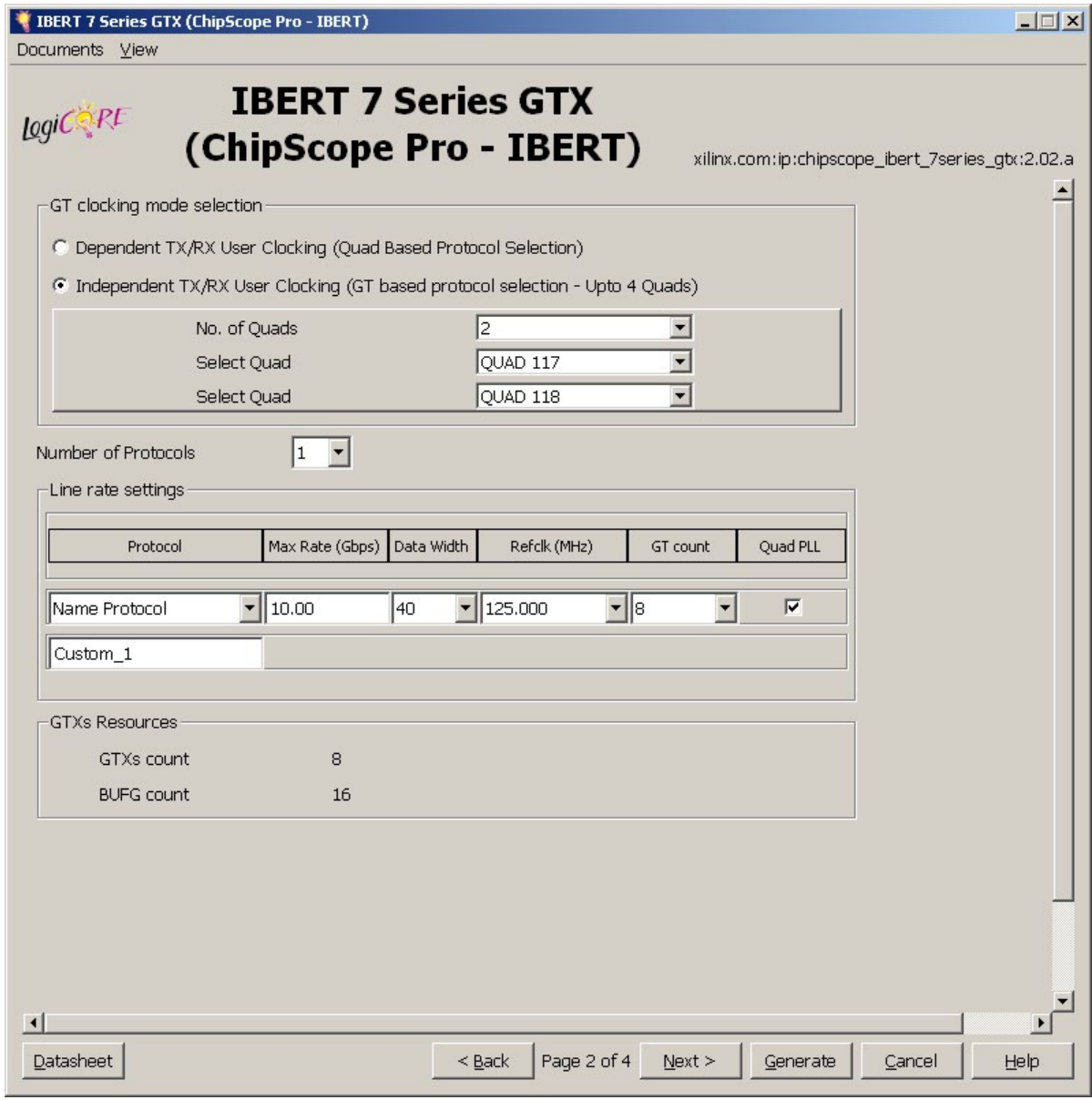
- **Make the following settings:**
  - Component name: **ibert_bank_117_118**
  - Set the GTX Naming Style to: **MGT m n**
  - Set the System Clock
    - Frequency: **200**
    - Pin Input standard: **LVDS**
    - P Pin Location: **AD12**
    - N Pin Location: **AD11**
    - Silicon Version: **General ES**
- **Click Next**




**Note:** Presentation applies to the KC705

# Create IBERT Design for Banks 117, 118

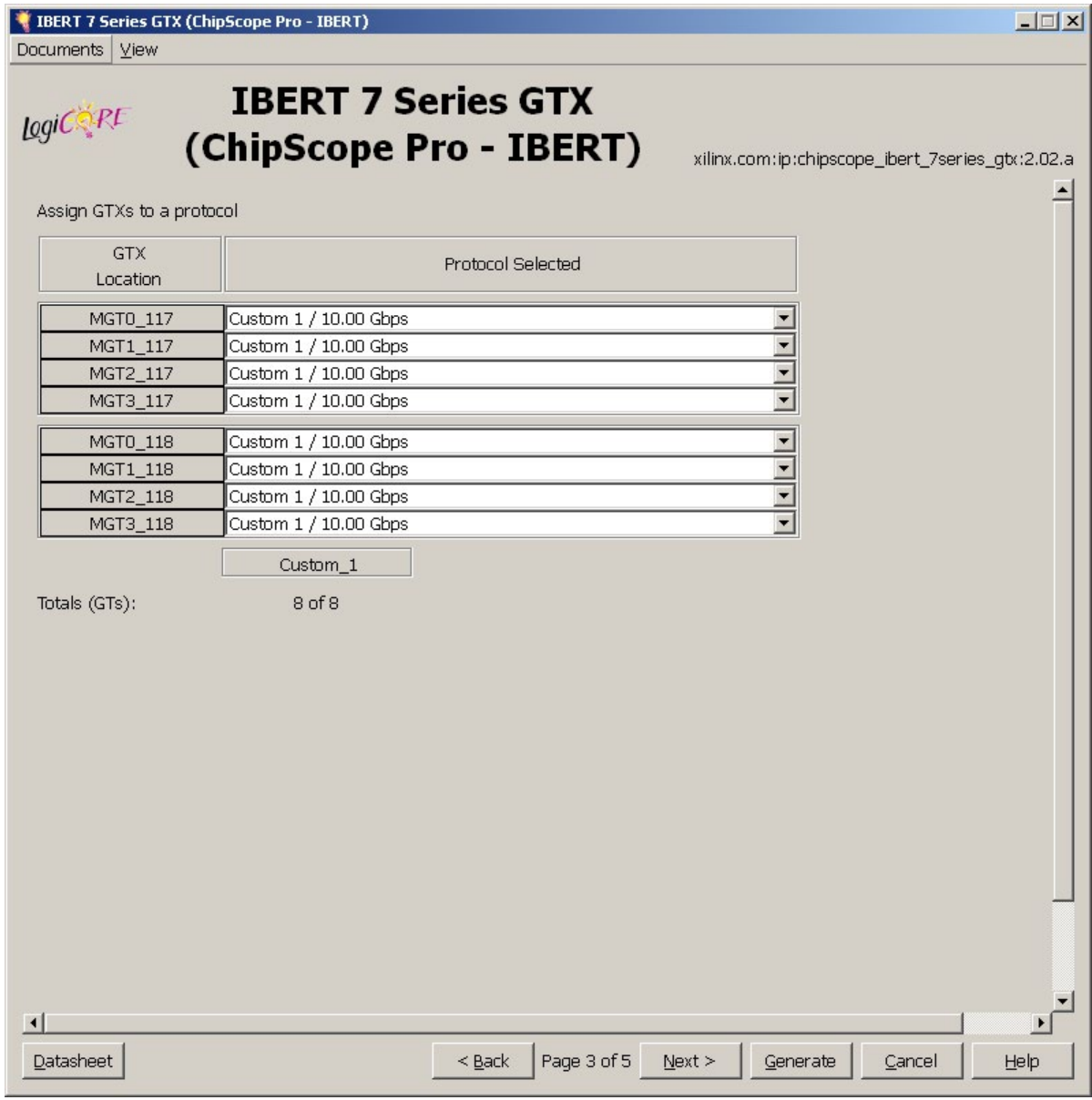
- **Make the following settings:**
  - Select: **Independent TX/RX User Clocking**
  - No. of Quads: **2**
  - Select: **QUAD 117** and **QUAD 118**
  - Max Rate (Gbps): **10.00**
  - Refclk (MHz): **125.000**
  - GTX Count: **8**
- **Click Next**




**Note:** Presentation applies to the KC705

# Create IBERT Design for Banks 117, 118

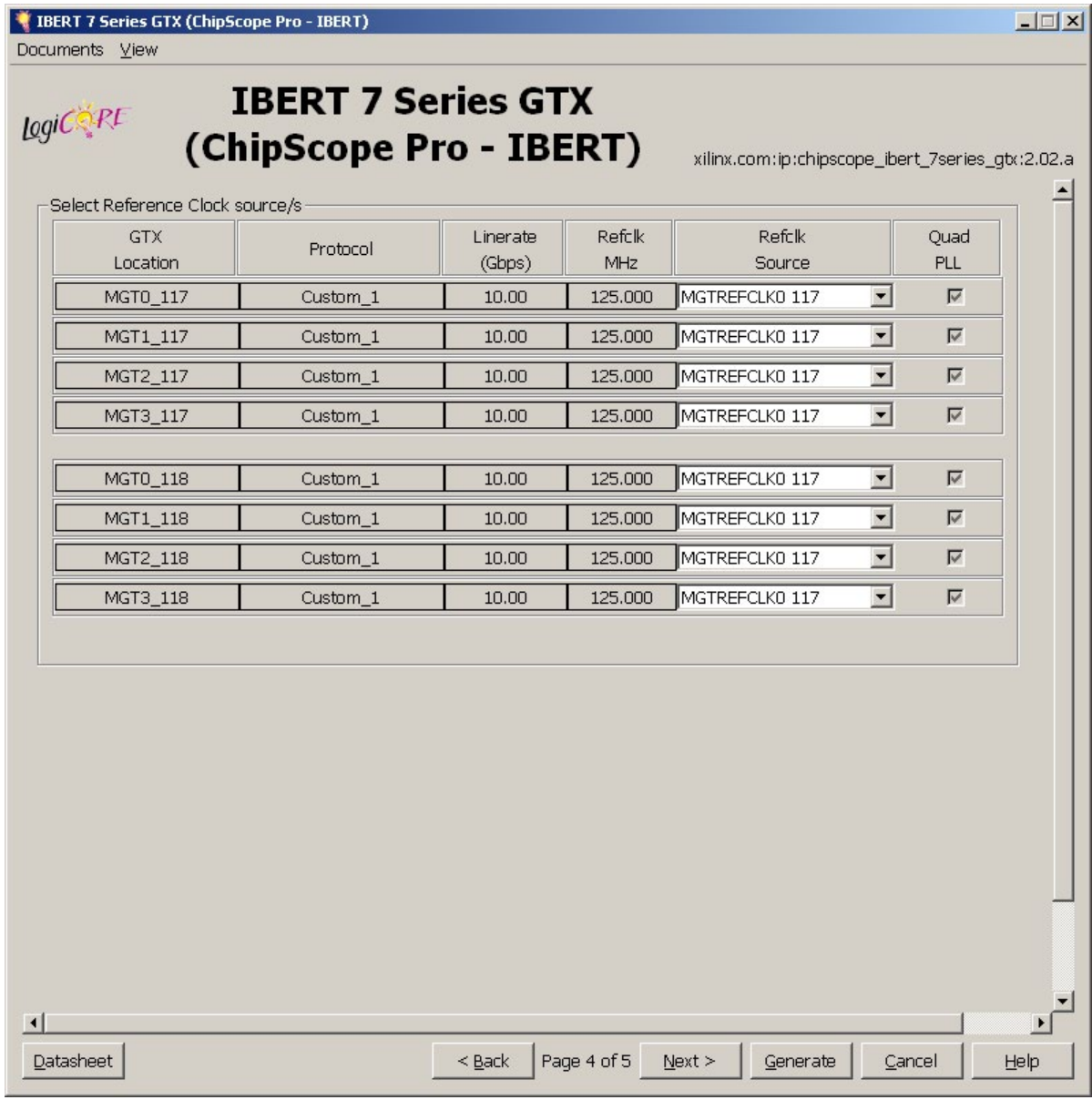
- **Set Banks 117 and 118 to:**
  - Custom 1 / 10.00 Gbps
- **Click Next**




**Note:** Presentation applies to the KC705

# Create IBERT Design for Banks 117, 118

- Set Banks 117 and 118 Refclk Sources to:
  - MGTREFCLK0 117
- Click Next

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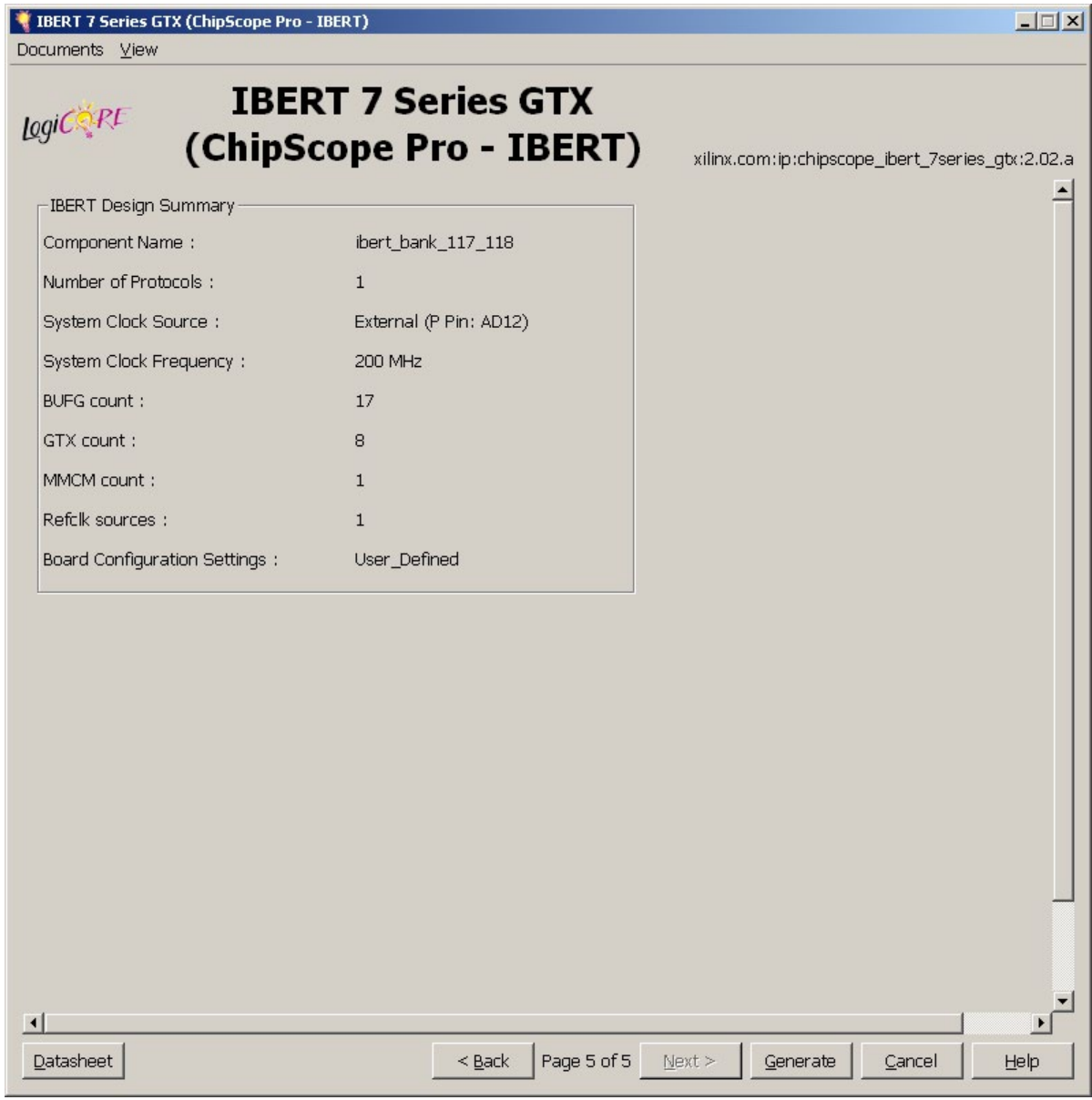
# Create IBERT Design for Banks 117, 118

- Click Generate

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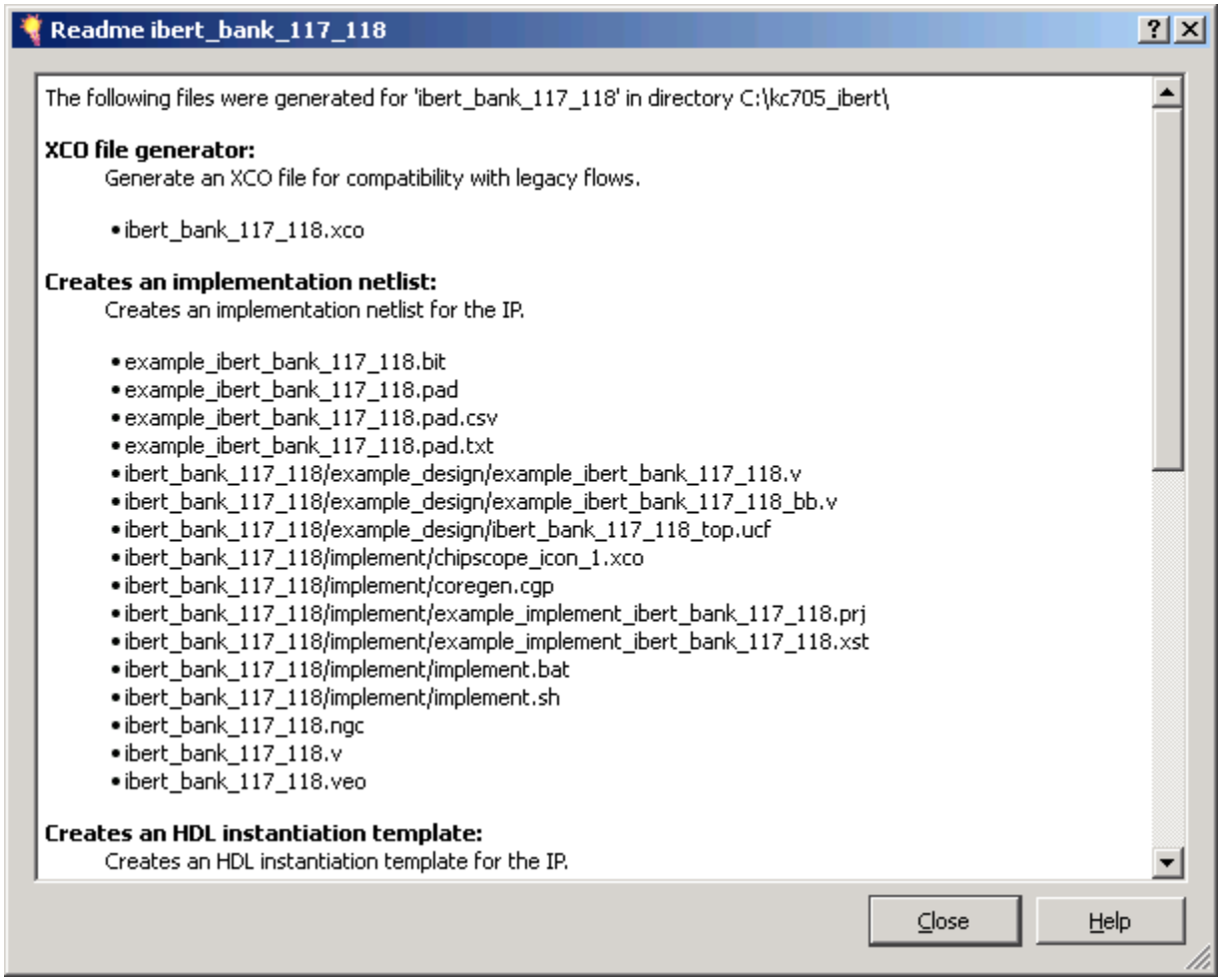
# Create IBERT Design for Banks 117, 118

- After the IBERT core finishes generating, click Close on the Readme File window




**Note:** Presentation applies to the KC705

# Optional Testing with User Provided Hardware

# Optional Testing with User Provided Hardware

- **SMA Cables**
  - www.rosenbergerna.com
  - Part number: 72D-32S1-32S1-00610A


- **SMA Quick connects**
  - RADIALL
  - Part number: R125791501
  - Available here or here

**Note:** Presentation applies to the KC705

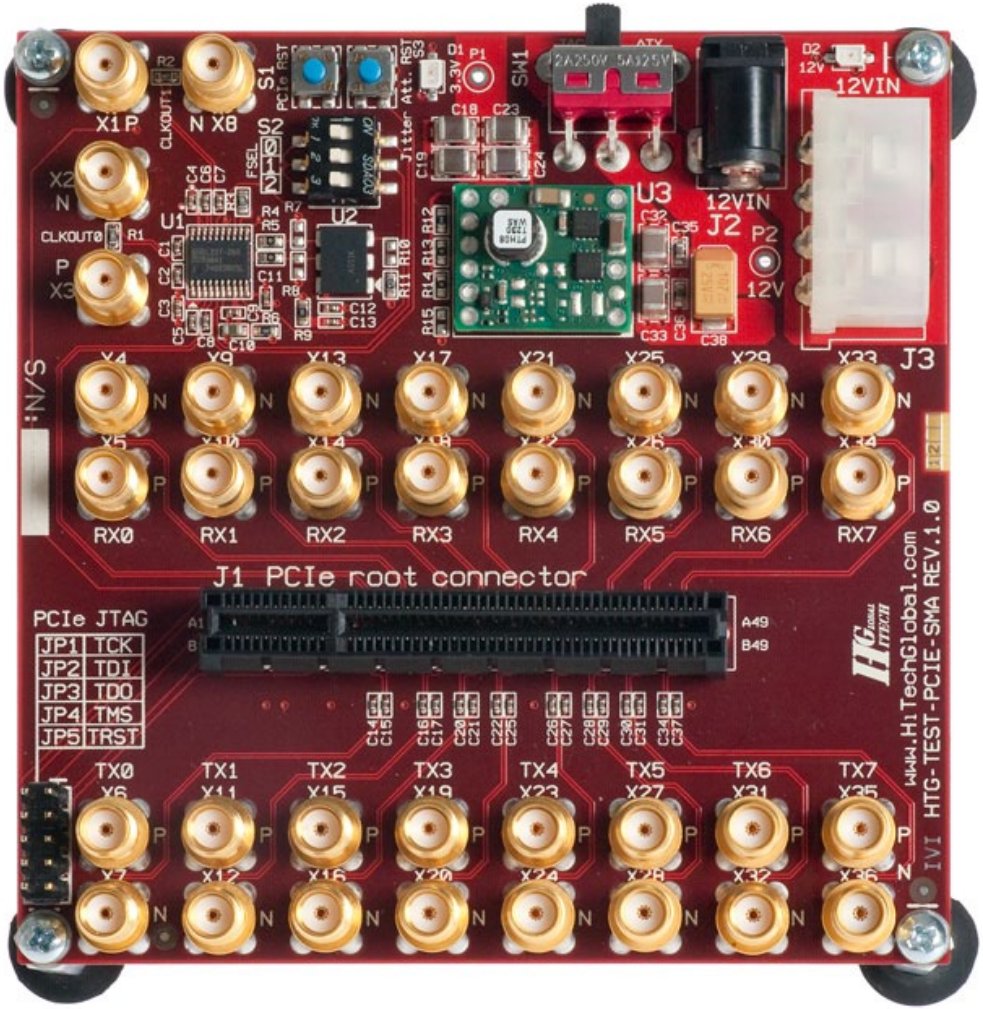
# Optional Testing with User Provided Hardware

- **Connect Optical Loopback Adapter**
  - www.molex.com
  - SFP Loopback Adapter, 5.0 db Attenuation
  - Part # 74765-0904


**Note:** Presentation applies to the KC705

# Optional Testing with User Provided Hardware

- **For testing Banks 115 and 116:**
- **PCIe Testing Hardware:**
  - HiTechGlobal PCI Express Test & SerialIO Expansion Module
  - HTG-TEST-PCIE-SMA
  - 16 SMA cables required
  - Requires power supply, either:
    - 4-pin Peripheral power connector from ATX power supply
  - Or:
    - HiTechGlobal PWR-12V-6A




**Note:** Presentation applies to the KC705

# Testing Banks 115 and 116 with Optional User Provided Hardware

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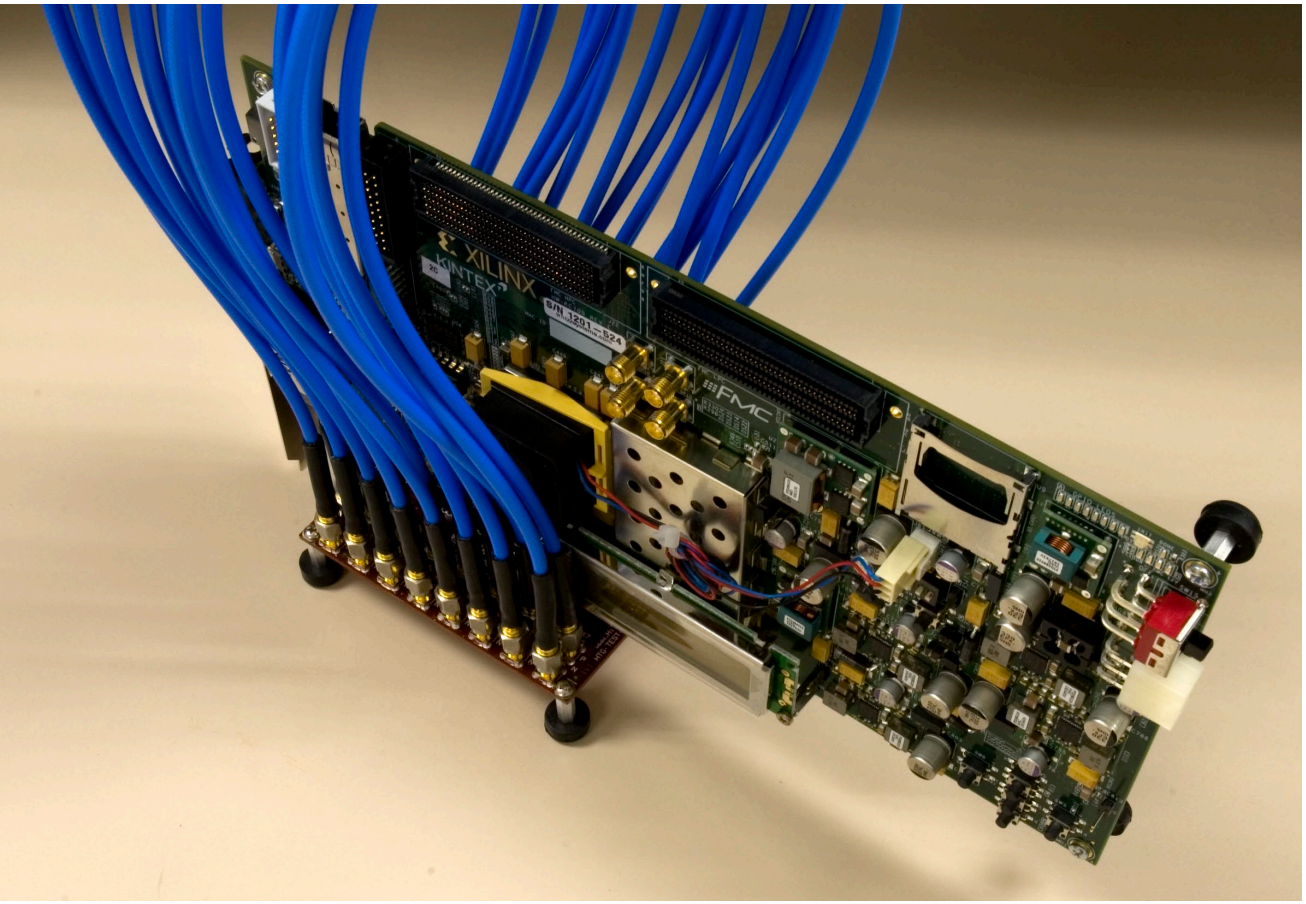
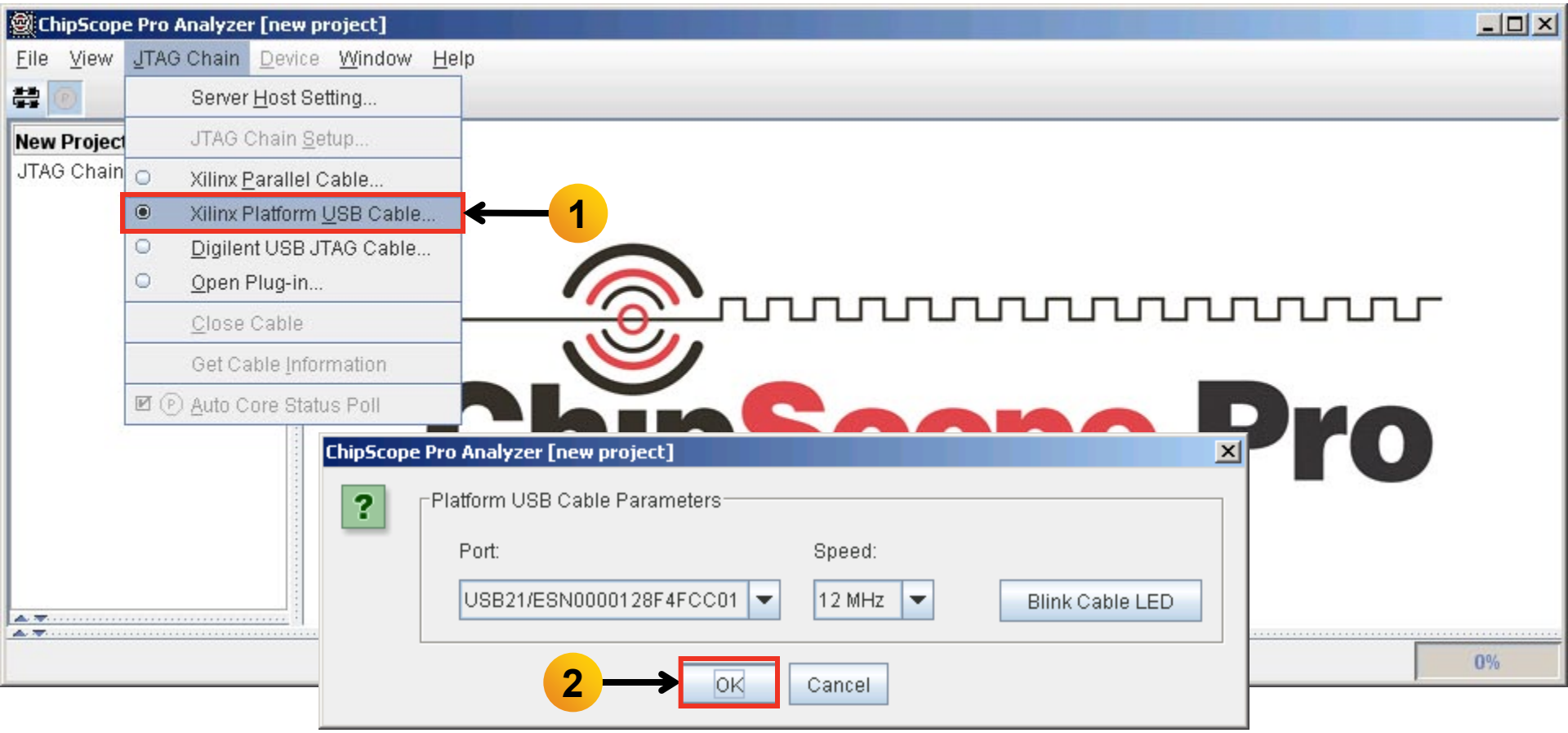



- **Connect SMA Cables:**
  - TX0 P/N to RX0 P/N, TX1 P/N to RX1 P/N, etc.
- **Insert KC705 into PCIe slot**
- **Connect the KC705 and HiTechGlobal power supplies**
- **Power up the KC705 and HiTechGlobal boards**

**Note:** Presentation applies to the KC705

# Testing Banks 115 and 116 with Optional User Provided Hardware

- Open ChipScope Pro and select JTAG Chain → USB Cable… (1)
- Click OK (2)

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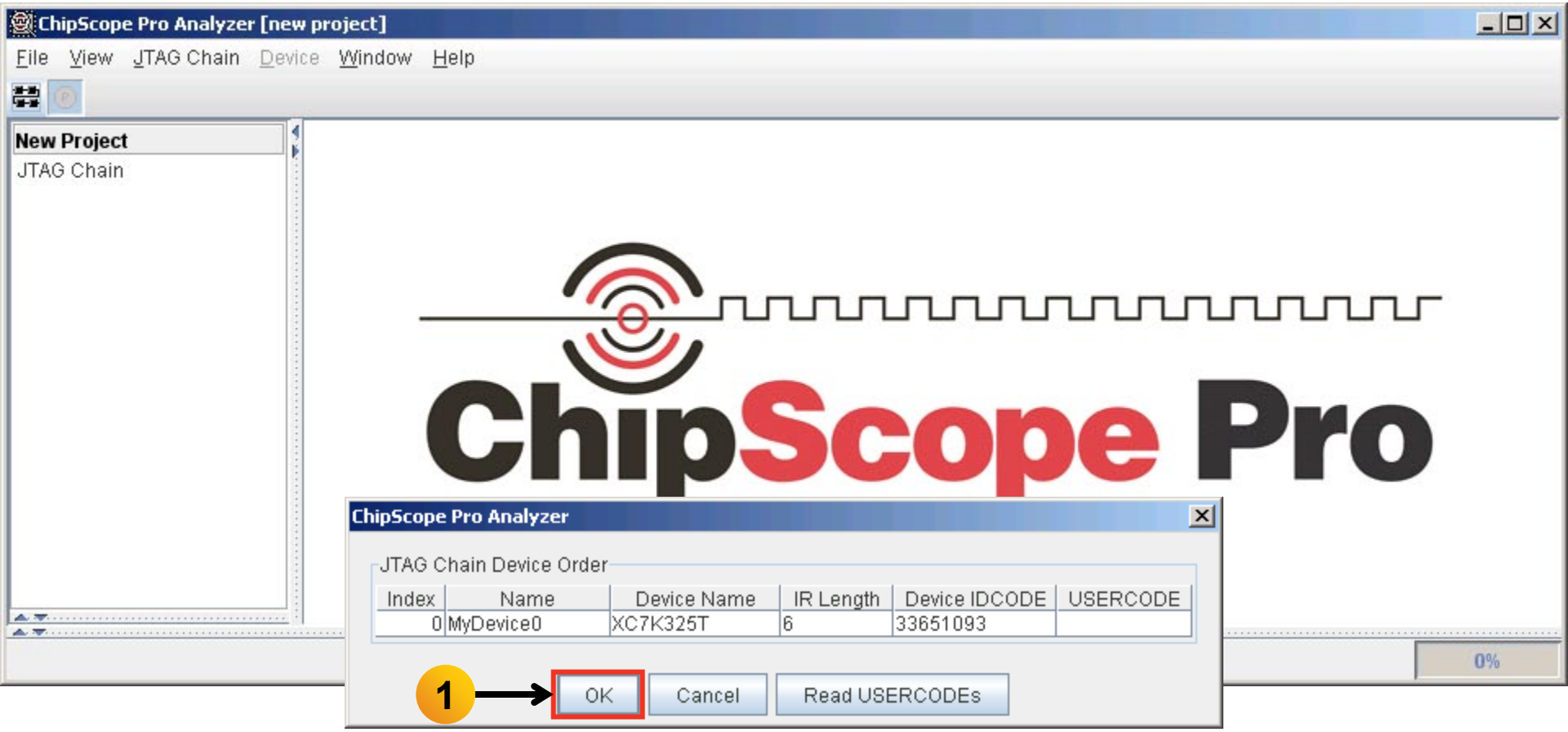
# Testing Banks 115 and 116 with Optional User Provided Hardware

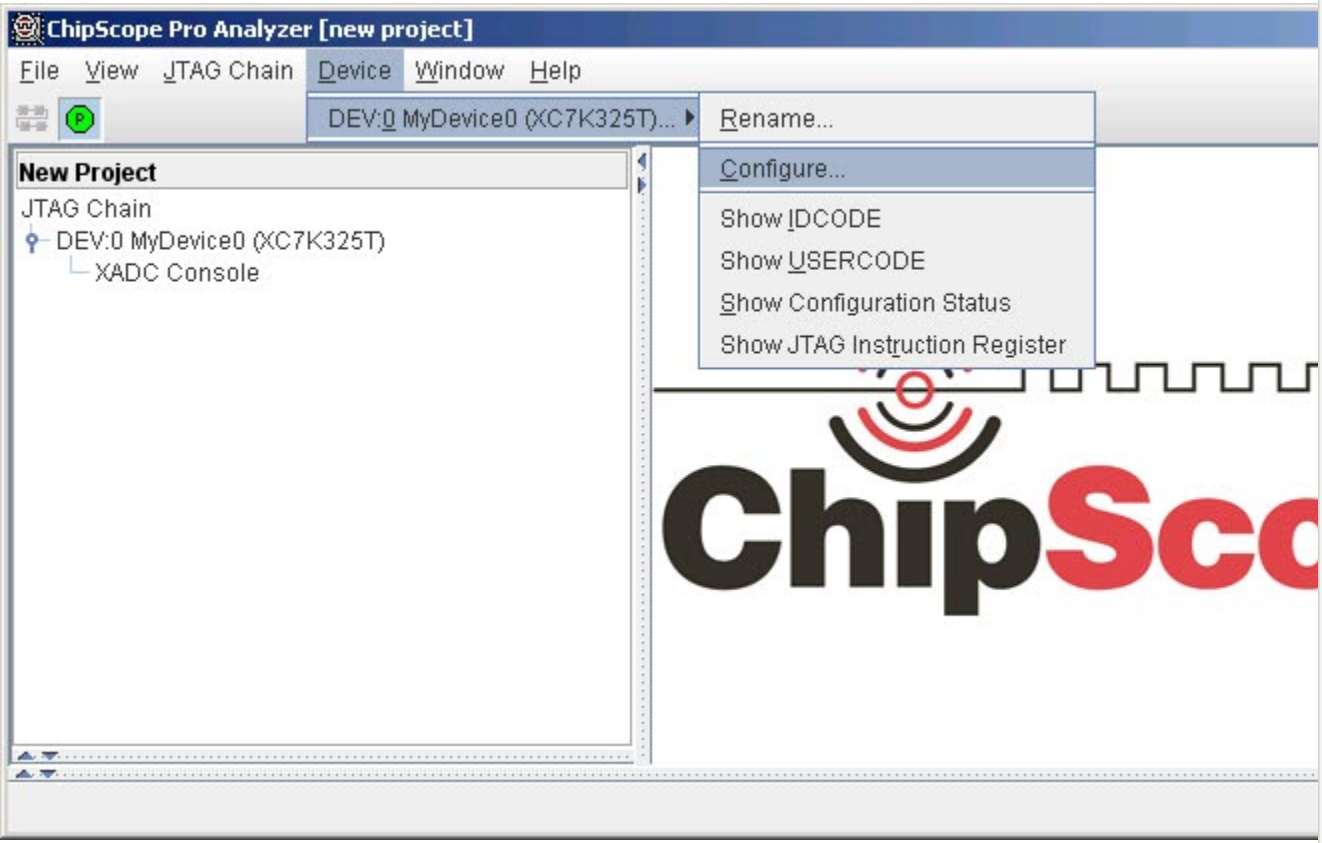
- Click OK (2)

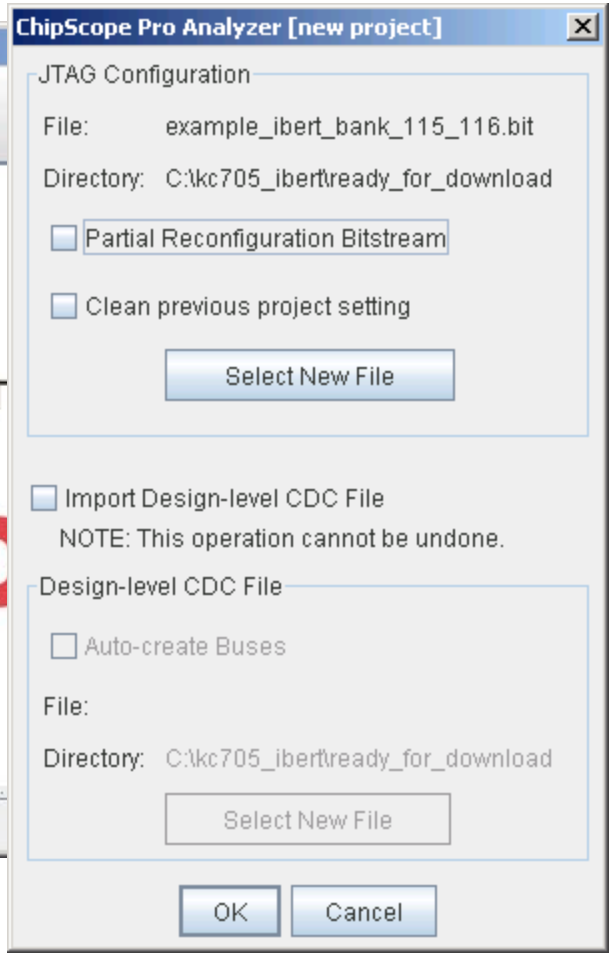



**Note:** Presentation applies to the KC705

# Testing Banks 115 and 116 with Optional User Provided Hardware

- Select Device → DEV:0 MyDevice0 (XC7K325T)… → Configure…
- Select <Design Path>\ready_for_download\ example_ibert_bank_115_116.bit

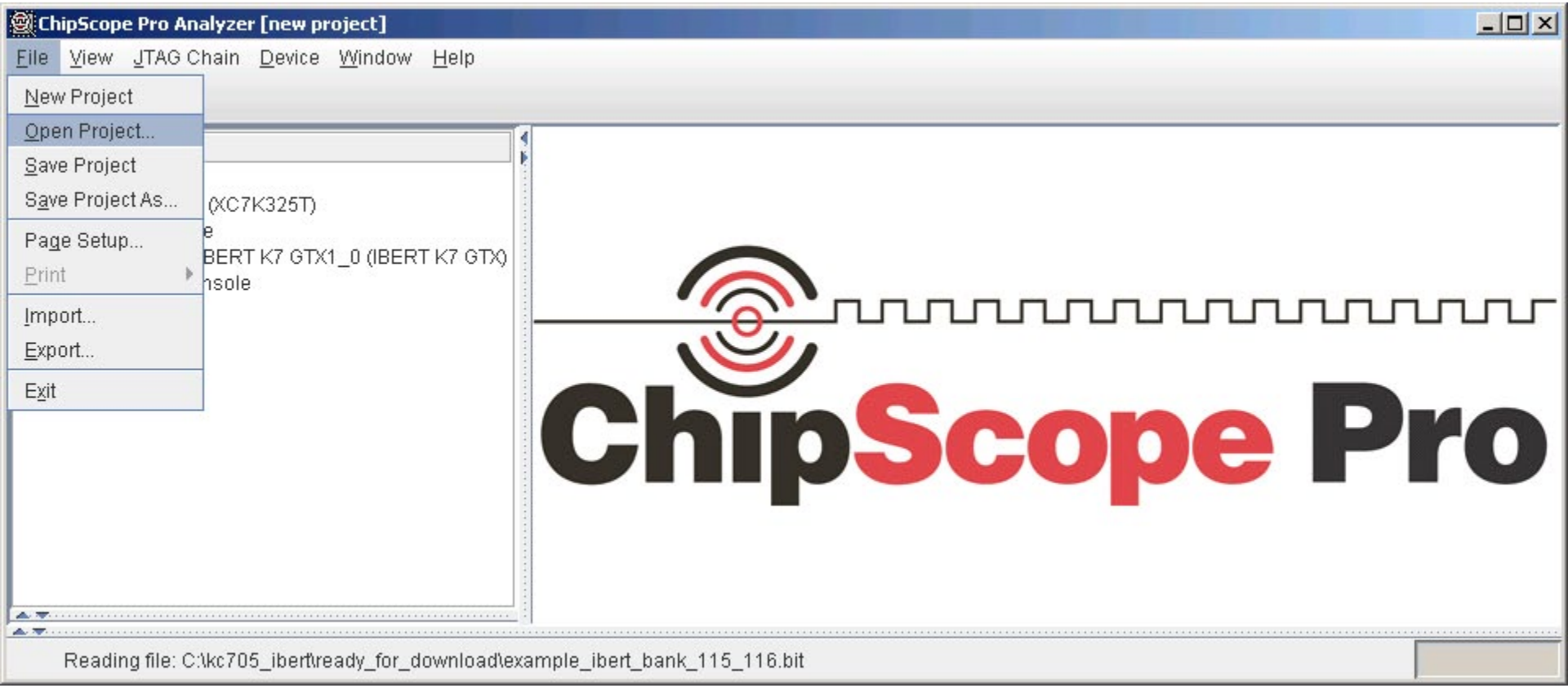



**Note:** Presentation applies to the KC705

# Testing Banks 115 and 116 with Optional User Provided Hardware

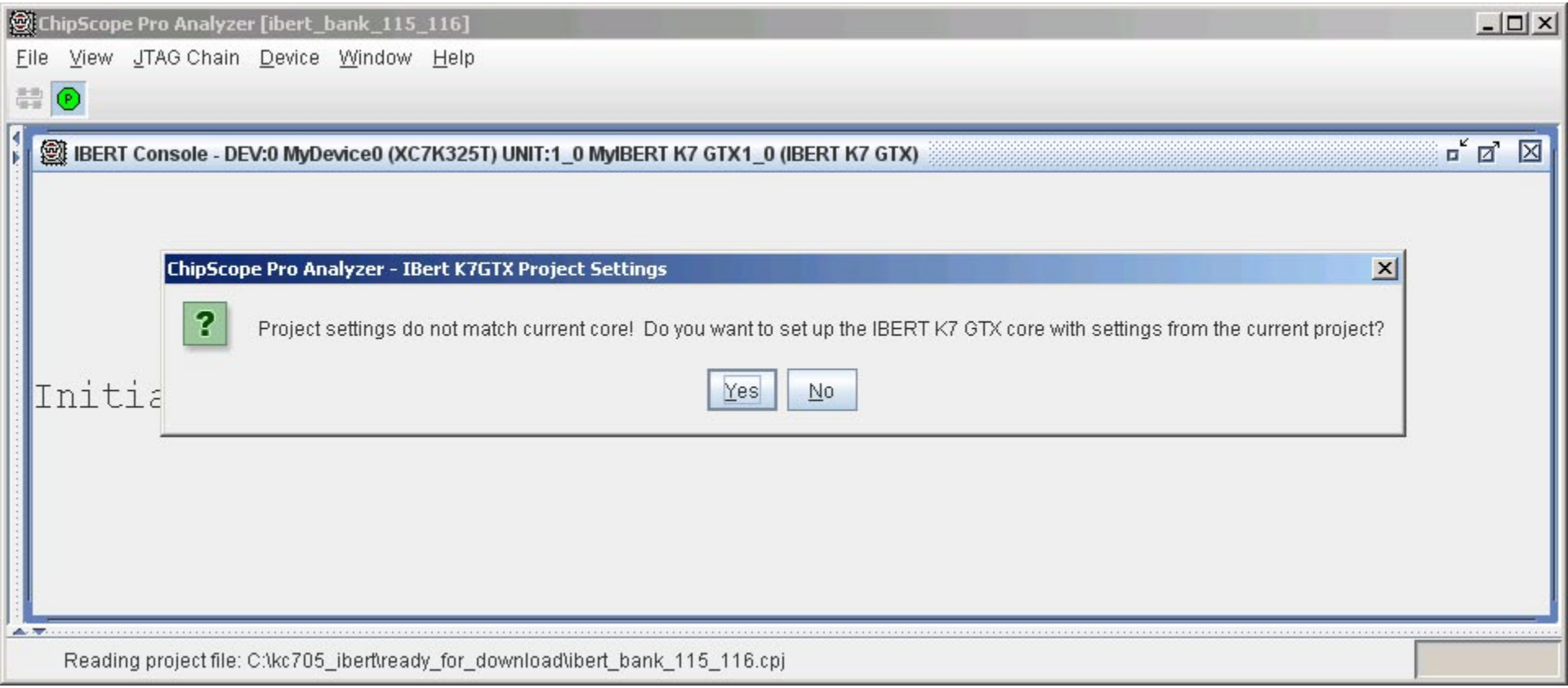
- Select File → Open Project…
- Select <Design Path>\ready_for_download\ibert_bank115_116.cpj




**Note:** Presentation applies to the KC705

# Testing Banks 115 and 116 with Optional User Provided Hardware

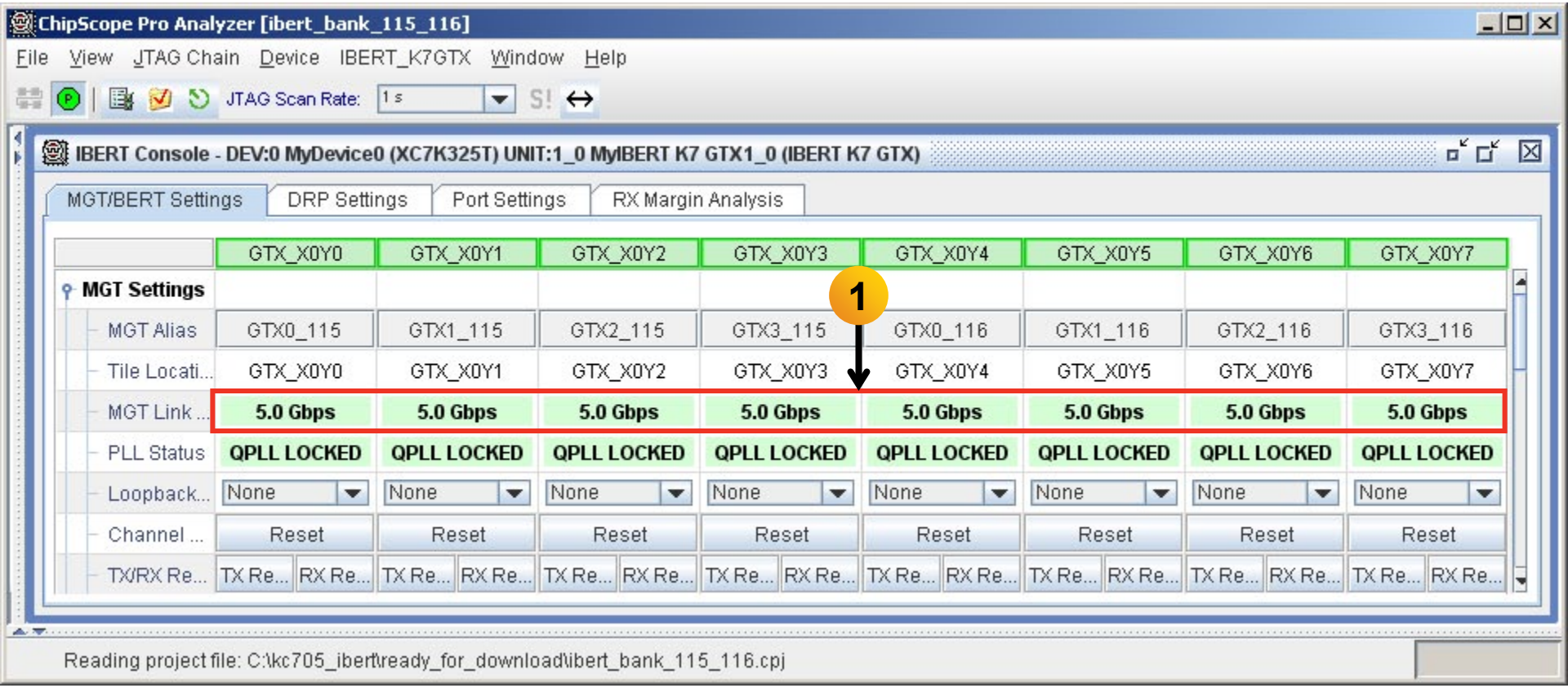
- Click Yes on this Dialog




**Note:** Presentation applies to the KC705

# Testing Banks 115 and 116 with Optional User Provided Hardware

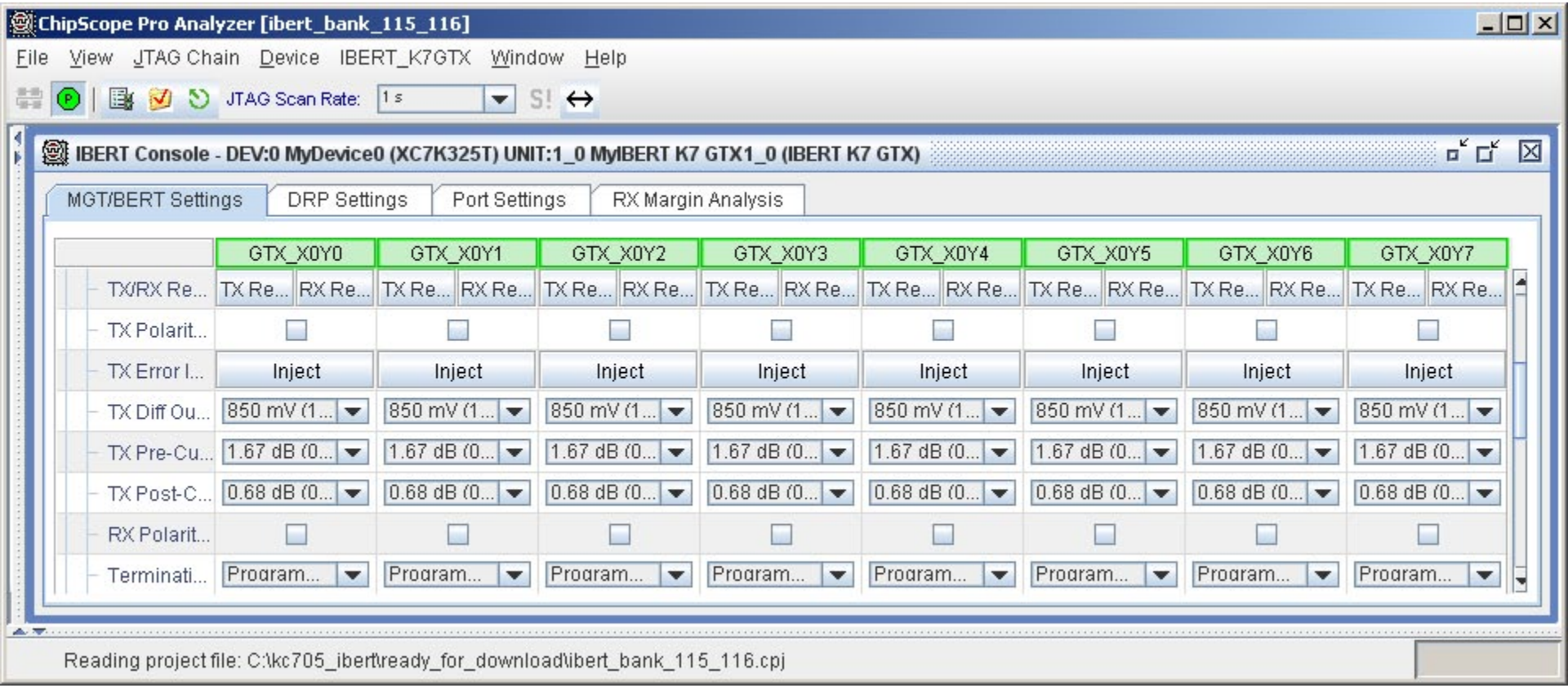
- The line rate is 5.0 Gbps for all GTXs (1)




**Note:** Bank 115, 116: PCIe

# Testing Banks 115 and 116 with Optional User Provided Hardware

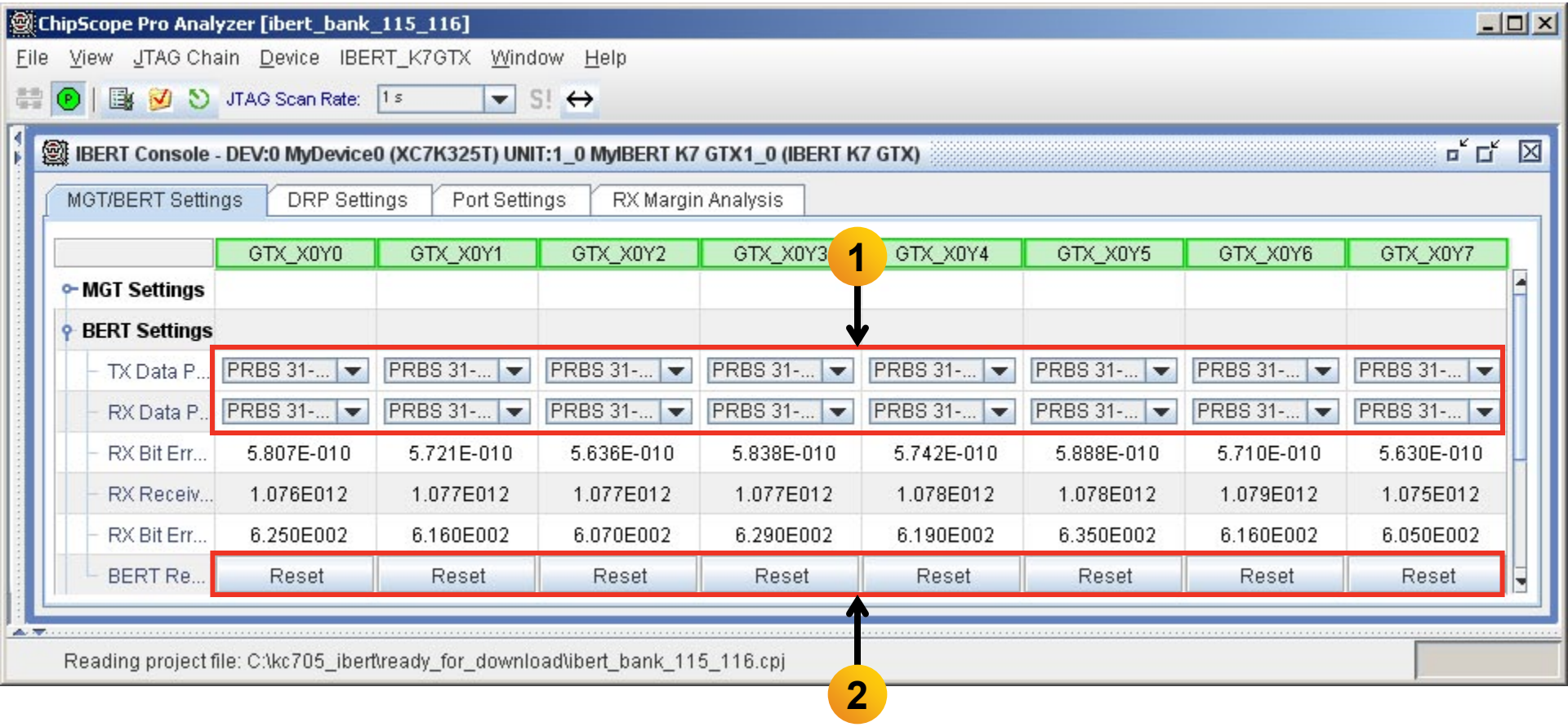
- TX Diff Output Swing = 850 mV
- TX Pre-Cursor = 1.67 dB; TX Post-Cursor = 0.68 dB




**Note:** Presentation applies to the KC705

# Testing Banks 115 and 116 with Optional User Provided Hardware

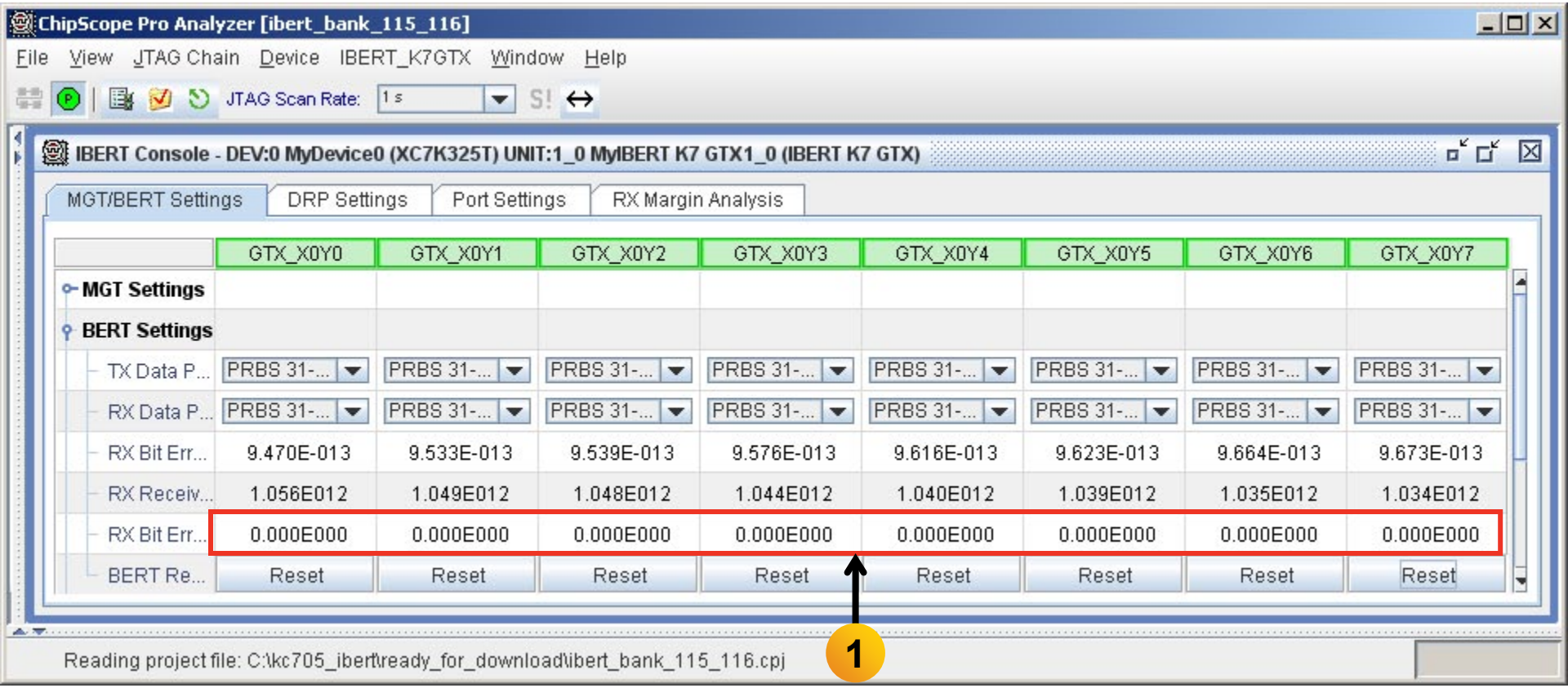
- TX/RX Data Patterns are set to PRBS 31-bit (1)
- Click BERT Reset buttons (2)




**Note:** Presentation applies to the KC705

# Testing Banks 115 and 116 with Optional User Provided Hardware

- View the RX Bit Error Count (1)

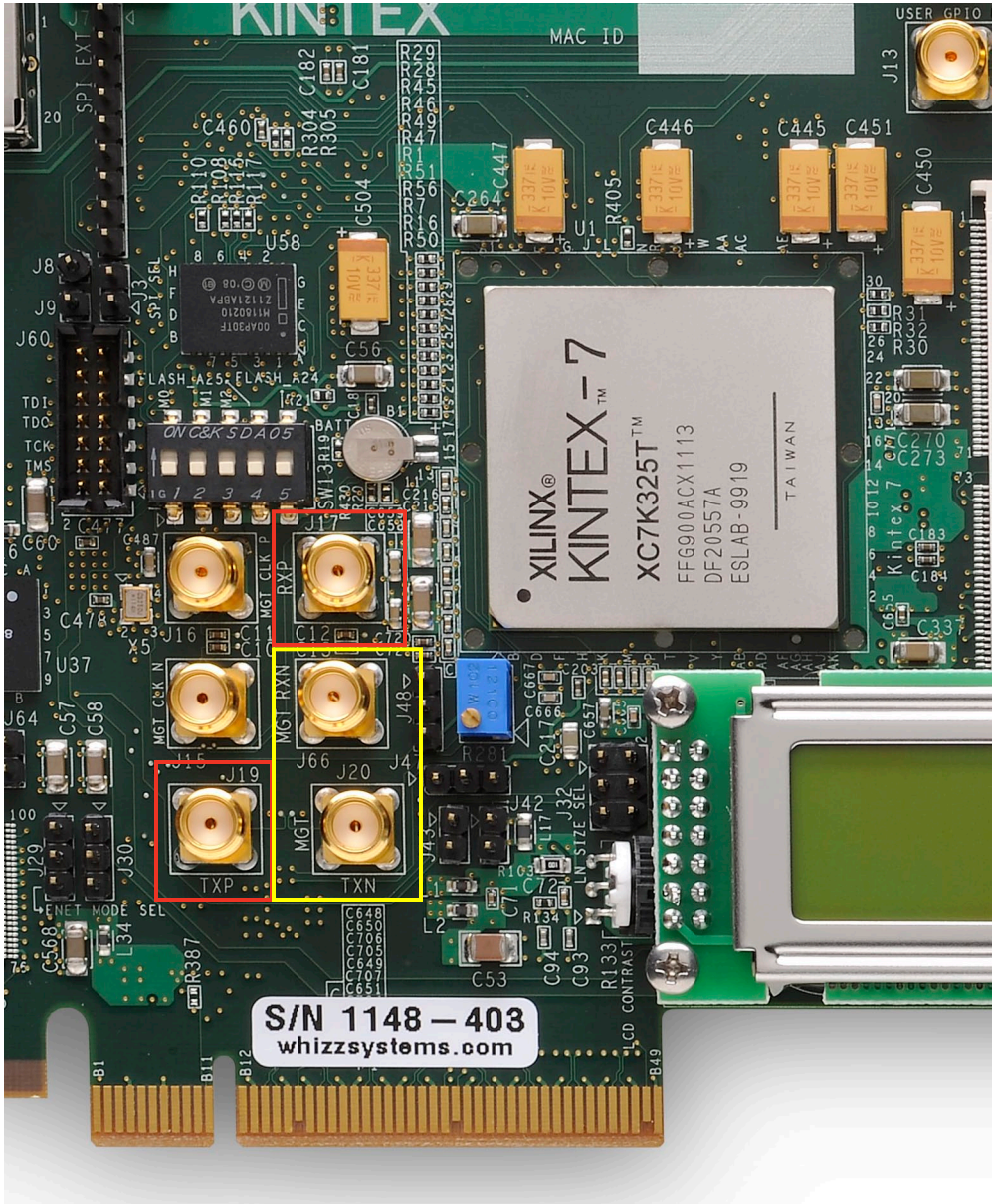



**Note:** Presentation applies to the KC705

# Testing Bank 117 and 118 with Optional User Provided Hardware

# Testing Bank 117 and 118 with Optional User Provided Hardware

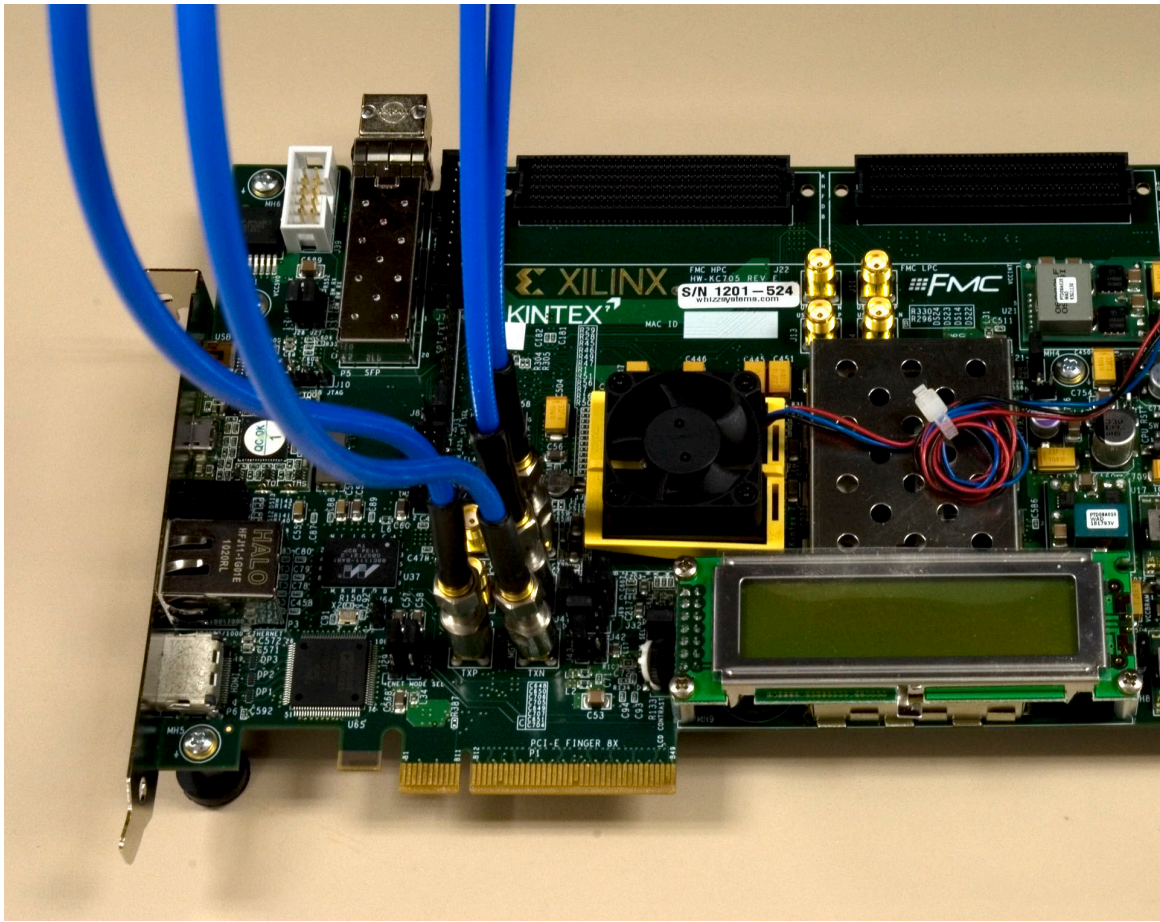
- **Using the SMA cables:**
  - Connect J19 to J17
  - Connect J20 to J66




**Note:** Presentation applies to the KC705

# Testing Bank 117 and 118 with Optional User Provided Hardware

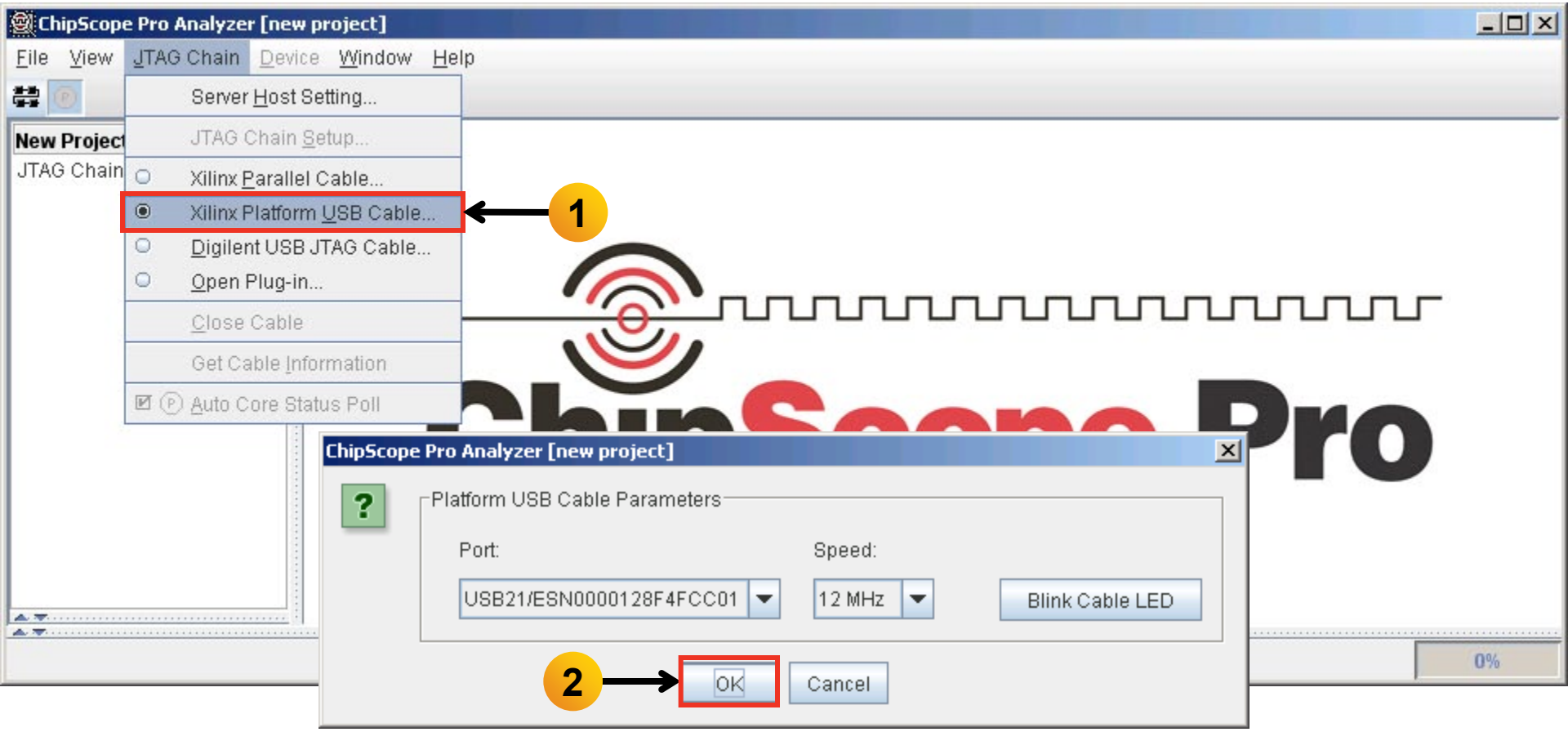
- Insert the SFP Loopback Adapter
- Power on the KC705 board




**Note:** Presentation applies to the KC705

# Testing Bank 117 and 118 with Optional User Provided Hardware

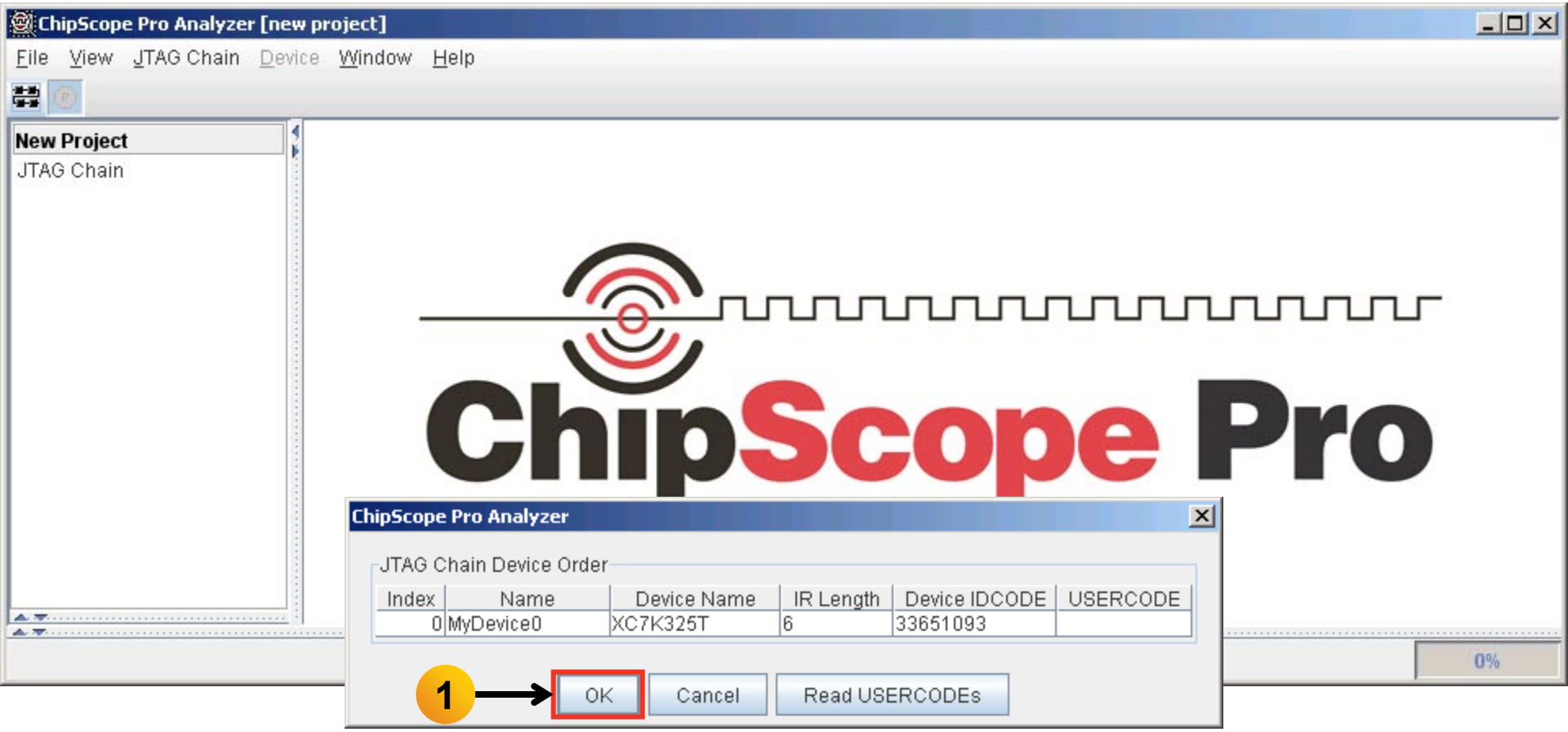
- Open ChipScope Pro and select JTAG Chain → USB Cable… (1)
- Click OK (2)




**Note:** Presentation applies to the KC705

# Testing Bank 117 and 118 with Optional User Provided Hardware

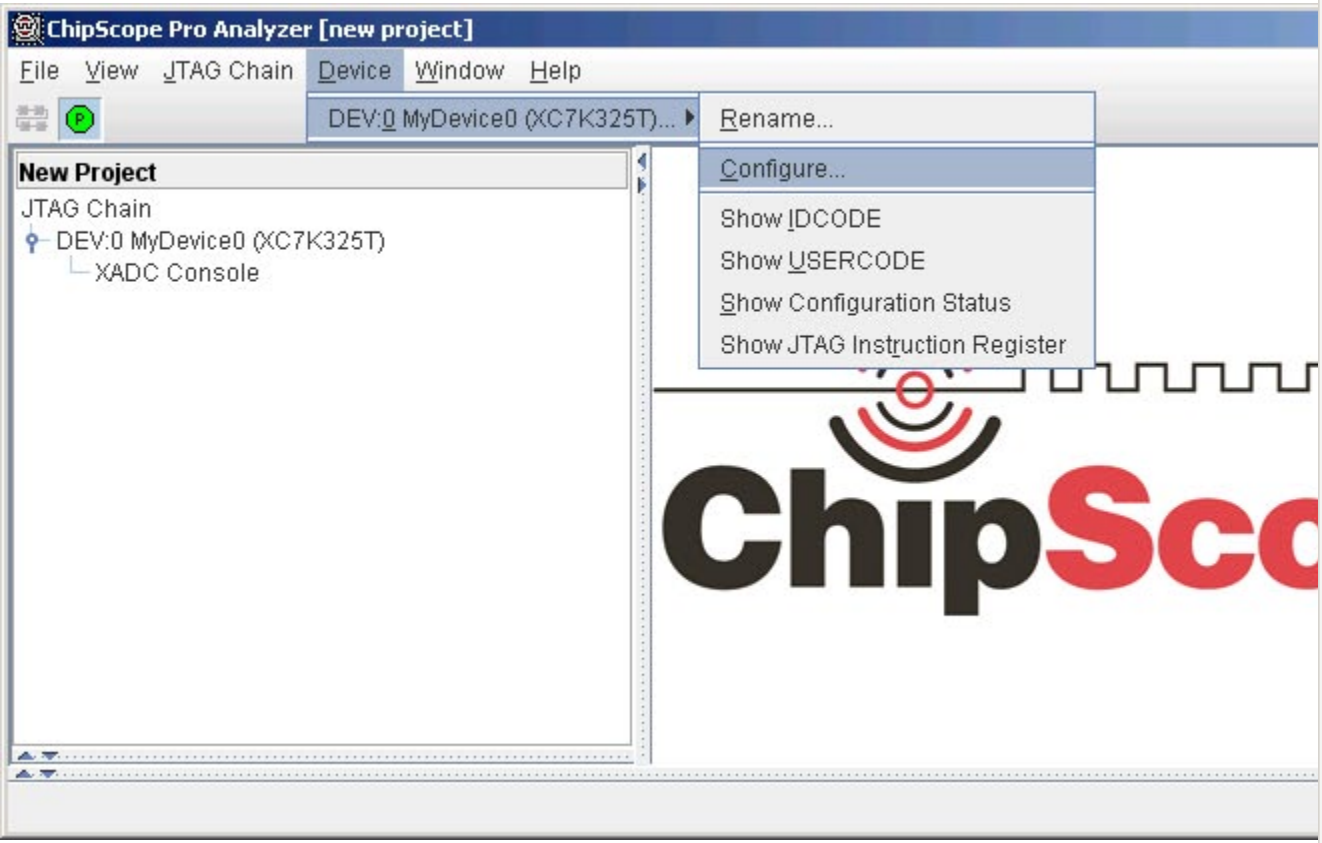
- Click OK (1)

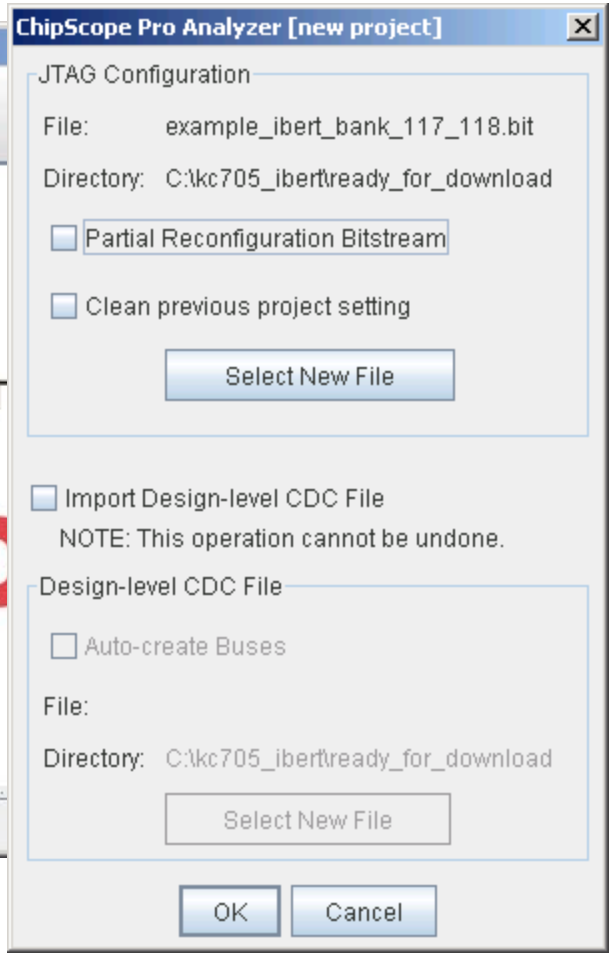



**Note:** Presentation applies to the KC705

# Testing Bank 117 and 118 with Optional User Provided Hardware

- Select Device → DEV:0 MyDevice0 (XC7K325T)… → Configure…
- Select <Design Path>\ready_for_download\ example_ibert_bank_117_118.bit

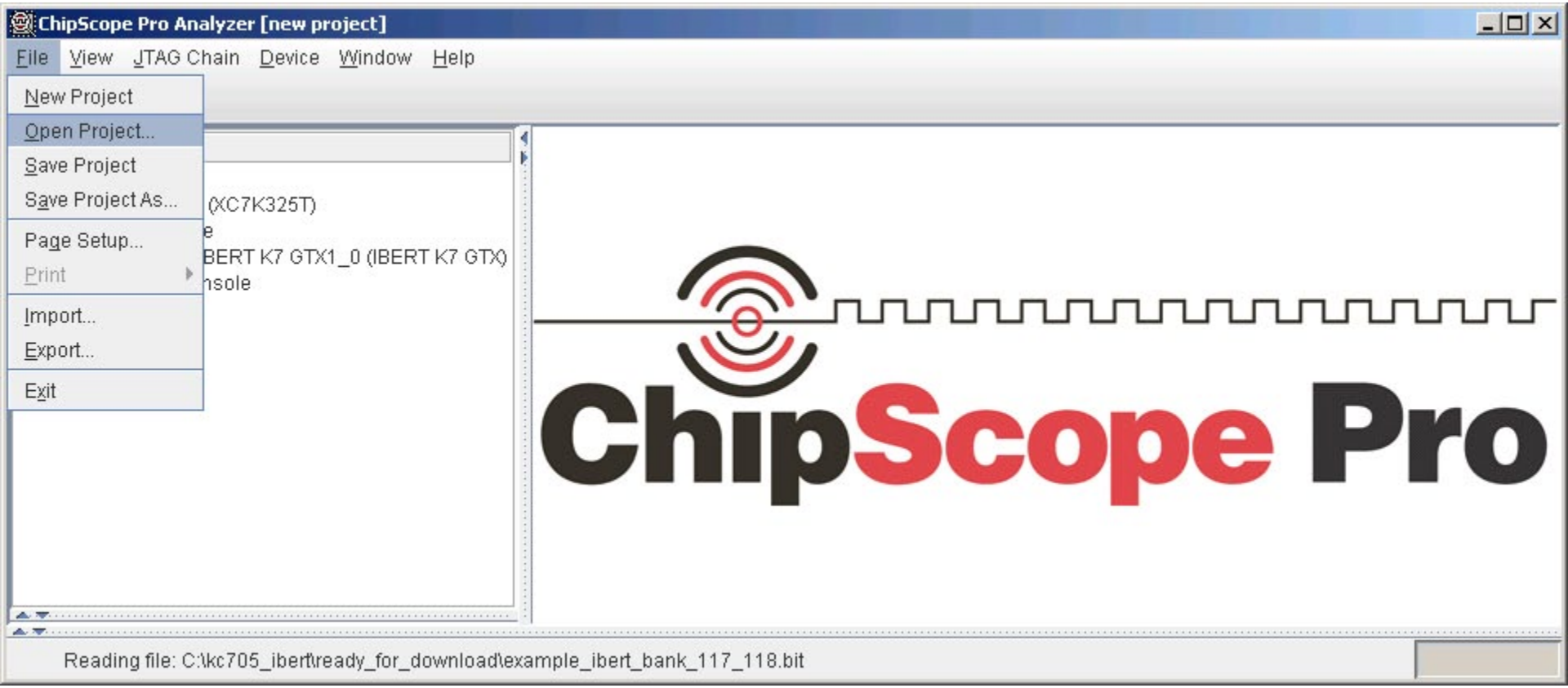



**Note:** Presentation applies to the KC705

# Testing Bank 117 and 118 with Optional User Provided Hardware

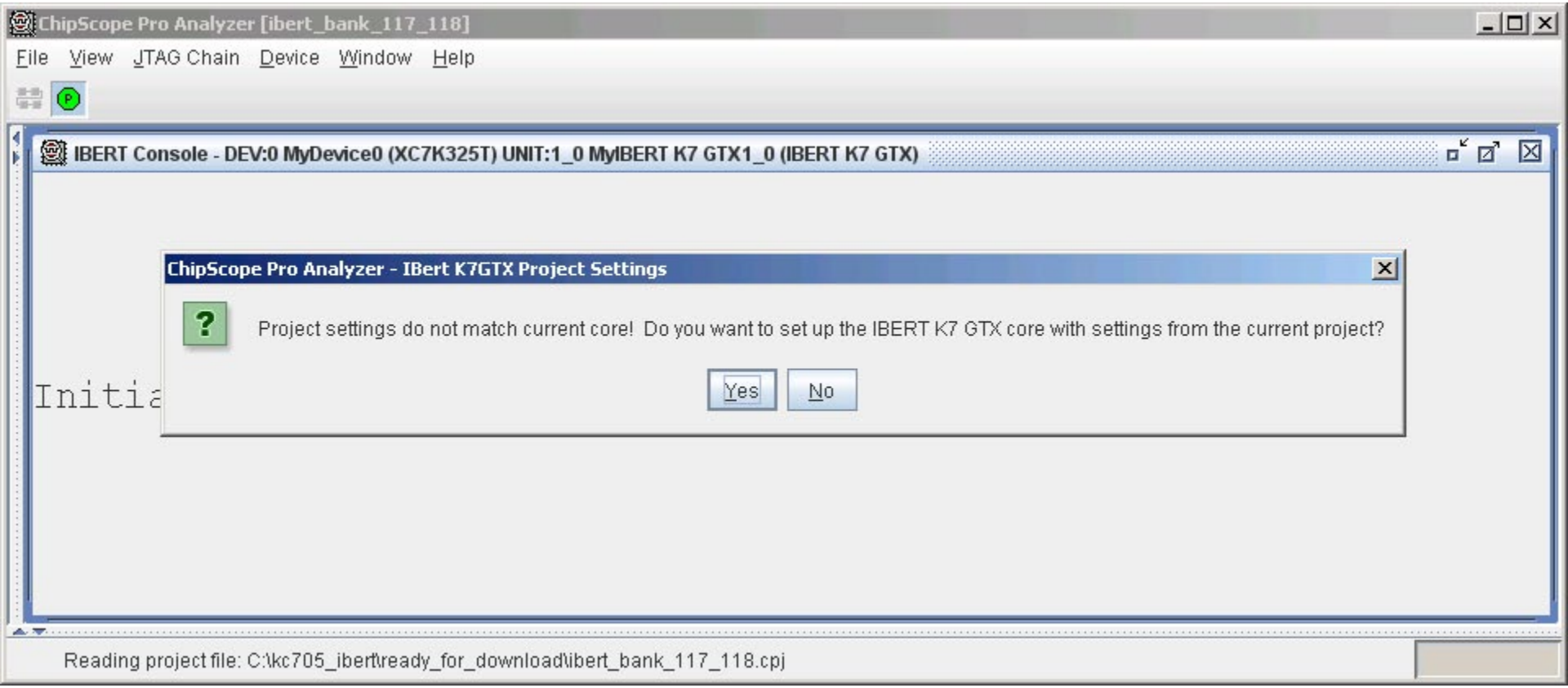
- Select File → Open Project…
- Select <Design Path>\ready_for_download\ibert_bank117_118.cpj




**Note:** Presentation applies to the KC705

# Testing Bank 117 and 118 with Optional User Provided Hardware

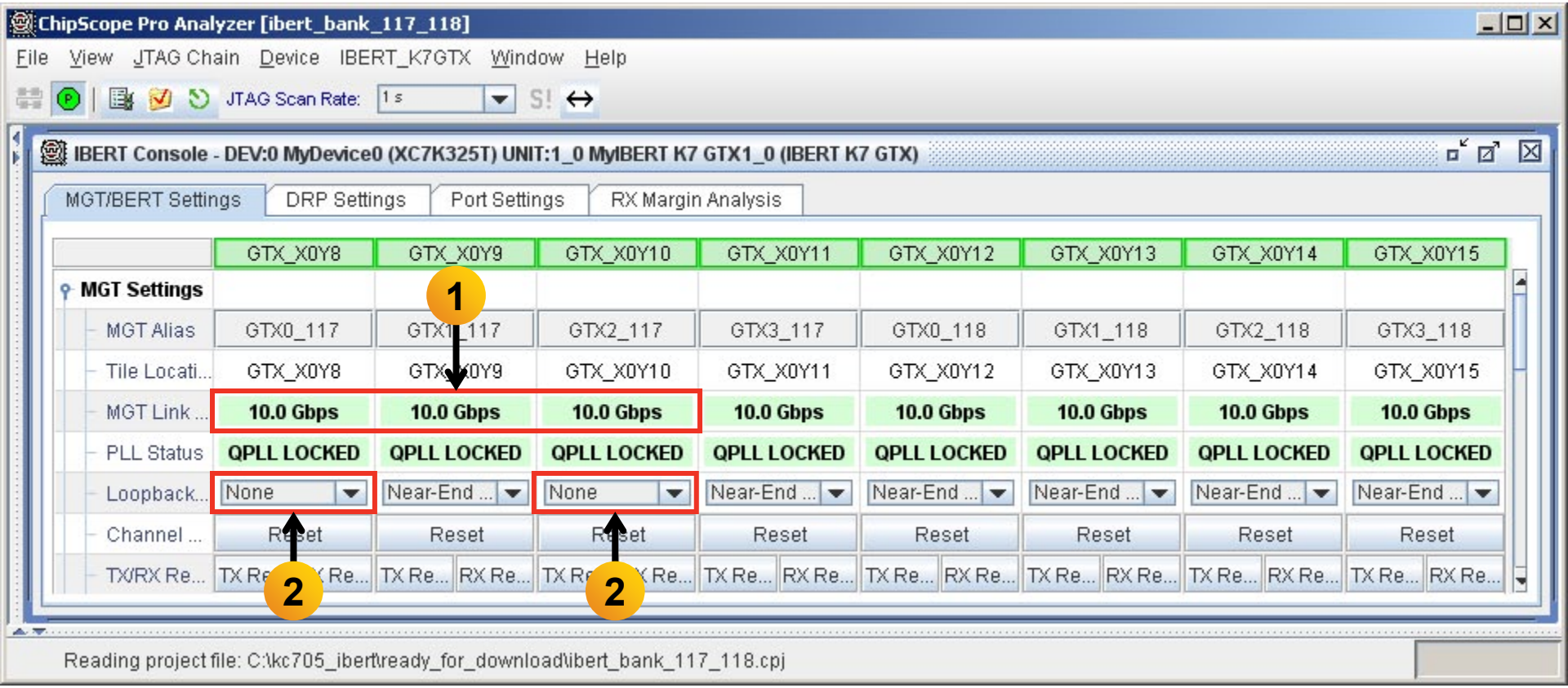
- Click Yes on this Dialog




**Note:** Presentation applies to the KC705

# Testing Bank 117 and 118 with Optional User Provided Hardware

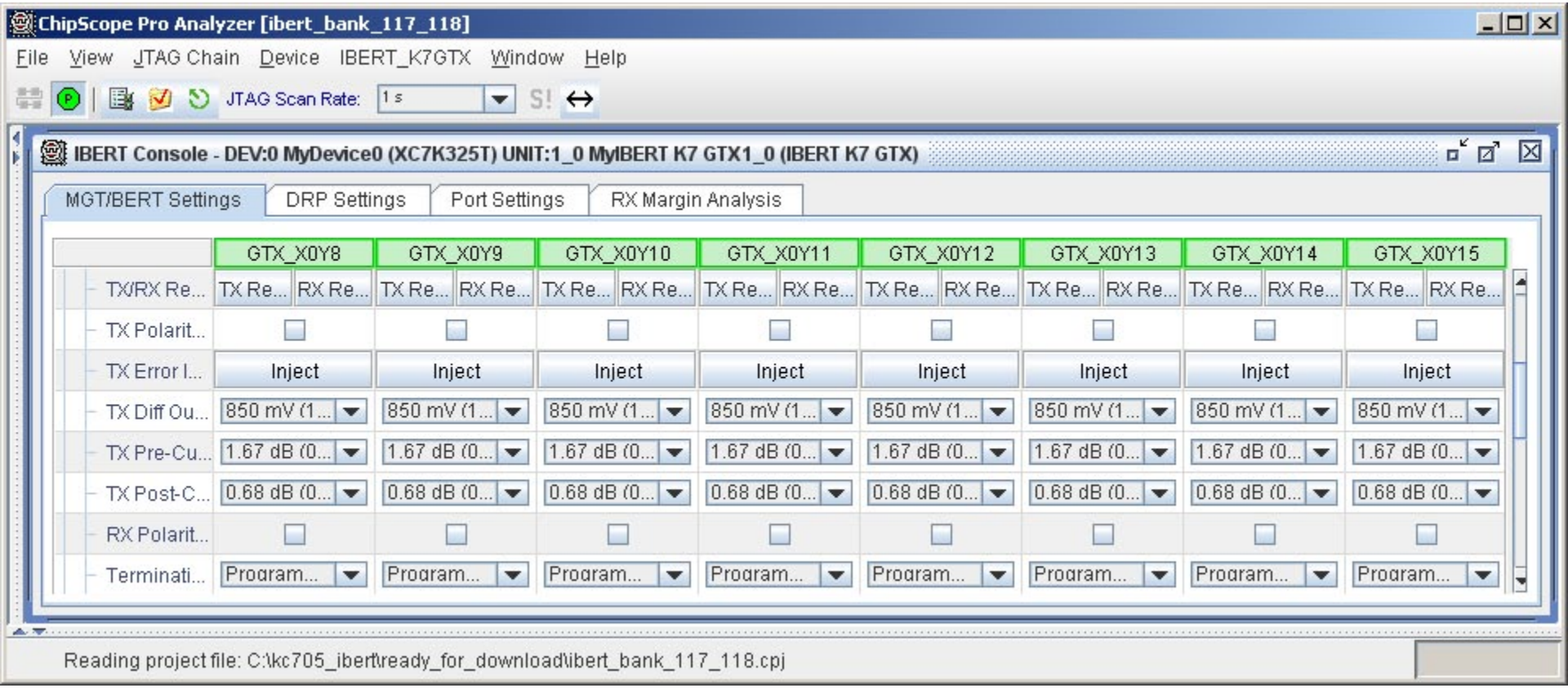
- The line rate is 10.0 Gbps for all GTXs (1)
- Set GTX0_117 and GTX2_117 to None (2)




**Note:** Bank 117,118: SMA, SGMII, SFP, FMC

# Testing Bank 117 and 118 with Optional User Provided Hardware

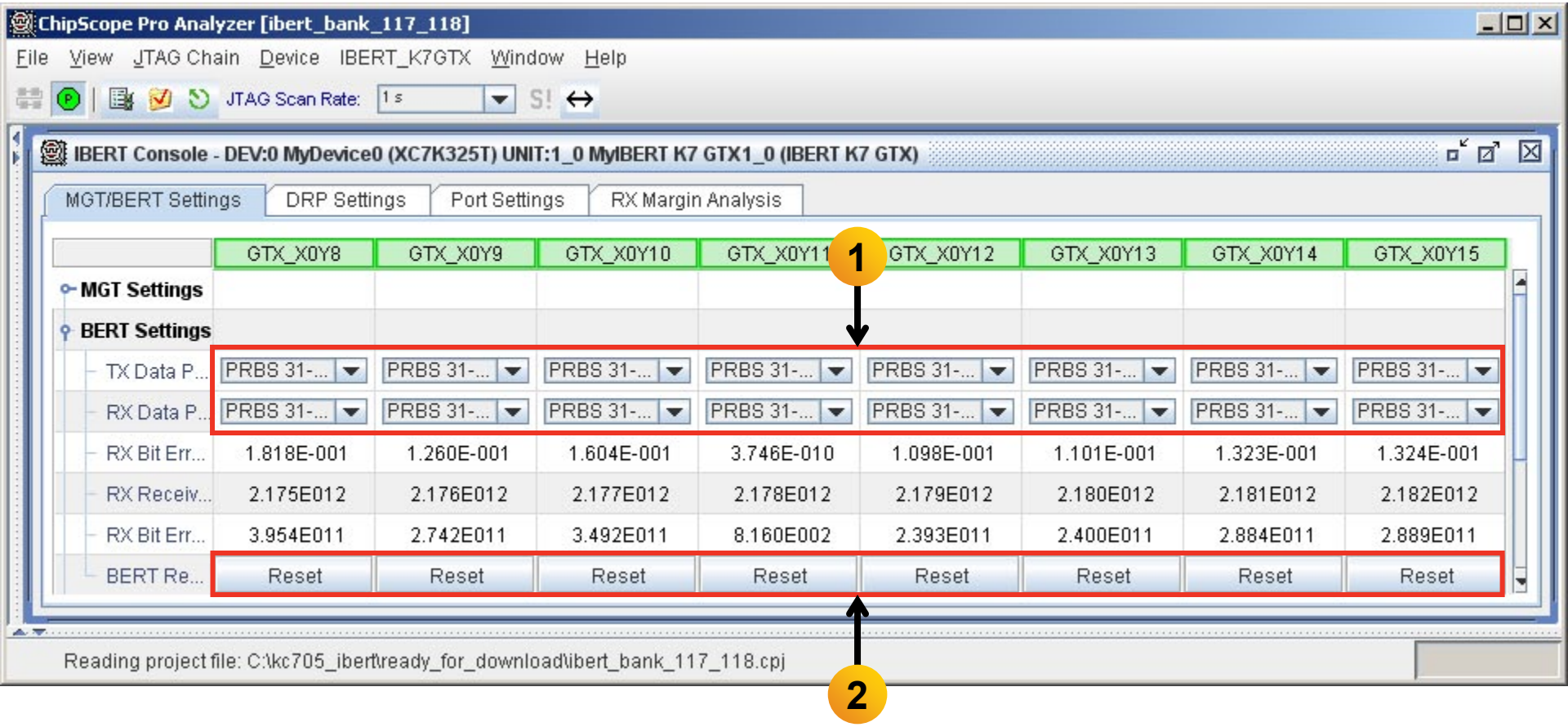
- TX Diff Output Swing = 850 mV
- TX Pre-Cursor = 1.67 dB; TX Post-Cursor = 0.68 dB




**Note:** Presentation applies to the KC705

# Testing Bank 117 and 118 with Optional User Provided Hardware

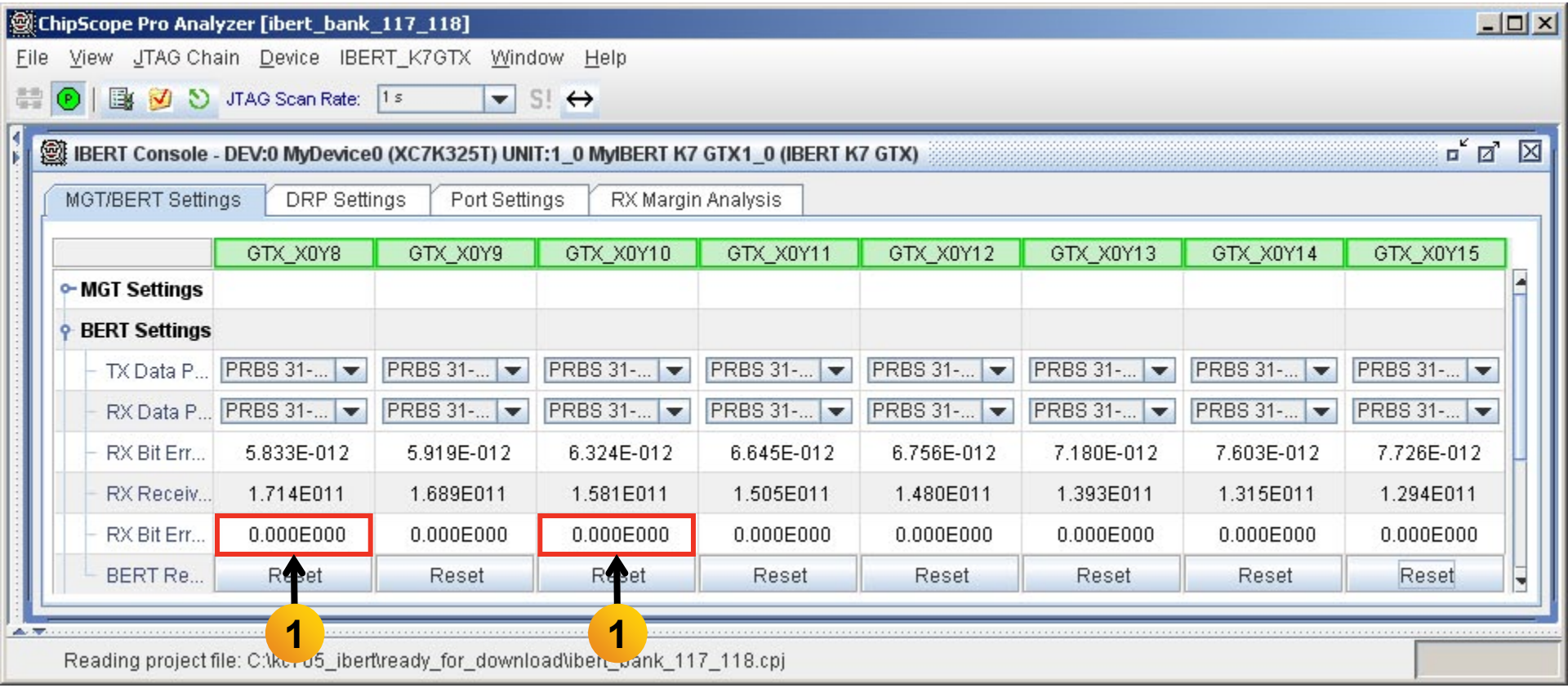
- TX/RX Data Patterns are set to PRBS 31-bit (1)
- Click BERT Reset buttons (2)




**Note:** Presentation applies to the KC705

# Testing Bank 117 and 118 with Optional User Provided Hardware

- View the RX Bit Error Count on the SMA and SFP (1)




**Note:** Presentation applies to the KC705

# References

# References

- **ChipScope Pro**
  - ChipScope Pro Software and Cores User Guide
    - http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_3/chipscope_pro_sw_cores_ug029.pdf

# Documentation

# Documentation

- **Kintex-7**
  - Kintex-7 FPGA Family
    - http://www.xilinx.com/products/silicon-devices/fpga/kintex-7/index.htm
- **KC705 Documentation**
  - Kintex-7 FPGA KC705 Evaluation Kit
    - http://www.xilinx.com/products/boards-and-kits/EK-K7-KC705-G.htm
  - KC705 Getting Started Guide
    - http://www.xilinx.com/support/documentation/boards_and_kits/ug883_K7_KC705_Eval_Kit.pdf
  - KC705 User Guide
    - http://www.xilinx.com/support/documentation/boards_and_kits/ug810_KC705_Eval_Bd.pdf
  - KC705 Reference Design User Guide
    - http://www.xilinx.com/support/documentation/boards_and_kits/ug845_Ref_Design.pdf