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# **KC705 GTX IBERT Design Creation**

**October 2012**

XTP103

# Revision History

Date	Version	Description
10/23/12	4.0	Regenerated for 14.3.
07/25/12	3.0	Regenerated for 14.2. Added AR50886.
05/30/12	2.1	Minor updates.
05/08/12	2.0	Regenerated for 14.1. AR46253 fixed.
04/12/12	1.1	Minor updates.
01/18/11	1.0	Initial version for 13.4. Added AR46253.

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# KC705 IBERT Overview

- **Xilinx KC705 Board**
- **Software Requirements**
- **Setup for the KC705 IBERT Designs**
- **KC705 IBERT Design Creation**
- **References**

# KC705 IBERT Overview

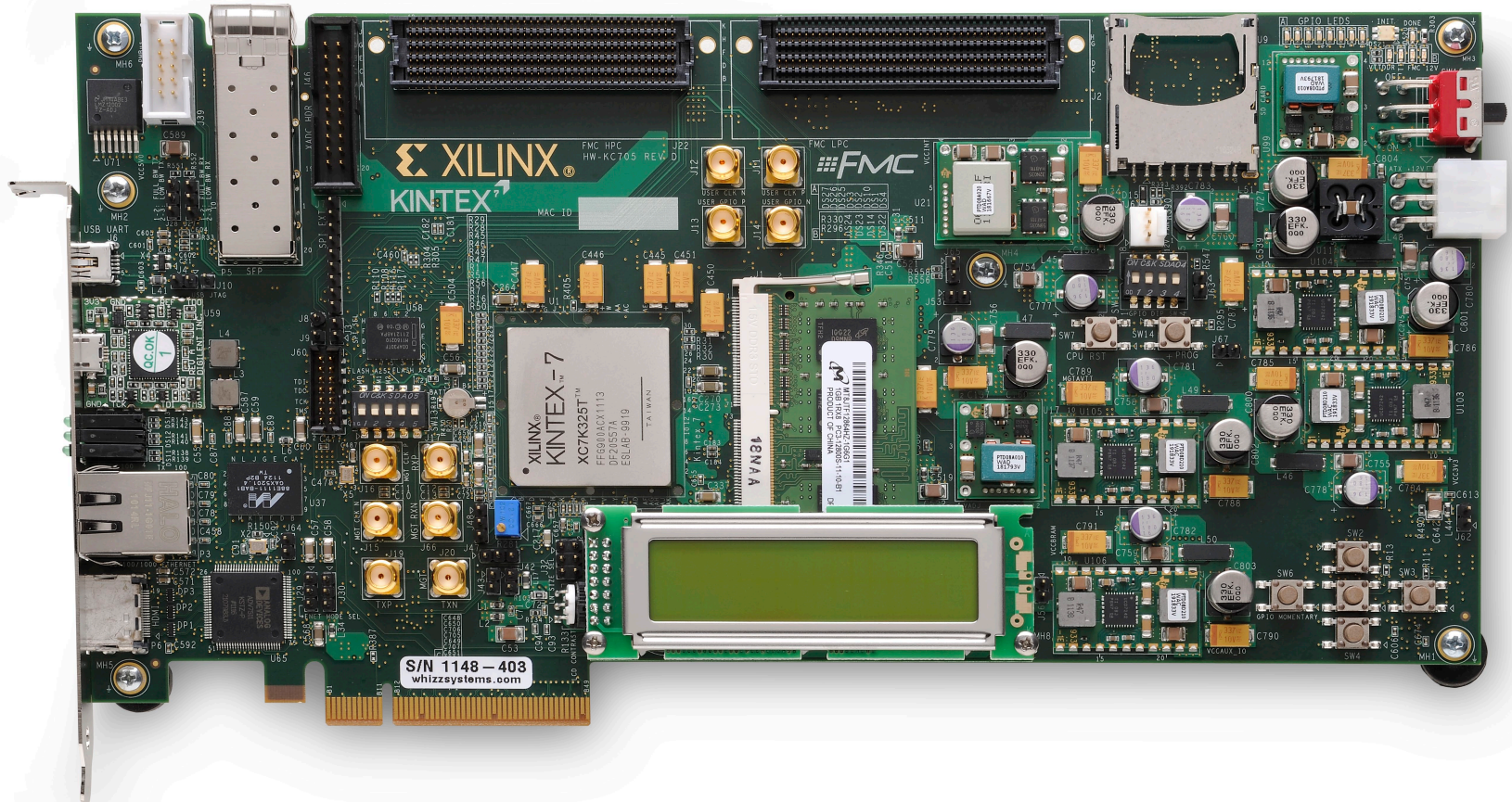
## ➤ Description

- The LogiCORE Integrated Bit Error Ratio (IBERT) core is used to create a pattern generation and verification design to exercise the Kintex-7 GTX transceivers. A graphical user interface is provided through the IBERT console window of the ChipScope Pro Analyzer

## ➤ Reference Design IP

- LogiCORE IBERT Example Designs
- ChipScope Pro Analyzer
  - ChipScope Pro Software and Cores User Guide (UG029)

# Xilinx KC705 Board



# ISE Software Requirement

## ➤ Xilinx ISE 14.3 software

- Apply [AR52368](#)



# ChipScope Pro Software Requirement

➤ Xilinx ChipScope Pro 14.3 software

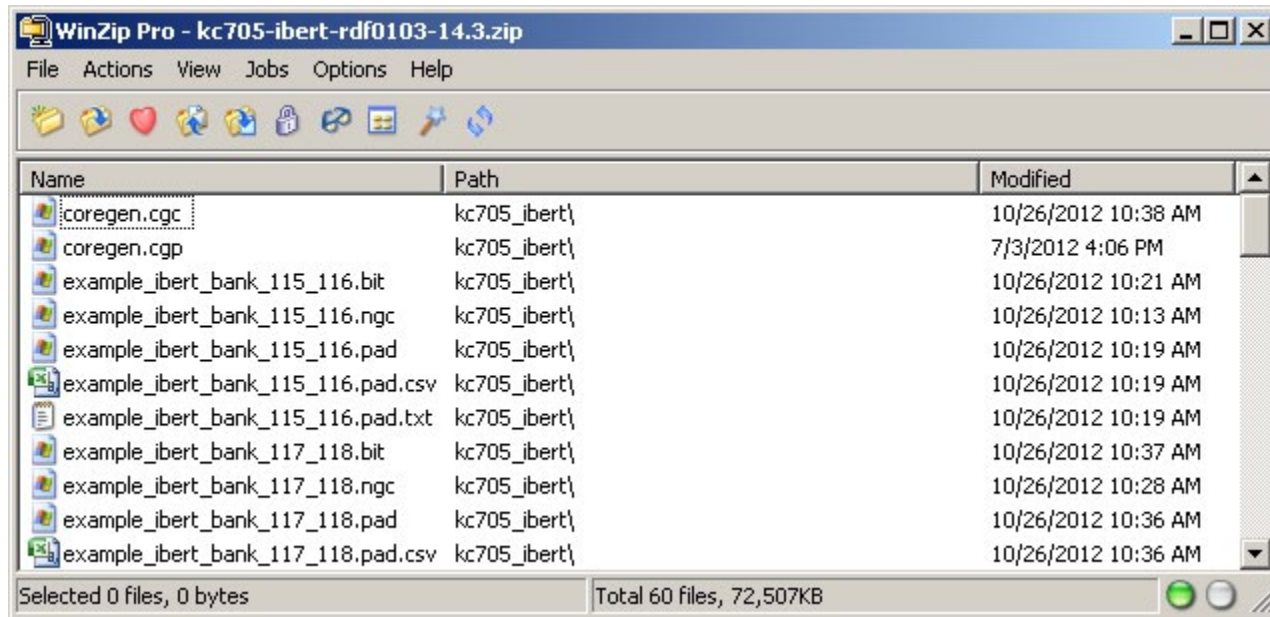


# Setup for the KC705 IBERT Designs



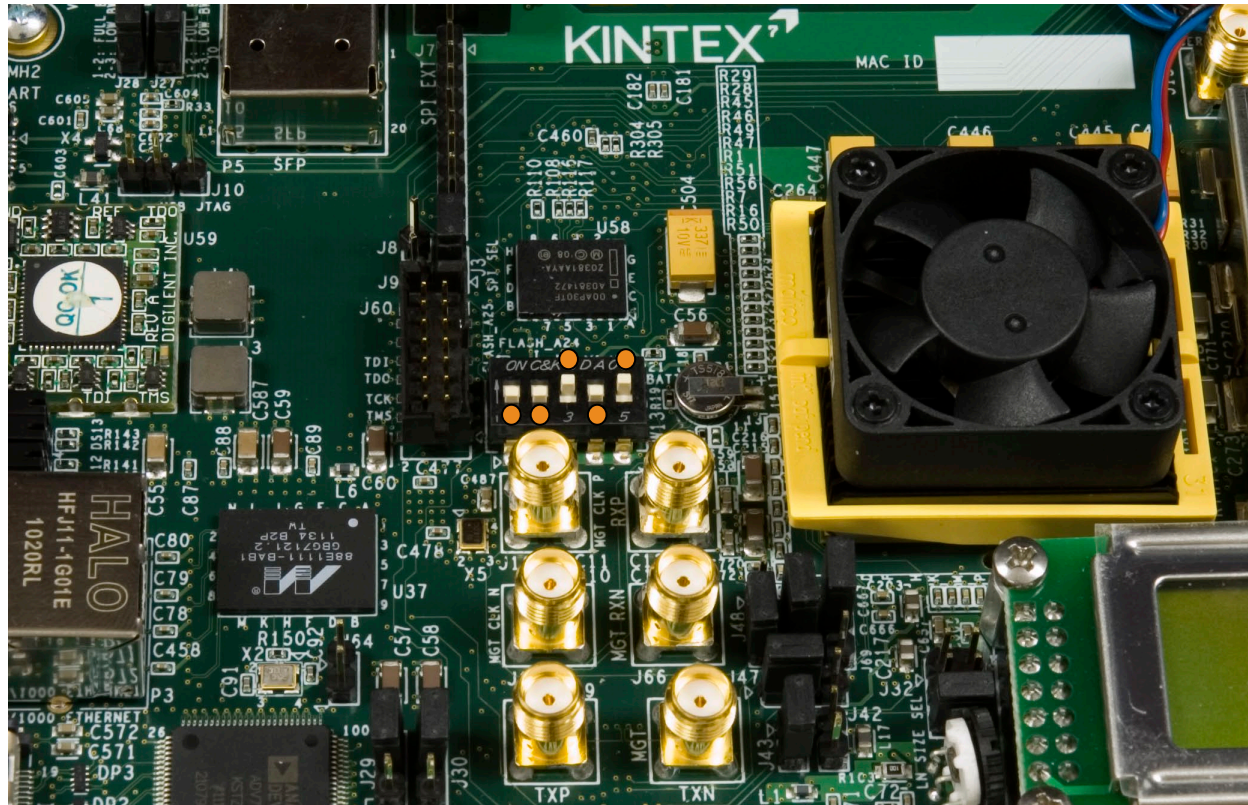
# Setup for the KC705 IBERT Designs

- Unzip the KC705 GTX IBERT Design Files (14.3 CES) to your C:\ drive
  - Available through <http://www.xilinx.com/kc705>



# Hardware Setup

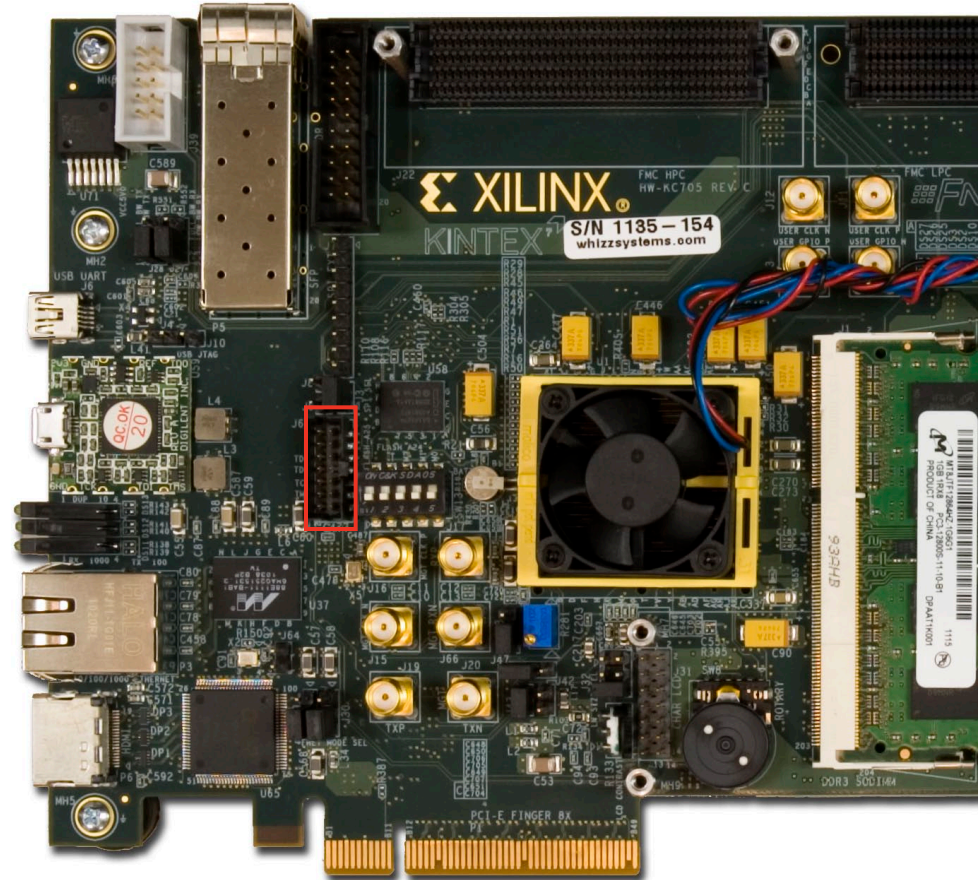
- Set S13 to 00101 (1 = on, Position 1 → Position 5)
  - This enables JTAG configuration



# Hardware Setup

## ➤ Connect a Platform Cable USB to the KC705

- Connect this cable to your PC

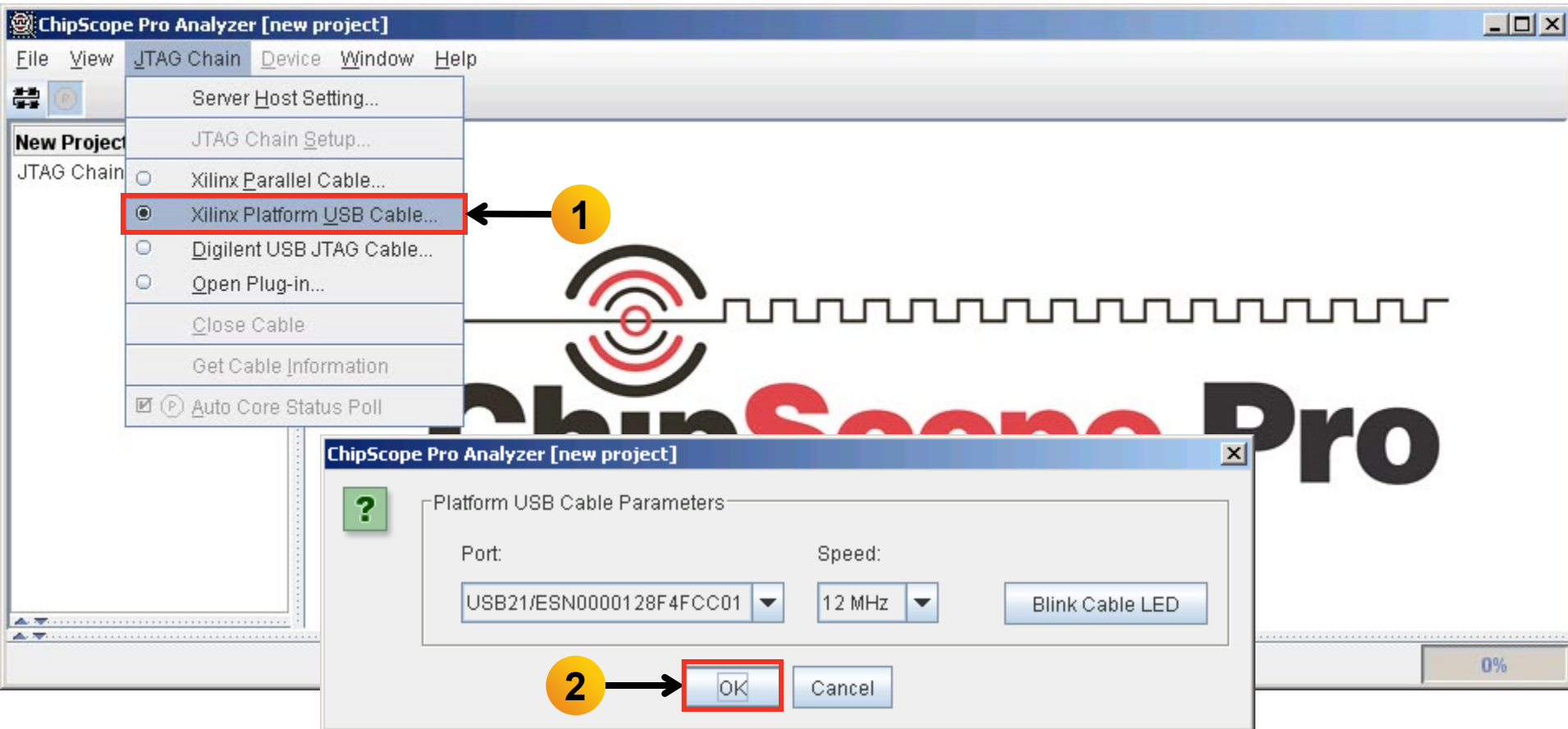


Note: Presentation applies to the KC705

# **KC705 GTX IBERT Design – Banks 117, 118**

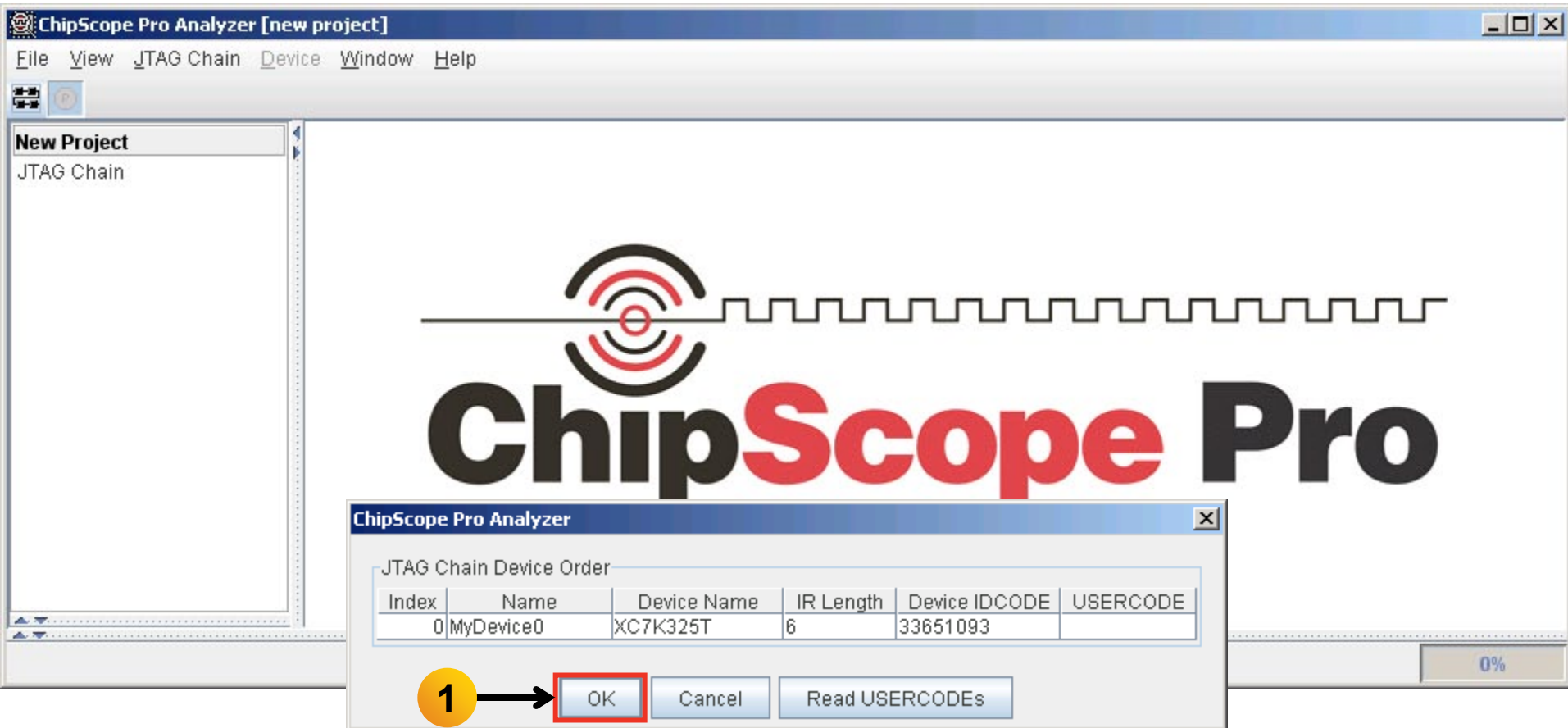
# KC705 GTX IBERT Design – Banks 117, 118

- Open ChipScope Pro and select JTAG Chain → USB Cable... (1)
- Click OK (2)



# KC705 GTX IBERT Design – Banks 117, 118

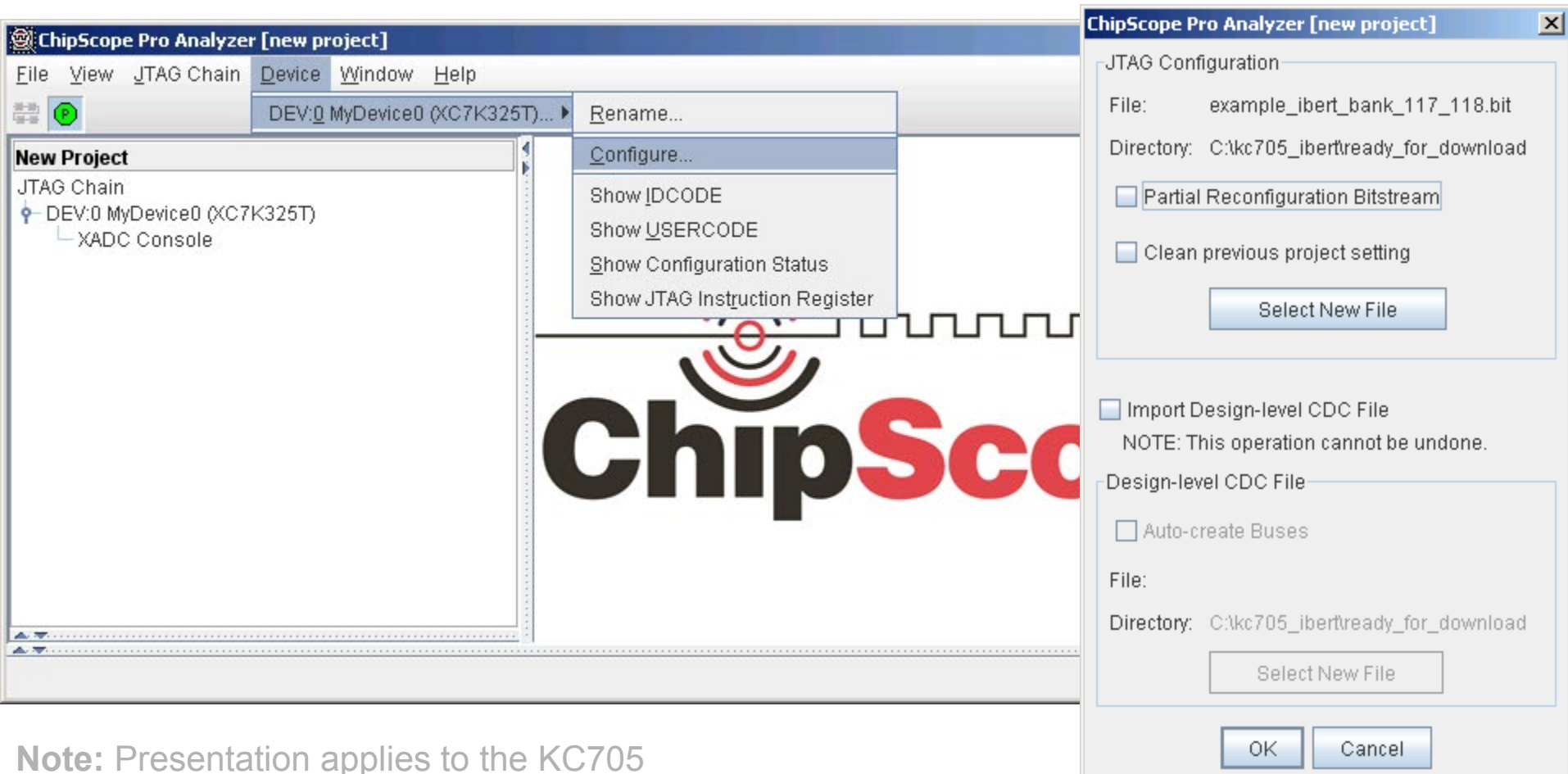
➤ Click OK (1)



Note: Presentation applies to the KC705

# KC705 GTX IBERT Design – Banks 117, 118

- Select Device → DEV:0 MyDevice0 (XC7K325T)... → Configure...
- Select <Design Path>\ready\_for\_download\  
example\_ibert\_bank\_117\_118.bit



The screenshot displays the ChipScope Pro Analyzer interface. The main window shows the 'New Project' dialog box with the 'Device' menu open, highlighting the 'Configure...' option. The 'Configure...' dialog box is open, showing the following settings:

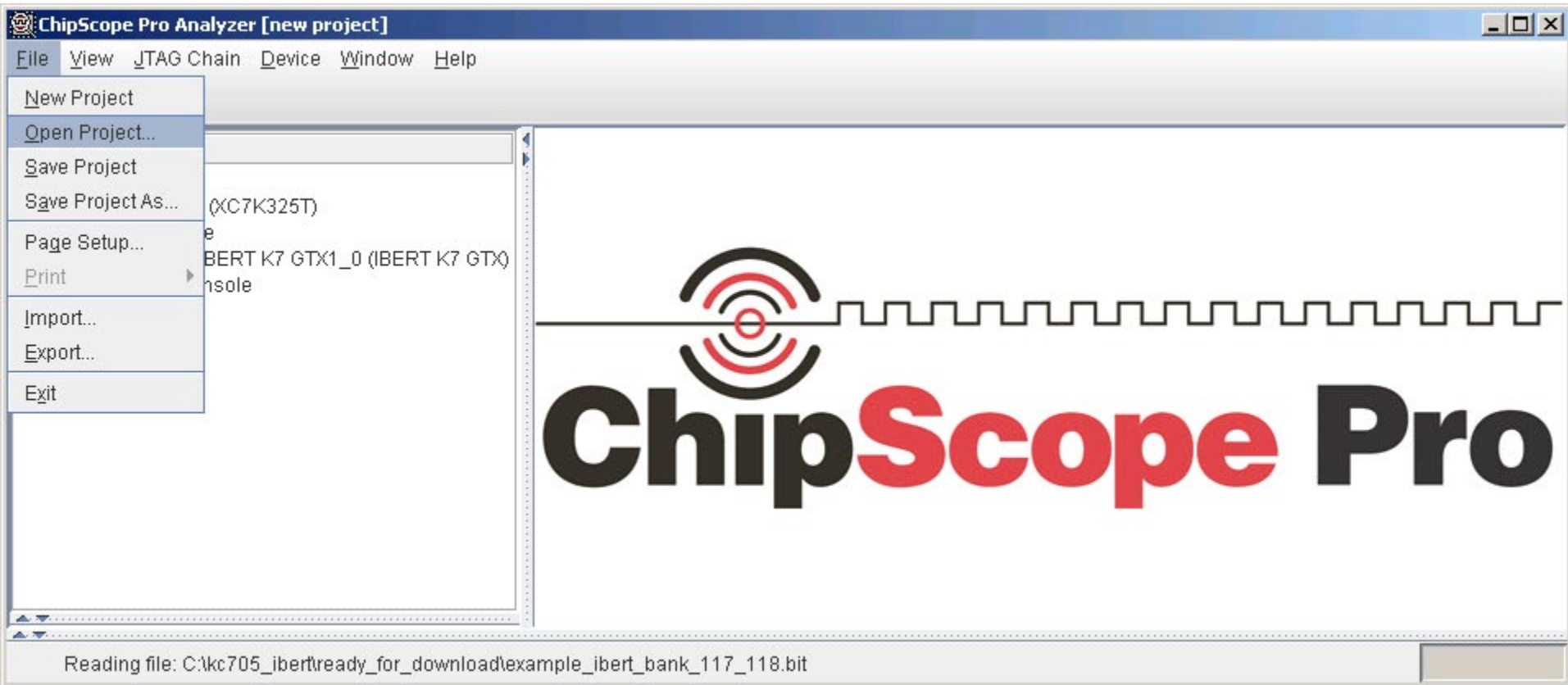
- JTAG Configuration
- File: example\_ibert\_bank\_117\_118.bit
- Directory: C:\kc705\_ibertready\_for\_download
- Partial Reconfiguration Bitstream
- Clean previous project setting
- 
- Import Design-level CDC File
- NOTE: This operation cannot be undone.
- Design-level CDC File
- Auto-create Buses
- File:
- Directory: C:\kc705\_ibertready\_for\_download
- 
- 

The background of the main window shows the 'New Project' dialog box with the 'JTAG Chain' section expanded to show 'DEV:0 MyDevice0 (XC7K325T)' and 'XADC Console'. The ChipScope logo is visible in the bottom right corner of the main window.

**Note:** Presentation applies to the KC705

# KC705 GTX IBERT Design – Banks 117, 118

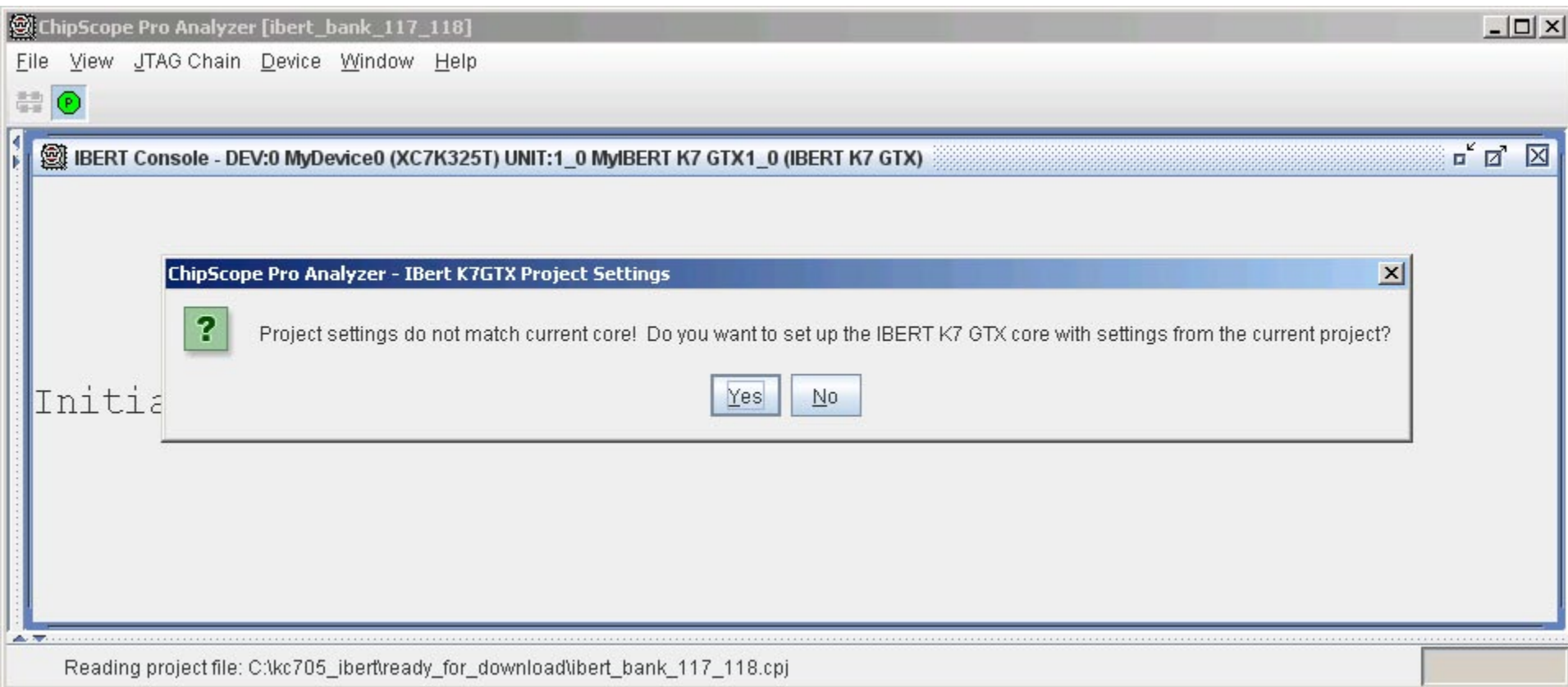
- Select File → Open Project...
- Select <Design Path>\ready\_for\_download\ibert\_bank\_117\_118.cpj





# KC705 GTX IBERT Design – Banks 117, 118

➤ Click Yes on this Dialog



Initia

# KC705 GTX IBERT Design – Banks 117, 118

- The line rate is 10.0 Gbps for all GTXs (1)
- All GTXs are in Near-End PCS loopback (2)

ChipScope Pro Analyzer [ibert\_bank\_117\_118]

File View JTAG Chain Device IBERT\_K7GTX Window Help

JTAG Scan Rate: 1 s S!

IBERT Console - DEV:0 MyDevice0 (XC7K325T) UNIT:1\_0 MyIBERT K7 GTX1\_0 (IBERT K7 GTX)

MGT/IBERT Settings | DRP Settings | Port Settings | RX Margin Analysis

	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
<b>MGT Settings</b>								
- MGT Alias	GTX0_117	GTX1_117	GTX2_117	GTX3_117	GTX0_118	GTX1_118	GTX2_118	GTX3_118
- Tile Locati...	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
- MGT Link ...	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps
- PLL Status	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED
- Loopback...	Near-End ...	Near-End ...	Near-End ...	Near-End ...	Near-End ...	Near-End ...	Near-End ...	Near-End ...
- Channel ...	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset
- TX/RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...

Reading project file: C:\kc705\_ibertready\_for\_download\ibert\_bank\_117\_118.cpj

**Note:** Bank 117, 118: SMA, SFP+, SGMII, LPC, HPC

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# KC705 GTX IBERT Design – Banks 117, 118

- TX Diff Output Swing = 850 mV
- TX Pre-Cursor = 1.67 dB; TX Post-Cursor = 0.68 dB

ChipScope Pro Analyzer [ibert\_bank\_117\_118]

File View JTAG Chain Device IBERT\_K7GTX Window Help

JTAG Scan Rate: 1 s S! ↔

IBERT Console - DEV:0 MyDevice0 (XC7K325T) UNIT:1\_0 MyIBERT K7 GTX1\_0 (IBERT K7 GTX)

MGT/IBERT Settings | DRP Settings | Port Settings | RX Margin Analysis

	GTX_X0Y8		GTX_X0Y9		GTX_X0Y10		GTX_X0Y11		GTX_X0Y12		GTX_X0Y13		GTX_X0Y14		GTX_X0Y15	
- TX/RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...
- TX Polari...	<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>	
- TX Error I...	Inject		Inject		Inject		Inject		Inject		Inject		Inject		Inject	
- TX Diff Ou...	850 mV (1...		850 mV (1...		850 mV (1...		850 mV (1...		850 mV (1...		850 mV (1...		850 mV (1...		850 mV (1...	
- TX Pre-Cu...	1.67 dB (0...		1.67 dB (0...		1.67 dB (0...		1.67 dB (0...		1.67 dB (0...		1.67 dB (0...		1.67 dB (0...		1.67 dB (0...	
- TX Post-C...	0.68 dB (0...		0.68 dB (0...		0.68 dB (0...		0.68 dB (0...		0.68 dB (0...		0.68 dB (0...		0.68 dB (0...		0.68 dB (0...	
- RX Polari...	<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>	
- Terminati...	Program...		Program...		Program...		Program...		Program...		Program...		Program...		Program...	

Reading project file: C:\kc705\_ibertready\_for\_download\ibert\_bank\_117\_118.cpj

# KC705 GTX IBERT Design – Banks 117, 118

- TX/RX Data Patterns are set to PRBS 31-bit (1)
- Click BERT Reset buttons (2)

ChipScope Pro Analyzer [ibert\_bank\_117\_118]

File View JTAG Chain Device IBERT\_K7GTX Window Help

JTAG Scan Rate: 1 s S! ↔

IBERT Console - DEV:0 MyDevice0 (XC7K325T) UNIT:1\_0 MyIBERT K7 GTX1\_0 (IBERT K7 GTX)

MGT/BERT Settings DRP Settings Port Settings RX Margin Analysis

	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
<b>MGT Settings</b>								
<b>BERT Settings</b>								
- TX Data P...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...
- RX Data P...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...
- RX Bit Err...	2.002E-001	2.003E-001	1.920E-001	4.635E-010	1.671E-001	1.673E-001	2.012E-001	1.931E-001
- RX Receiv...	1.693E012	1.694E012	1.695E012	1.696E012	1.696E012	1.697E012	1.698E012	1.699E012
- RX Bit Err...	3.389E011	3.393E011	3.254E011	7.860E002	2.835E011	2.839E011	3.418E011	3.281E011
- BERT Re...	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset

Reading project file: C:\kc705\_ibertready\_for\_download\ibert\_bank\_117\_118.cpj

# KC705 GTX IBERT Design – Banks 117, 118

- View the RX Bit Error Count (1)
- Close ChipScope Pro Analyzer and cycle KC705 board power

The screenshot shows the ChipScope Pro Analyzer interface for the project 'ibert\_bank\_117\_118'. The main window is titled 'IBERT Console - DEV:0 MyDevice0 (XC7K325T) UNIT:1\_0 MyIBERT K7 GTX1\_0 (IBERT K7 GTX)'. The 'RX Margin Analysis' tab is selected, displaying a table of RX Bit Error Count (RX Bit Err...) for various GTX banks (GTX\_X0Y8 to GTX\_X0Y15). The RX Bit Error Count for all banks is 0.000E000, which is highlighted with a red box. A yellow circle with the number '1' and an arrow points to the 'Reset' button for the GTX\_X0Y11 bank.

	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
<b>MGT Settings</b>								
<b>BERT Settings</b>								
TX Data P...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...
RX Data P...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...
RX Bit Err...	3.457E-013	3.472E-013	3.483E-013	3.494E-013	3.496E-013	3.507E-013	3.518E-013	3.520E-013
RX Receiv...	2.893E012	2.880E012	2.871E012	2.862E012	2.860E012	2.851E012	2.843E012	2.841E012
RX Bit Err...	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000
BERT Re...	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset

Reading project file: C:\kc705\_ibertready\_for\_download\ibert\_bank\_117\_118.cpj

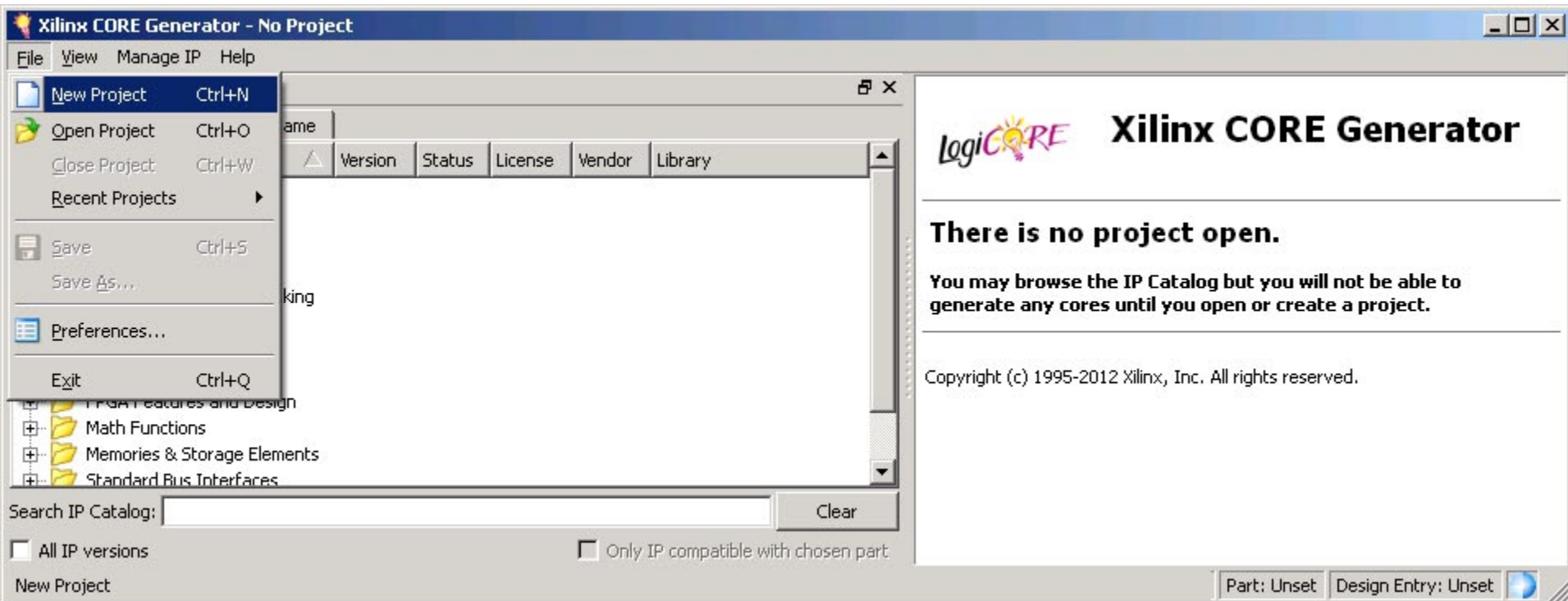
# KC705 IBERT Design Creation

# Create IBERT CORE Generator Project

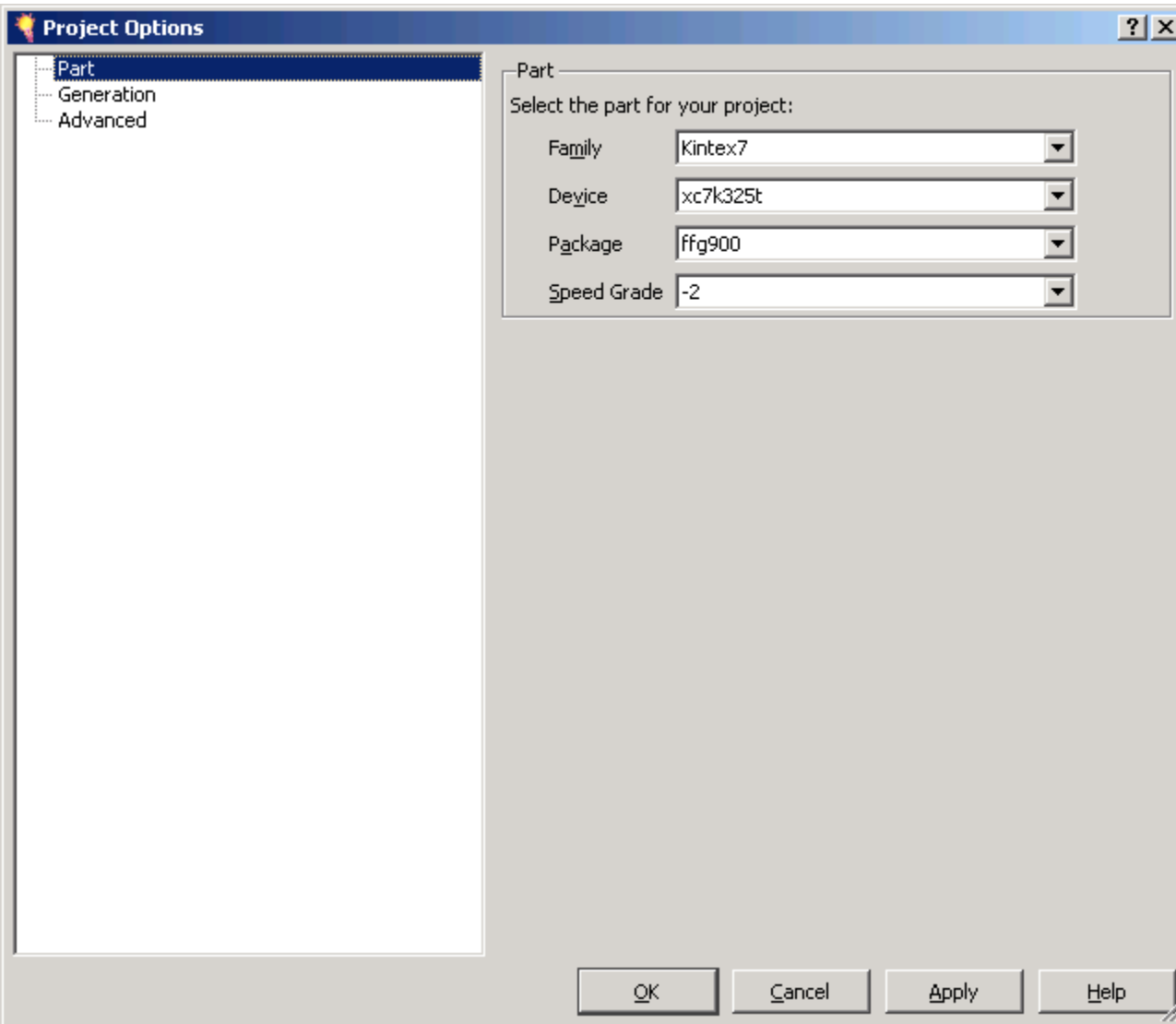
## ➤ Open the CORE Generator

Start → All Programs → Xilinx Design Tools → ISE Design Suite 14.3 → ISE Design Tools → 32-bit Tools → CORE Generator

## ➤ Create a new project; select File → New Project



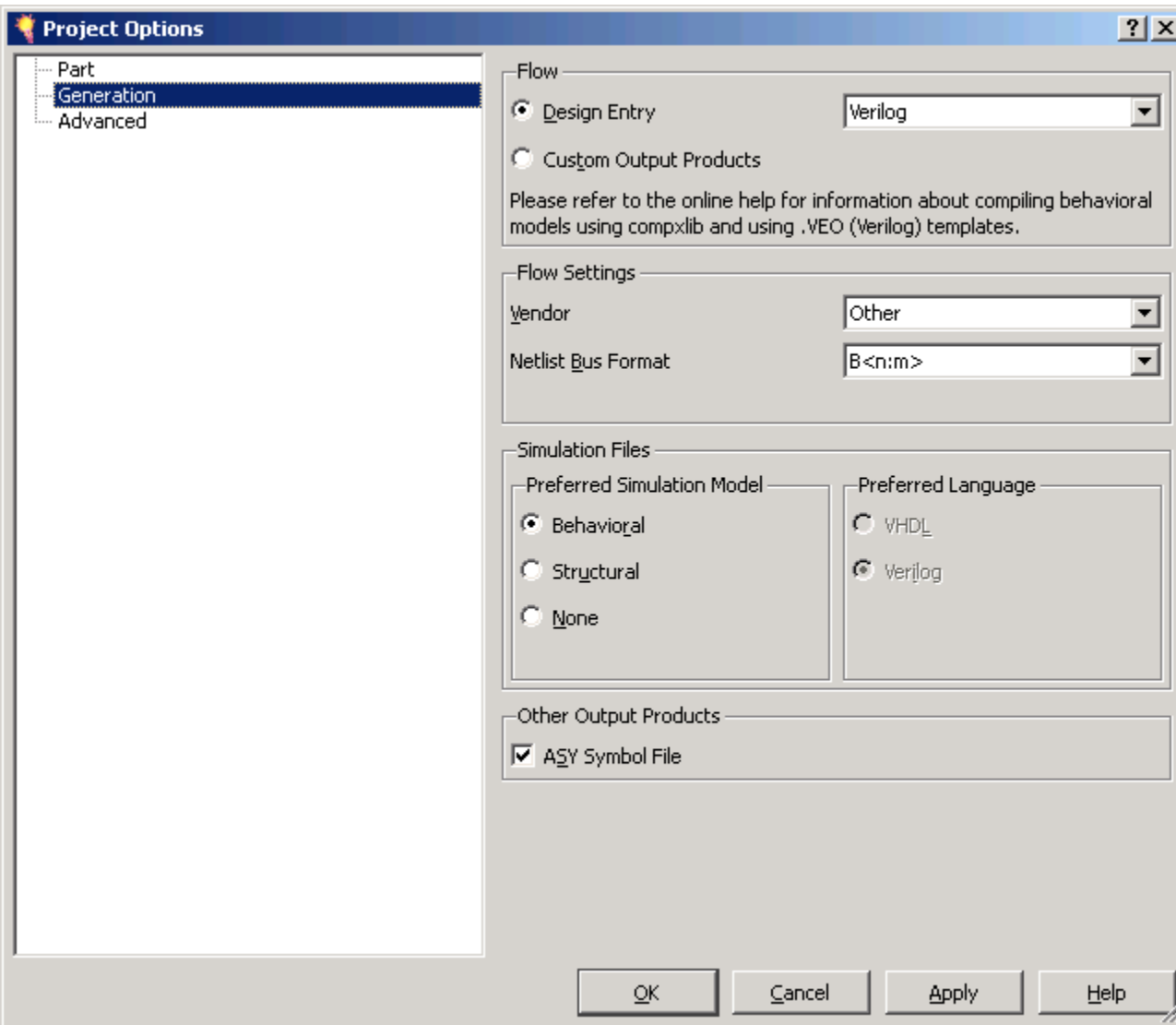
# Create IBERT CORE Generator Project



- Create a project in a new directory named:
  - kc705\_ibert
- Select Part
- Set the Part (as seen here):
  - Family: Kintex7
  - Device: xc7k325t
  - Package: ffg900
  - Speed Grade: -2
- Select Generation



# Create IBERT CORE Generator Project



➤ Select Verilog

➤ Click OK

**Create IBERT Design for Banks 115, 116**

# Create IBERT Design for Banks 115, 116

- Select the IBERT 7 Series GTX (ChipScope Pro - IBERT), Version 2.02.a

The screenshot shows the Xilinx CORE Generator IP Catalog window. The 'Name' column is selected, and the 'IBERT 7 Series GTX (ChipScope Pro - IBERT)' entry is highlighted. The table below shows the details of the selected IP core.

Name	Version	Status	License	Vendor	Library
Debug & Verification					
AXI Bus Functional Model	2.1	Pre-Production		xilinx.com	ip
Debug					
ATC2 (ChipScope Pro - Agilent Trace Core 2)	1.05.a	Production		xilinx.com	ip
AXI Chipscope Monitor	3.04.a	Pre-Production		xilinx.com	ip
IBERT 7 Series GTH (ChipScope Pro - IBERT)	2.00.a			xilinx.com	ip
<b>IBERT 7 Series GTX (ChipScope Pro - IBERT)</b>	<b>2.02.a</b>	<b>Production</b>		<b>xilinx.com</b>	<b>ip</b>
IBERT Spartan6 GTP (ChipScope Pro - IBERT)	2.02.a			xilinx.com	ip
IBERT Virtex5 GTX (ChipScope Pro - IBERT)	2.01.a			xilinx.com	ip
IBERT Virtex6 GTH (ChipScope Pro - IBERT)	2.03.a			xilinx.com	ip
IBERT Virtex6 GTX (ChipScope Pro - IBERT)	2.06.a			xilinx.com	ip
ICON (ChipScope Pro - Integrated Controller)	1.06.a	Production		xilinx.com	in

Search IP Catalog:  Clear

All IP versions  Only IP compatible with chosen part

**IBERT 7 Series GTX (ChipScope Pro - IBERT)**

This core is supported at status **Production** by your chosen part.

**Information**

Core type: IBERT 7 Series GTX (ChipScope Pro - IBERT)  
Version: 2.02.a  
Identify: xilinx.com:ip:chipscope\_ibert

Part: xc7k325t-2ffg900 Design Entry: Verilog

# Create IBERT Design for Banks 115, 116

- Right click on the IBERT Kintex7 GTX (ChipScope Pro - IBERT), Version 2.02.a
  - Select **Customize and Generate**

The screenshot shows the Xilinx CORE Generator interface. The IP Catalog is displayed with a table of IP cores. The 'IBERT 7 Series GTX (ChipScope Pro - IBERT)' core is selected, and the 'Customize and Generate' context menu is open over it. The right-hand pane shows the core's details, including its name, version (2.02.a), and status (Production).

Name	Version	Status	License	Vendor	Library
AXI Bus Functional Model	2.1	Pre-Production		xilinx.com	ip
AXI Chipscope Monitor	3.04.a	Pre-Production		xilinx.com	ip
ATC2 (ChipScope Pro - Agilent Trace Core 2)	1.05.a	Production		xilinx.com	ip
IBERT 7 Series GTX (ChipScope Pro - IBERT)	2.02.a	Production		xilinx.com	ip
IBERT Spartan6 GTP (ChipScope Pro - IBERT)					
IBERT Virtex5 GTX (ChipScope Pro - IBERT)					
IBERT Virtex6 GTX (ChipScope Pro - IBERT)					
ICON (ChipScope Pro - Integrated Controller)					

**IBERT 7 Series GTX (ChipScope Pro - IBERT)**

This core is supported at status **Production** by your chosen part.

**Information**

Core type: IBERT 7 Series GTX (ChipScope Pro - IBERT)  
Version: 2.02.a  
Identify: xilinx.com/ipcores/ibert

Part: xc7k325t-2ffg900 Design Entry: Verilog

# Create IBERT Design for Banks 115, 116

## ➤ Make the following settings:

- Component name:  
**ibert\_bank\_115\_116**
- Set the GTX Naming Style to: **MGT m n**
- Set the System Clock
  - Frequency: **200**
  - Pin Input standard: **LVDS**
  - P Pin Location: **AD12**
  - N Pin Location: **AD11**
  - Silicon Version:  
**General ES**

## ➤ Click Next

IBERT 7 Series GTX (ChipScope Pro - IBERT)

Documents View

LogiCORE

**IBERT 7 Series GTX  
(ChipScope Pro - IBERT)** xilinx.com:ip:chipscope\_ibert\_7series\_gbx:2.02.a

Component Name

Board Configuration Settings

Generate Bitstream

When using ISE, enable 'Generate Bitstream using ISE tools' checkbox

Generate Bitstream using ISE Tools

When using Vivado, source the generated v\_rdi\_implementation.tcl

System Design

Add RXOUTCLK probe

GTX Naming Style  ex. MGT0\_113 / MGTREFCLK0\_113

System Clock

Use External clock source

Enable Diff Term

Frequency  MHz

P Pin Location

N Pin Location

Pin Input Standard

Silicon Version

Silicon Version

Datasheet < Back Page 1 of 5 Next > Generate Cancel Help

# Create IBERT Design for Banks 115, 116

## ➤ Make the following settings:

- Select: **Independent TX/RX User Clocking**
- No. of Quads: **2**
- Select: **QUAD 115 and QUAD 116**
- Max Rate (Gbps): **5.00**
- Refclk (MHz): **100.000**
- GTX Count: **8**

## ➤ Click Next

IBERT 7 Series GTX (ChipScope Pro - IBERT)

Documents View

LogiCORE

### IBERT 7 Series GTX (ChipScope Pro - IBERT)

xilinx.com:ip:chipscope\_ibert\_7series\_gbx:2.02.a

GT clocking mode selection

Dependent TX/RX User Clocking (Quad Based Protocol Selection)

Independent TX/RX User Clocking (GT based protocol selection - Upto 4 Quads)

No. of Quads	2
Select Quad	QUAD 115
Select Quad	QUAD 116

Number of Protocols: 1

Line rate settings

Protocol	Max Rate (Gbps)	Data Width	Refclk (MHz)	GT count	Quad PLL
Name Protocol	5.00	40	100.000	8	<input checked="" type="checkbox"/>
Custom_1					

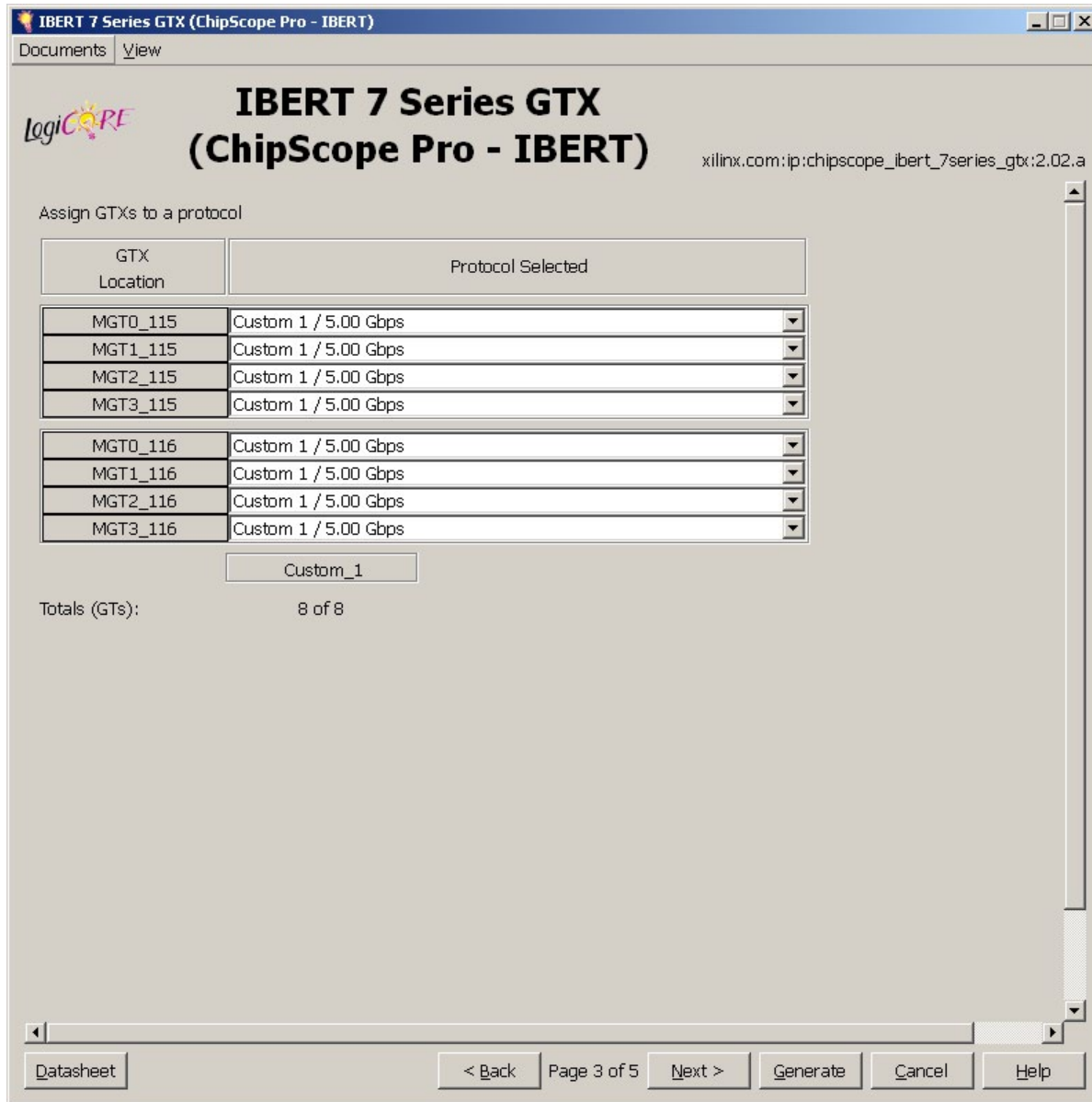
GTXs Resources

GTXs count	8
BUFG count	16

Datasheet < Back Page 2 of 4 Next > Generate Cancel Help

# Create IBERT Design for Banks 115, 116

- Set Banks 115 and 116 to:
  - Custom 1 / 5.00 Gbps
- Click Next



Note: Presentation applies to the KC705

# Create IBERT Design for Banks 115, 116

- Set Banks 115 and 116 Refclk Sources to:
  - MGTREFCLK1 115
- Click Next

IBERT 7 Series GTX (ChipScope Pro - IBERT)

Documents View

LogiCORE

IBERT 7 Series GTX (ChipScope Pro - IBERT)

xilinx.com:ip:chipscope\_ibert\_7series\_gbx:2.02.a

Select Reference Clock source/s

GTX Location	Protocol	Linerate (Gbps)	Refclk MHz	Refclk Source	Quad PLL
MGT0_115	Custom_1	5.00	100.000	MGTREFCLK1 115	<input checked="" type="checkbox"/>
MGT1_115	Custom_1	5.00	100.000	MGTREFCLK1 115	<input checked="" type="checkbox"/>
MGT2_115	Custom_1	5.00	100.000	MGTREFCLK1 115	<input checked="" type="checkbox"/>
MGT3_115	Custom_1	5.00	100.000	MGTREFCLK1 115	<input checked="" type="checkbox"/>
MGT0_116	Custom_1	5.00	100.000	MGTREFCLK1 115	<input checked="" type="checkbox"/>
MGT1_116	Custom_1	5.00	100.000	MGTREFCLK1 115	<input checked="" type="checkbox"/>
MGT2_116	Custom_1	5.00	100.000	MGTREFCLK1 115	<input checked="" type="checkbox"/>
MGT3_116	Custom_1	5.00	100.000	MGTREFCLK1 115	<input checked="" type="checkbox"/>

Datasheet < Back Page 4 of 5 Next > Generate Cancel Help

Note: Presentation applies to the KC705



# Create IBERT Design for Banks 115, 116

➤ Click Generate

IBERT 7 Series GTX (ChipScope Pro - IBERT)

Documents View

**IBERT 7 Series GTX  
(ChipScope Pro - IBERT)**

xilinx.com:ip:chipscope\_ibert\_7series\_gtx:2.02.a

IBERT Design Summary

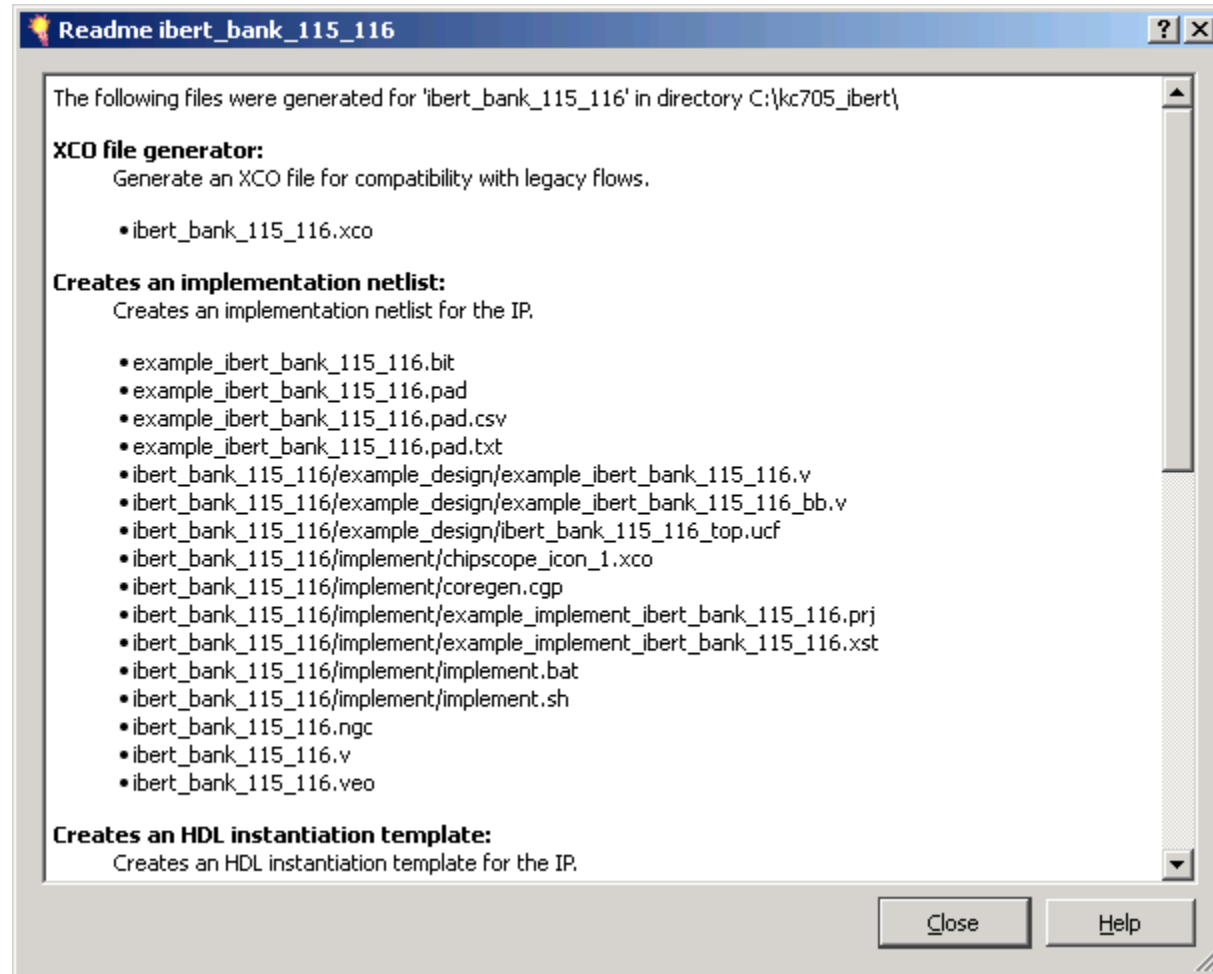
Component Name :	ibert_bank_115_116
Number of Protocols :	1
System Clock Source :	External (P Pin: AD12)
System Clock Frequency :	200 MHz
BUFG count :	17
GTX count :	8
MMCM count :	1
Refclk sources :	1
Board Configuration Settings :	User_Defined

< Datasheet > Back Page 5 of 5 Next > Generate Cancel Help

**Note:** Presentation applies to the KC705

# Create IBERT Design for Banks 115, 116

- After the IBERT core finishes generating, click **Close** on the **Readme File** window



**Create IBERT Design for Banks 117, 118**

# Create IBERT Design for Banks 117, 118

- Select the IBERT 7 Series GTX (ChipScope Pro - IBERT), Version 2.02.a

The screenshot shows the Xilinx CORE Generator IP Catalog window. The 'View by Function' tab is selected, and the 'IBERT 7 Series GTX (ChipScope Pro - IBERT)' entry is highlighted in the list. The right-hand pane displays the core's details, including its name, status (Production), and version (2.02.a).

Name	Version	Status	License	Vendor	Library
AXI Bus Functional Model	2.1	Pre-Production		xilinx.com	ip
AXI Chipscope Monitor	3.04.a	Pre-Production		xilinx.com	ip
IBERT 7 Series GTX (ChipScope Pro - IBERT)	2.02.a	Production		xilinx.com	ip
IBERT Spartan6 GTP (ChipScope Pro - IBERT)	2.02.a			xilinx.com	ip
IBERT Virtex5 GTX (ChipScope Pro - IBERT)	2.01.a			xilinx.com	ip
IBERT Virtex6 GTH (ChipScope Pro - IBERT)	2.03.a			xilinx.com	ip

**IBERT 7 Series GTX (ChipScope Pro - IBERT)**

This core is supported at status **Production** by your chosen part.

**Information**

Core type: IBERT 7 Series GTX (ChipScope Pro - IBERT)  
Version: 2.02.a  
Identify: xilinx.com:ip:chipscope\_ibert

Part: xc7k325t-2ffg900 Design Entry: Verilog

# Create IBERT Design for Banks 117, 118

- Right click on the IBERT Kintex7 GTX (ChipScope Pro - IBERT), Version 2.02.a
  - Select Customize and Generate

The screenshot shows the Xilinx CORE Generator interface. The IP Catalog window is open, displaying a list of IP cores. The 'IBERT 7 Series GTX (ChipScope Pro - IBERT)' core is selected, and a context menu is open over it, showing the 'Customize and Generate' option. The core's status is 'Production'.

Name	Version	Status	License	Vendor	Library
AXI Bus Functional Model	2.1	Pre-Production		xilinx.com	ip
AXI Chipscope Monitor	3.04.a	Pre-Production		xilinx.com	ip
ATC2 (ChipScope Pro - Agilent Trace Core 2)	1.05.a	Production		xilinx.com	ip
IBERT 7 Series GTX (ChipScope Pro - IBERT)	2.02.a	Production		xilinx.com	ip
IBERT Spartan6 GTP (ChipScope Pro - IBERT)					
IBERT Virtex5 GTX (ChipScope Pro - IBERT)					
IBERT Virtex6 GTX (ChipScope Pro - IBERT)					

**IBERT 7 Series GTX (ChipScope Pro - IBERT)**

This core is supported at status **Production** by your chosen part.

**Information**

Core type: IBERT 7 Series GTX (ChipScope Pro - IBERT)  
Version: 2.02.a  
Identify: xilinx.com/ipcores/ibert

Part: xc7k325t-2ffg900 Design Entry: Verilog

# Create IBERT Design for Banks 117, 118

## ➤ Make the following settings:

- Component name:  
**ibert\_bank\_117\_118**
- Set the GTX Naming Style to: **MGT m n**
- Set the System Clock
  - Frequency: **200**
  - Pin Input standard: **LVDS**
  - P Pin Location: **AD12**
  - N Pin Location: **AD11**
  - Silicon Version:  
**General ES**

## ➤ Click Next

IBERT 7 Series GTX (ChipScope Pro - IBERT)

Documents View

LogiCORE

**IBERT 7 Series GTX  
(ChipScope Pro - IBERT)** xilinx.com:ip:chipscope\_ibert\_7series\_gbx:2.02.a

Component Name:

Board Configuration Settings:

Generate Bitstream

When using ISE, enable 'Generate Bitstream using ISE tools' checkbox

Generate Bitstream using ISE Tools

When using Vivado, source the generated v\_rdi\_implement.tcl

System Design

Add RXOUTCLK probe

GTX Naming Style:  ex. MGT0\_113 / MGTREFCLK0\_113

System Clock

Use External clock source

Enable Diff Term

Frequency:  MHz

P Pin Location:

N Pin Location:

Pin Input Standard:

Silicon Version

Silicon Version:

Datasheet < Back Page 1 of 5 Next > Generate Cancel Help

# Create IBERT Design for Banks 117, 118

## ➤ Make the following settings:

- Select: **Independent TX/RX User Clocking**
- No. of Quads: **2**
- Select: **QUAD 117** and **QUAD 118**
- Max Rate (Gbps): **10.00**
- Refclk (MHz): **125.000**
- GTX Count: **8**

## ➤ Click Next

IBERT 7 Series GTX (ChipScope Pro - IBERT)

Documents View

LogiCORE

### IBERT 7 Series GTX (ChipScope Pro - IBERT)

xilinx.com:ip:chipscope\_ibert\_7series\_gbx:2.02.a

GT clocking mode selection

Dependent TX/RX User Clocking (Quad Based Protocol Selection)

Independent TX/RX User Clocking (GT based protocol selection - Upto 4 Quads)

No. of Quads	2
Select Quad	QUAD 117
Select Quad	QUAD 118

Number of Protocols: 1

Line rate settings

Protocol	Max Rate (Gbps)	Data Width	Refclk (MHz)	GT count	Quad PLL
Name Protocol	10.00	40	125.000	8	<input checked="" type="checkbox"/>
Custom_1					

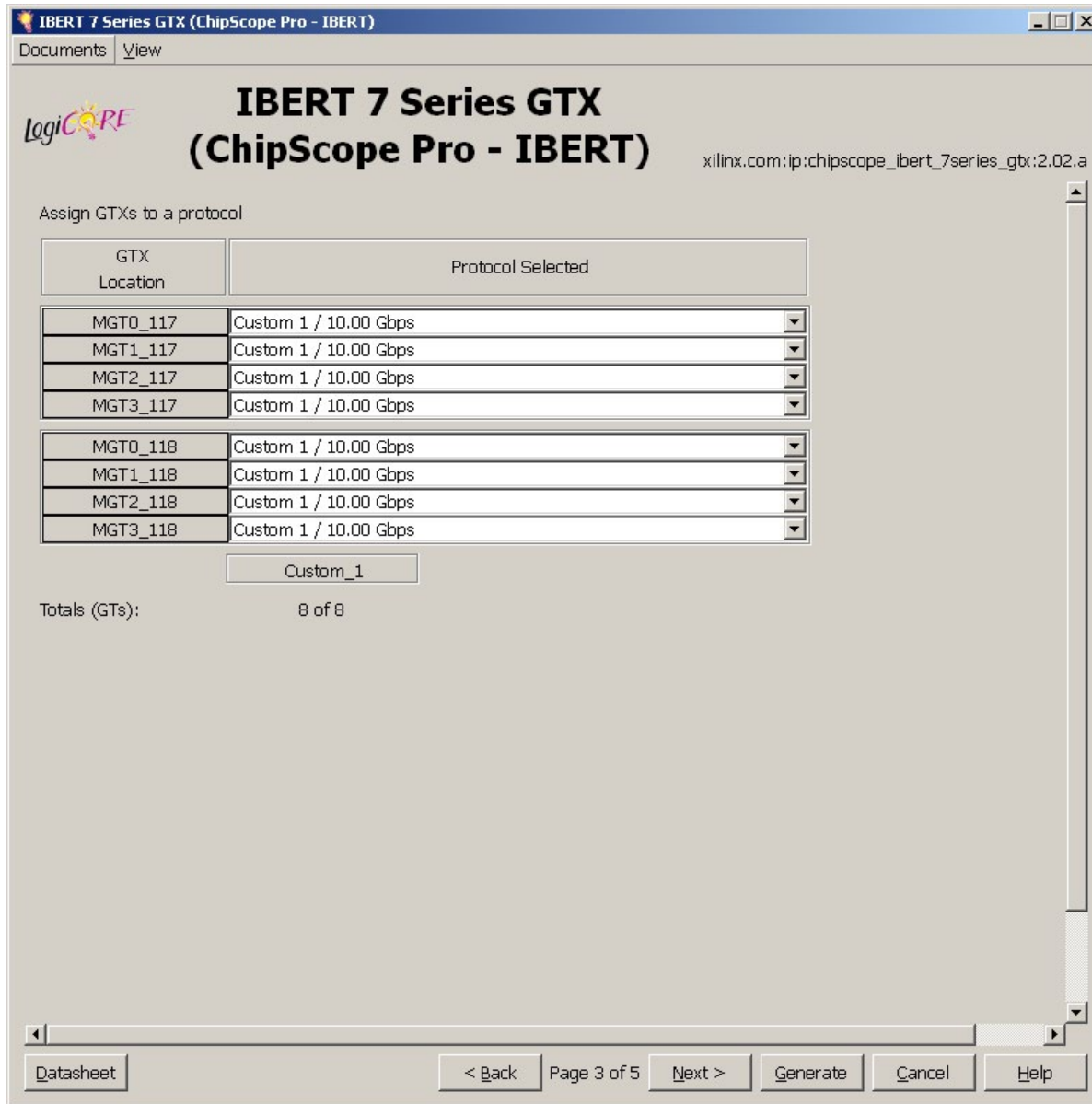
GTXs Resources

GTXs count	8
BUFG count	16

< Back Page 2 of 4 Next > Generate Cancel Help

# Create IBERT Design for Banks 117, 118

- Set Banks 117 and 118 to:
  - Custom 1 / 10.00 Gbps
- Click Next





# Create IBERT Design for Banks 117, 118

- Set Banks 117 and 118 Refclk Sources to:
  - MGTREFCLK0 117
- Click Next

IBERT 7 Series GTX (ChipScope Pro - IBERT)

Documents View

LogiCORE

**IBERT 7 Series GTX (ChipScope Pro - IBERT)** xilinx.com:ip:chipscope\_ibert\_7series\_gbx:2.02.a

Select Reference Clock source/s

GTX Location	Protocol	Linerate (Gbps)	Refclk MHz	Refclk Source	Quad PLL
MGT0_117	Custom_1	10.00	125.000	MGTREFCLK0 117	<input checked="" type="checkbox"/>
MGT1_117	Custom_1	10.00	125.000	MGTREFCLK0 117	<input checked="" type="checkbox"/>
MGT2_117	Custom_1	10.00	125.000	MGTREFCLK0 117	<input checked="" type="checkbox"/>
MGT3_117	Custom_1	10.00	125.000	MGTREFCLK0 117	<input checked="" type="checkbox"/>
MGT0_118	Custom_1	10.00	125.000	MGTREFCLK0 117	<input checked="" type="checkbox"/>
MGT1_118	Custom_1	10.00	125.000	MGTREFCLK0 117	<input checked="" type="checkbox"/>
MGT2_118	Custom_1	10.00	125.000	MGTREFCLK0 117	<input checked="" type="checkbox"/>
MGT3_118	Custom_1	10.00	125.000	MGTREFCLK0 117	<input checked="" type="checkbox"/>

Datasheet < Back Page 4 of 5 Next > Generate Cancel Help

Note: Presentation applies to the KC705

# Create IBERT Design for Banks 117, 118

➤ Click Generate

IBERT 7 Series GTX (ChipScope Pro - IBERT)

Documents View

**IBERT 7 Series GTX  
(ChipScope Pro - IBERT)**

xilinx.com:ip:chipscope\_ibert\_7series\_gtx:2.02.a

IBERT Design Summary

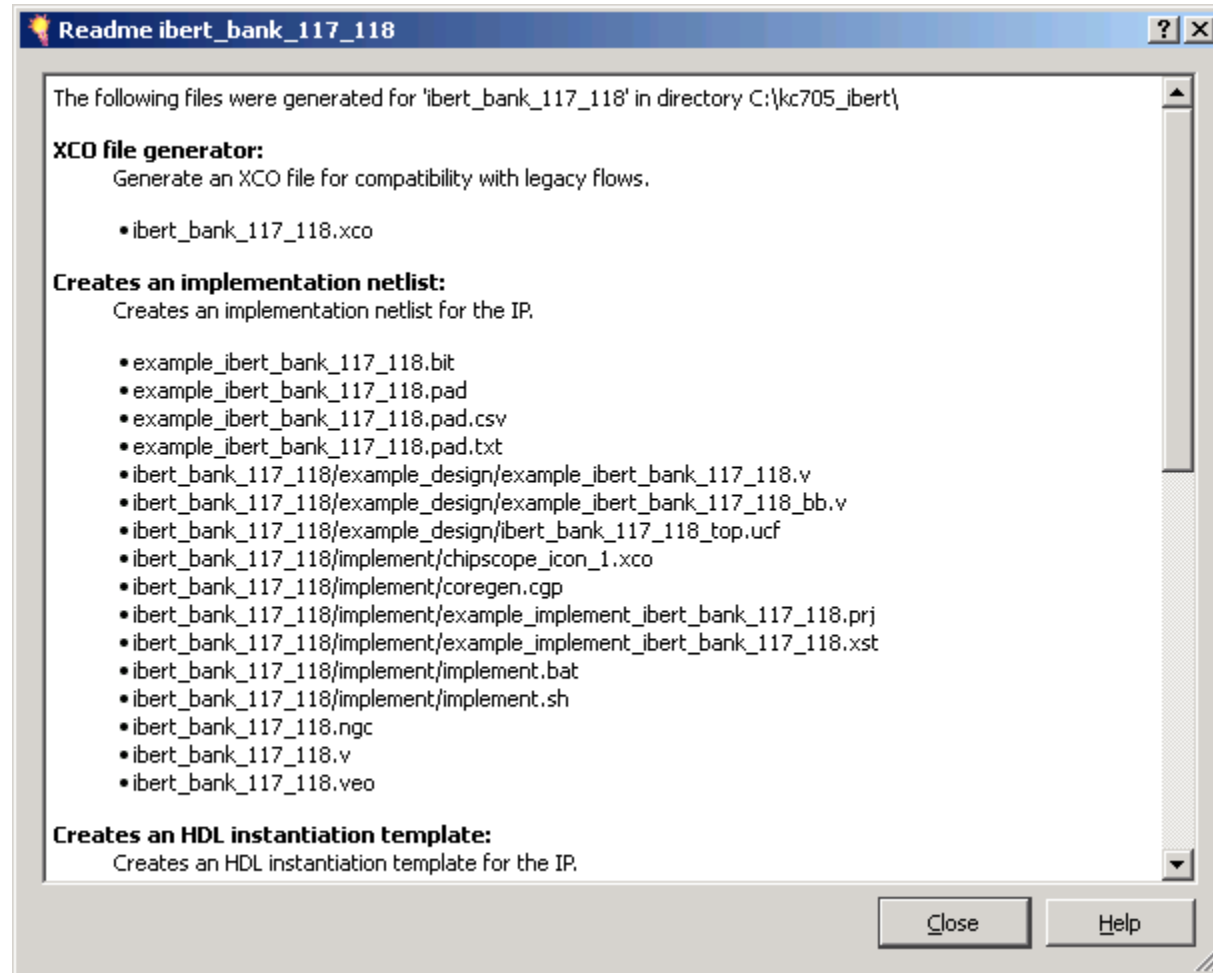
Component Name :	ibert_bank_117_118
Number of Protocols :	1
System Clock Source :	External (P Pin: AD12)
System Clock Frequency :	200 MHz
BUFG count :	17
GTX count :	8
MMCM count :	1
Refclk sources :	1
Board Configuration Settings :	User_Defined

Datasheet < Back Page 5 of 5 Next > Generate Cancel Help

**Note:** Presentation applies to the KC705

# Create IBERT Design for Banks 117, 118

- After the IBERT core finishes generating, click **Close** on the **Readme File** window



# Optional Testing with User Provided Hardware

# Optional Testing with User Provided Hardware

## ➤ SMA Cables

- [www.rosenbergerna.com](http://www.rosenbergerna.com)
- Part number:  
72D-32S1-32S1-00610A

## ➤ SMA Quick connects

- RADIALL
- Part number: R125791501
- Available [here](#) or [here](#)



# Optional Testing with User Provided Hardware

## ➤ Connect Optical Loopback Adapter

- [www.molex.com](http://www.molex.com)
- SFP Loopback Adapter, 5.0 db Attenuation
- Part # [74765-0904](#)



# Optional Testing with User Provided Hardware

➤ For testing Banks 115 and 116:

➤ PCIe Testing Hardware:

– HiTechGlobal PCI Express Test & SerialIO Expansion Module

– [HTG-TEST-PCIE-SMA](#)

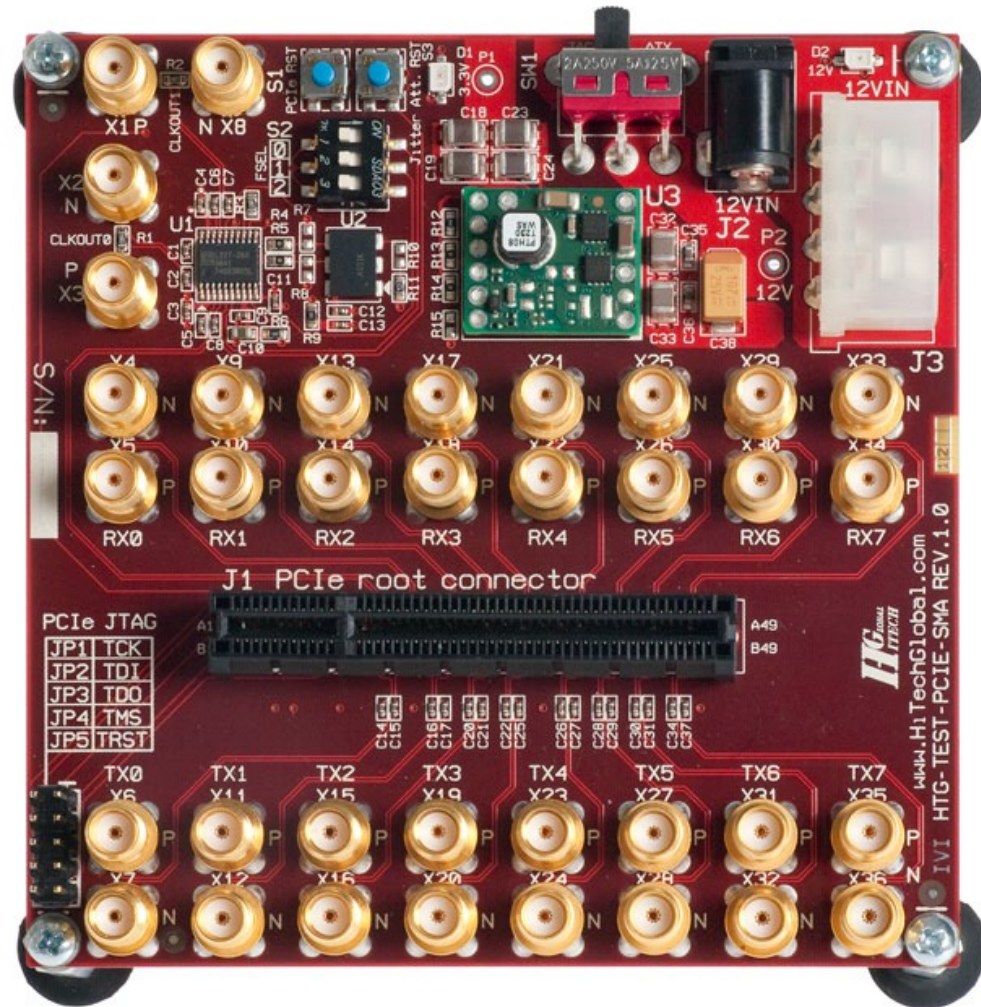
– 16 SMA cables required

– Requires power supply, either:

- 4-pin Peripheral power connector from ATX power supply

– Or:

- HiTechGlobal [PWR-12V-6A](#)

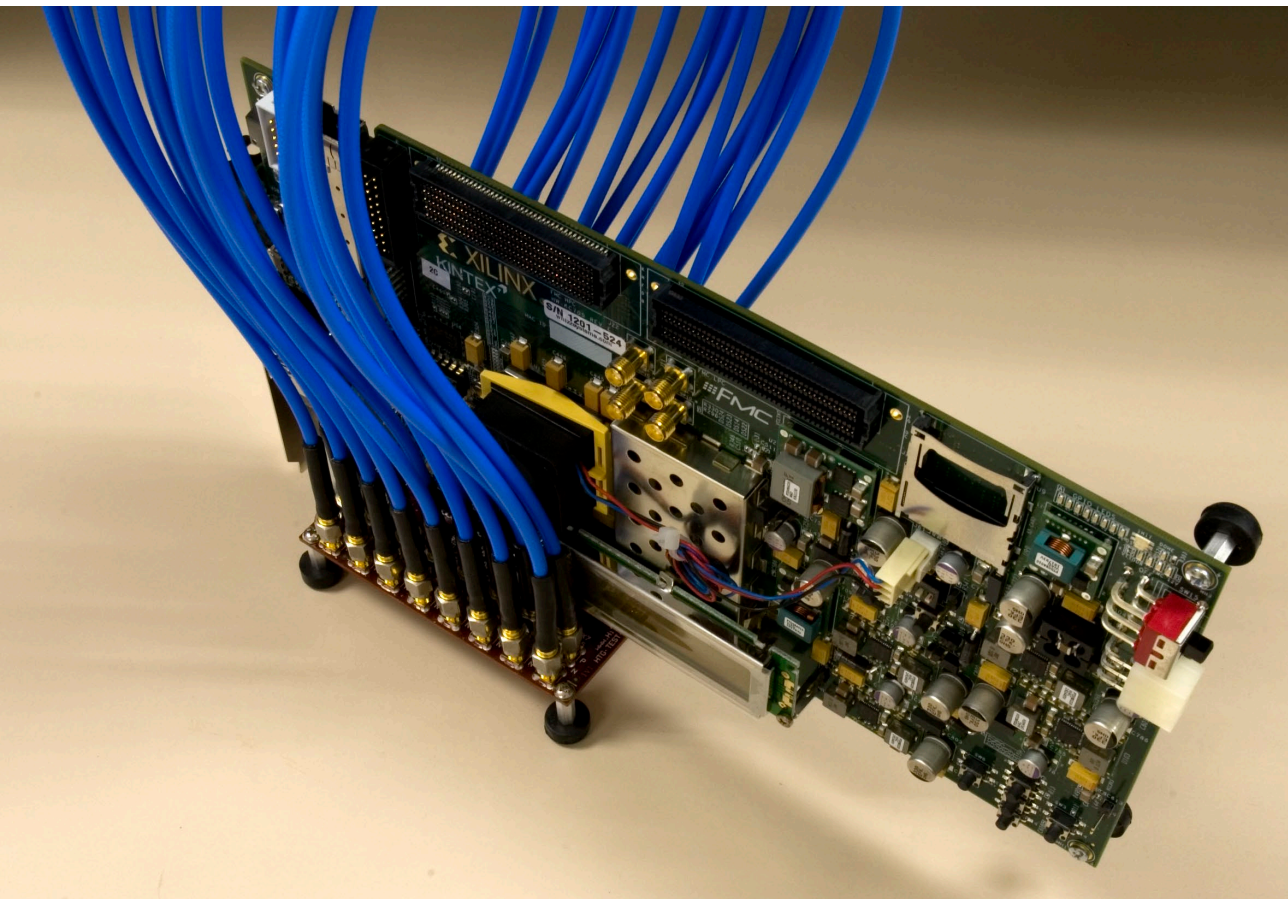




# **Testing Banks 115 and 116 with Optional User Provided Hardware**



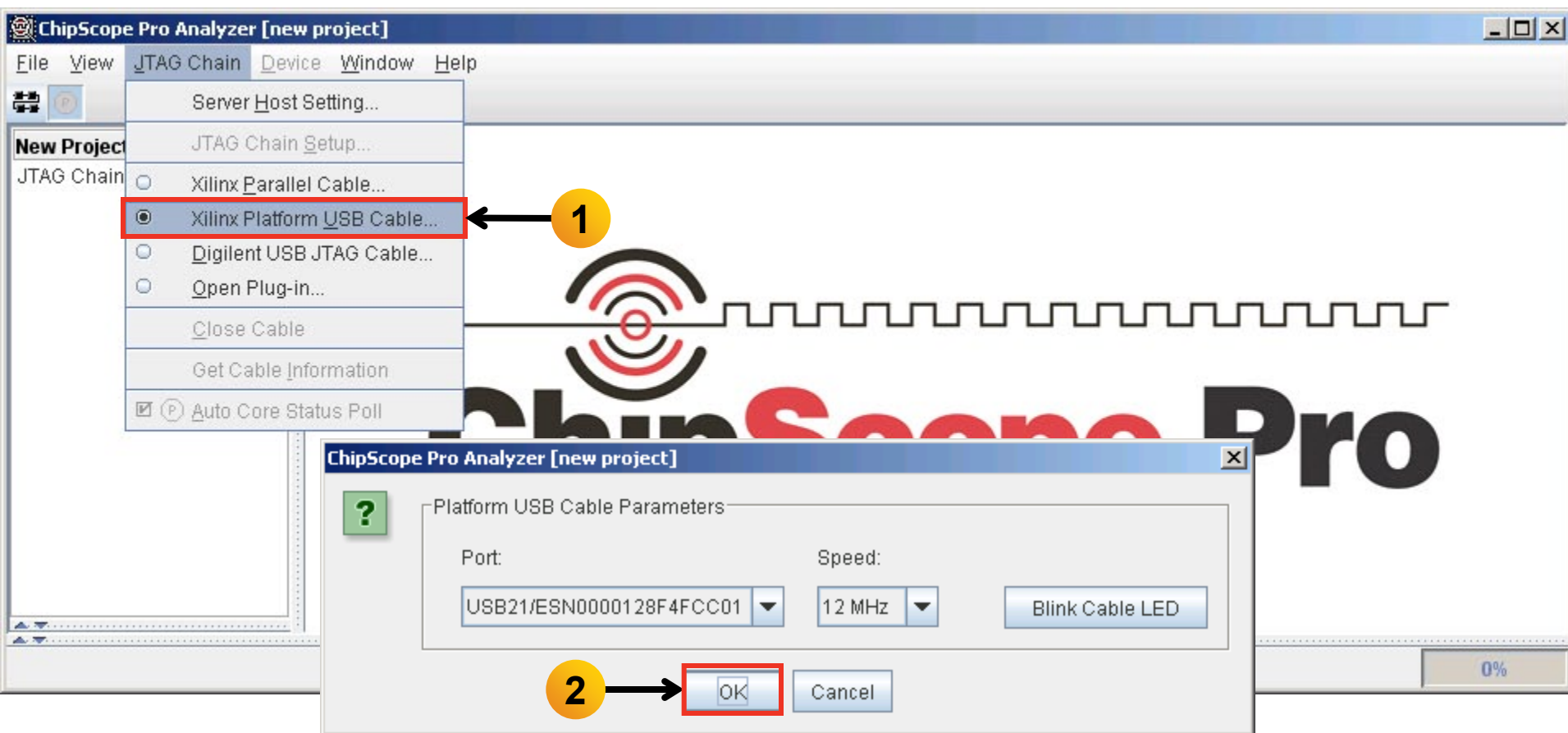
# Testing Banks 115 and 116 with Optional User Provided Hardware



- **Connect SMA Cables:**
  - TX0 P/N to RX0 P/N, TX1 P/N to RX1 P/N, etc.
- **Insert KC705 into PCIe slot**
- **Connect the KC705 and HiTechGlobal power supplies**
- **Power up the KC705 and HiTechGlobal boards**

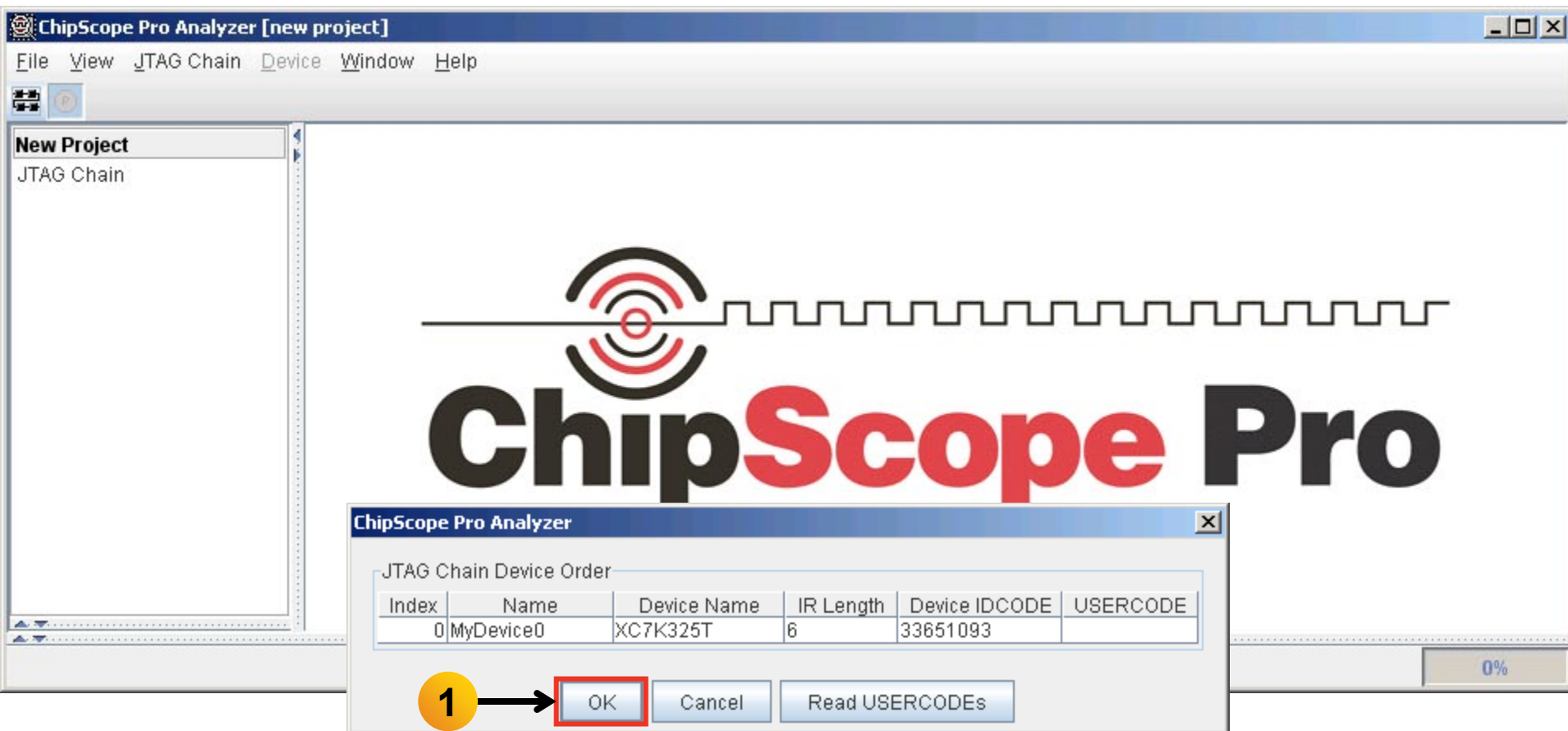
# Testing Banks 115 and 116 with Optional User Provided Hardware

- Open ChipScope Pro and select JTAG Chain → USB Cable... (1)
- Click OK (2)



# Testing Banks 115 and 116 with Optional User Provided Hardware

➤ Click OK (2)



The screenshot shows the ChipScope Pro Analyzer interface. The main window displays the "New Project" dialog box with the "JTAG Chain" tab selected. A smaller dialog box titled "ChipScope Pro Analyzer" is overlaid on the main window, showing the "JTAG Chain Device Order" table. The table contains one entry with Index 0, Name MyDevice0, Device Name XC7K325T, IR Length 6, Device IDCODE 33851093, and USERCODE. The "OK" button is highlighted with a red box and a yellow circle with the number 1, indicating the next step in the process.

Index	Name	Device Name	IR Length	Device IDCODE	USERCODE
0	MyDevice0	XC7K325T	6	33851093	

**Note:** Presentation applies to the KC705

# Testing Banks 115 and 116 with Optional User Provided Hardware

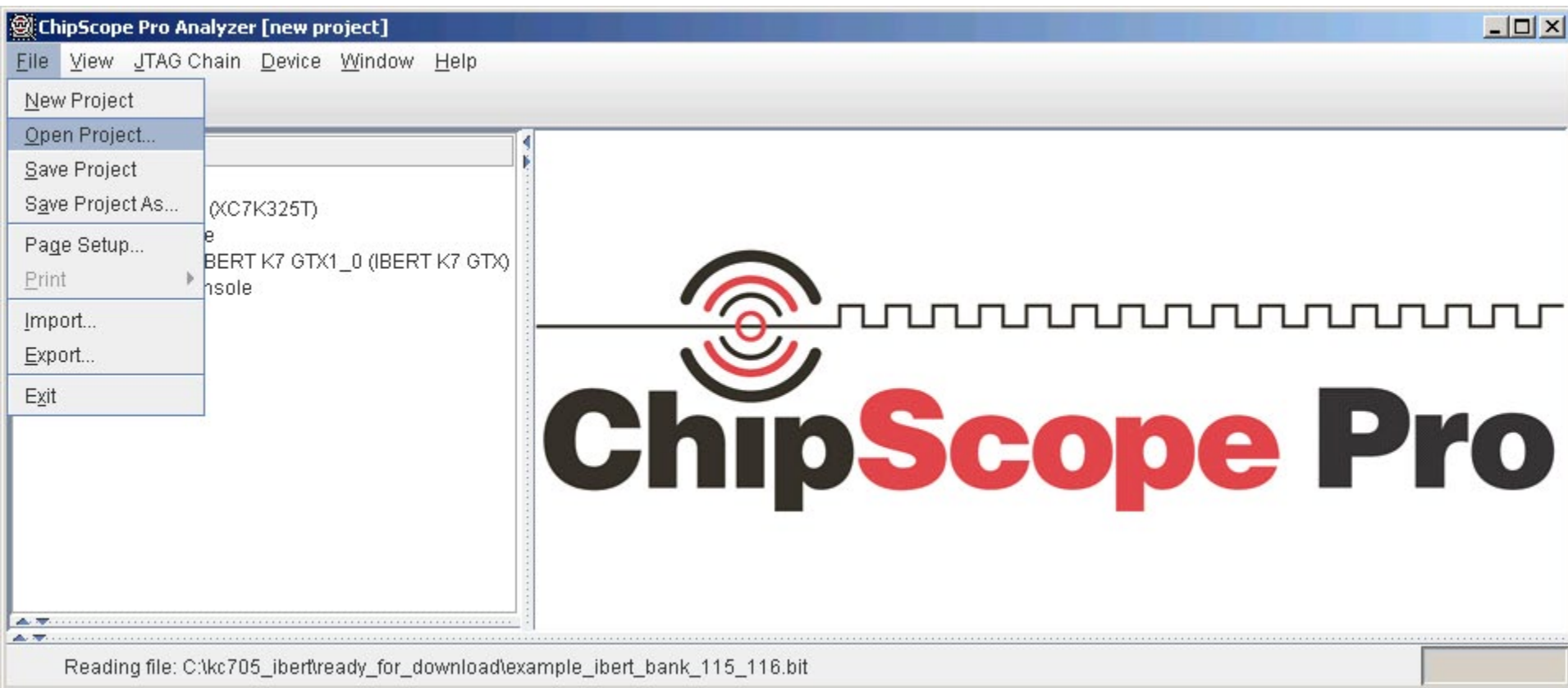
- Select Device → DEV:0 MyDevice0 (XC7K325T)... → Configure...
- Select <Design Path>\ready\_for\_download\  
example\_ibert\_bank\_115\_116.bit

The screenshot displays the ChipScope Pro Analyzer interface. The main window shows the JTAG Chain with 'DEV:0 MyDevice0 (XC7K325T)' selected. A context menu is open over the device name, with 'Configure...' highlighted. A dialog box titled 'ChipScope Pro Analyzer [new project]' is open on the right, showing the 'JTAG Configuration' section. The 'File' field is set to 'example\_ibert\_bank\_115\_116.bit' and the 'Directory' is 'C:\kc705\_ibertready\_for\_download'. There are checkboxes for 'Partial Reconfiguration Bitstream' and 'Clean previous project setting'. Below this is a 'Select New File' button. The 'Design-level CDC File' section is also visible, with a checkbox for 'Auto-create Buses' and its own 'File' and 'Directory' fields, also with a 'Select New File' button. At the bottom of the dialog are 'OK' and 'Cancel' buttons.

**Note:** Presentation applies to the KC705

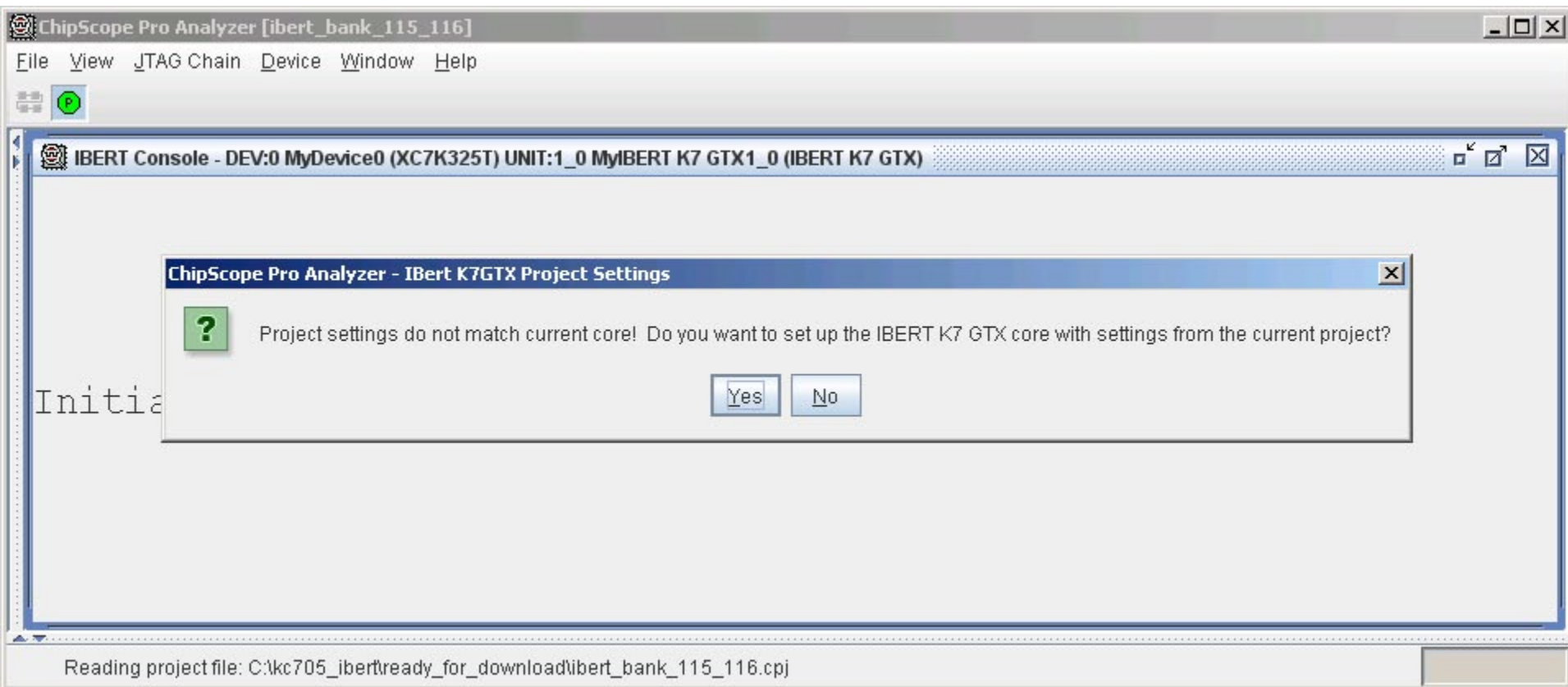
# Testing Banks 115 and 116 with Optional User Provided Hardware

- Select File → Open Project...
- Select <Design Path>\ready\_for\_download\ibert\_bank115\_116.cpj



# Testing Banks 115 and 116 with Optional User Provided Hardware

➤ Click Yes on this Dialog



# Testing Banks 115 and 116 with Optional User Provided Hardware

➤ The line rate is 5.0 Gbps for all GTXs (1)

ChipScope Pro Analyzer [ibert\_bank\_115\_116]

File View JTAG Chain Device IBERT\_K7GTX Window Help

JTAG Scan Rate: 1 s S! ↔

IBERT Console - DEV:0 MyDevice0 (XC7K325T) UNIT:1\_0 MyIBERT K7 GTX1\_0 (IBERT K7 GTX)

MGT/BERT Settings | DRP Settings | Port Settings | RX Margin Analysis

	GTX_X0Y0	GTX_X0Y1	GTX_X0Y2	GTX_X0Y3	GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7
<b>MGT Settings</b>								
- MGT Alias	GTX0_115	GTX1_115	GTX2_115	GTX3_115	GTX0_116	GTX1_116	GTX2_116	GTX3_116
- Tile Locati...	GTX_X0Y0	GTX_X0Y1	GTX_X0Y2	GTX_X0Y3	GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7
- MGT Link ...	5.0 Gbps	5.0 Gbps	5.0 Gbps	5.0 Gbps	5.0 Gbps	5.0 Gbps	5.0 Gbps	5.0 Gbps
- PLL Status	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED
- Loopback...	None	None	None	None	None	None	None	None
- Channel ...	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset
- TX/RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...

Reading project file: C:\kc705\_ibertready\_for\_download\ibert\_bank\_115\_116.cpj

Note: Bank 115, 116: PCIe

# Testing Banks 115 and 116 with Optional User Provided Hardware

- TX Diff Output Swing = 850 mV
- TX Pre-Cursor = 1.67 dB; TX Post-Cursor = 0.68 dB

ChipScope Pro Analyzer [ibert\_bank\_115\_116]

File View JTAG Chain Device IBERT\_K7GTX Window Help

JTAG Scan Rate: 1 s S! ↔

IBERT Console - DEV:0 MyDevice0 (XC7K325T) UNIT:1\_0 MyIBERT K7 GTX1\_0 (IBERT K7 GTX)

MGT/BERT Settings DRP Settings Port Settings RX Margin Analysis

	GTX_X0Y0		GTX_X0Y1		GTX_X0Y2		GTX_X0Y3		GTX_X0Y4		GTX_X0Y5		GTX_X0Y6		GTX_X0Y7	
- TX/RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...
- TX Polarity...	<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>	
- TX Error I...	Inject		Inject		Inject		Inject		Inject		Inject		Inject		Inject	
- TX Diff Ou...	850 mV (1...		850 mV (1...		850 mV (1...		850 mV (1...		850 mV (1...		850 mV (1...		850 mV (1...		850 mV (1...	
- TX Pre-Cu...	1.67 dB (0...		1.67 dB (0...		1.67 dB (0...		1.67 dB (0...		1.67 dB (0...		1.67 dB (0...		1.67 dB (0...		1.67 dB (0...	
- TX Post-C...	0.68 dB (0...		0.68 dB (0...		0.68 dB (0...		0.68 dB (0...		0.68 dB (0...		0.68 dB (0...		0.68 dB (0...		0.68 dB (0...	
- RX Polarity...	<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>	
- Terminati...	Program...		Program...		Program...		Program...		Program...		Program...		Program...		Program...	

Reading project file: C:\kc705\_ibertready\_for\_download\ibert\_bank\_115\_116.cpj



# Testing Banks 115 and 116 with Optional User Provided Hardware

- TX/RX Data Patterns are set to PRBS 31-bit (1)
- Click BERT Reset buttons (2)

ChipScope Pro Analyzer [ibert\_bank\_115\_116]

File View JTAG Chain Device IBERT\_K7GTX Window Help

JTAG Scan Rate: 1 s S! ↔

IBERT Console - DEV:0 MyDevice0 (XC7K325T) UNIT:1\_0 MyIBERT K7 GTX1\_0 (IBERT K7 GTX)

MGT/BERT Settings DRP Settings Port Settings RX Margin Analysis

	GTX_X0Y0	GTX_X0Y1	GTX_X0Y2	GTX_X0Y3	GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7
<b>MGT Settings</b>								
<b>BERT Settings</b>								
- TX Data P...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...
- RX Data P...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...
- RX Bit Err...	5.807E-010	5.721E-010	5.636E-010	5.838E-010	5.742E-010	5.888E-010	5.710E-010	5.630E-010
- RX Receiv...	1.076E012	1.077E012	1.077E012	1.077E012	1.078E012	1.078E012	1.079E012	1.075E012
- RX Bit Err...	6.250E002	6.160E002	6.070E002	6.290E002	6.190E002	6.350E002	6.160E002	6.050E002
- BERT Re...	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset

Reading project file: C:\kc705\_ibertready\_for\_download\ibert\_bank\_115\_116.cpj

# Testing Banks 115 and 116 with Optional User Provided Hardware

## ➤ View the RX Bit Error Count (1)

The screenshot shows the ChipScope Pro Analyzer interface. The main window is titled "IBERT Console - DEV:0 MyDevice0 (XC7K325T) UNIT:1\_0 MyIBERT K7 GTX1\_0 (IBERT K7 GTX)". The "RX Margin Analysis" tab is selected, displaying a table of RX Bit Error Count (RX Bit Err...) for eight GTX channels (GTX\_X0Y0 to GTX\_X0Y7). The RX Bit Error Count for all channels is 0.000E000, which is highlighted with a red border. A yellow circle with the number "1" and an arrow points to the "Reset" button for the GTX\_X0Y3 channel.

	GTX_X0Y0	GTX_X0Y1	GTX_X0Y2	GTX_X0Y3	GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7
<b>MGT Settings</b>								
<b>BERT Settings</b>								
- TX Data P...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...
- RX Data P...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...
- RX Bit Err...	9.470E-013	9.533E-013	9.539E-013	9.576E-013	9.616E-013	9.623E-013	9.664E-013	9.673E-013
- RX Receiv...	1.056E012	1.049E012	1.048E012	1.044E012	1.040E012	1.039E012	1.035E012	1.034E012
- RX Bit Err...	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000
- BERT Re...	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset

Reading project file: C:\kc705\_ibertready\_for\_download\ibert\_bank\_115\_116.cpj

1

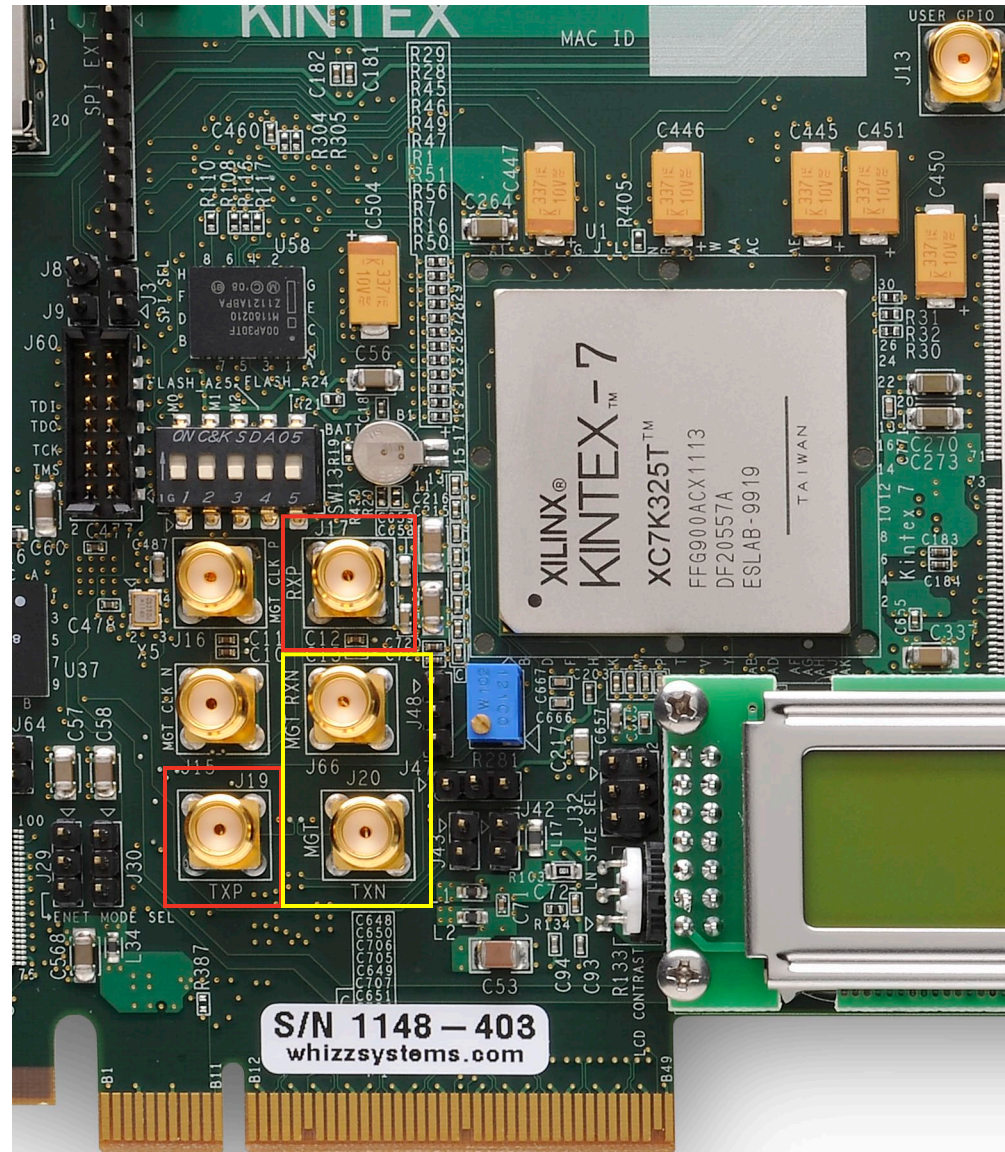


# **Testing Bank 117 and 118 with Optional User Provided Hardware**

# Testing Bank 117 and 118 with Optional User Provided Hardware

## ➤ Using the SMA cables:

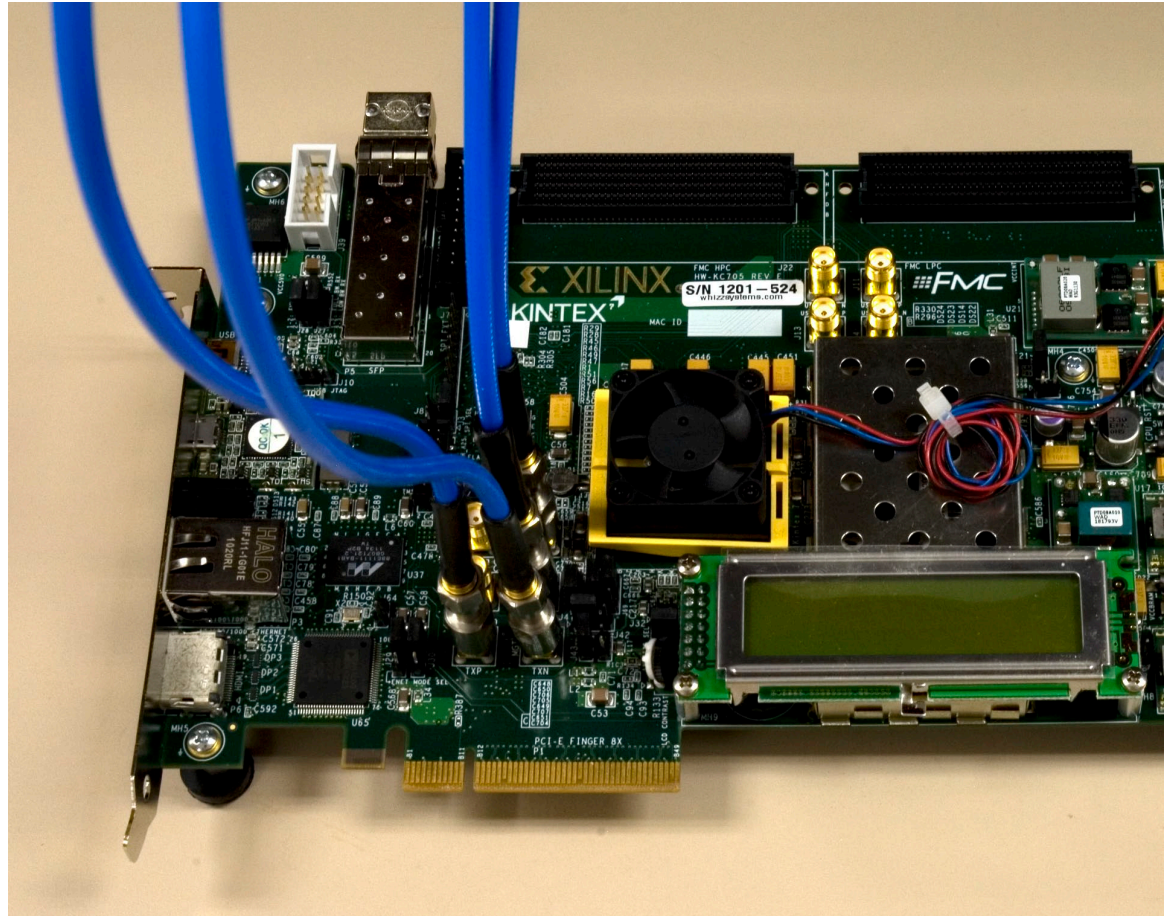
- Connect J19 to J17
- Connect J20 to J66



Note: Presentation applies to the KC705

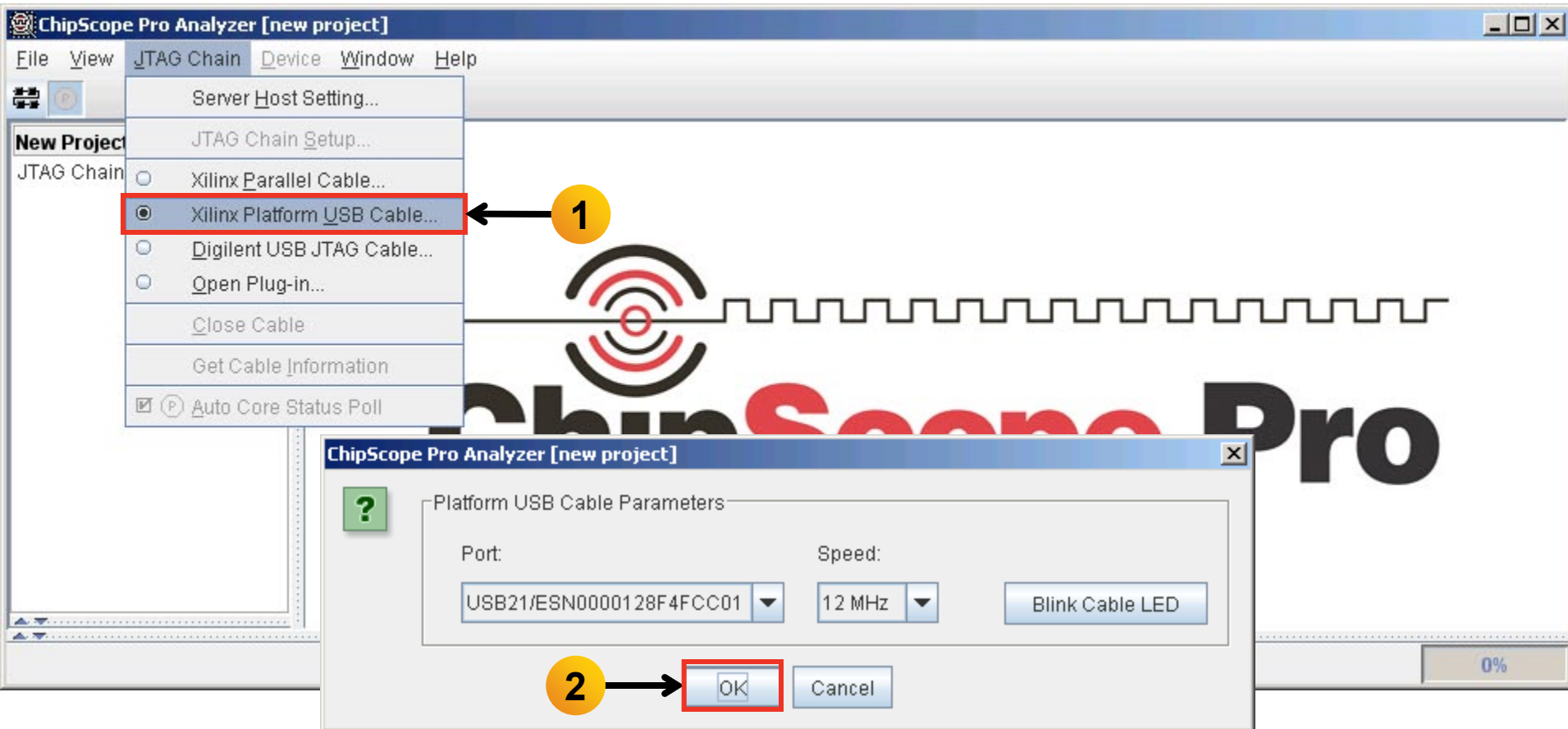
# Testing Bank 117 and 118 with Optional User Provided Hardware

- Insert the SFP Loopback Adapter
- Power on the KC705 board



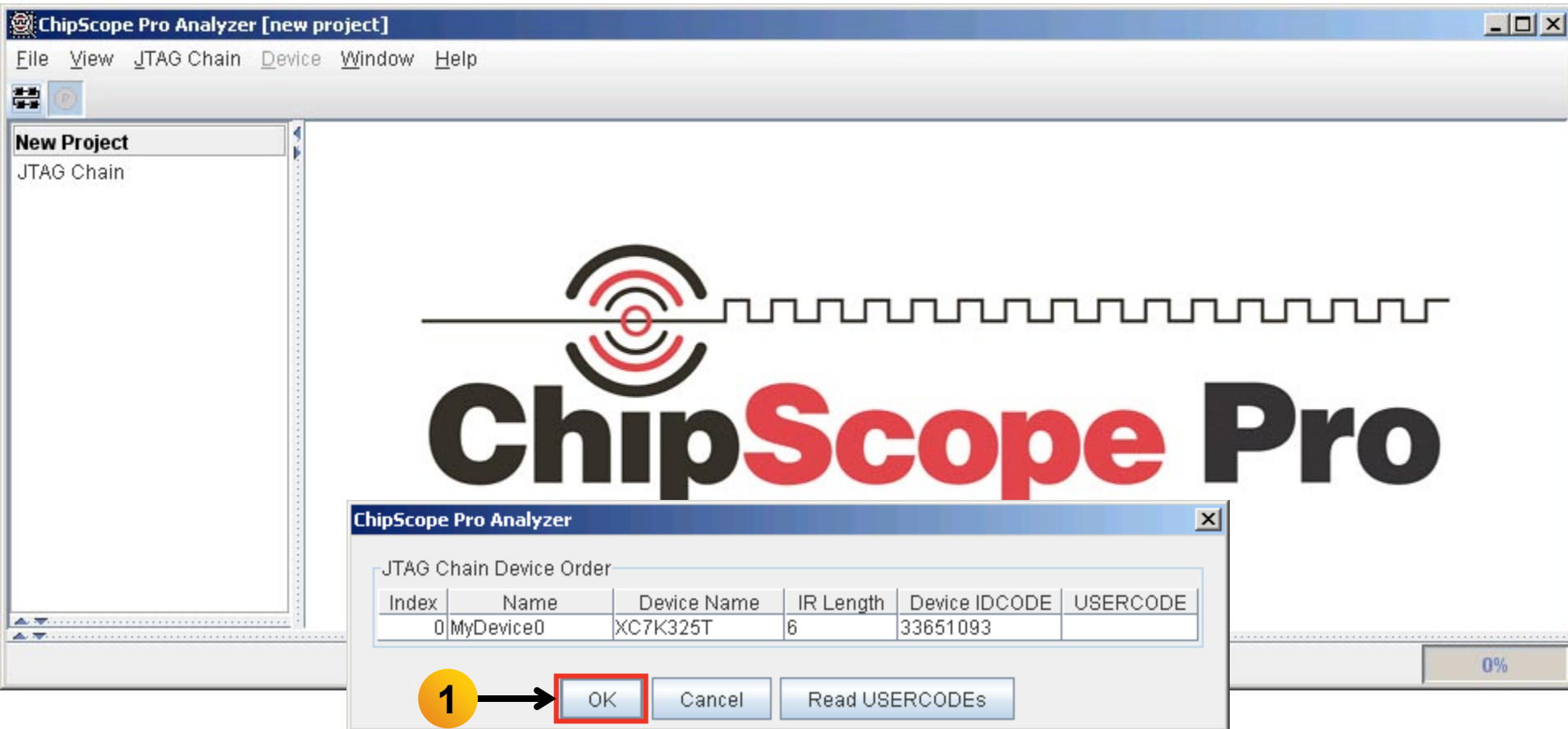
# Testing Bank 117 and 118 with Optional User Provided Hardware

- Open ChipScope Pro and select JTAG Chain → USB Cable... (1)
- Click OK (2)



# Testing Bank 117 and 118 with Optional User Provided Hardware

➤ Click OK (1)



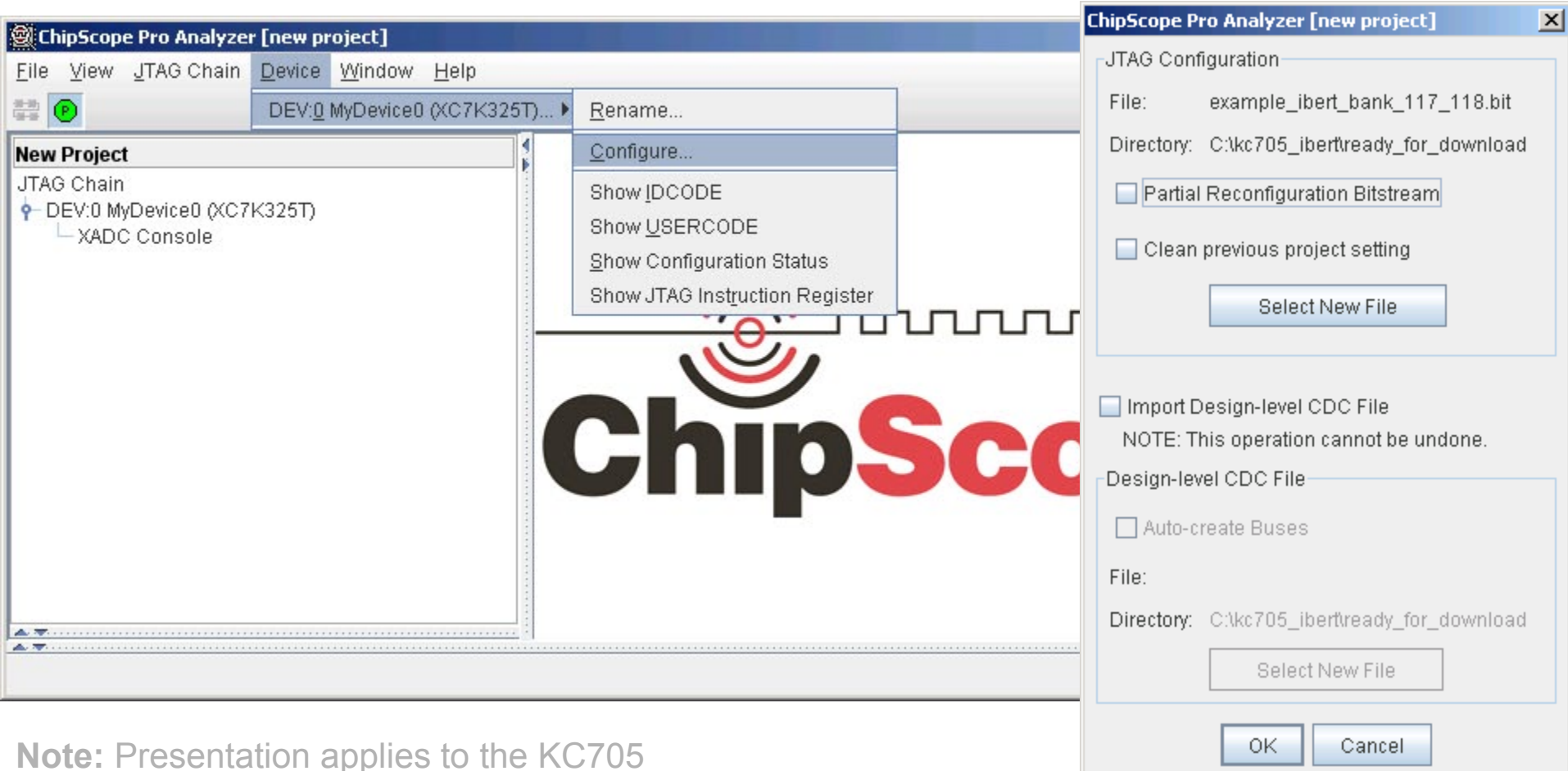
The screenshot shows the ChipScope Pro Analyzer interface. The main window displays the "New Project" dialog box with the "JTAG Chain" tab selected. A smaller dialog box titled "ChipScope Pro Analyzer" is overlaid on the main window, showing the "JTAG Chain Device Order" table. The table contains one entry: Index 0, Name MyDevice0, Device Name XC7K325T, IR Length 6, Device IDCODE 33851093, and USERCODE. The "OK" button in this dialog box is highlighted with a red box and a yellow circle with the number 1, indicating the step to click OK.

Index	Name	Device Name	IR Length	Device IDCODE	USERCODE
0	MyDevice0	XC7K325T	6	33851093	

**Note:** Presentation applies to the KC705

# Testing Bank 117 and 118 with Optional User Provided Hardware

- Select Device → DEV:0 MyDevice0 (XC7K325T)... → Configure...
- Select <Design Path>\ready\_for\_download\  
example\_ibert\_bank\_117\_118.bit



The screenshot displays the ChipScope Pro Analyzer software interface. The main window shows the 'New Project' dialog box, which is used to configure the JTAG configuration and design-level CDC file. The 'JTAG Configuration' section includes fields for 'File' (example\_ibert\_bank\_117\_118.bit) and 'Directory' (C:\kc705\_ibertready\_for\_download). There are checkboxes for 'Partial Reconfiguration Bitstream' and 'Clean previous project setting'. A 'Select New File' button is present. The 'Design-level CDC File' section includes a checkbox for 'Auto-create Buses' and fields for 'File' and 'Directory' (C:\kc705\_ibertready\_for\_download). There is another 'Select New File' button. The 'OK' and 'Cancel' buttons are at the bottom.

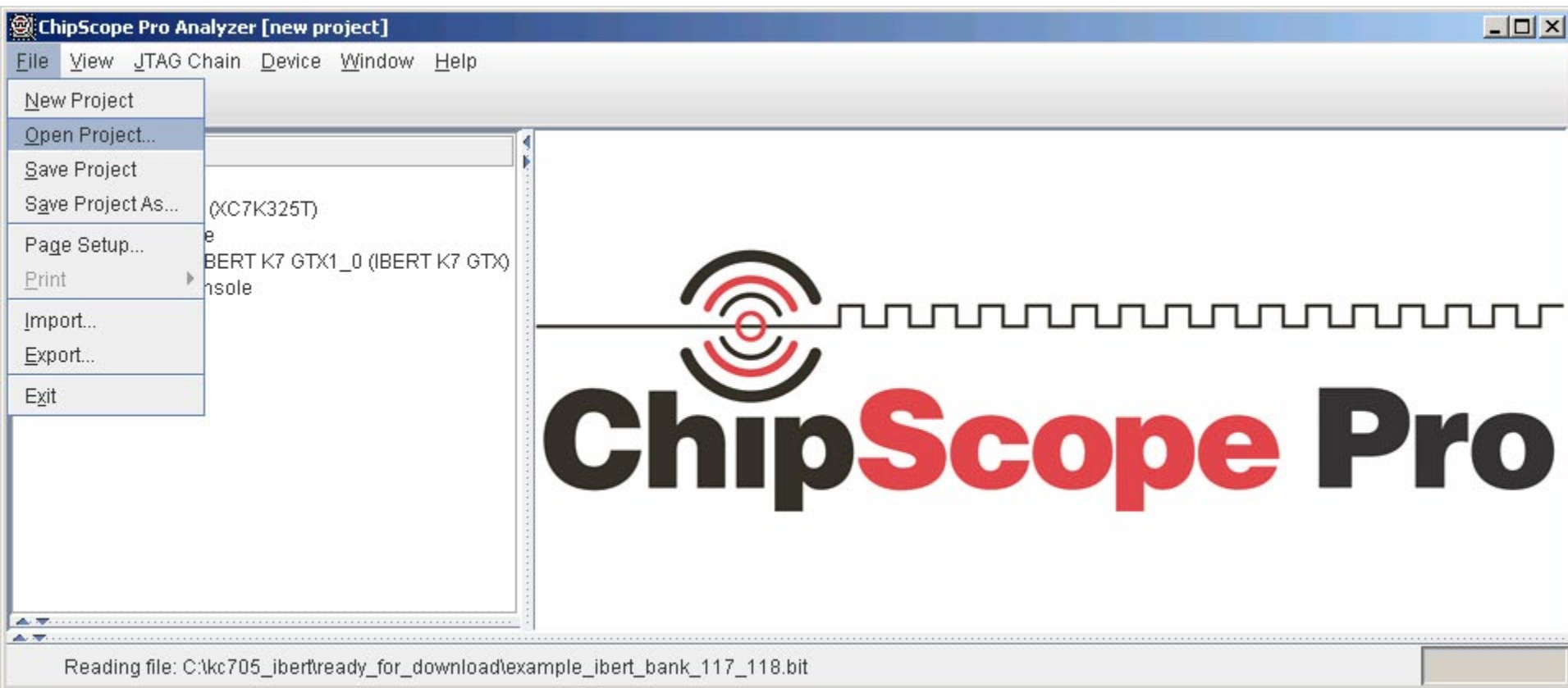
The 'Device' menu is open, showing options for 'DEV:0 MyDevice0 (XC7K325T)...'. The 'Configure...' option is highlighted. Other options include 'Rename...', 'Show IDCODE', 'Show USERCODE', 'Show Configuration Status', and 'Show JTAG Instruction Register'.

**Note:** Presentation applies to the KC705



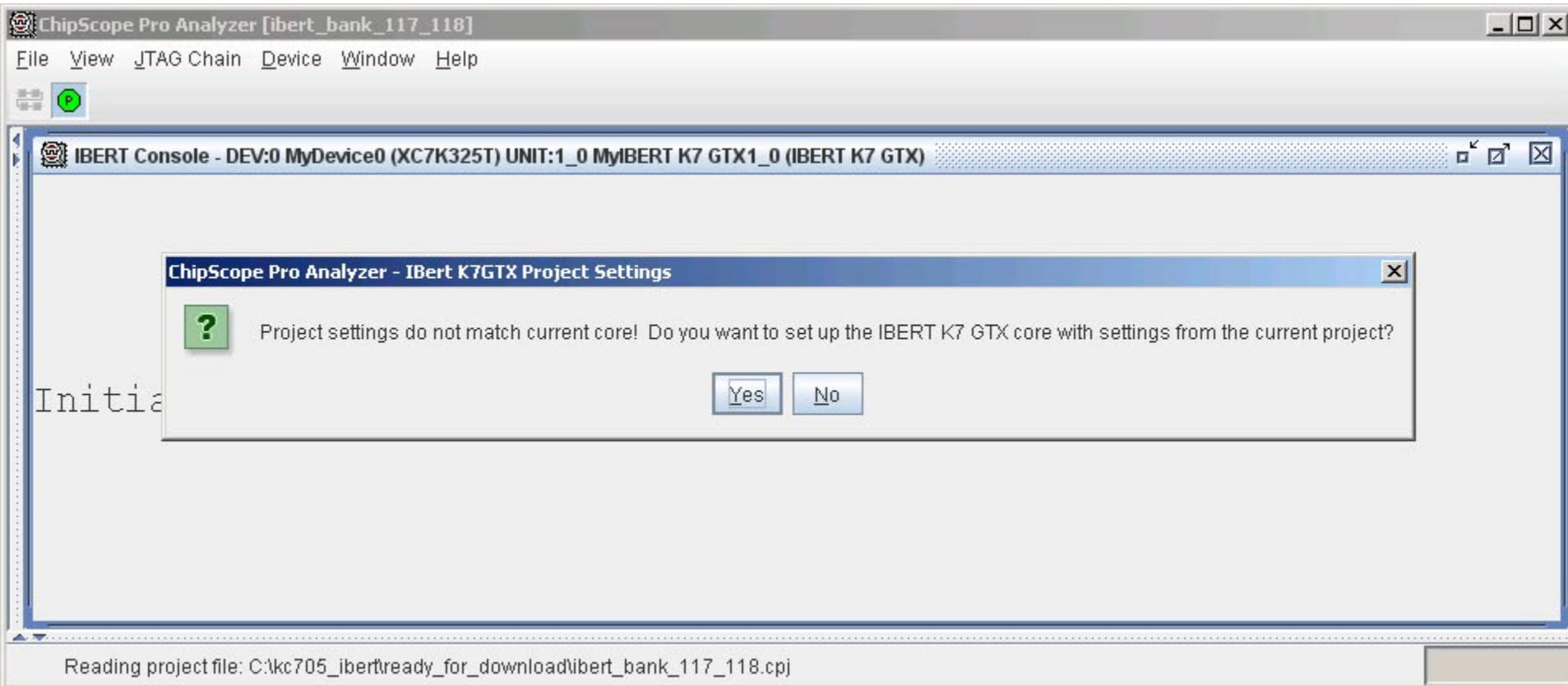
# Testing Bank 117 and 118 with Optional User Provided Hardware

- Select File → Open Project...
- Select <Design Path>\ready\_for\_download\ibert\_bank117\_118.cpj



# Testing Bank 117 and 118 with Optional User Provided Hardware

➤ Click Yes on this Dialog



# Testing Bank 117 and 118 with Optional User Provided Hardware

- The line rate is 10.0 Gbps for all GTXs (1)
- Set GTX0\_117 and GTX2\_117 to None (2)

ChipScope Pro Analyzer [ibert\_bank\_117\_118]

IBERT Console - DEV:0 MyDevice0 (XC7K325T) UNIT:1\_0 MyIBERT K7 GTX1\_0 (IBERT K7 GTX)

MGT/BERT Settings | DRP Settings | Port Settings | RX Margin Analysis

	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
<b>MGT Settings</b>								
- MGT Alias	GTX0_117	GTX1_117	GTX2_117	GTX3_117	GTX0_118	GTX1_118	GTX2_118	GTX3_118
- Tile Locati...	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
- MGT Link ...	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps
- PLL Status	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED
- Loopback...	None	Near-End ...	None	Near-End ...	Near-End ...	Near-End ...	Near-End ...	Near-End ...
- Channel ...	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset
- TX/RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...	TX Re... RX Re...

Reading project file: C:\kc705\_ibertready\_for\_download\ibert\_bank\_117\_118.cpj

**Note:** Bank 117,118: SMA, SGMII, SFP, FMC

# Testing Bank 117 and 118 with Optional User Provided Hardware

- TX Diff Output Swing = 850 mV
- TX Pre-Cursor = 1.67 dB; TX Post-Cursor = 0.68 dB

ChipScope Pro Analyzer [ibert\_bank\_117\_118]

File View JTAG Chain Device IBERT\_K7GTX Window Help

JTAG Scan Rate: 1 s S! ↔

IBERT Console - DEV:0 MyDevice0 (XC7K325T) UNIT:1\_0 MyIBERT K7 GTX1\_0 (IBERT K7 GTX)

MGT/BERT Settings | DRP Settings | Port Settings | RX Margin Analysis

	GTX_X0Y8		GTX_X0Y9		GTX_X0Y10		GTX_X0Y11		GTX_X0Y12		GTX_X0Y13		GTX_X0Y14		GTX_X0Y15	
- TX/RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...	TX Re...	RX Re...
- TX Polarit...	<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>	
- TX Error I...	Inject		Inject		Inject		Inject		Inject		Inject		Inject		Inject	
- TX Diff Ou...	850 mV (1...		850 mV (1...		850 mV (1...		850 mV (1...		850 mV (1...		850 mV (1...		850 mV (1...		850 mV (1...	
- TX Pre-Cu...	1.67 dB (0...		1.67 dB (0...		1.67 dB (0...		1.67 dB (0...		1.67 dB (0...		1.67 dB (0...		1.67 dB (0...		1.67 dB (0...	
- TX Post-C...	0.68 dB (0...		0.68 dB (0...		0.68 dB (0...		0.68 dB (0...		0.68 dB (0...		0.68 dB (0...		0.68 dB (0...		0.68 dB (0...	
- RX Polarit...	<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>	
- Terminati...	Program...		Program...		Program...		Program...		Program...		Program...		Program...		Program...	

Reading project file: C:\kc705\_ibertready\_for\_download\ibert\_bank\_117\_118.cpj

# Testing Bank 117 and 118 with Optional User Provided Hardware

- TX/RX Data Patterns are set to PRBS 31-bit (1)
- Click BERT Reset buttons (2)

The screenshot shows the ChipScope Pro Analyzer interface for the IBERT console. The 'MGT/BERT Settings' tab is active, displaying a table of settings for eight GTX banks (GTX\_X0Y8 to GTX\_X0Y15). The table is divided into 'MGT Settings' and 'BERT Settings' sections. The 'BERT Settings' section includes rows for TX Data P., RX Data P., RX Bit Err., RX Receiv., and BERT Re... (Reset buttons). A red box highlights the PRBS 31-bit settings and the Reset buttons for all banks. A yellow circle with the number '1' points to the PRBS dropdown menus, and a yellow circle with the number '2' points to the Reset buttons.

	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
<b>MGT Settings</b>								
<b>BERT Settings</b>								
- TX Data P...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...
- RX Data P...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...
- RX Bit Err...	1.818E-001	1.260E-001	1.604E-001	3.746E-010	1.098E-001	1.101E-001	1.323E-001	1.324E-001
- RX Receiv...	2.175E012	2.176E012	2.177E012	2.178E012	2.179E012	2.180E012	2.181E012	2.182E012
- RX Bit Err...	3.954E011	2.742E011	3.492E011	8.160E002	2.393E011	2.400E011	2.884E011	2.889E011
- BERT Re...	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset

# Testing Bank 117 and 118 with Optional User Provided Hardware

- View the RX Bit Error Count on the SMA and SFP (1)

The screenshot displays the ChipScope Pro Analyzer interface for the IBERT Console. The window title is "ChipScope Pro Analyzer [ibert\_bank\_117\_118]". The main window shows the "IBERT Console - DEV:0 MyDevice0 (XC7K325T) UNIT:1\_0 MyIBERT K7 GTX1\_0 (IBERT K7 GTX)" with tabs for "MGT/BERT Settings", "DRP Settings", "Port Settings", and "RX Margin Analysis". The "RX Margin Analysis" tab is active, showing a table of RX Bit Error Counts for various GTX channels. The table has columns for GTX\_X0Y8 through GTX\_X0Y15. The "RX Bit Err..." row shows values ranging from 5.833E-012 to 7.726E-012. The "RX Bit Err..." row shows values of 0.000E000 for GTX\_X0Y8 and GTX\_X0Y10, which are highlighted with red boxes. Below these boxes are "Reset" buttons, each with a yellow circle containing the number "1" and an arrow pointing to the button.

	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
<b>MGT Settings</b>								
<b>BERT Settings</b>								
- TX Data P...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...
- RX Data P...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...
- RX Bit Err...	5.833E-012	5.919E-012	6.324E-012	6.645E-012	6.756E-012	7.180E-012	7.603E-012	7.726E-012
- RX Receiv...	1.714E011	1.689E011	1.581E011	1.505E011	1.480E011	1.393E011	1.315E011	1.294E011
- RX Bit Err...	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000
- BERT Re...	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset

Reading project file: C:\ker\_05\_ibertready\_for\_download\ibert\_bank\_117\_118.cpj



## References

# References

## ➤ ChipScope Pro

– ChipScope Pro Software and Cores User Guide

- [http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx14\\_3/chipscope\\_pro\\_sw\\_cores\\_ug029.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_3/chipscope_pro_sw_cores_ug029.pdf)



# Documentation

# Documentation

## ➤ Kintex-7

- Kintex-7 FPGA Family

- <http://www.xilinx.com/products/silicon-devices/fpga/kintex-7/index.htm>

## ➤ KC705 Documentation

- Kintex-7 FPGA KC705 Evaluation Kit

- <http://www.xilinx.com/products/boards-and-kits/EK-K7-KC705-G.htm>

- KC705 Getting Started Guide

- [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug883\\_K7\\_KC705\\_Eval\\_Kit.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug883_K7_KC705_Eval_Kit.pdf)

- KC705 User Guide

- [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug810\\_KC705\\_Eval\\_Bd.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug810_KC705_Eval_Bd.pdf)

- KC705 Reference Design User Guide

- [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug845\\_Ref\\_Design.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug845_Ref_Design.pdf)