Optique - état de l'art
(futurs composants optiques)

C2N

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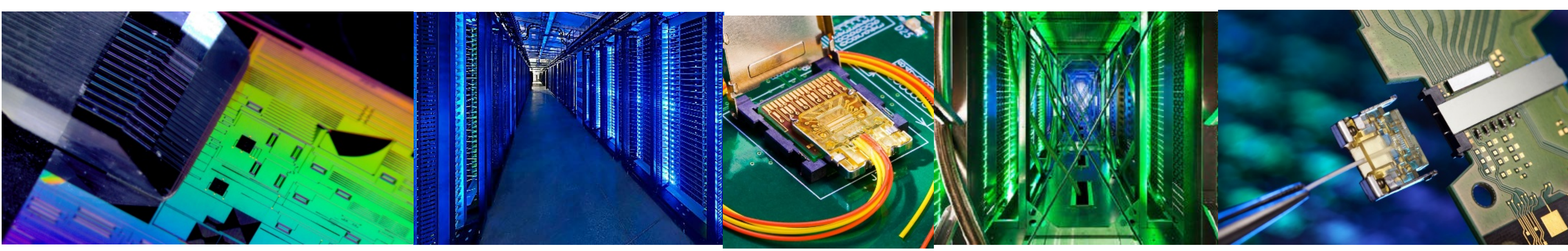
http://silicon-photonics.ief.u-psud.fr/



Source of images: Intel, Google

Outline

- Motivation
  - √ Photonics – integrated optics and optoelectronics
  - √ Why do we want to use silicon for photonic applications?
  - √ What are the main challenges?
  - √ Is silicon a good material for optics applications?
  - √ What are the markets?
- Main building blocks in photonics
  - √ Light propagation
  - √ Optical modulation
  - √ Light detection
  - √ Light emission
- Conclusion

FTTH

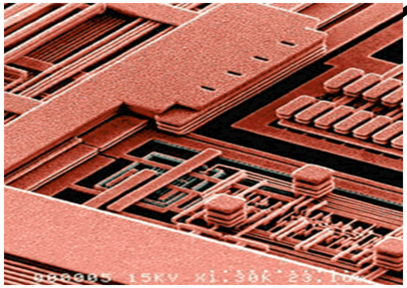
Optical telecommunications

Environment

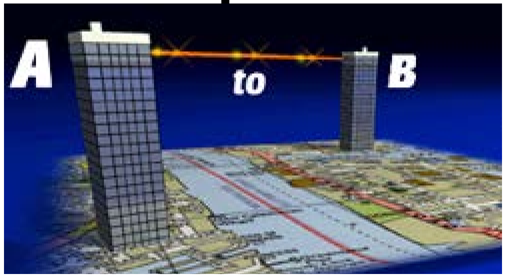
Data centers

Photonics

Chemical/Biological sensors



Interconnects



Free space communications

Military

… among the « hot topics » in photonics

Silicon Photonics

Photonic integration…

1958

Integrated Circuit
Jack Kilby

2010

1960

LASER
Theodore Maiman

Source: Wim Bogaerts – Gent Univ. and IMEC

Battle between Optics and Copper

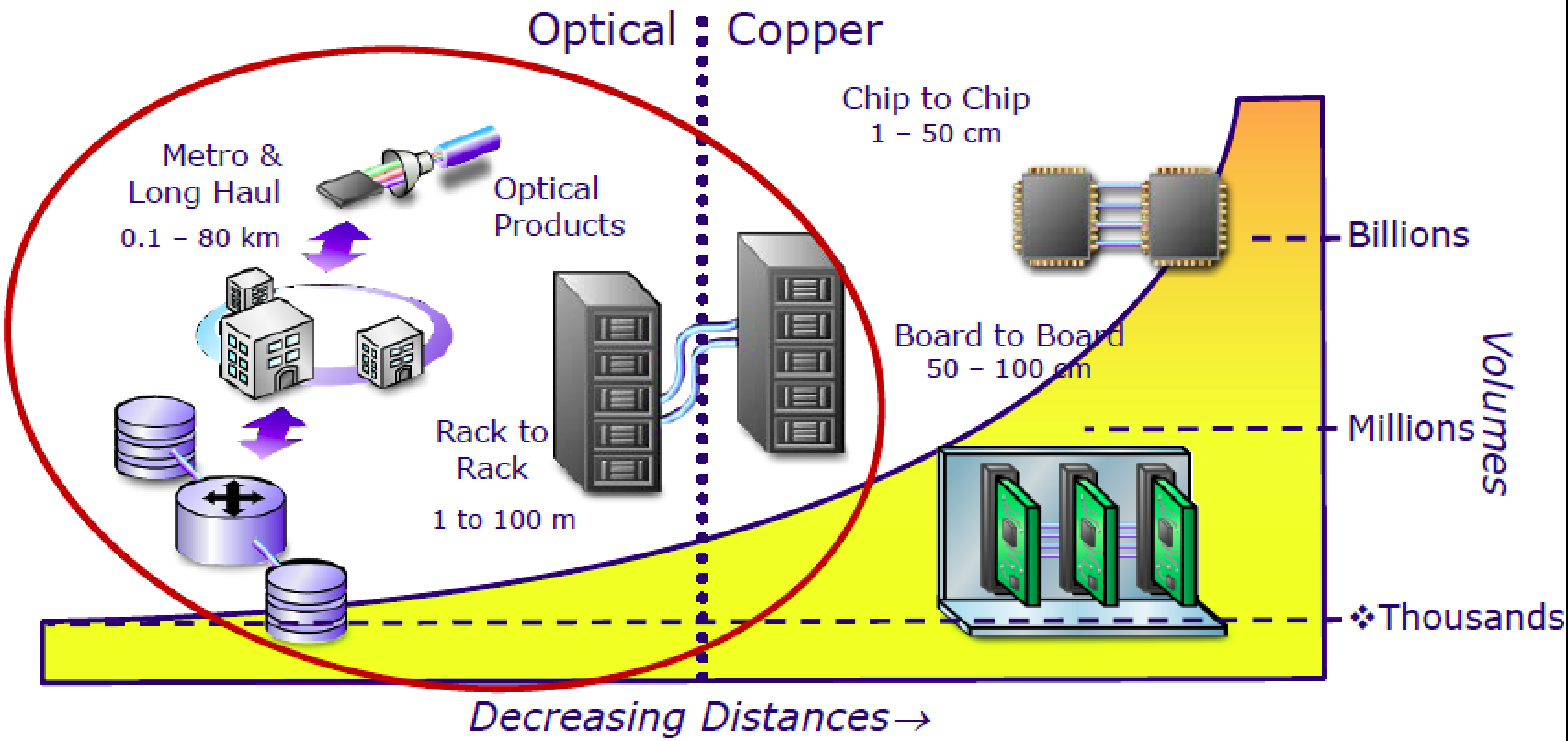


Figure Courtesy of Mario Paniccia, Intel

Optics has progressively eliminated copper in the metro and long haul network in the last 20 years

Global internet traffic

Source of images: Google

VIDEO, HD TV

File sharing

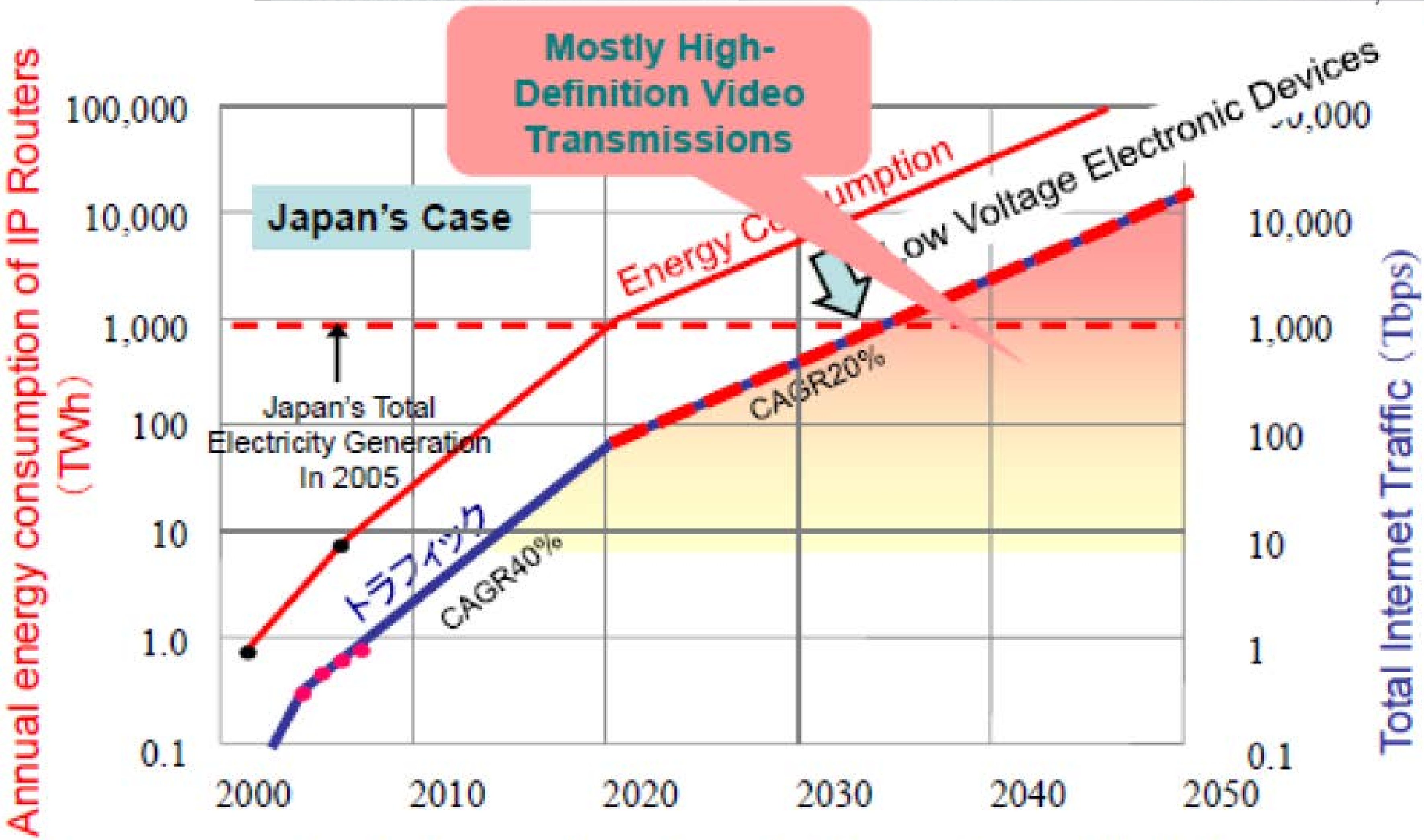
On-line games

Internet traffic doubling every 18 months

Estimated trans-atlantic traffic in 2025: 400 Tbit/s

E. Desurvire, J.Lightwave Technol., vol. 24, no. 12, (2006), "Capacity Demand…Next…

Evolution in Japan

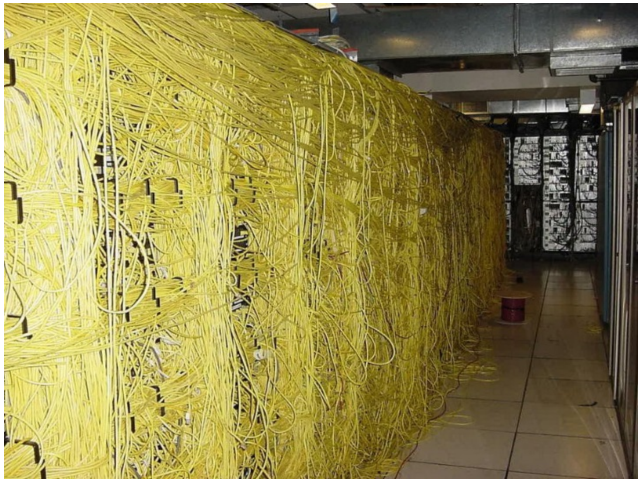


- The current technologies can't scale to the increasing traffic in future.
- 3-4 digit energy saving is necessary, which means we need a new paradigm.

S. Namiki et al., OECC2009, FT2, Hong Kong

http://www.aist.go.jp

Data centres

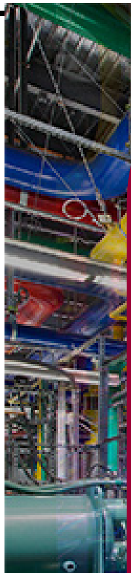


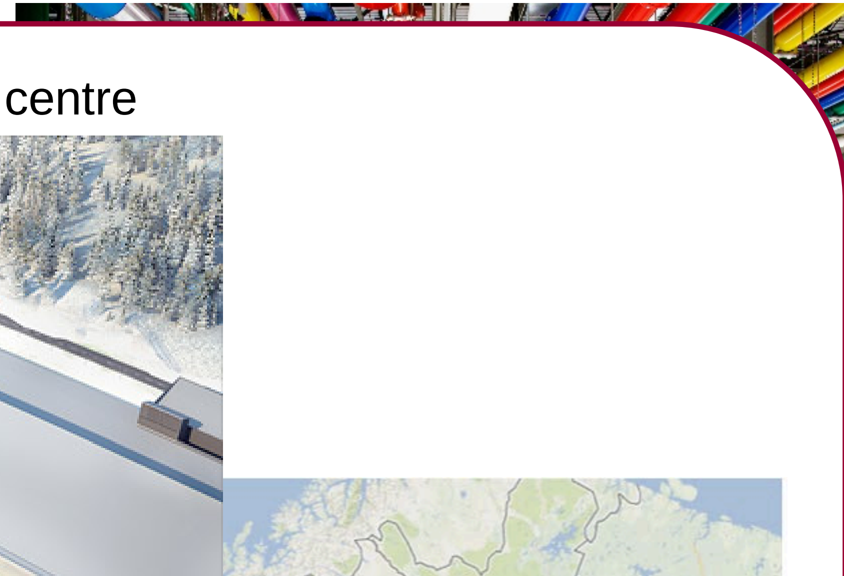
100 000+ x 10 Gbit/s servers in data centre

80% data centre traffic inside data centre (>1km)

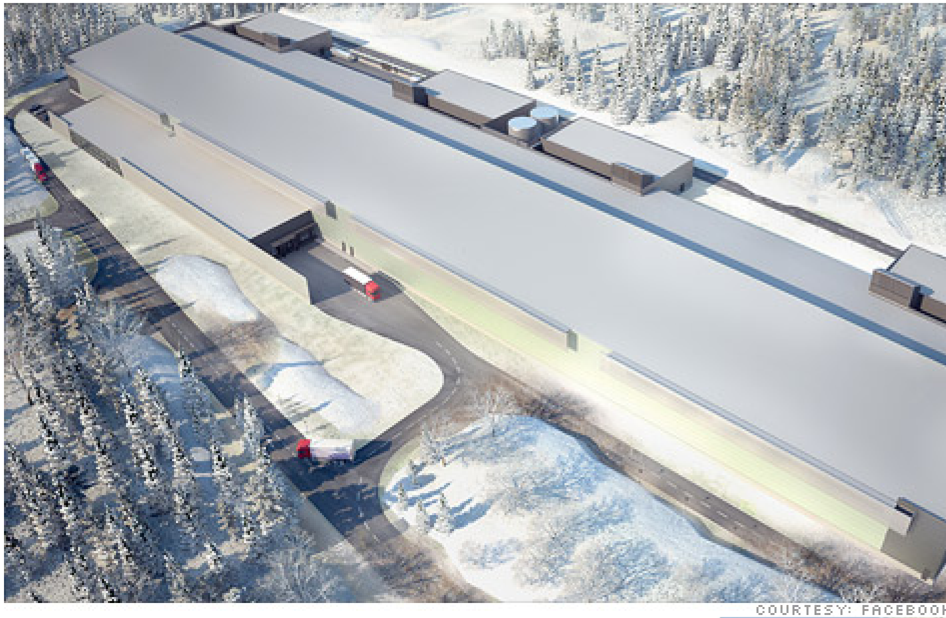
50% of data centre power for cooling

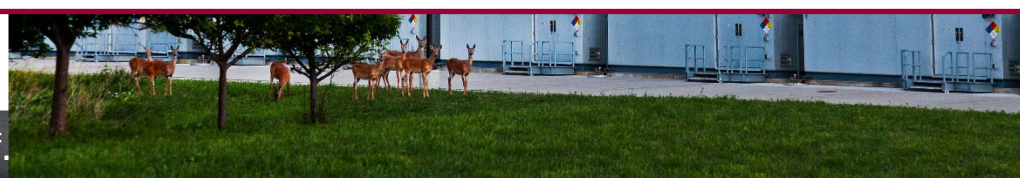
Cooling system !?





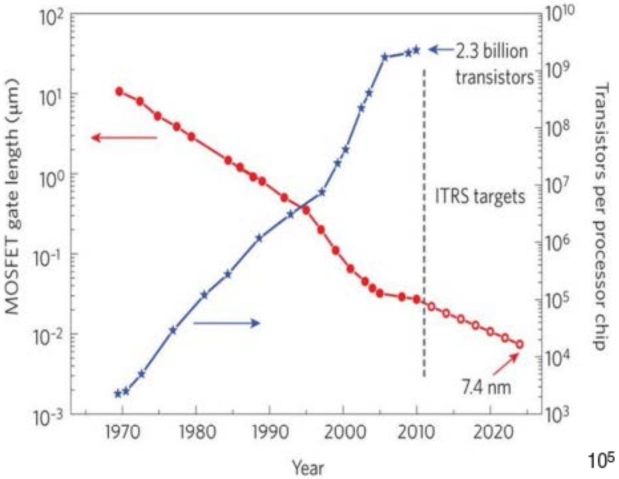
Facebook launches Arctic data centre

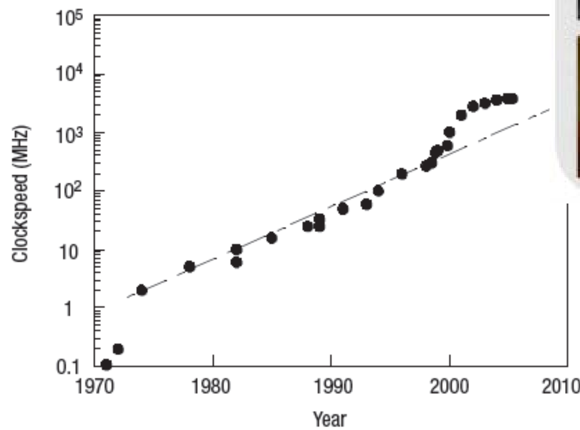


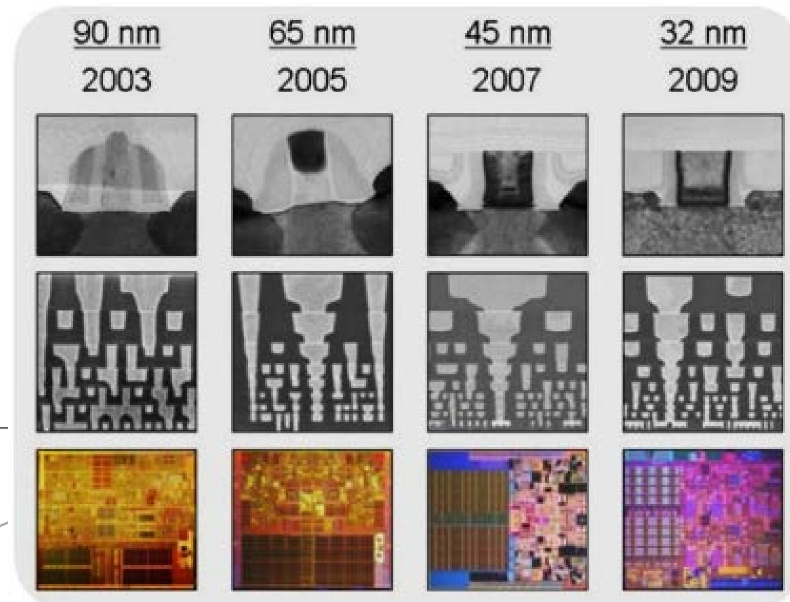


Copper interconnects in IC

- Increase of integrated circuit complexity
  - √ Number of transistors
  - √ Frequency operation
  - √ Length and density of metallic interconnects



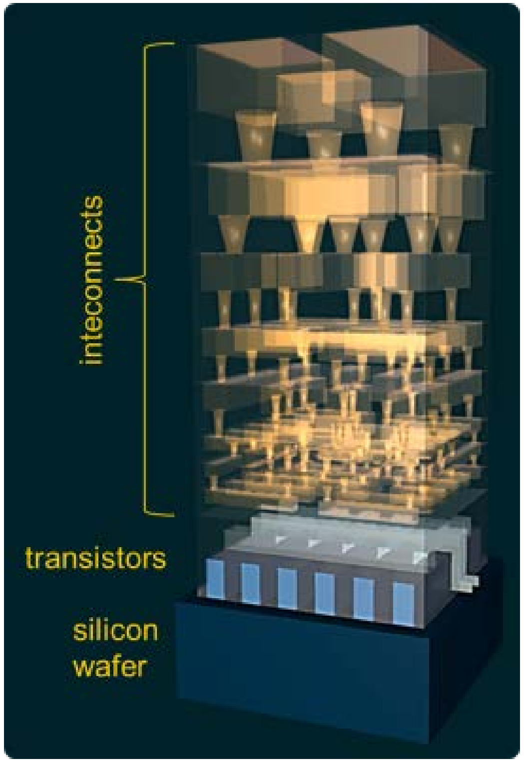




Source: ITRS and Intel

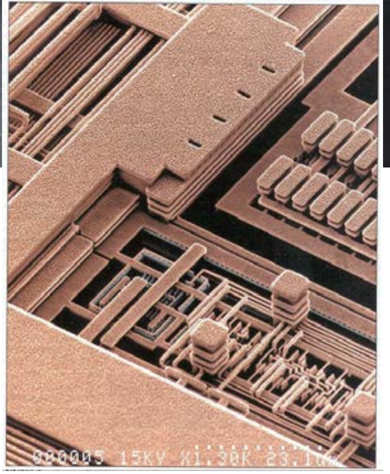
DA. Muller, Nature Mat. 4, 645, 2005

Reverse scaling



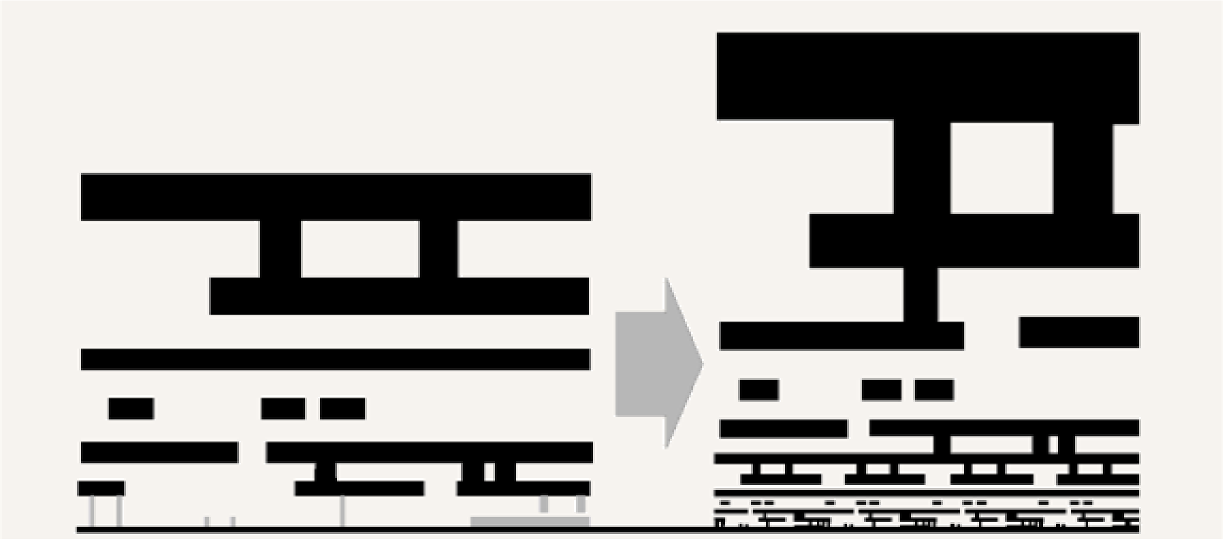
Source: http://semimd.com/

R and C increase !



Source: IBM

Metallic interconnects

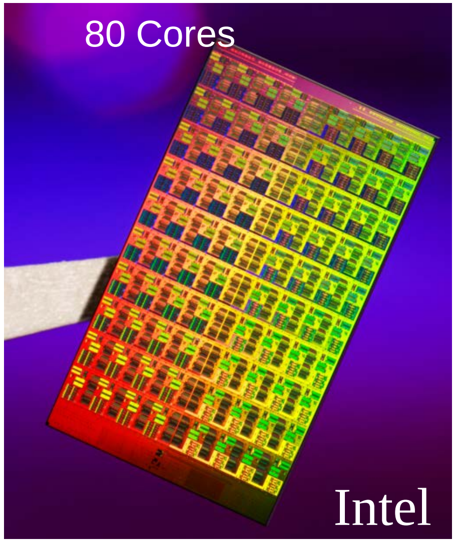


To improve performances

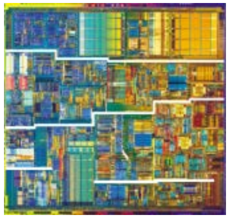
Performance = Parallelism x Frequency

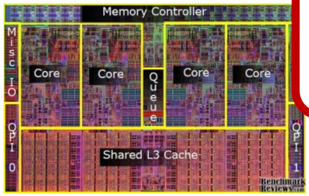
- Need more cores, memories, switches
- More integration

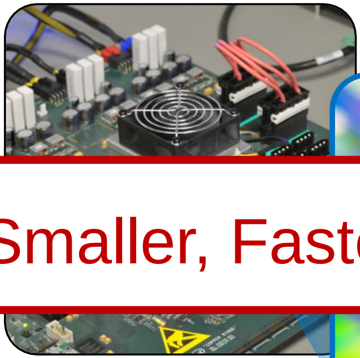
- Cu interconnect limitations

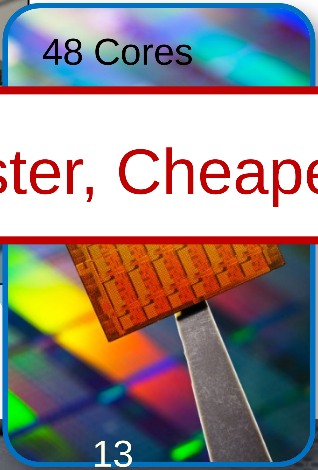


Examples:



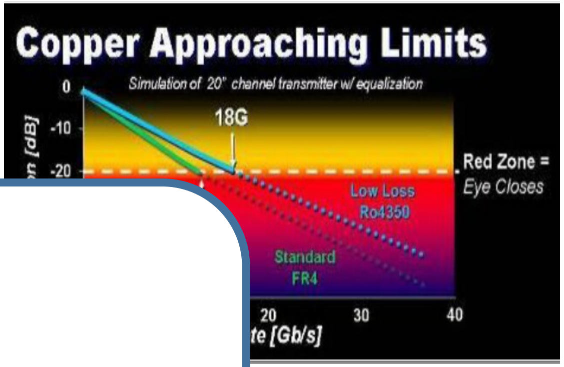






Smaller, Faster, Cheaper

The problems for the next generation of communication systems



Source: Intel

- √ Attenuation of Cu vs propagation length
- √ Energy consumption
- √ Interconnect
- √ Frequency

Use photonics at the chip scale to:

- ➢ Increase the data transmission
- ➢ Reduce the power consumption

Convergence between electronics and photonics

- ➢ Increase the data processing

- √ length (speed
- √ bend radius,
- √ Weight
- √ Thickness (compactness)

Optical Fiber

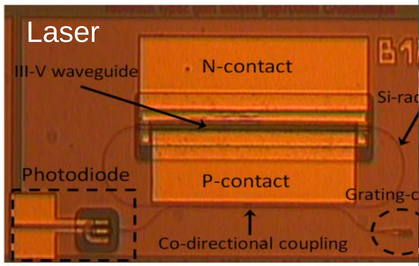
In data centers

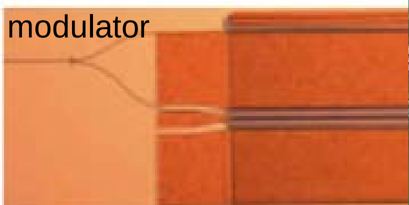
Source: IBM

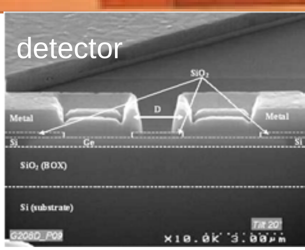
Towards at the end…

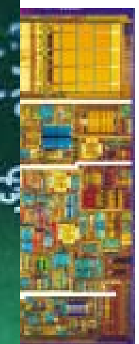
Silicon
Photonic

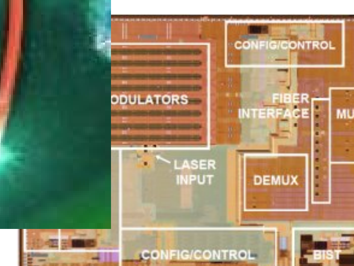
alog
Circuits











Source: Luxtera

Optics vs microelectronics

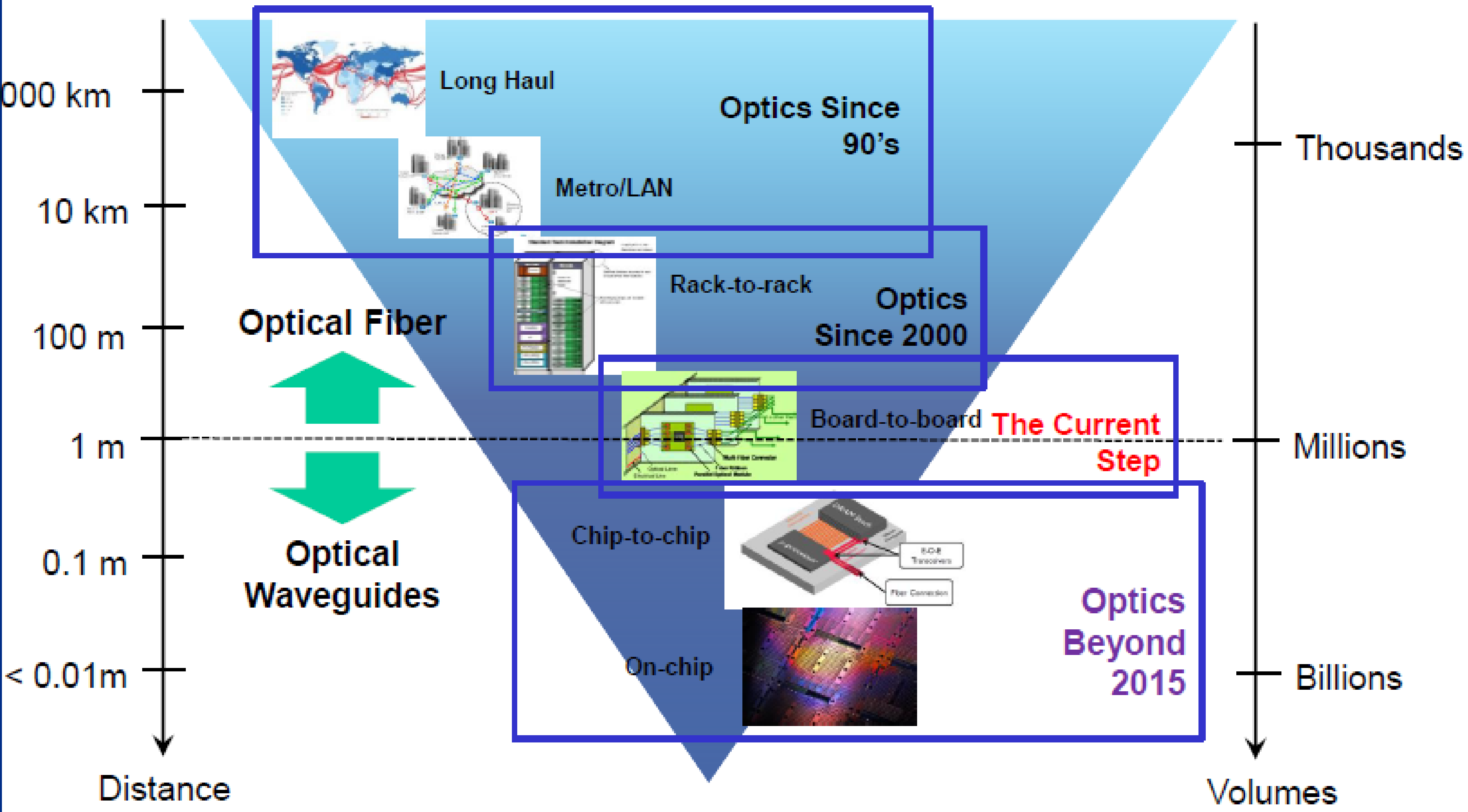
	Microelectronics
Building blocks	Transistor
Material	Silicon
Manufacturing technology	CMOS

Optics vs microelectronics

	Microelectronics	**Silicon Photonics**
Building blocks	Transistor	Laser, waveguides, photodetectors, modulator, microresonators, …
Material	Silicon	Silicon-based III-V? Other?
Manufacturing technology	CMOS	CMOS *“compatible process”*

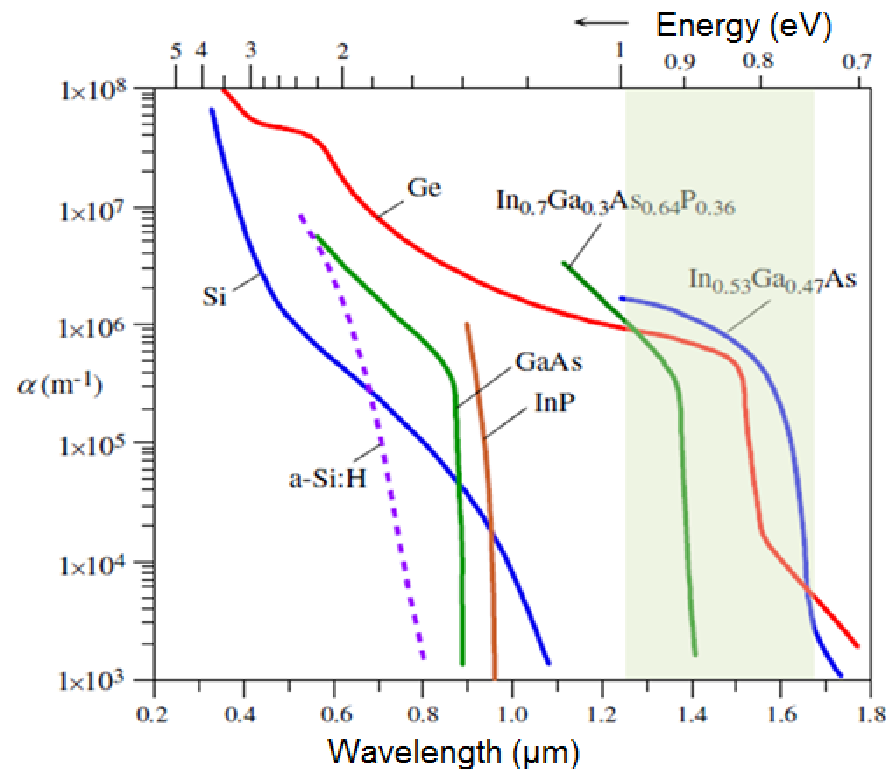
Photonics is much more complex to integrate

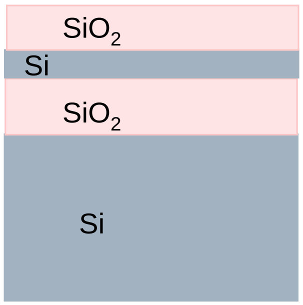
Optical Interconnects

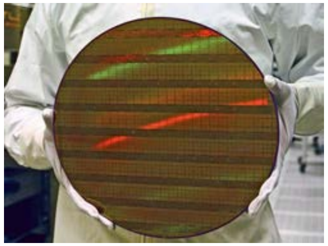


Silicon for optics: Pro's and Cons

- Transparent in 1.3-1.6 µm region
- Take advantage of CMOS platform
  - √ Mature technology
  - √ High production volume
- Low cost
- Silicon On Insulator (SOI) wafer
  - √ Natural optical waveguide
- High-index contrast (n_{Si}=3.5 – n_{SiO2}=1.5)
  - √ Strong light confinement
    - ➢Small footprint (450nm x 220nm)



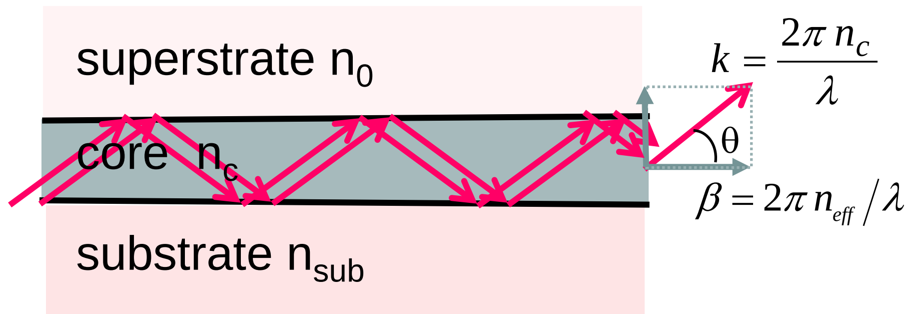




Outline

- Motivation
- Main building blocks in photonics
  - √ Light propagation
    - ➢ Waveguides
    - ➢ Bends, splitters
    - ➢ Fiber coupler
  - √ Optical modulation
  - √ Light detection
  - √ Light emission
- Conclusion

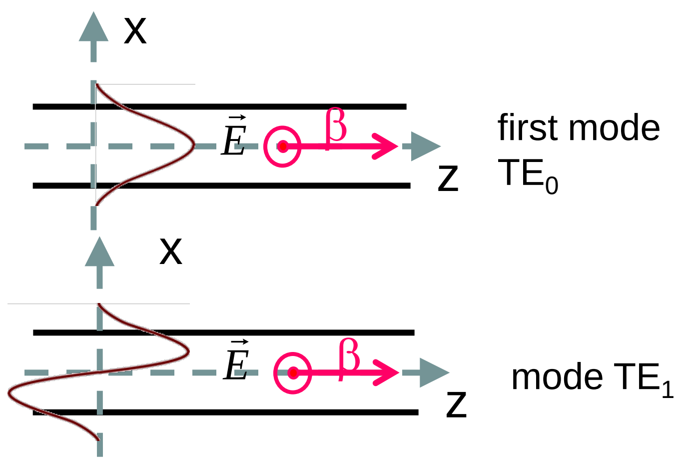
First approach: the simplified picture of ray-optics



$n_c > n_{sub} > n_0 \Rightarrow$ total reflexion

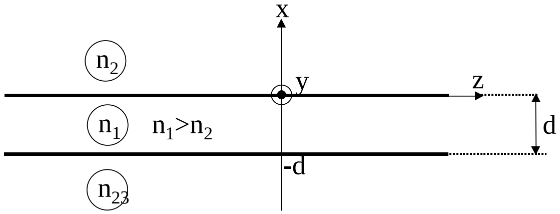
Interferences $\Rightarrow$ a discret set of β is obtained

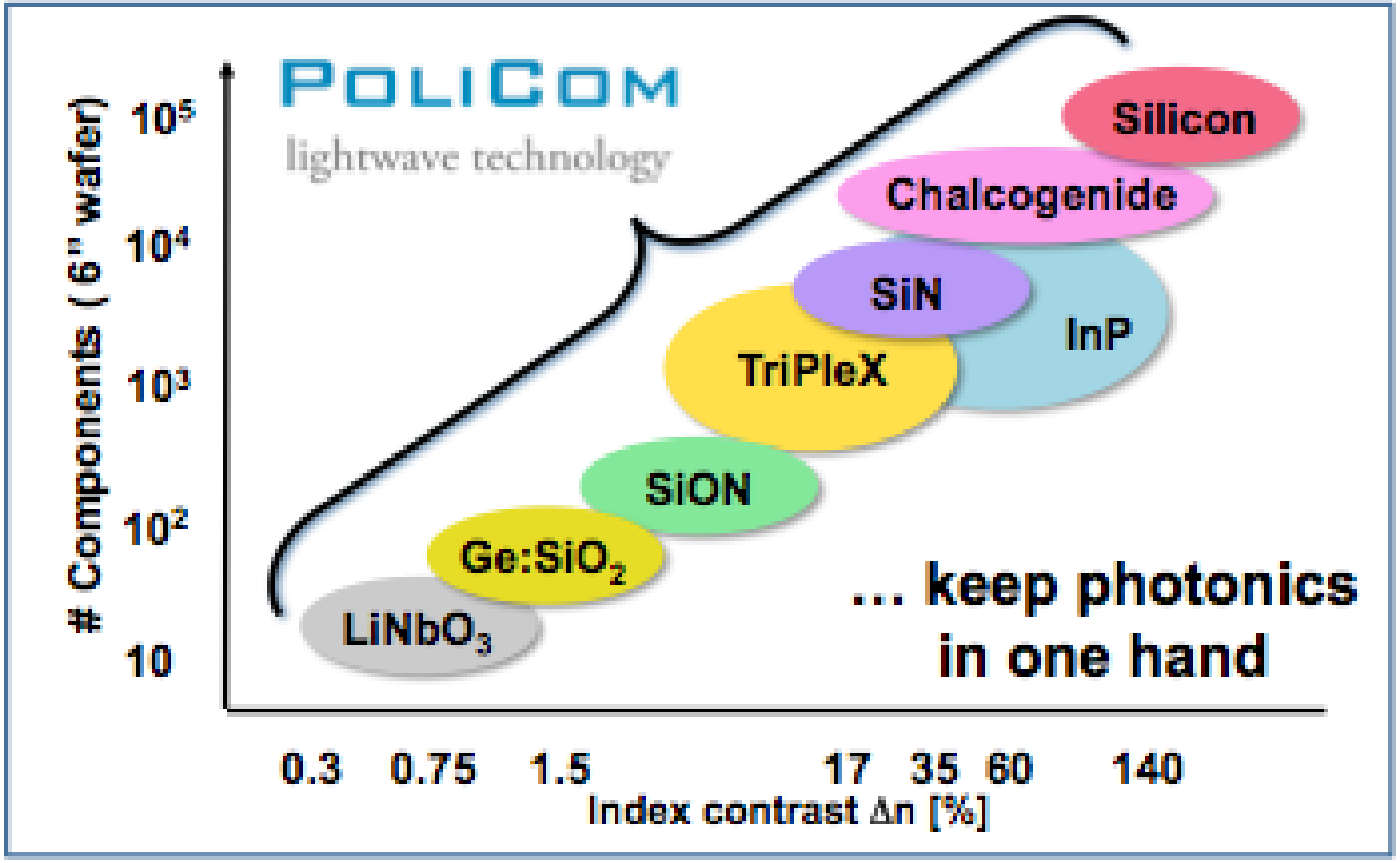
$\Rightarrow$ guided modes (n_{eff})



$$\beta > \max\left(n_{sub}\frac{\omega}{c}, n_0\frac{\omega}{c} \right)$$

Substrates: Refractive index contrast

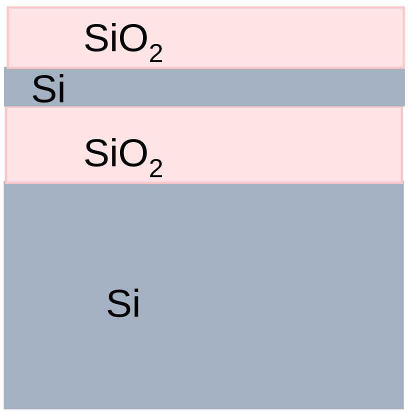


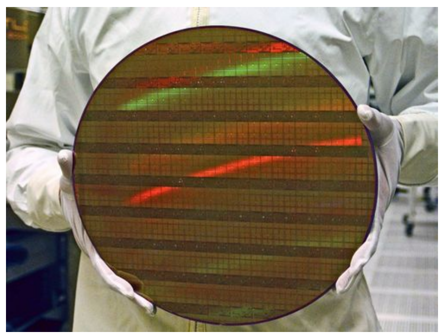


Source: **PoliCom** (**POLI**tecnico **C**omunicazioni **O**ttiche **M**ilano)

Silicon on Insulator substrate (SOI)

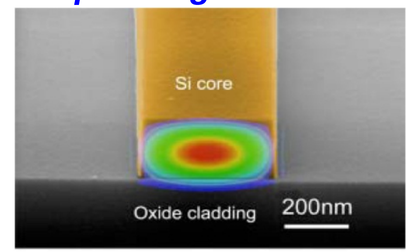
SOI waveguides: the basic device





SOI wafer = Optical planar waveguide

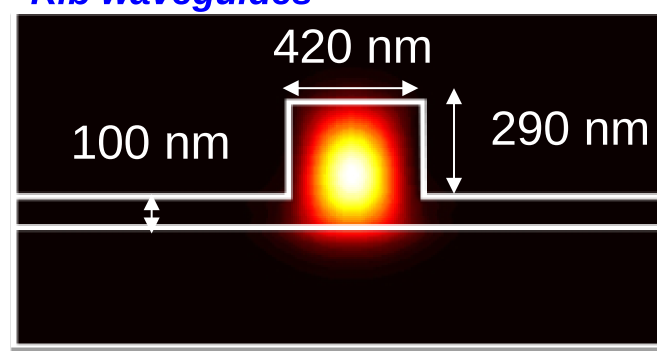
Strip waveguides



Mode size ~ $0.1\mu m^2$

Propagation loss ~ 1dB/cm

Rib waveguides



Mode size ~ $0.2\mu m^2$
Propagation loss ~ 0.5dB/cm

λ=1.55µm

Higher refractive index contrast, smaller cores, tighter bends

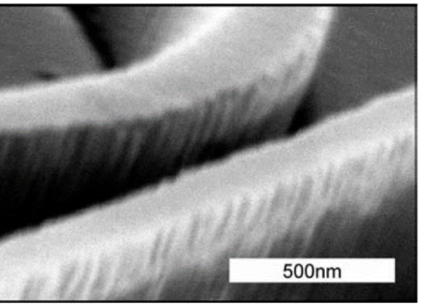
Silica on silicon

Contrast ~ 0.01 – 0.1
Mode diameter ~ 8µm
Bend radius ~ 5mm
Size ~ 10 cm²

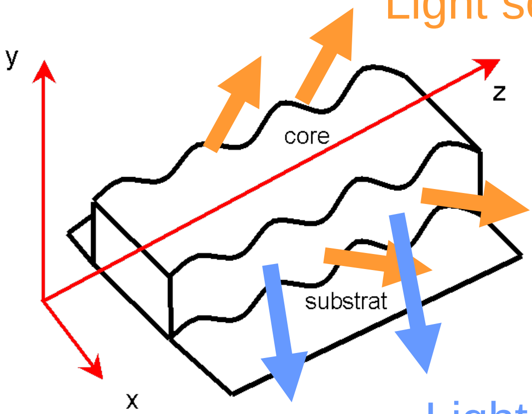
Downscaling of photonics

Source: Slide from Wim Bogaerts – Summer school 2011 St Andrews

Strip waveguides: total loss (leakage and scattering)

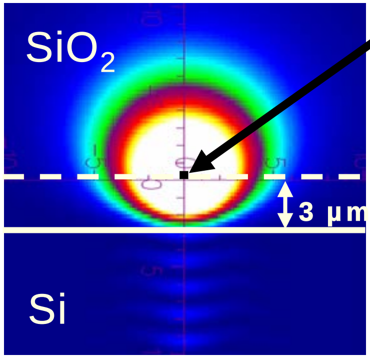


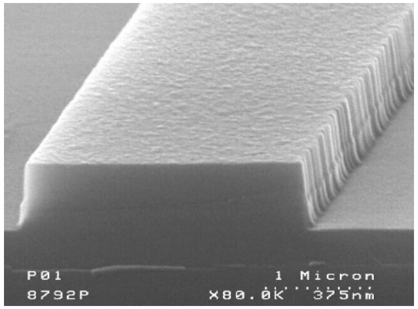
Light scattering



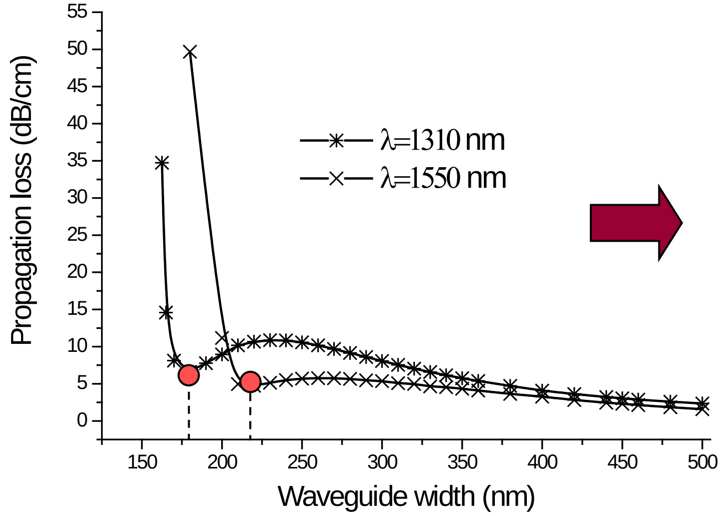
Light leakage

150 nmx150 nm
SOI waveguide



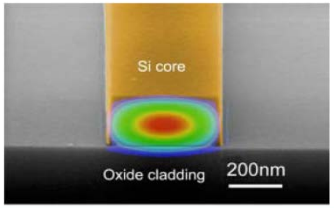


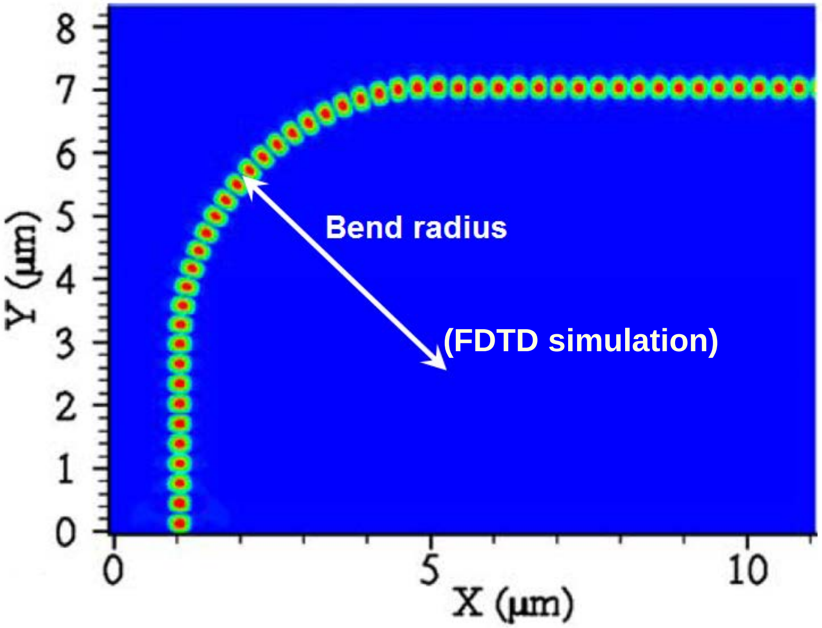
Total losses: $\alpha_{total} = \alpha_{roughness} + \alpha_{leakage}$



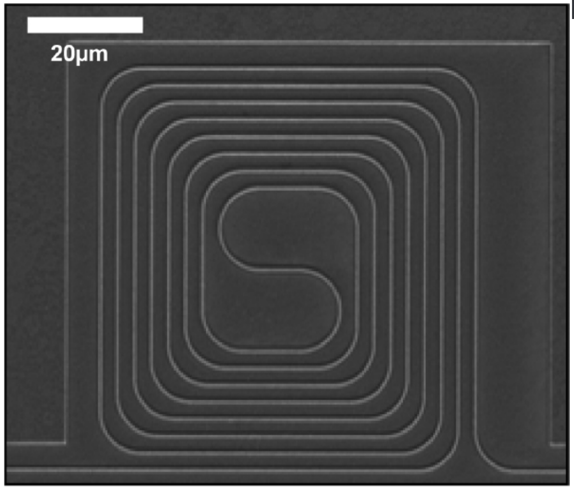
Compromise between scattering and leakage losses

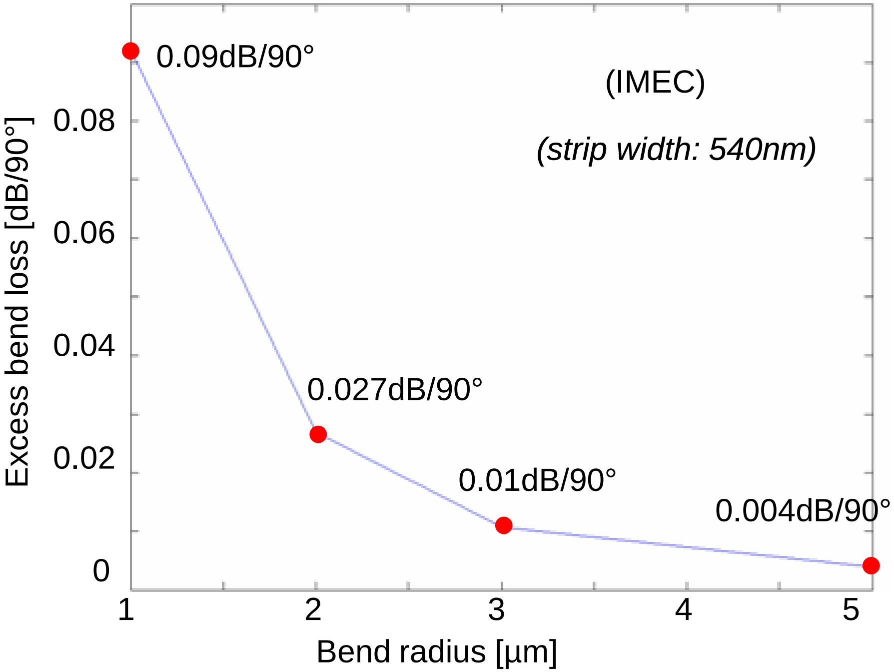
Bends to turn the guided light





Testing device:

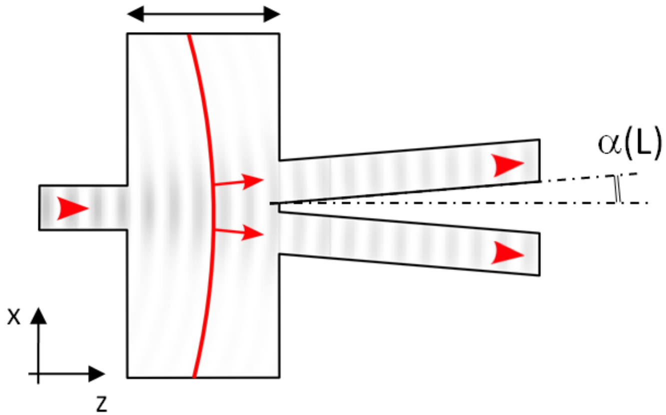




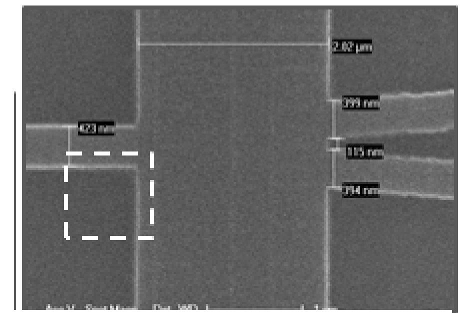
- Increase for narrower waveguides:
  - Weaker confinement: bend radiation
  - More sensitive to roughness
- Increase for smaller bend radii

Beam splitter

- Star splitter

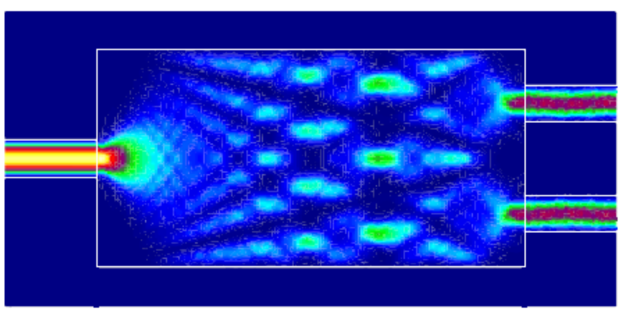


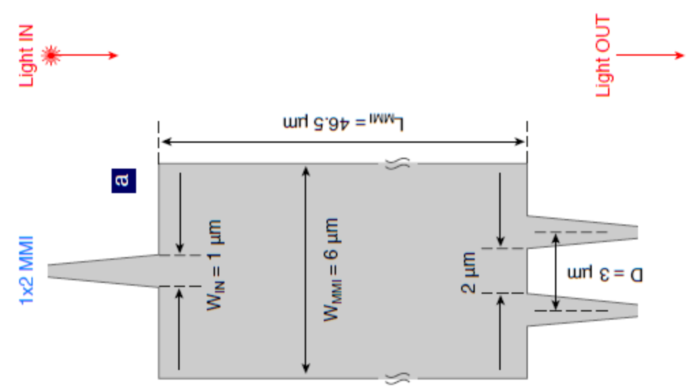
Compact structure (L ~ µm)



Source : G.Rasigade et al, optics letters 2010

- MultiMode interferometer

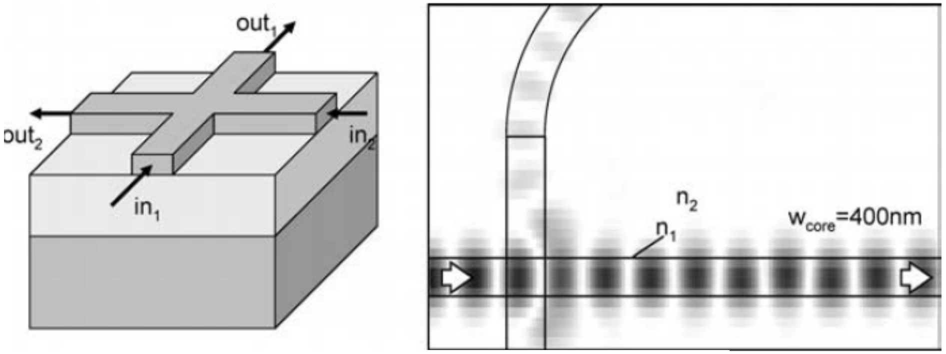




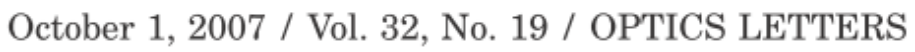
Interference conditions => depend of the optical path => depend of the wavelength
Spectral bandwidth: several tens nm

Waveguide crossings !?

λ= 1,55 µm
T ≈ 93%
crosstalk ≈ 2%



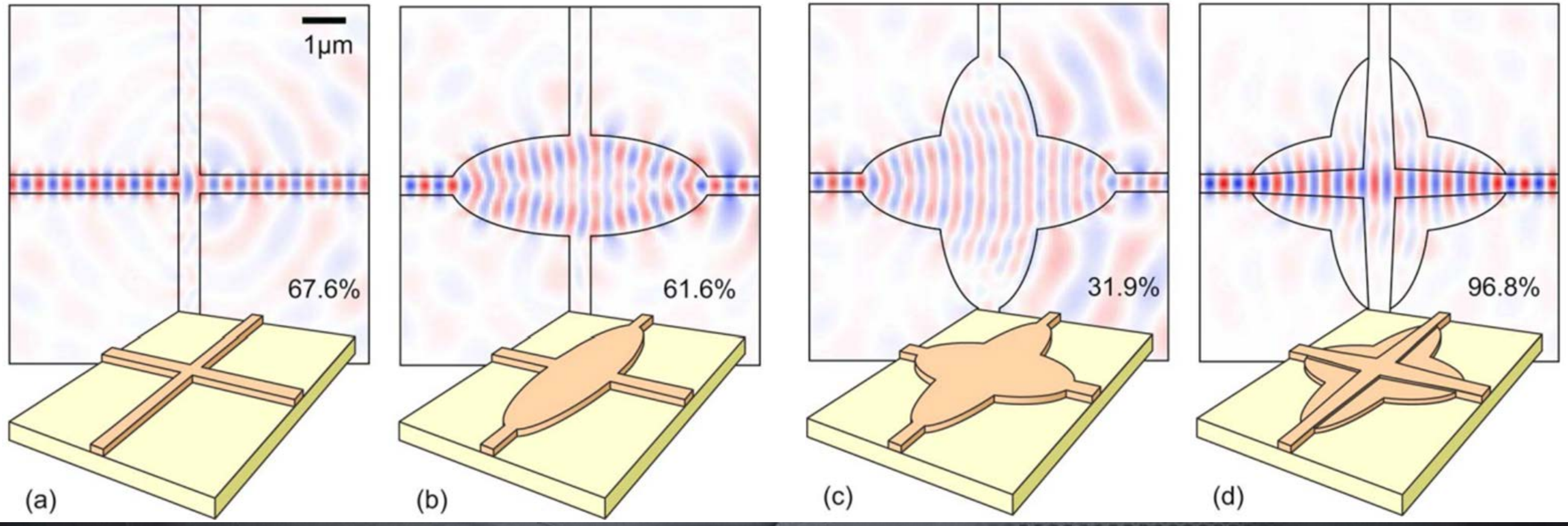
Not so large optical crosstalk but …


October 1, 2007 / Vol. 32, No. 19 / OPTICS LETTERS

Low-loss, low-cross-talk crossings for silicon-on-insulator nanophotonic waveguides

Wim Bogaerts,* Pieter Dumon, Dries Van Thourhout, and Roel Baets

Ghent University - IMEC, Department of Information Technology, Photonics Research Group,

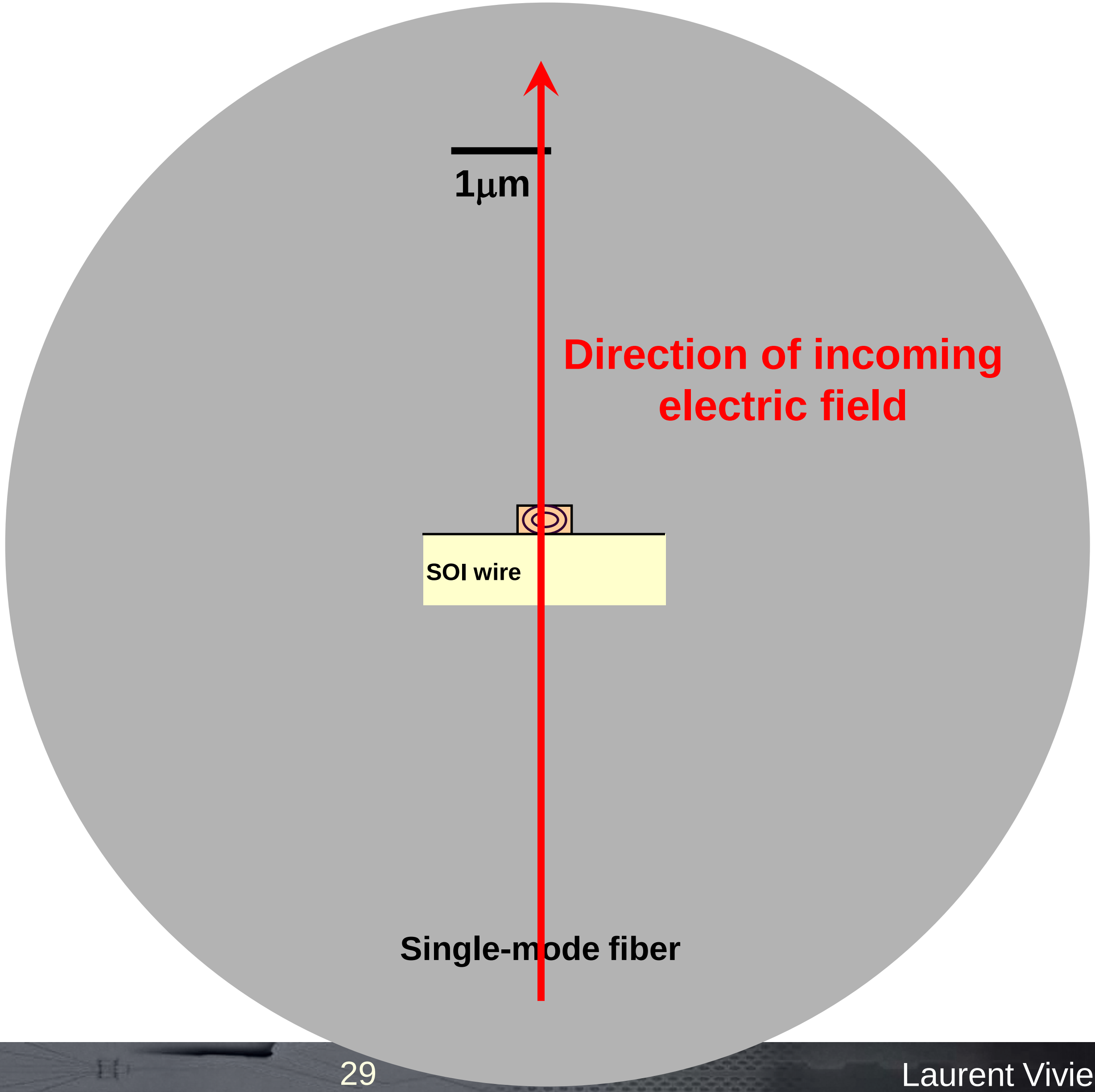


Injection of light in/from an optical fiber: The problem to be solved

The waveguide mode mismatch

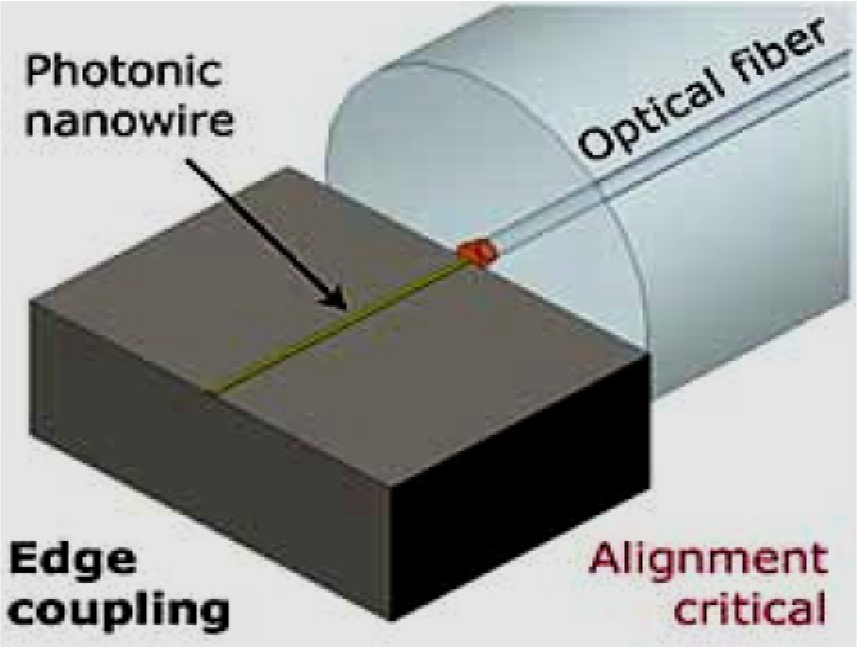
…

… and the light polarization issue.



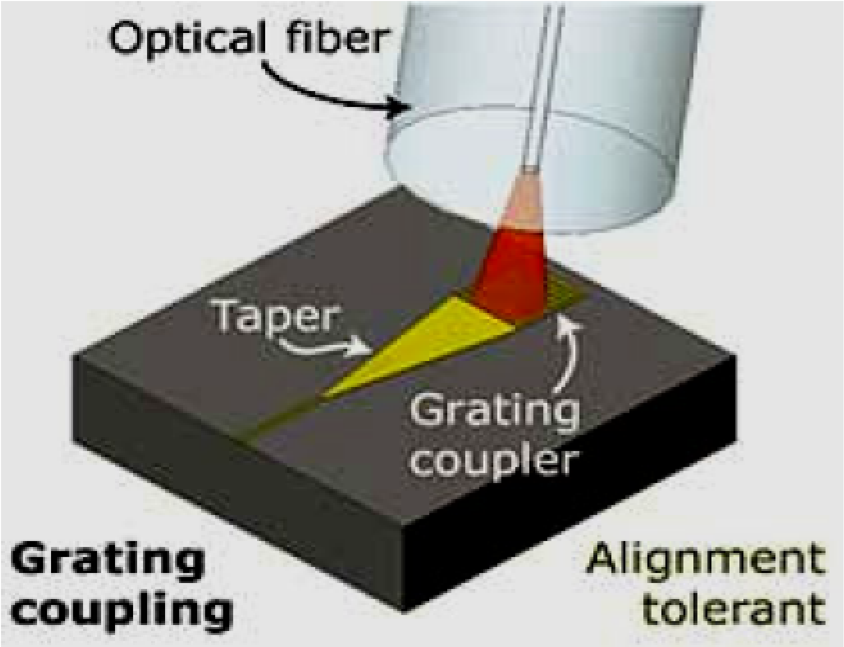
Injection of light in/from an optical fiber: the main approaches

Butt-coupling



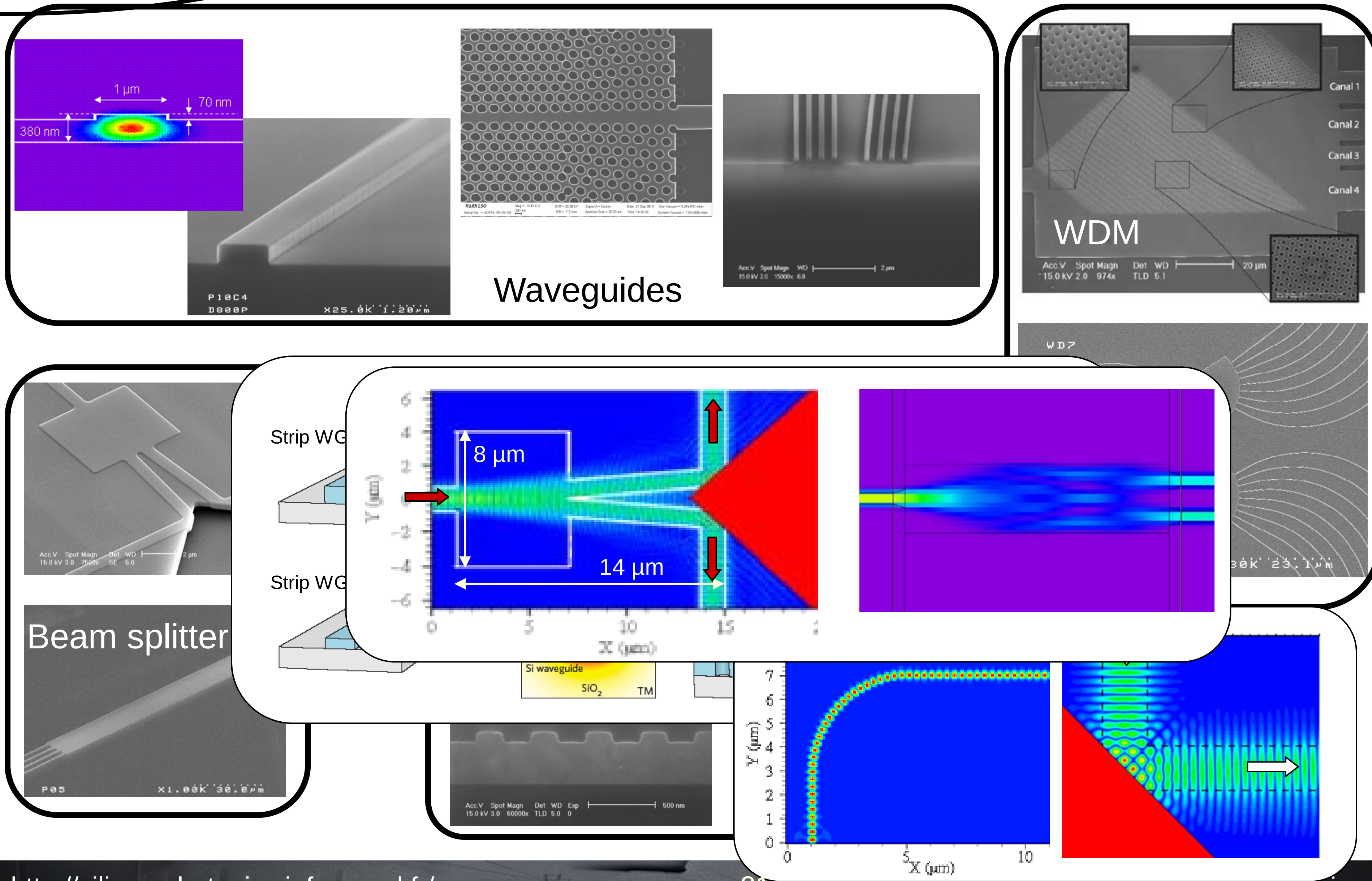
- ☹ Alignment critical;
- ☹ Need facet dicing/polishing;
- ☺ Polarization-insensitive;
- ☺ Large bandwidth;

Vertical-coupling



- ☺ Alignment tolerant;
- ☺ Test in wafer scale (no facet dicing/polishing);
- ☹ Polarization-sensitive;
- ☹ Relatively small bandwidth;

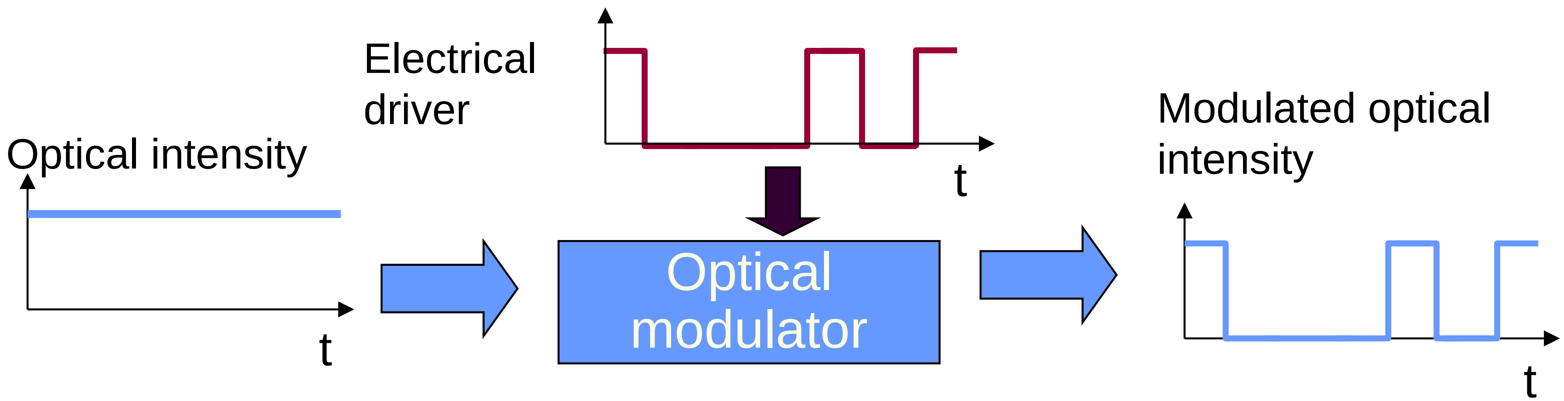
Passive photonic devices

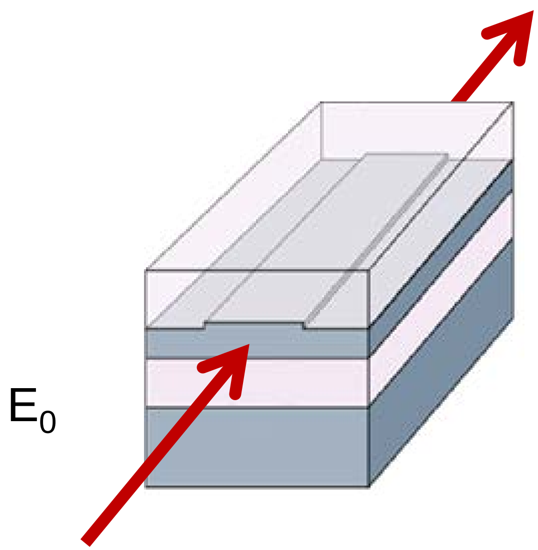


Outline

- Motivation
- Main building blocks in photonics
  - √ Light propagation
  - √ Optical modulation
    - ➢ Principle
    - ➢ Physical effect
    - ➢ Recent advances
  - √ Light detection
  - √ Light emission
- Conclusion

Optical modulation



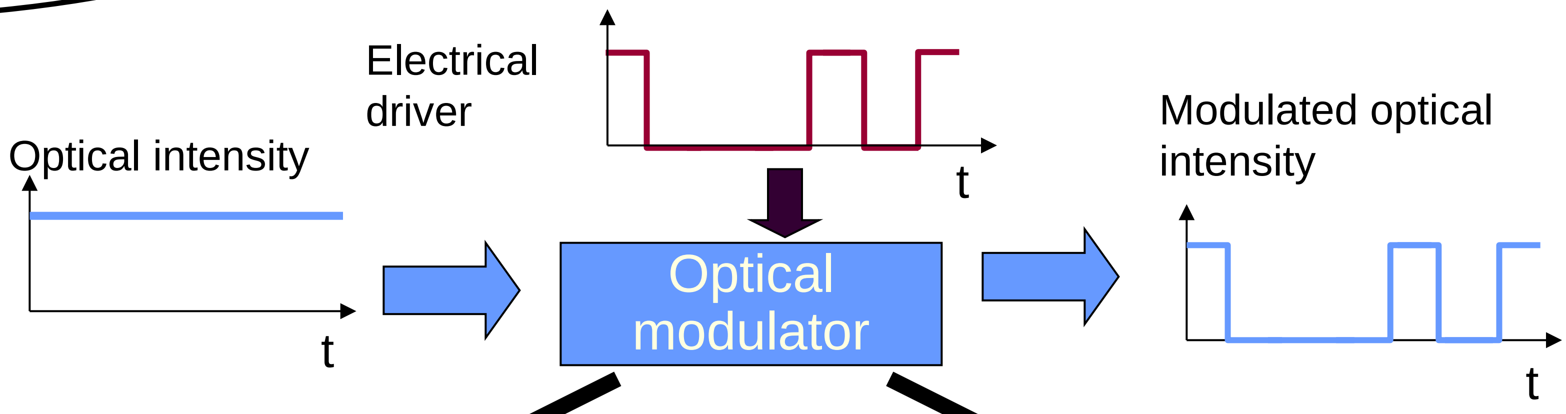


$$E_0\, e^{-\alpha L/2}\, e^{j2\pi n L/\lambda}$$

Electro-absorption

Electro-refraction

Optical modulation



Electroabsorption

Absorption coefficient variation under an electric field

Intensity modulation

Electrorefraction

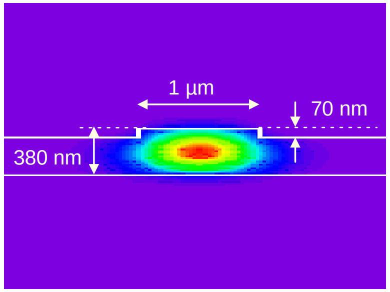
Refractive index variation under an electric field

Phase modulation

interferometer

Intensity modulation

Electro-refraction effect

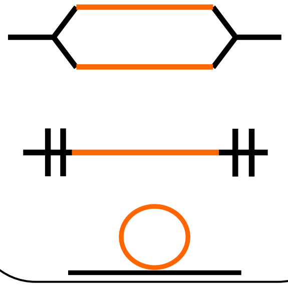


Refractive index variation

Effective index variation of the guided optical mode

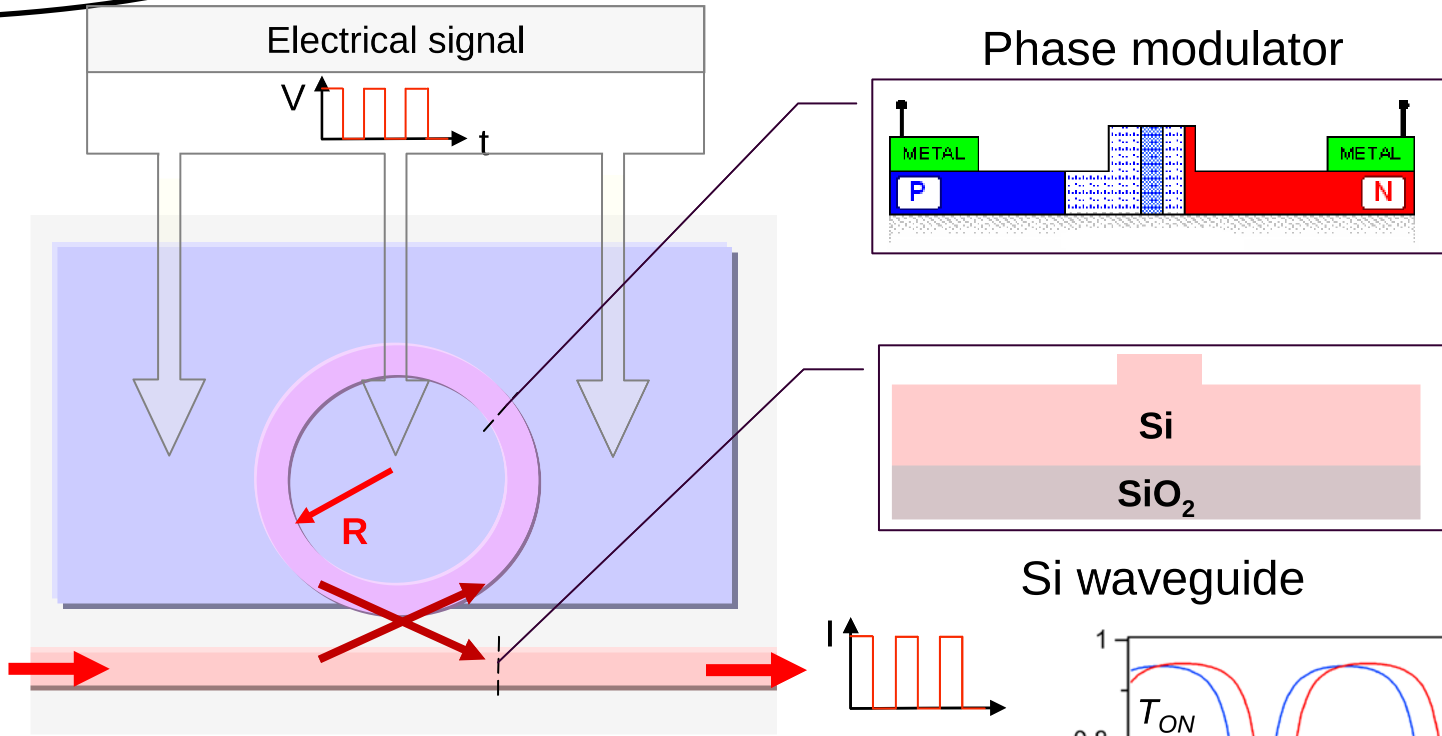
Phase variation

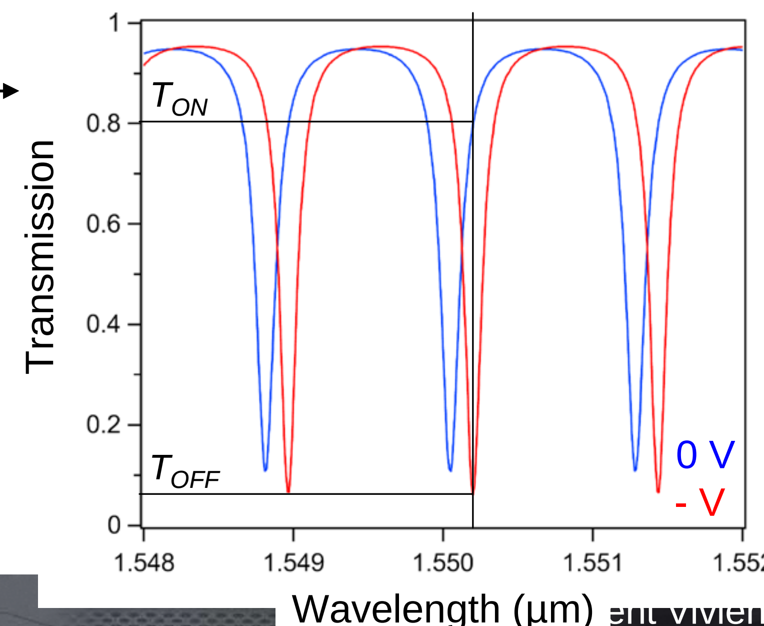
Interferometers



Optical intensity variation

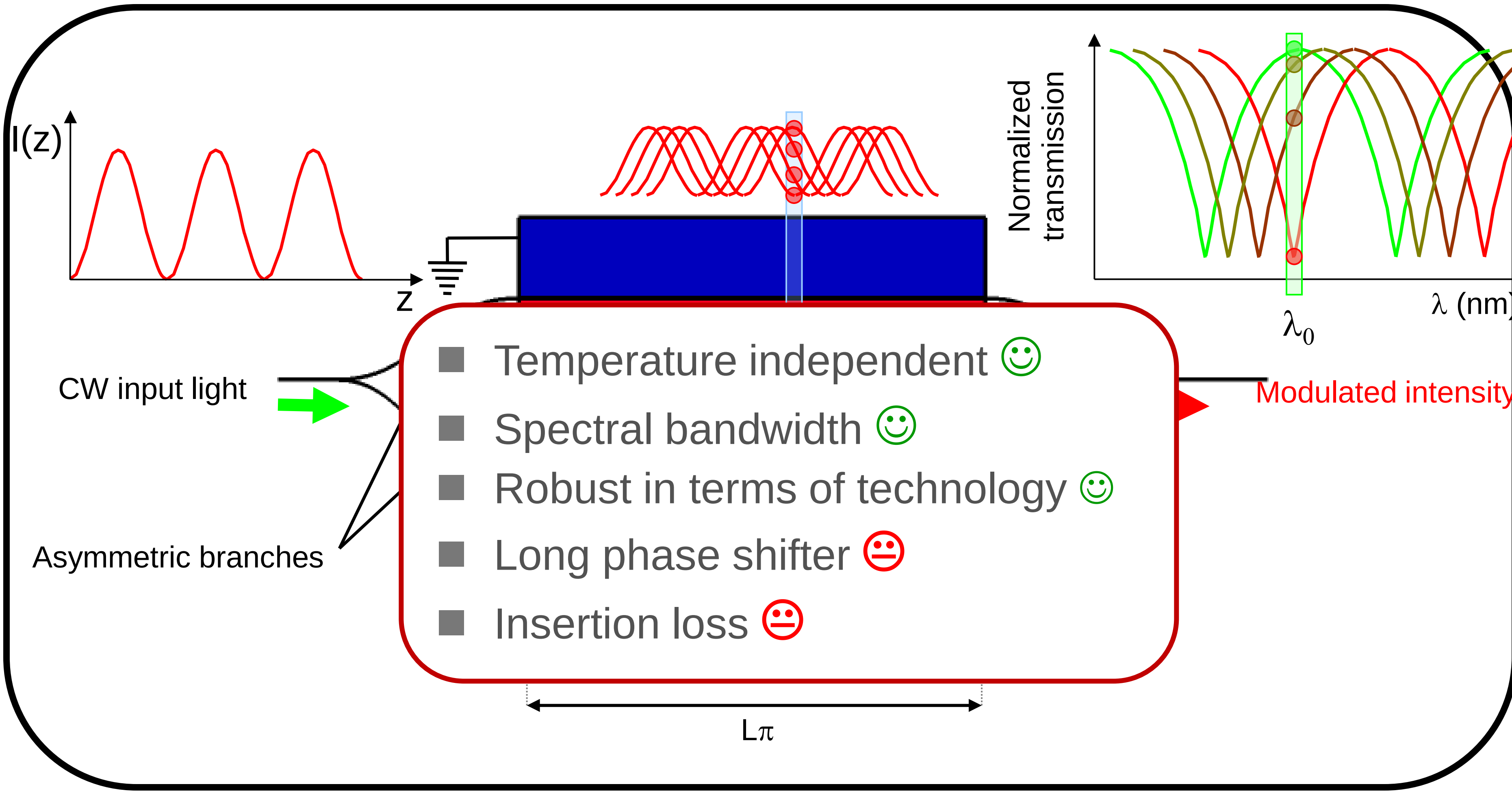
Ring resonators





- Compact ☺
- Low insertion loss ☺
- Low power consumption ☺
- Temperature dependent 😐
- Limited spectral wavelength bandwidth 😐

- Asymmetric MZI



- Temperature independent ☺
- Spectral bandwidth ☺
- Robust in terms of technology ☺
- Long phase shifter 😐
- Insertion loss 😐

What are the EO effects?

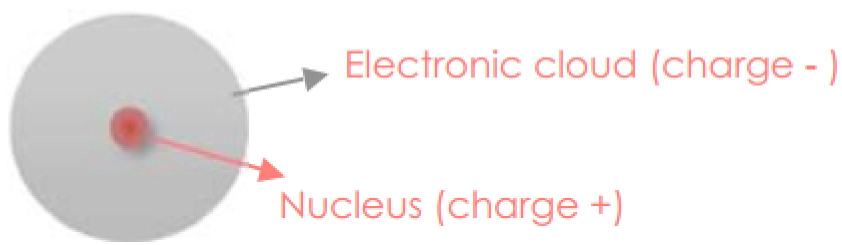
- ✓ Thermal effect — Slow (few 10 kHz)
- ✓ Nonlinear effects:
  - ➢ Pockels effect
  - ➢ Kerr effect
- ✓ Plasma effect

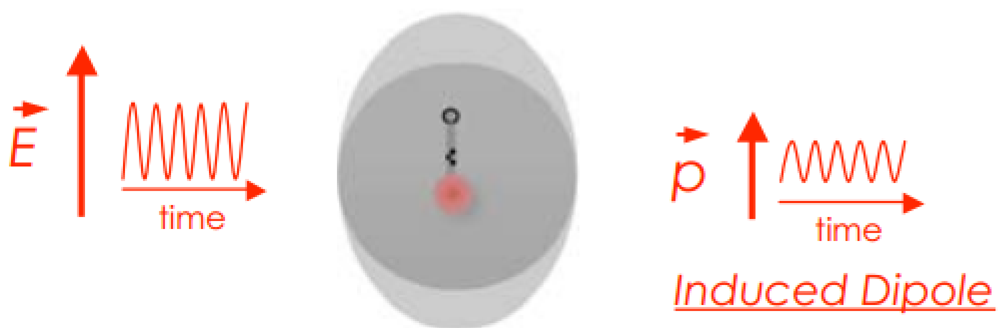
Electro-optic effect

Nonlinear Polarization:

$$\tilde{P}(t) = \chi^{(1)}\tilde{E}(t) + \chi^{(2)}\tilde{E}^2(t) + \chi^{(3)}\tilde{E}^3(t) + \cdots$$

Simplistic model for an atom =





Nonlinear Polarization:

In silicon

$$\tilde{P}(t) = \chi^{(1)}\tilde{E}(t) + \chi^{(2)}\tilde{E}^2(t) + \chi^{(3)}\tilde{E}^3(t) + \cdots$$

√ **Pockels effect**:
- Linear electro-optic effect

√ Wavelength conversion
- Second Harmonic Generation (SHG)

Silicon is a centro-symetric material !

√ **Kerr effect**:
- Nonlinear electro-optic effect

√ Wavelength conversion
- Four wave mixing (FWM)

Weak effect in silicon to be efficient for modulation

$$n = n_0 + I * n_2$$

$$n_2^{Si} \sim 10^{-14}\,\mathrm{cm}^2/\mathrm{W} \quad >> \quad n_2^{glass} \sim 10^{-16}\,\mathrm{cm}^2/\mathrm{W}$$

Nonlinear Polarization:

$$\tilde{P}(t) = \chi^{(1)}\tilde{E}(t) + \chi^{(2)}\tilde{E}^2(t) + \chi^{(3)}\tilde{E}^3(t) + \cdots$$

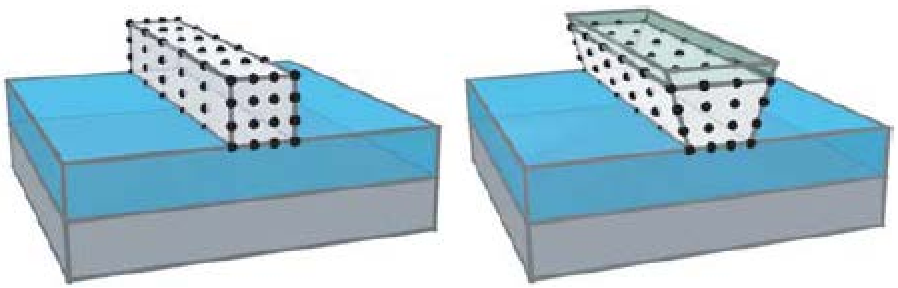
√ **Pockels effect:**

➢ Linear electro- … effect

…ric material !

√ \ …

G)



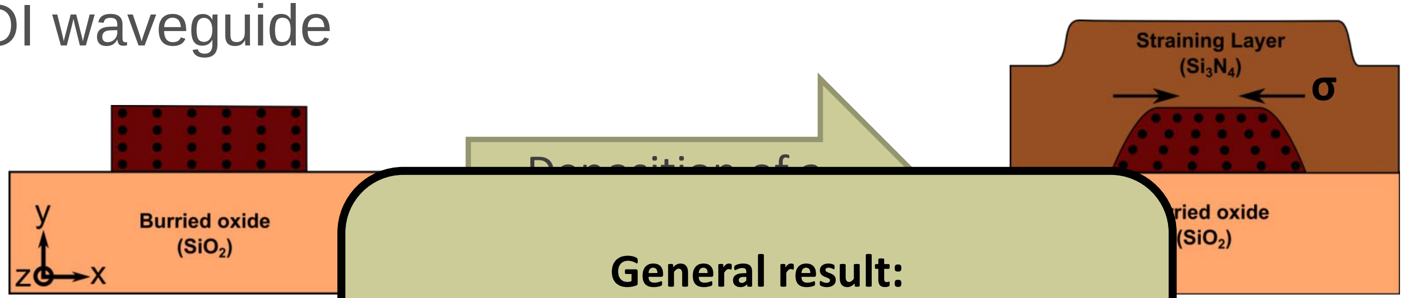
Break the symmetry of silicon crystal

⇩

Strained silicon photonics

How to strain silicon?

- Strain induced by a **straining overlayer**
  - √ SOI waveguide



- Stress dependen

General result:

χ

$\chi^{(2)}$ *is **proportional** to the initial stress **σ** applied to the crystal*

Thermal stress

Intrinsic Stress

conditions

VD etc)

Pockels effect is still weak in silicon. Progress has to be done!

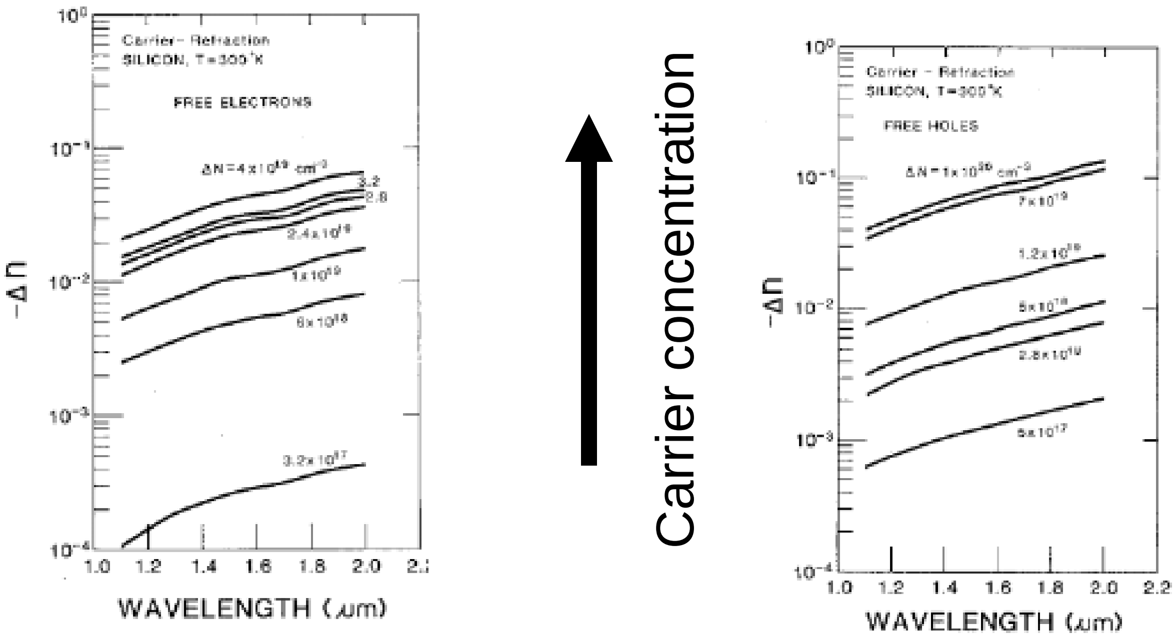
➢ Epitaxial stress

(Usualy) Small Contribution

(Usualy) The main contribution!!!

Free carrier density variation in silicon

- Refractive index are modified by free-carrier concentration variations:
  - Plasma dispersion effect



Free electrons

Free holes

Soref et al IEEE JQE QE-23 (1), (1987).

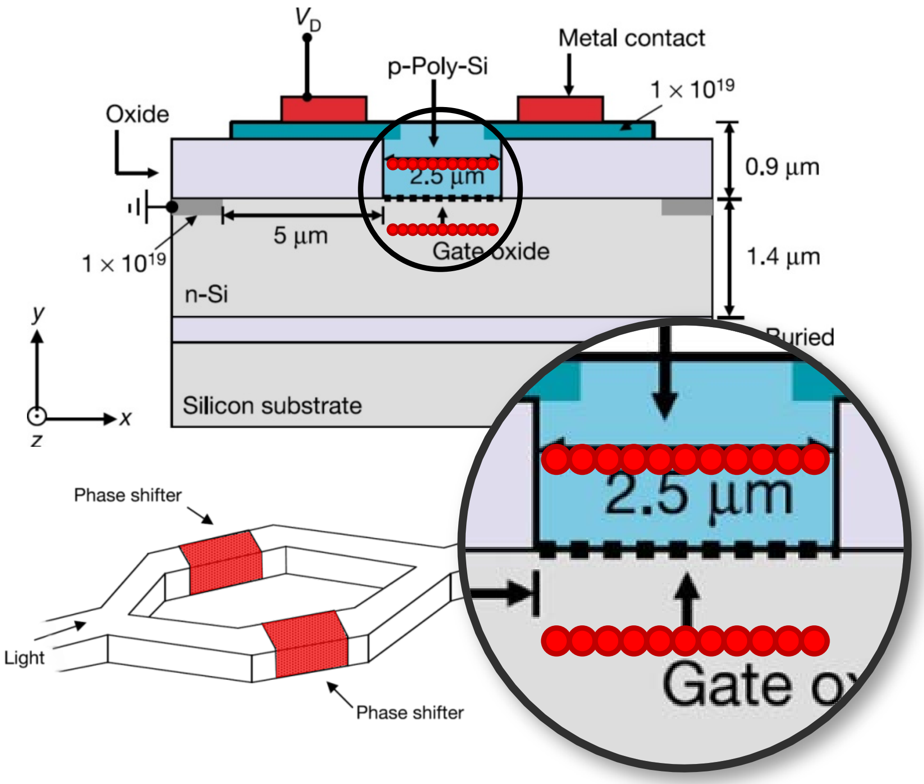
Free carrier variation effect

What are the possibilities to obtain a free carrier concentration variation in silicon-based materials ?

- Carrier injection in pin diode under forward bias voltage
- Carrier accumulation in metal-oxide-semiconductor (MOS) capacitors
- Carrier depletion in a pin diode under reverse bias voltage

Modulator based on carrier accumulation

- Intel (2004) : 1st optical modulator working at 1 GHz.

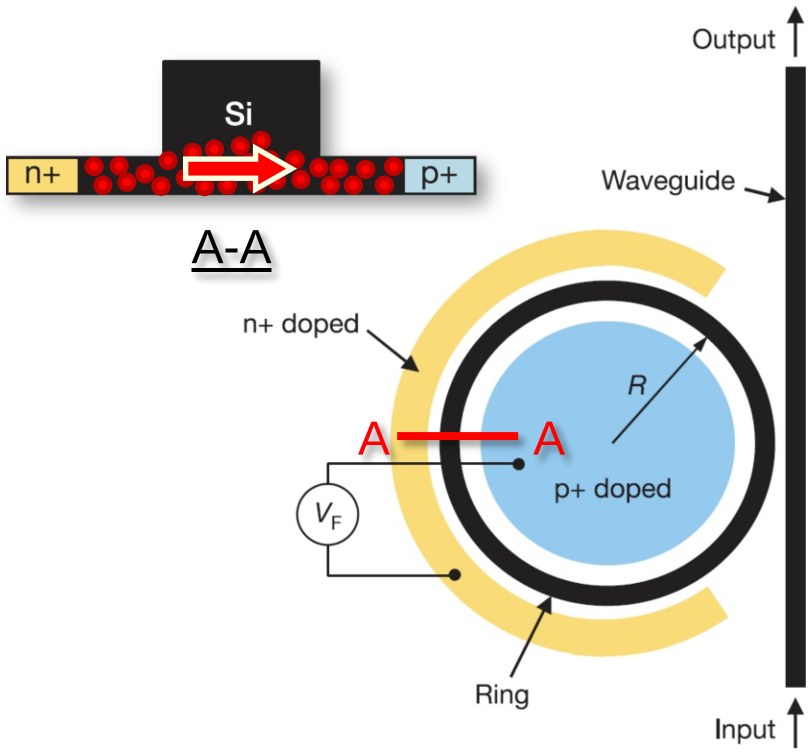


<u>Research lab now involved</u>

- [1] A. Liu et al, « A high-speed silicon optical modulator based on a metal-oxide-semiconductor capacitor », Nature, vol. 427, pp. 615-618 (2004).
- [2] L. Liao et al, « High speed silicon Mach-Zehnder modulator », Optics Express, vol. 13, pp. 3129-3135 (2005).

Modulator based on carrier injection

- Cornell Univ : modulator based on carrier injection in a ring resonator



Research lab now involved :

Cornell University

University of Cambridge

C2N

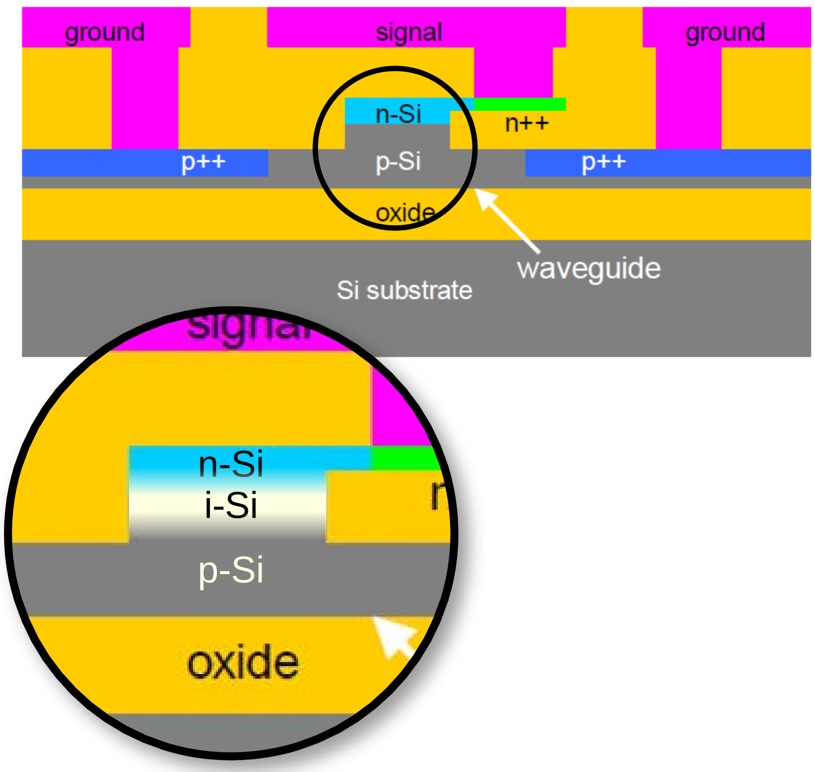
Agency for Science, Technology and Research Singapore

IBM

- [1] Q. Xu et al, « Micrometer-scale silicon electro-optic modulator », Nature, vol. 435, pp-325-327 (2005).
- [2] L. Chen et al, « Integrated GHz silicon photonic interconnect with micrometer-scale modulators and detectors », Optics Express, vol. 17, pp.15248-15256 (2009).

Modulator based on carrier depletion

- Intel : 1st modulator working up to 40 Gbit/s



<u>Research lab now involved :</u>

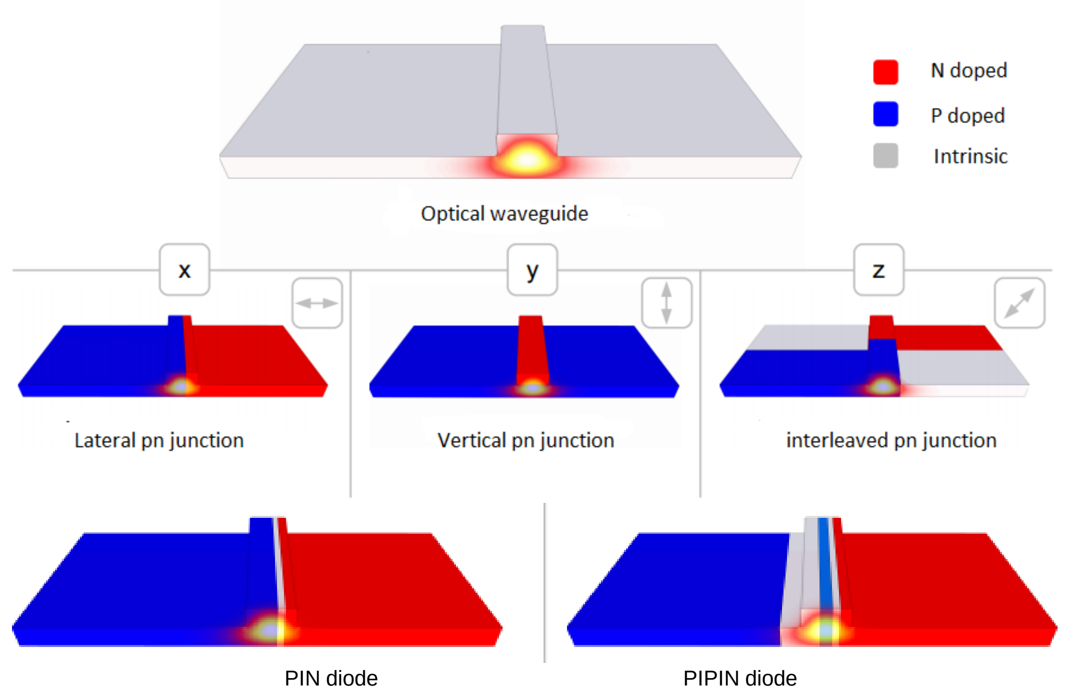
C2N
cnrs
UNIVERSITÉ PARIS SUD
UNIVERSITY OF Southampton
intel
Agency for Science, Technology and Research SINGAPORE
life.augmented
Massachusetts Institute of Technology
cea leti

- [1] A. Liu et al, « High-speed optical modulation based on carrier depletion in a silicon waveguide », Optics Express, vol. 15, pp. 660-668 (2007).

Optical modulators based on carrier depletion

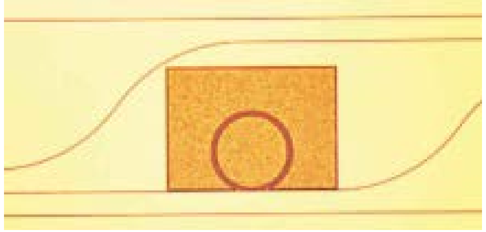
❑ Phase shifters:

- ➢ PN diode
- ➢ Interleaved PN diode
- ➢ PIN diode
- ➢ PIPIN diode



❑ Interferometers

- ➢ Ring resonator
- ➢ Mach-Zehnder
- ➢ Photonic cristals

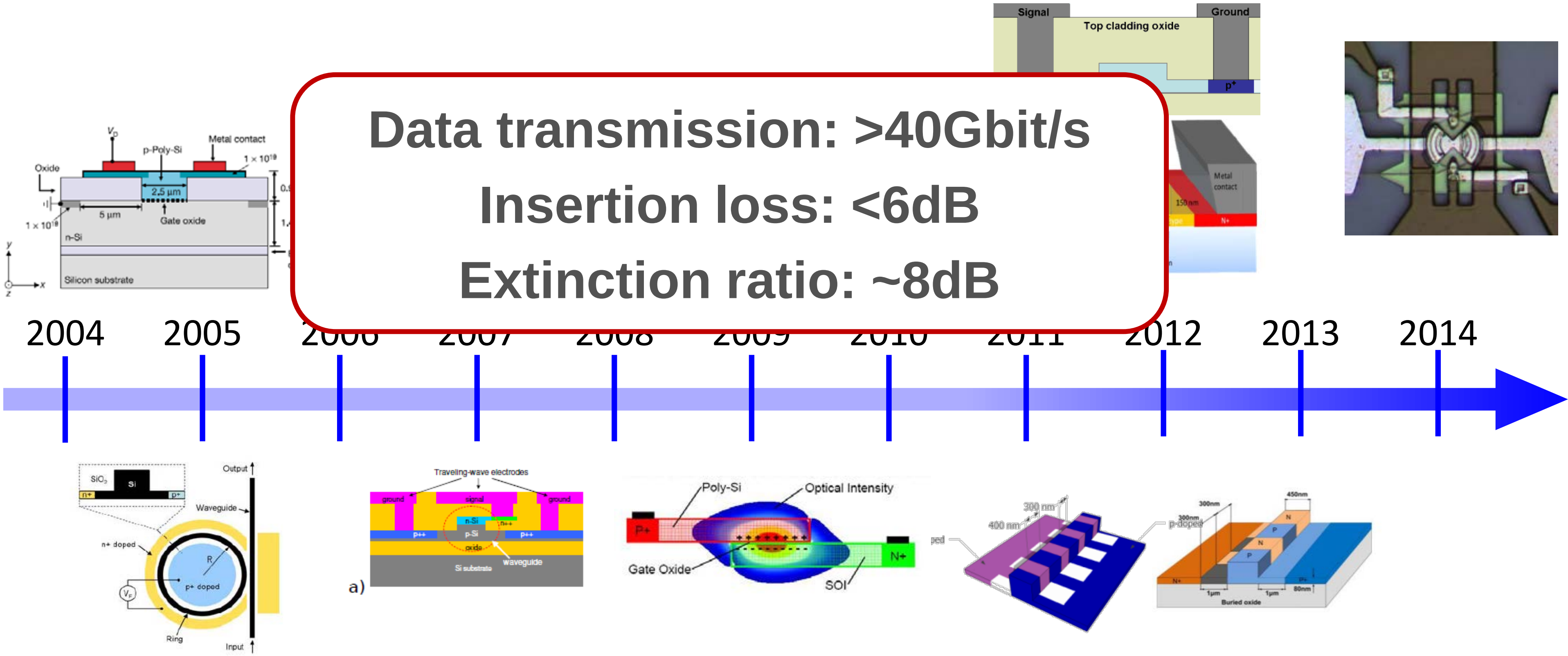


Si optical modulators based on Plasma-dispersion effect

Data transmission: >40Gbit/s

Insertion loss: <6dB

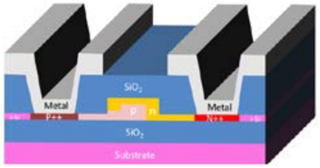
Extinction ratio: ~8dB



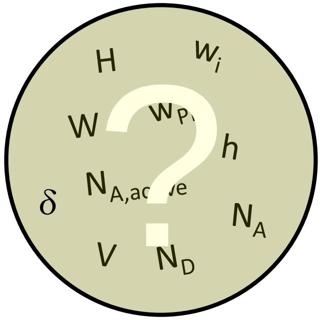
Europe: Univ. Paris Sud, CEA Leti, IMEC/Gent Univ., Univ. of Southampton, UPV, RWTH…

Asia: A*Star, Petra, AIST, Chinese Academy of Sciences, Samsung Electronics, Tokyo Institute of Technology, Pekin Univ. …

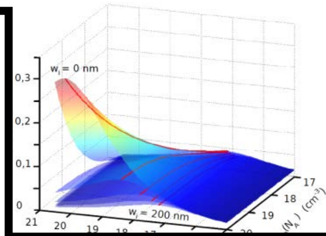
North America: Intel, IBM, Cornell, Luxtera, Ligthwire, Kotura, Oracle, MIT …

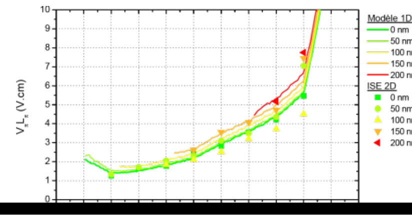


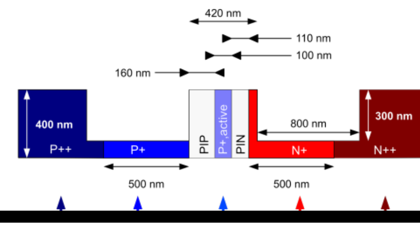
From the idea to the final device

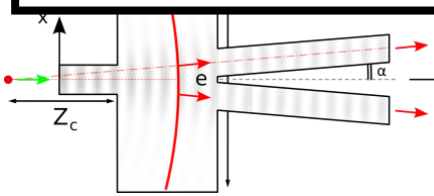


10 parameters need for optimization

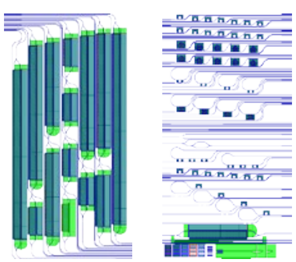




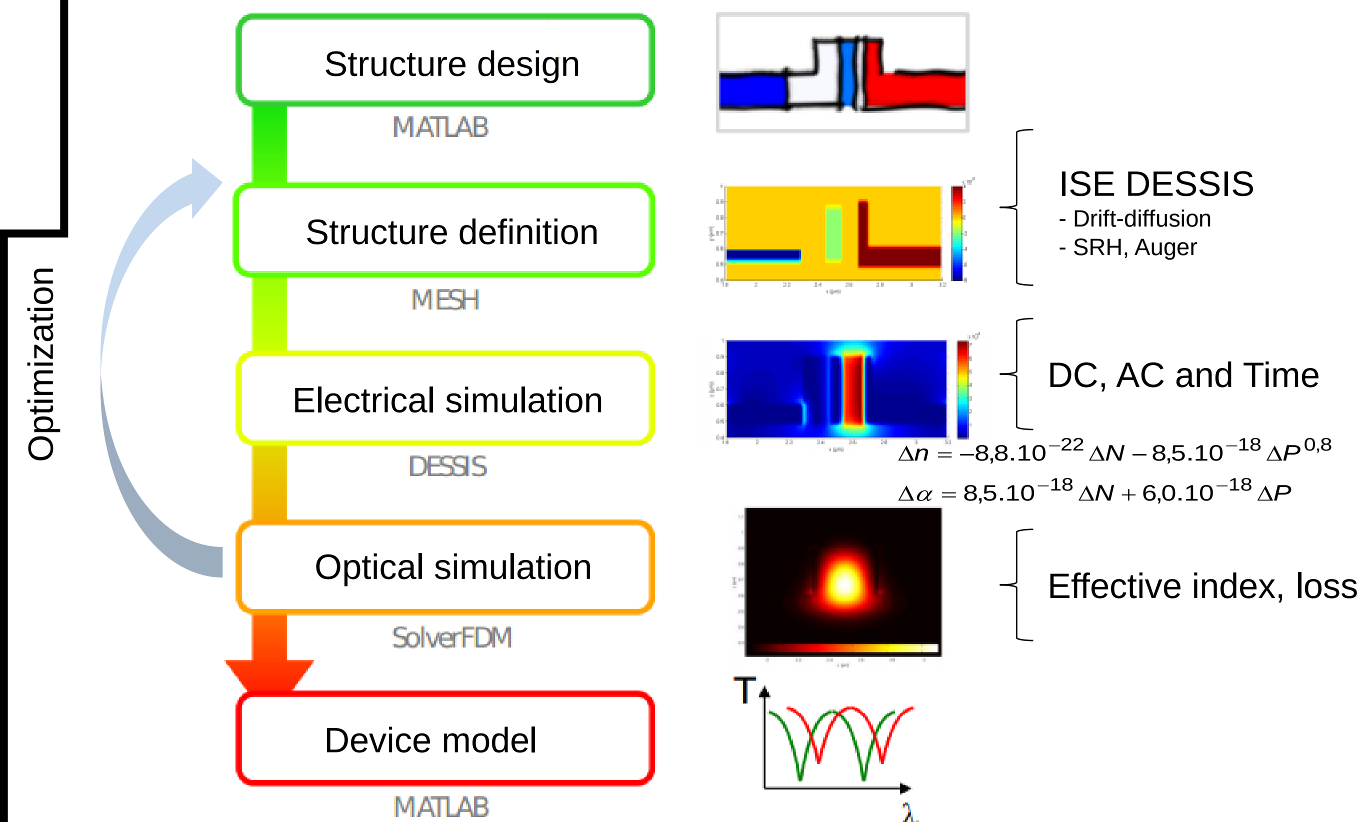




Couplers



Layout



Short distance and high volume applications (electrical bottleneck)

Optical interconnects

Data-center

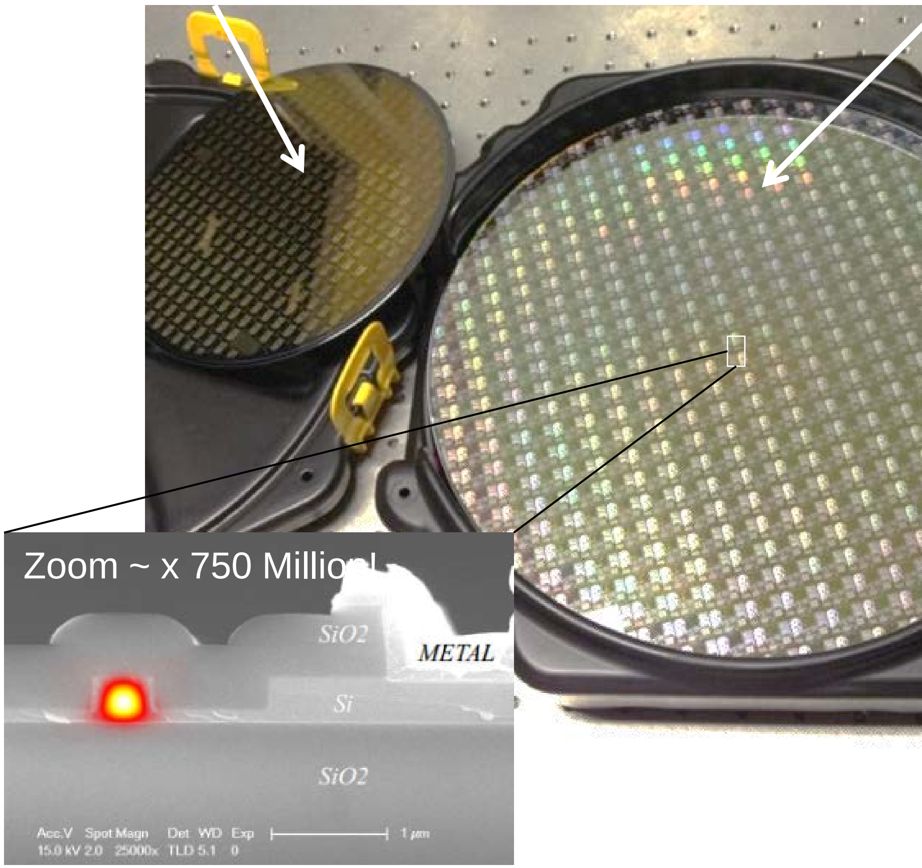
Main challenges:

- ✓ Follow the electronic technology
- ✓ Still reduce cost!

200 mm versus 300 mm

200mm wafer

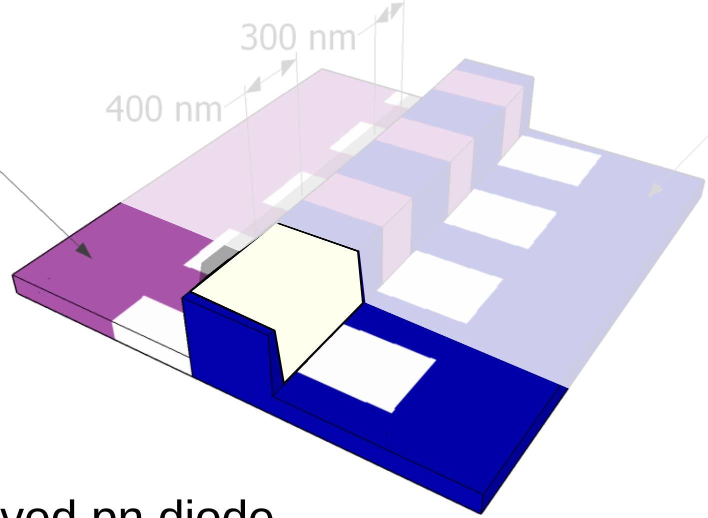
300mm wafer



- ✓ High volume
- ✓ Sub-65nm CMOS node
- ✓ 193nm immersion photolithography
  - ➢ Sub-50nm resolution
- ✓ Wafer thickness uniformity
  - ✓ < ±5nm on 300-mm
  - ✓ ~ ±10nm on 200-mm
- ✓ Yield

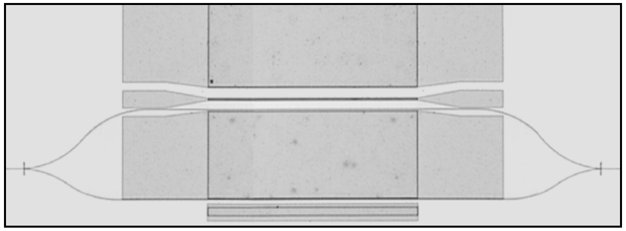
Fabrication – Crolles 2 (Fr)

Optical modulators



Interleaved pn diode

Mach-Zehnder Interferometer



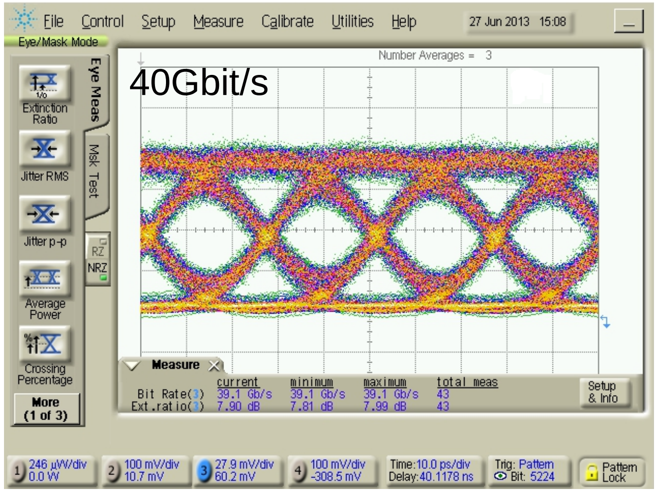
Length = 950 µm

$V_\pi L_\pi$ = 2.4 V.cm

Insertion loss = 4 dB

-3dB cut-off frequency > 20 GHz

ER ~8 dB @ 40 Gbit/s



Short distance and high volume applications (electrical bottleneck)

Optical interconnects

Data-center

Main challenges:

- ✓ Follow the electronic technology
- ✓ Still reduce of cost!
- ✓ Driving voltage of modulator
- ✓ Power consumption

ITRS Roadmap: Optical interconnect

- (…) A large variety of CMOS compatible modulators have been proposed in the literature (…)
- "The primary challenges for optical interconnects at the present time are producing <u>cost effective, low power components.</u>"

Power consumption

Energy to charge the device

$$\textbf{Energy/bit} = 1/4\,(CV_{pp})^2$$

Energy dissipation of photocurrent

$$\textbf{Energy/bit} = 1/B\,(I_{ph}V_{bias})$$

- Drive the modulator in push-pull configuration

How do we reduce the power consumption ?

  - √ Slow-wave device for reducing the length
  - √ Ring Modulators

Targets : **~100 fJ/bit** for longer off-chip distances, **10's of fJ/bit** for dense off-chip connections and **a few fJ/bit** for global on-chip connections.

D. A. B. Miller, Proc. IEEE ***97****(7), 1166–1185 (2009).*

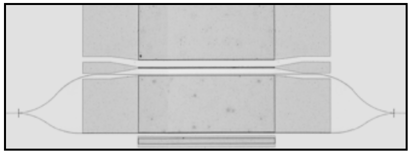
Power consumption

For emitters and short optical links:

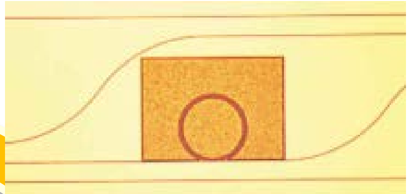
~100 fJ/bit down to fJ/bit

(D.A.B. Miller, Opt Exp. , 2012)

Mach Zehnder modulators
~ 3 pJ/bit



Ring resonator modulators
~ 0.5 pJ/bit



Power consumption

Energy to charge the device

$$\textbf{Energy/bit} = 1/4\,(CV_{pp})^2$$

Energy dissipation of photocurrent

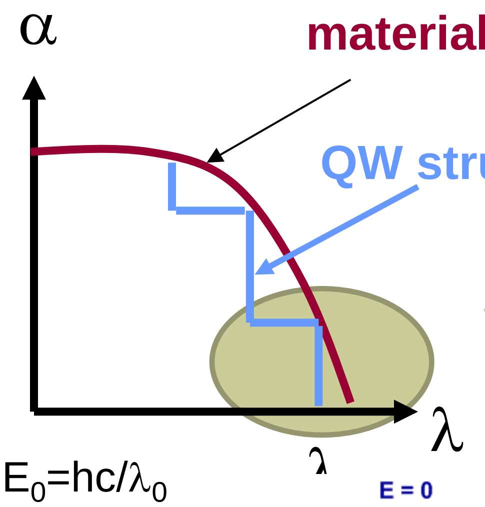
$$\textbf{Energy/bit} = 1/B\,(I_{ph}V_{bias})$$

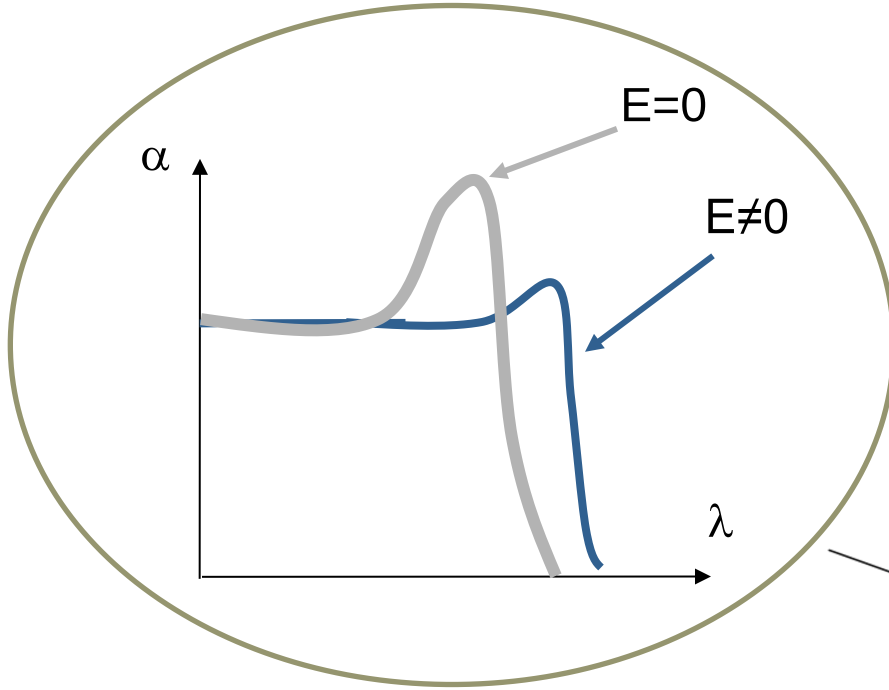
- Drive the modulator in push-pull mode
- Reduction of capacitance of depletion device
  - √ Slow-wave device for reducing the length
  - √ Ring Modulators
- Modulation efficiency (compactness)
  - √ Improve efficiency of Si modulator
  - √ MZM or EAM Hybrid modulator
  - √ Ge EAM modulators (QCSE or FK)

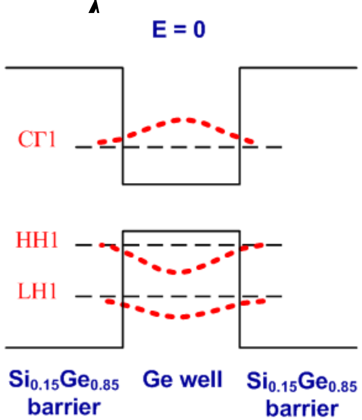
Targets : **~100 fJ/bit** for longer off-chip distances, **10's of fJ/bit** for dense off-chip connections and **a few fJ/bit** for global on-chip connections.

*D. A. B. Miller, Proc. IEEE **97**(7), 1166–1185 (2009).*

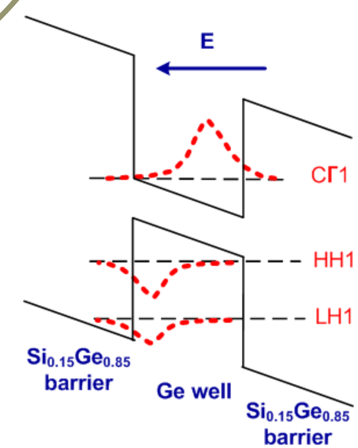
Electro-absorption modulator







Ge/SiGe quantum well structures

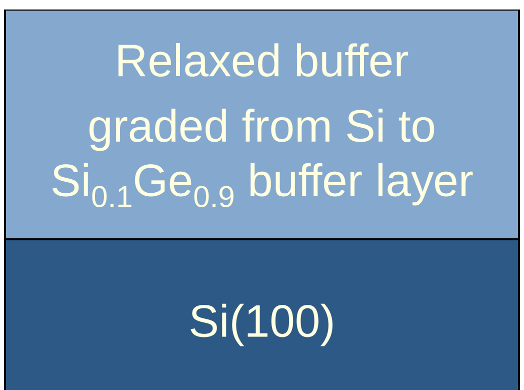


- ❑ Absorption edge in QW structures is more abrupt than in bulk material
- ❑ E_0 depends on the quantum well thickness
  - ➢ Adjustment of the wavelength is possible

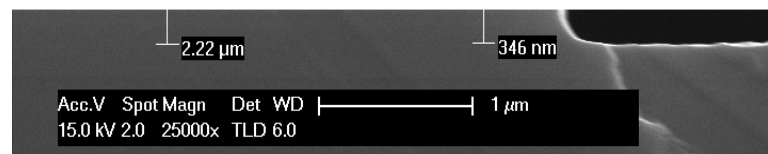
Epitaxial growth by LEPECVD

✓ Growth of Ge/SiGe multiple quantum wells

LEPECVD
Low energy plasma enhanced chemical vapor deposition



Low dislocation density - Best possible device performance

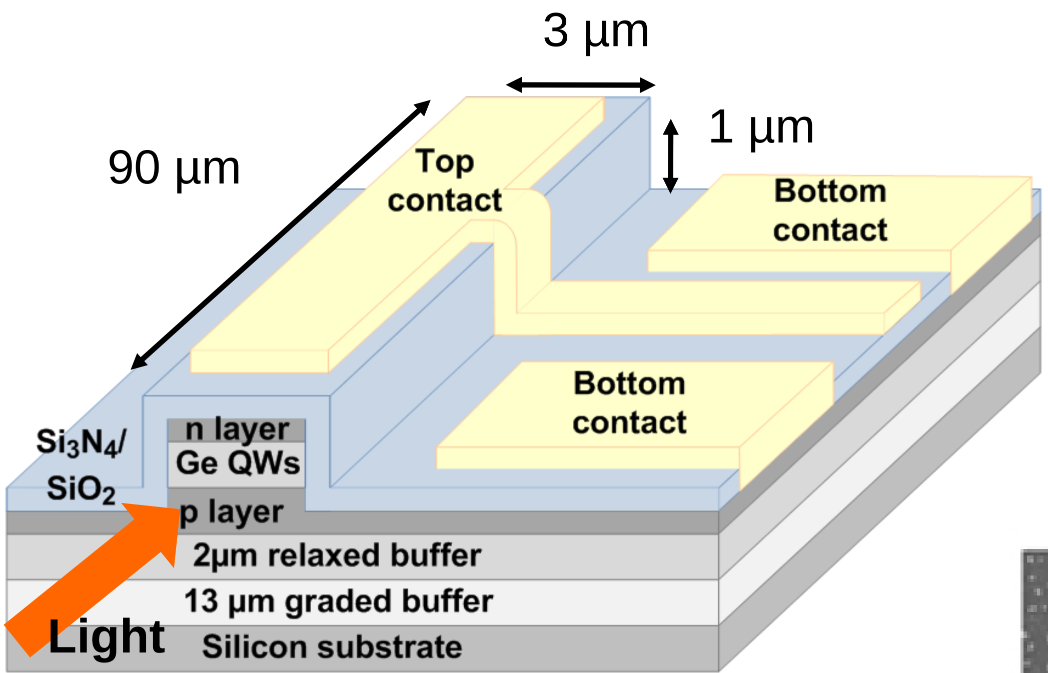


maximum efficiency

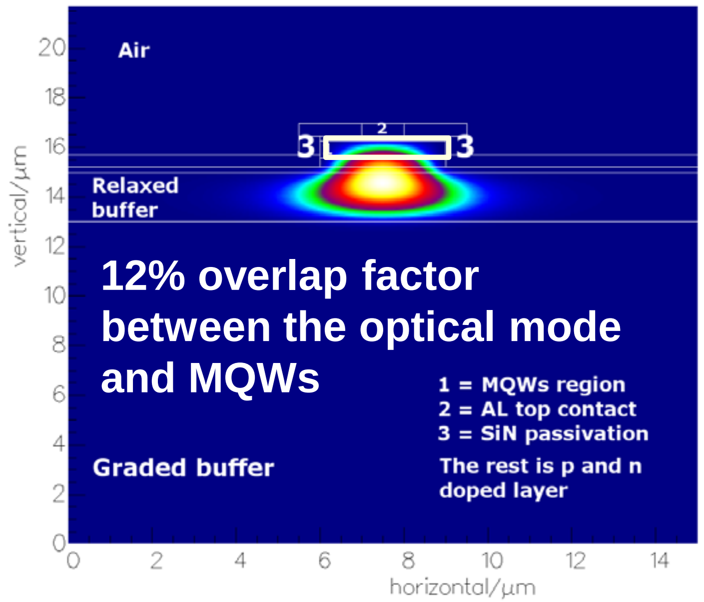
✓ Temperatures down to 400°C

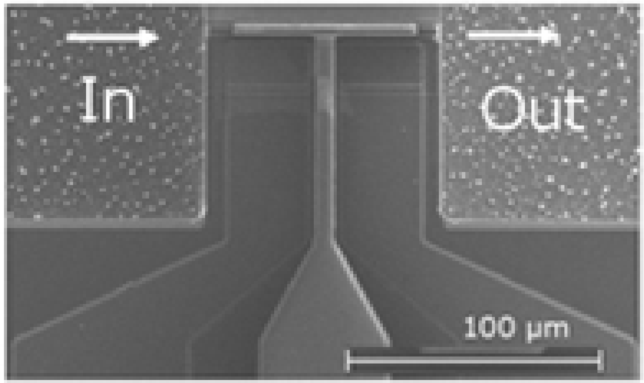
L-NESS
Como, Italy

Electroabsorption modulator



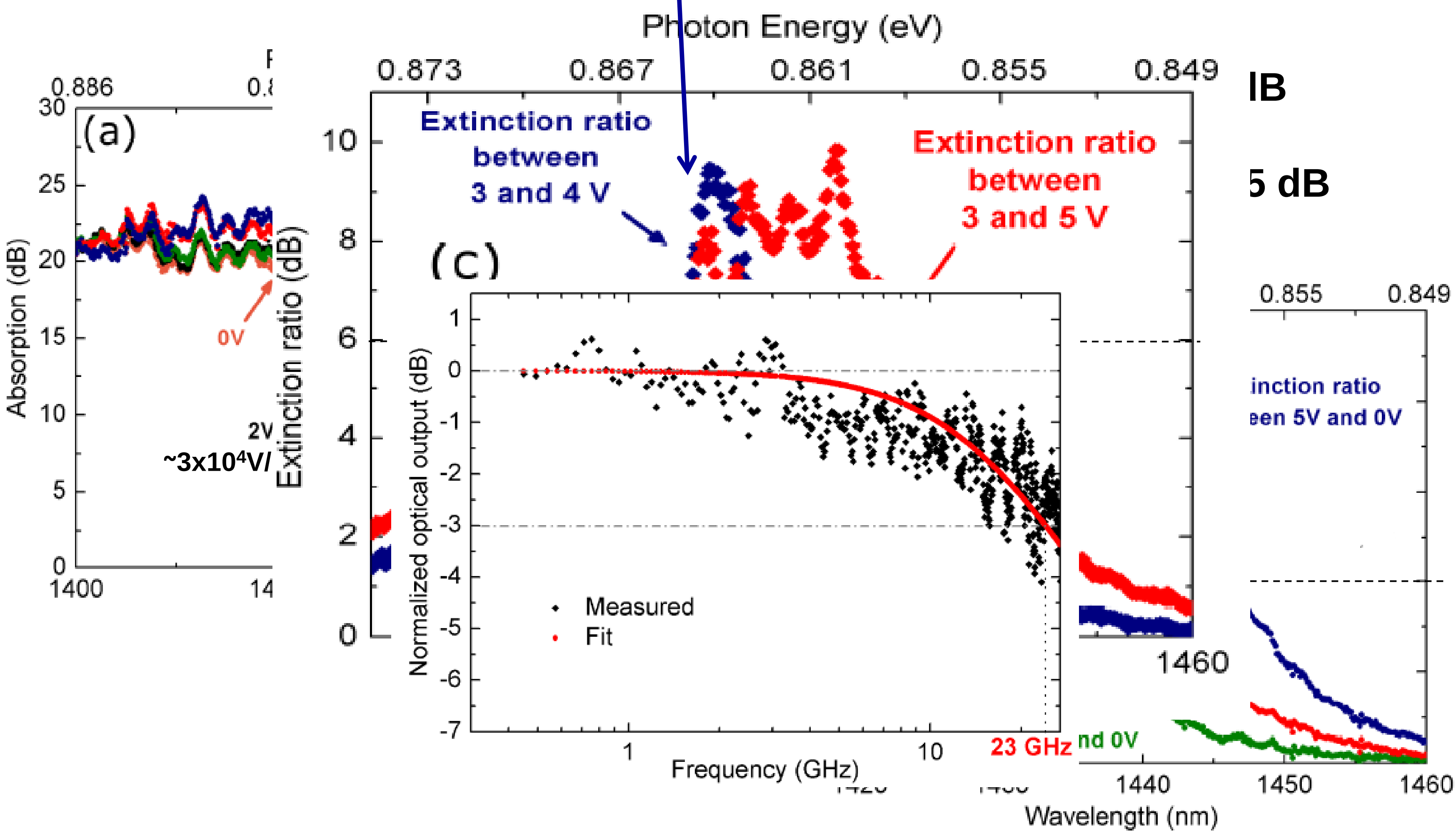
20 Ge/SiGe QW





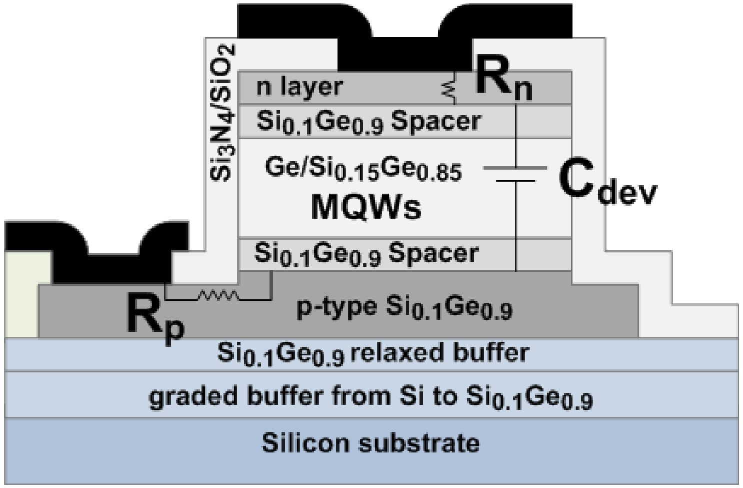
P. Chaisakul et al., Optics Express (2012).

1V swing **2V swing**



Energy consumption

$R_s = R_n + R_p$



Energy to charge the device

Energy/bit = 1/4 $(CV_{pp})^2$

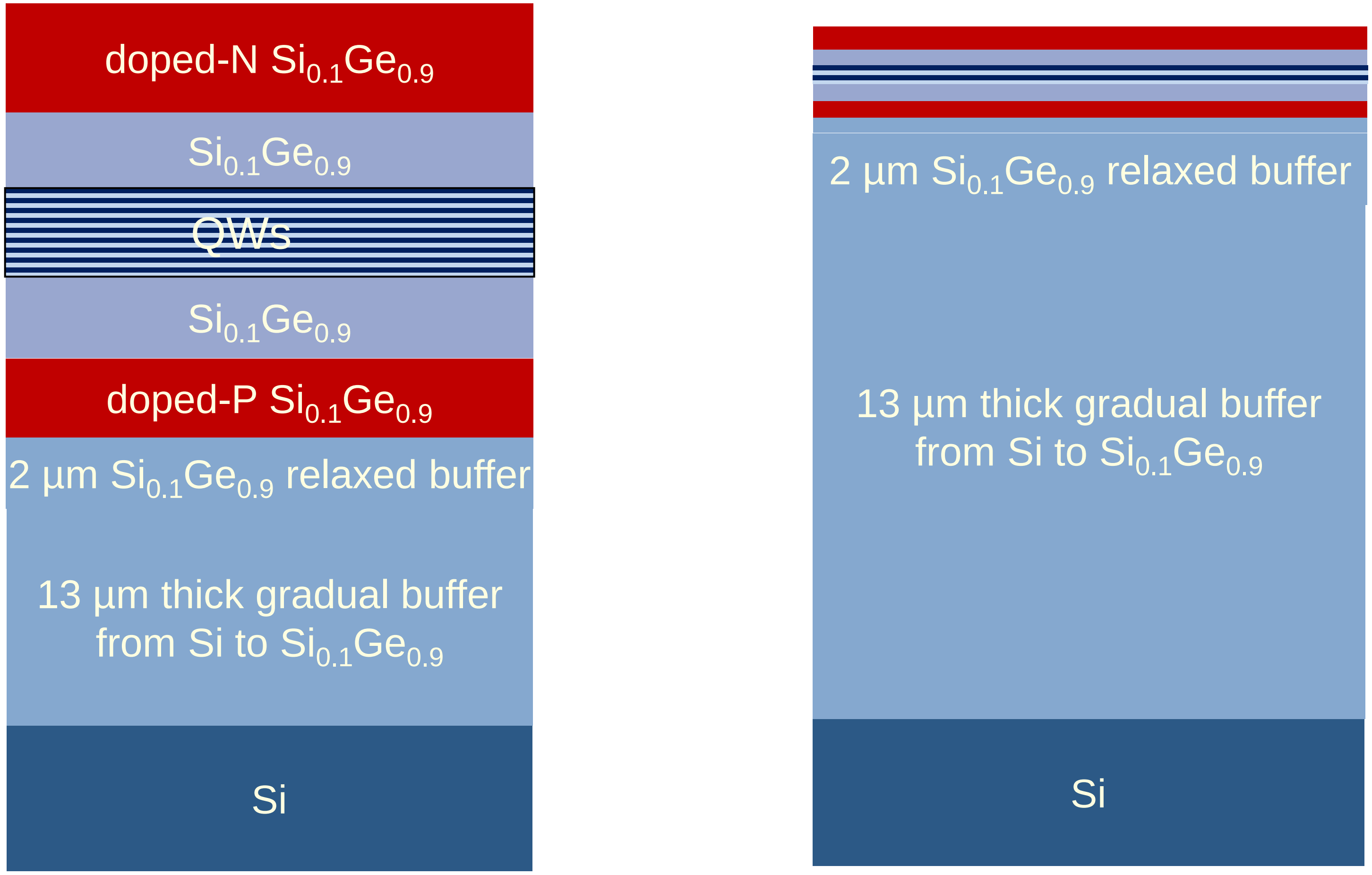
Energy dissipation of photocurrent

Energy/bit = 1/B $(I_{ph}V_{bias})$

C ~ 62 fF ➡ Energy/bit = **70 fJ/bit**

(for a voltage swing of 1 V , 20 Gbps, 0.5 mW input power)

Integrated circuits based on Ge/SiGe QW ?



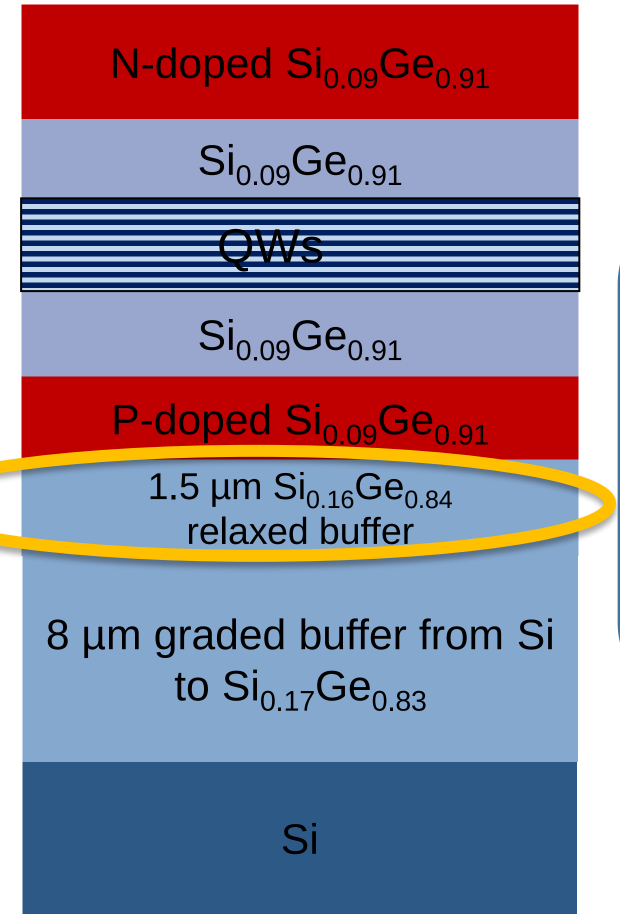
Schematic description

The real scale

Challenge: coupling the light from silicon to Ge/SiGe QW

Waveguide integration on bulk Si

1st Option: Waveguide based on the graded buffer
(The light is guided in the relaxed buffer layer).

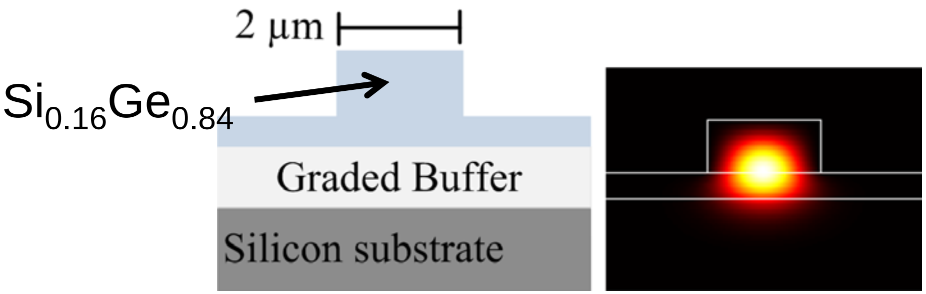


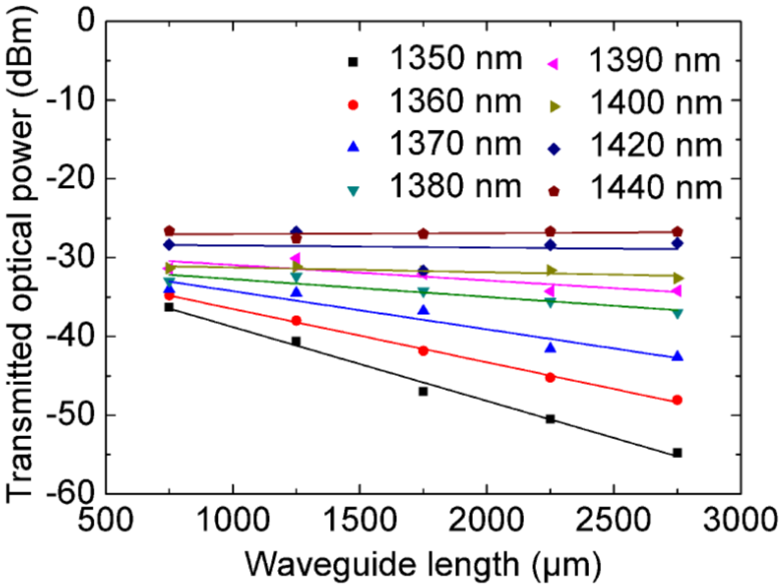
Challenge: Use the relaxed $Si_{1-y}Ge_y$ buffer layer as a low loss waveguide

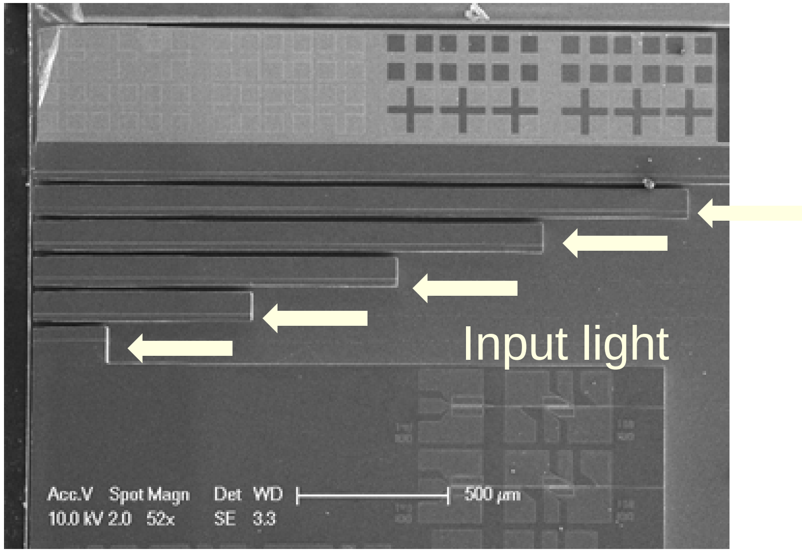
- If y is too high => high propagation loss
- If y is too low => strong strains occur => dislocations

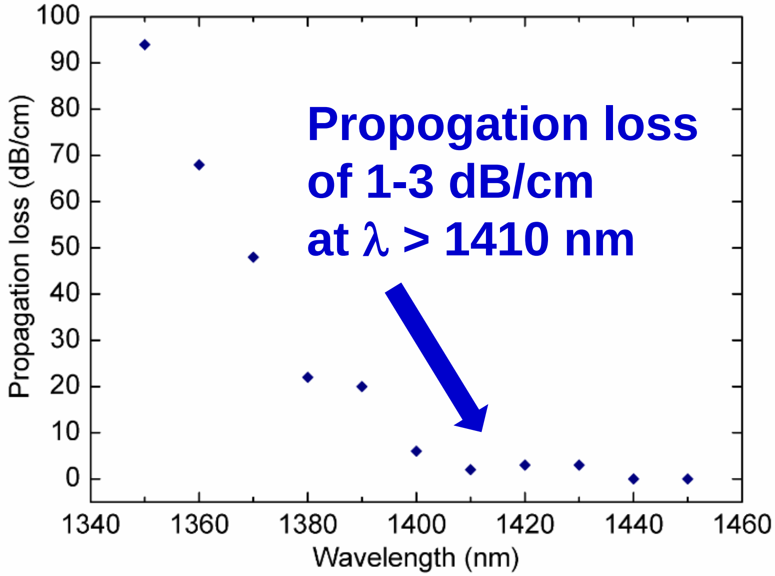
Waveguide integration on bulk Si

$Si_{0.16}Ge_{0.84}$ waveguide losses

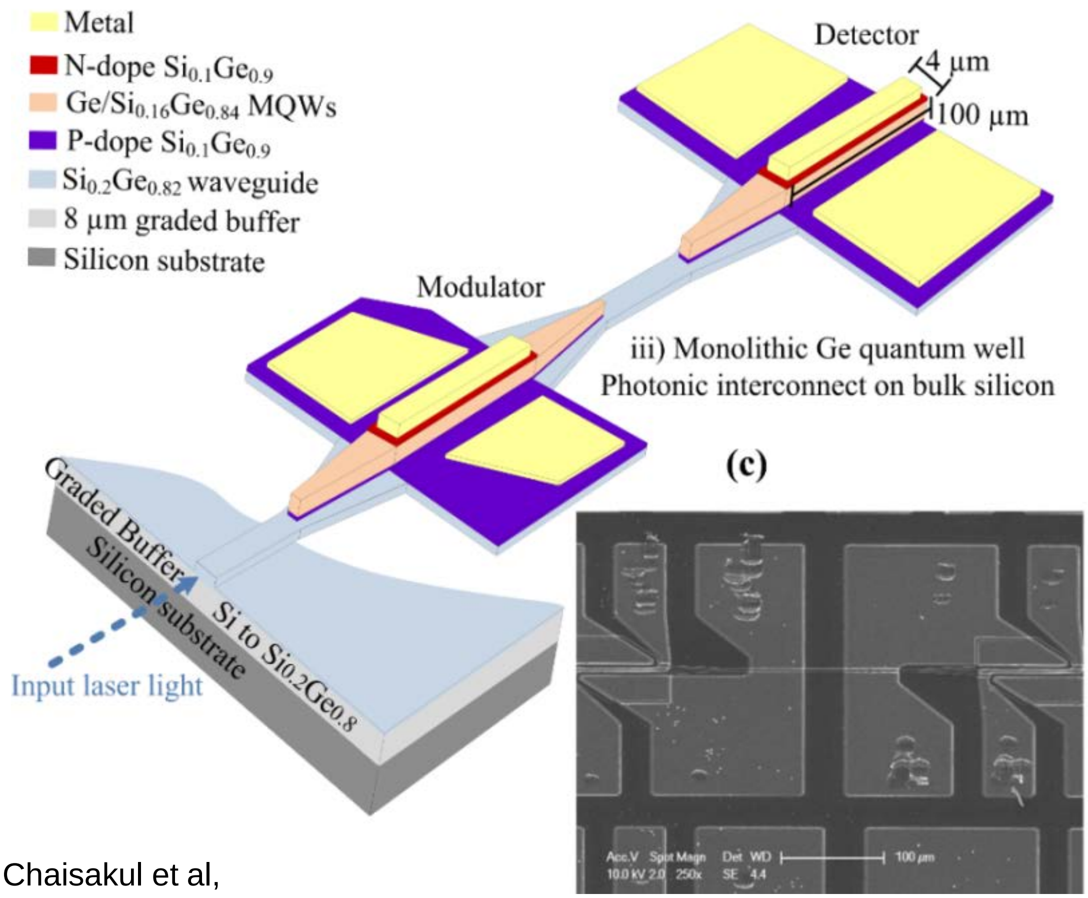








Optical link on bulk Si, based on Ge/SiGe QW active devices and SiGe waveguide on graded buffer



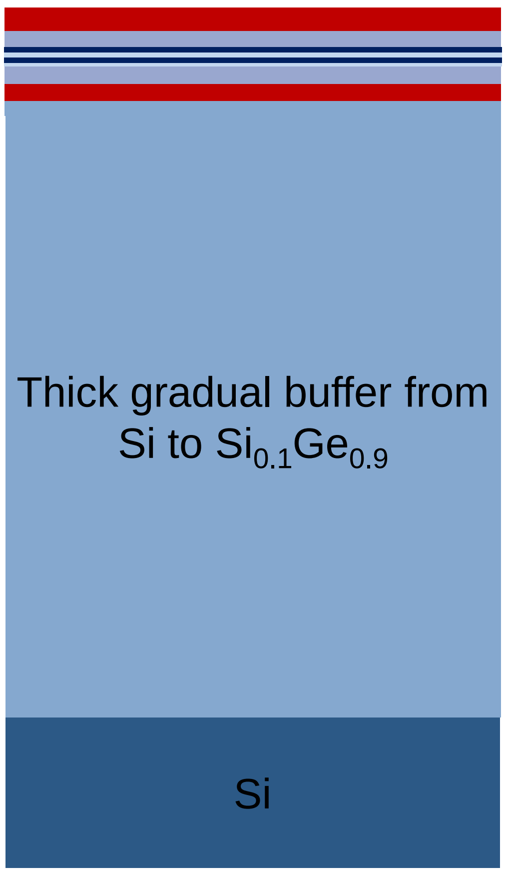
- Insertion loss: < 5 dB
- Modulator bandwidth : 6 GHz
- photodetector bandwidth : 4 GHz

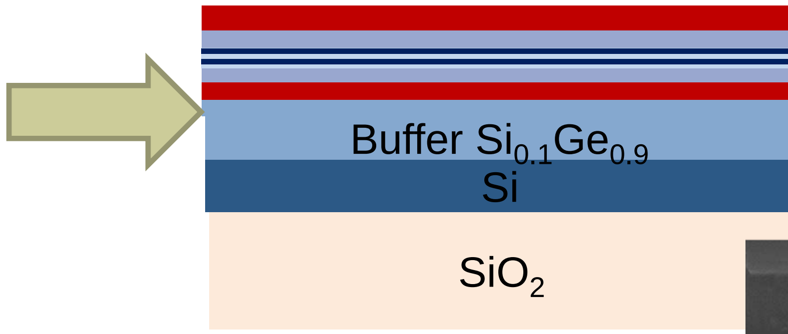
P. Chaisakul et al,
Nature Photonics 8, 482-488 (2014)

Integration on SOI

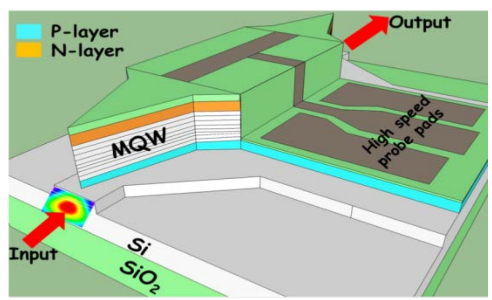
2nd option: decrease the thickness of the buffer layer

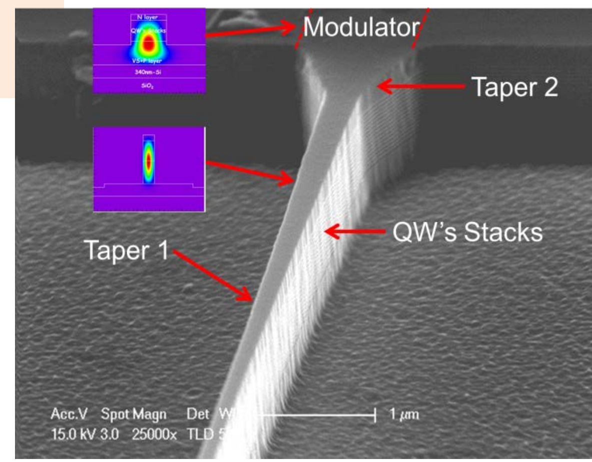
Challenge: keeping homogeneous and high quality layers





Fabrication is on-going





Ge/SiGe modulator integrated with SOI : estimated performance :
Extinction ratio = 7.7 dB, loss = 4 dB

M-S. Rouifed et al, IEEE JSTQE (2014)

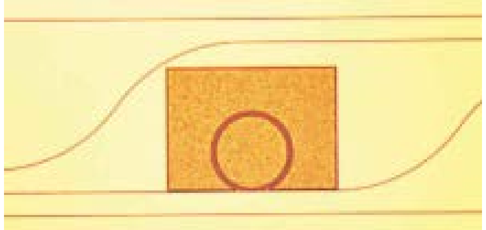
Evolution of Si-based modulators

Carrier depletion modulator MZi

Energy/bit ~ 5 pJ/bit

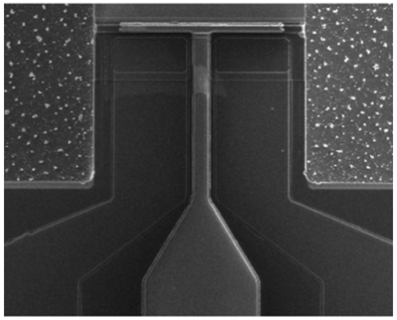
Ring resonator modulator

Energy/bit ~ 0.7 pJ/bit

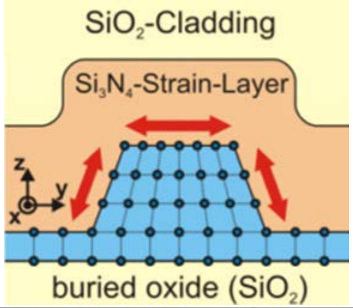


EA Ge/SiGe modulator

energy/bit ~ 0.07 pJ/bit



Strained modulator



Ultra low power consumption modulator

energy/bit ~ few fJ/bit

Outline

- Motivation
- Main building blocks in photonics
  - √ Light propagation
  - √ Optical modulation
    - ➢ Principle
    - ➢ Physical effect
    - ➢ Recent advances
  - √ Light detection
    - ➢ Ge photodiode
    - ➢ Avalanche PD
  - √ Light emission
- Conclusion

Specifications:

- ✓ High bandwidth (> 10GHz)
- ✓ High responsivity
- ✓ Compact
- ✓ Low power consumption
- ✓ Compatible with Si technology

Integrated photodetector on Si platform

Specifications:

- ✓ High bandwidth (> 10GHz)
- ✓ High responsivity
- ✓ Compact
- ✓ Low power consumption
- ✓ Compatible with Si technology

The sensitivity is defined as the minimal optical power which could be recorded for a given BER

$$P_{min} = \frac{1}{\mathcal{R}} \frac{1+r}{1-r} Q \langle {i_n}^2 \rangle^{1/2}$$

Responsivity[A/W]

Noise current [A]

$\boldsymbol{r}$: Extinction ratio (depend on the modulation format)
$\boldsymbol{Q}$: Q-factor is given by the BER (For a BER of 1.10^{-12}, $Q \approx 7$)

Objective: Reduce at the maximum $\boldsymbol{P_{min}}$

→ Reduction of the noise current

→ Increase the responsivity

RESPONSIVITY

Absorption
- Absorption coefficient
  - Layer quality
- Diode geometry
- Integration

Carrier collection
- Electric field
- Recombination

NOISE

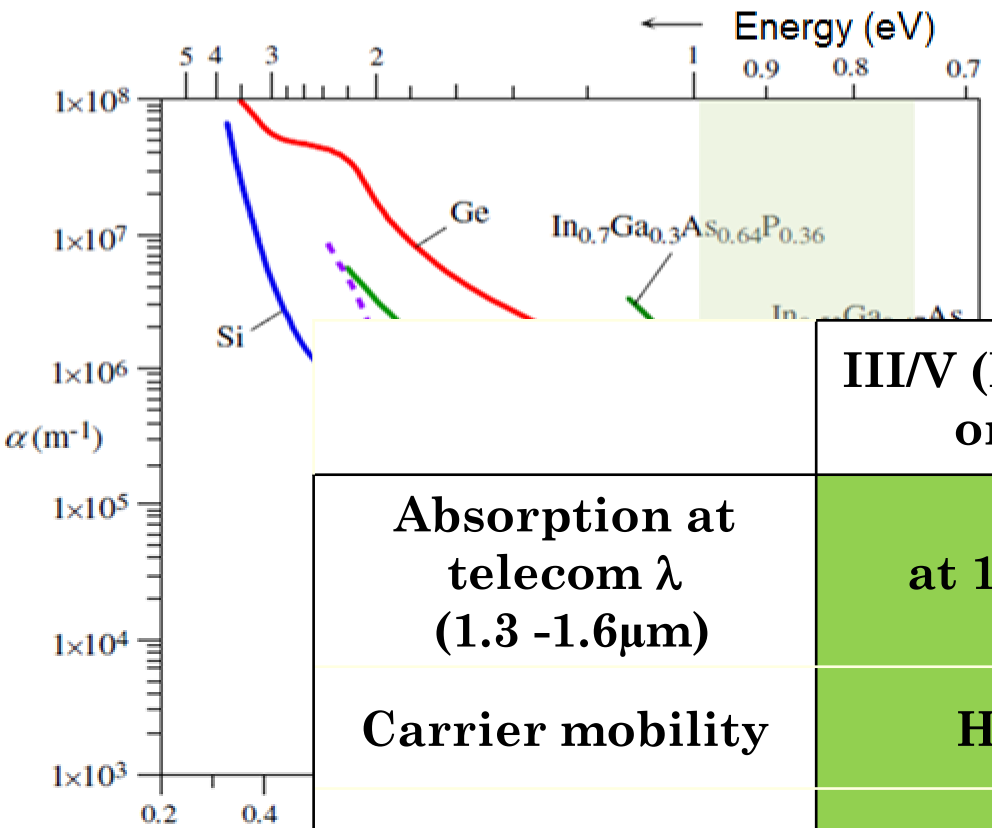
Thermal noise

$$\langle i_{jn}{}^2 \rangle^{1/2} = \sqrt{\frac{4k_B T \Delta f}{R_{éq}}}$$

Shot noise

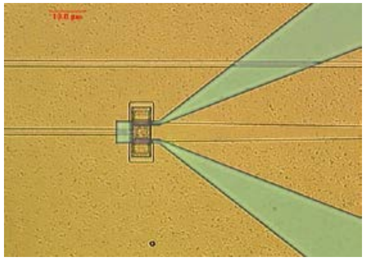
$$\langle i_{sn}{}^2 \rangle^{1/2} = \sqrt{2q(I_{photo} + I_{obs})\Delta f}$$

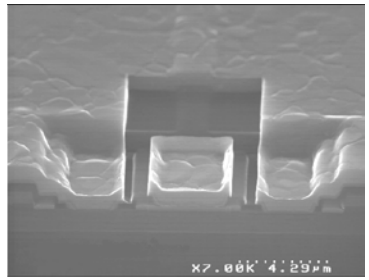
Material Choice

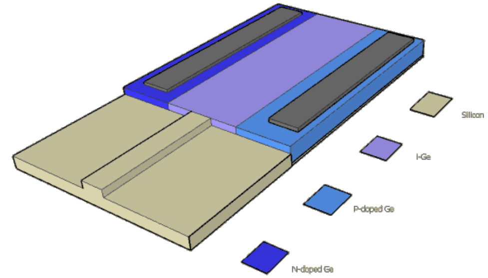


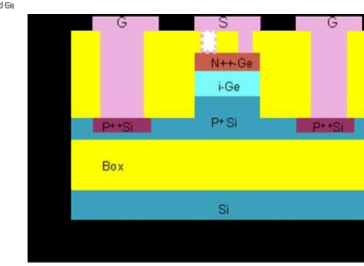
	III/V (InGaAs) on Si	Ge on Si
Absorption at telecom λ (1.3 -1.6µm)	at 1.55µm	at 1.55µm
Carrier mobility	High	High
Layer quality	Very good	Depend on epitaxy
Integration on Si	Flip-chip, direct bonding	Hetero-epitaxy on Si

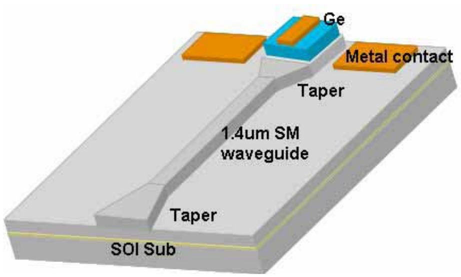
Ge Photodetectors

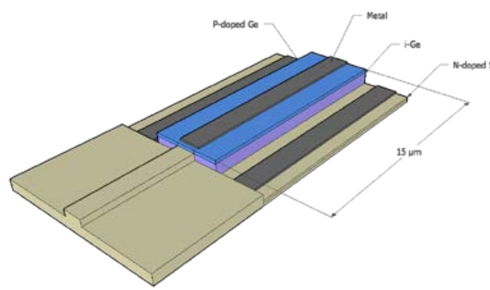


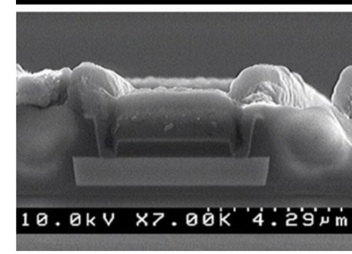


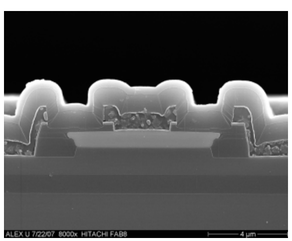










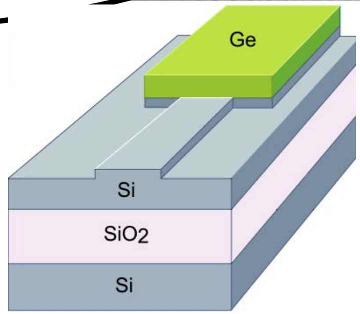


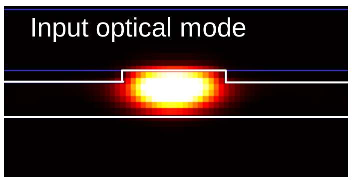
Europe: Univ. Paris Sud, CEA-Léti, Stuttgart Univ., Roma Univ. …

Asia: Tokyo Univ., A*Star, Petra, AIST, Chinese Academy of Sciences, …

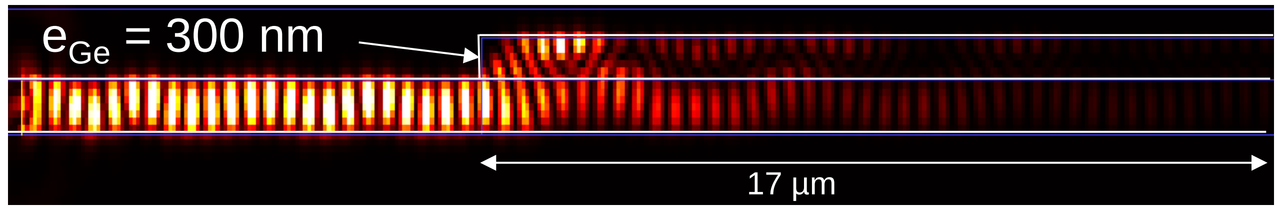
North America: Intel, MIT, IBM, Cornell, Luxtera, Ligthwire, Kortura, Oracle …

Ge photodetector: optical coupling

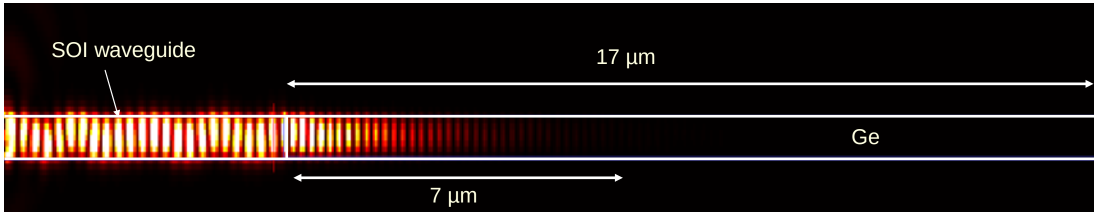


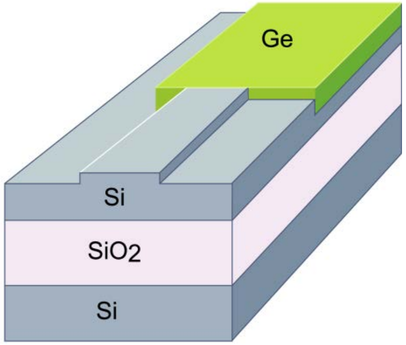


Vertical coupling



Butt coupling

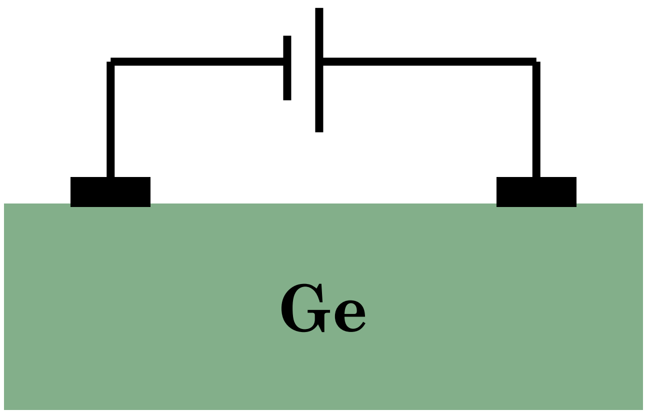




⇨ Short absorption length => Low capacitance

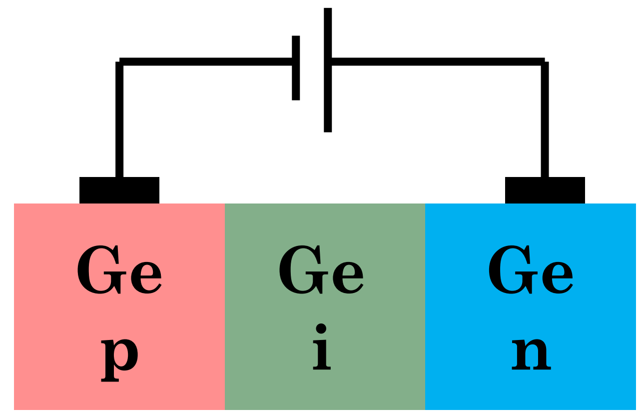
⇨ Light absorption is independent of Ge film thickness

Carrier collection efficiency



MSM

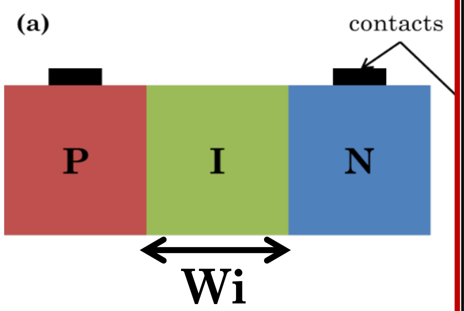
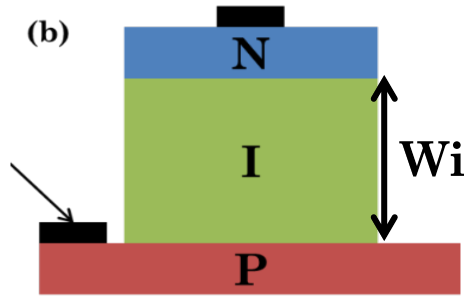
- Strong field dependence
- High noise
- Non uniform electric field



PiN

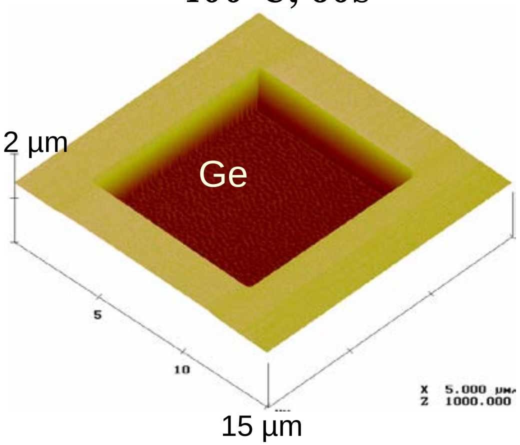
- Uniform electric field
- Internal electric field (under 0V)

PIN diode

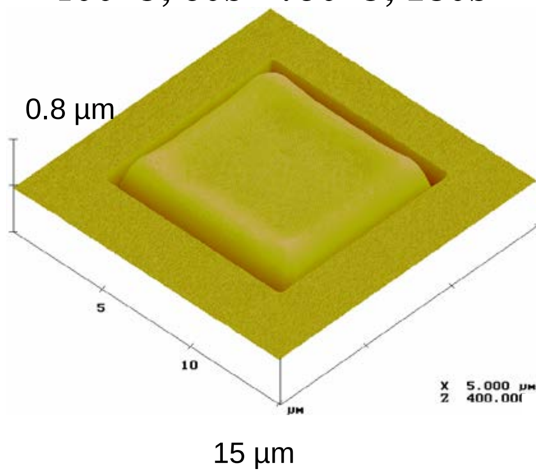
	Latérale	Verticale
Disposition des contacts		
Avantages	*Planar contacts*	*W_i define during the epitaxy (in-situ doping)*
drawbacks	*W_i define par ion implantation*	*Ge etching* *Bottom contact*

- **Two RPCVD steps to overcome lattice mismatch issue**

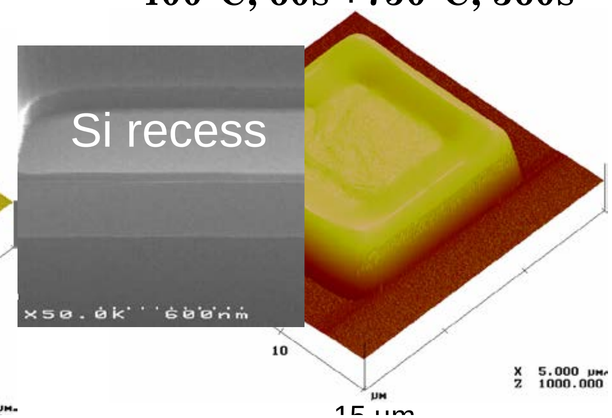
Ge « Seed » layer 400°C, 60s



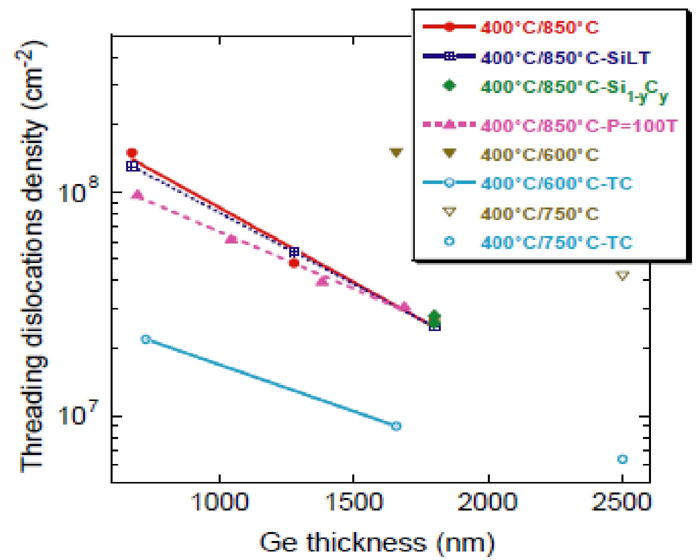
400°C, 60s +750°C, 180s



400°C, 60s +750°C, 360s



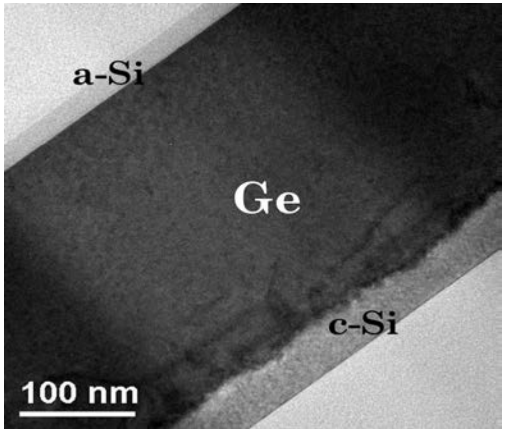
- Overgrowth of Ge
  - To avoid faceting inside the cavity
  - To reduce Threading Dislocation Density (TDD)

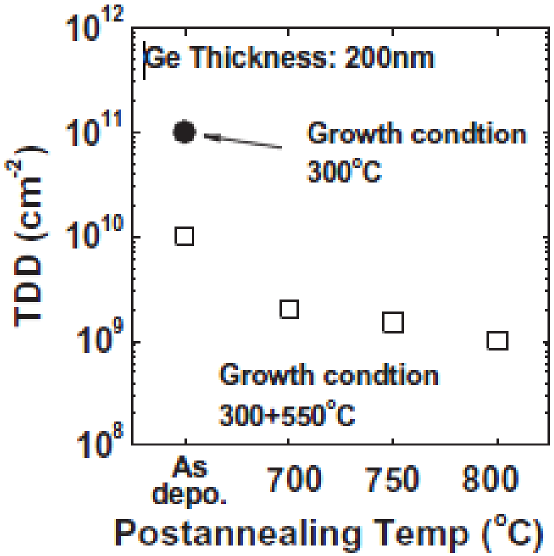


J.M. Hartmann et al., *J. Crystal Growth,* **274**, 90-99 (2005)

Device Fabrication: Ge Growth

- Post epitaxial thermal cycling to further reduce TDD in the Ge layer
- CMP step to remove protruded Ge
- SiO_2 encapsulation
- Ion implantation of Ge
  - √ N-type : Phosphorus
  - √ P-type : Boron
- Rapid Thermal Anneal



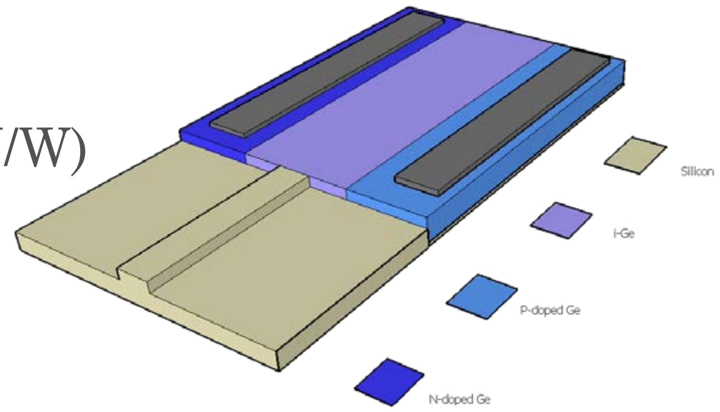


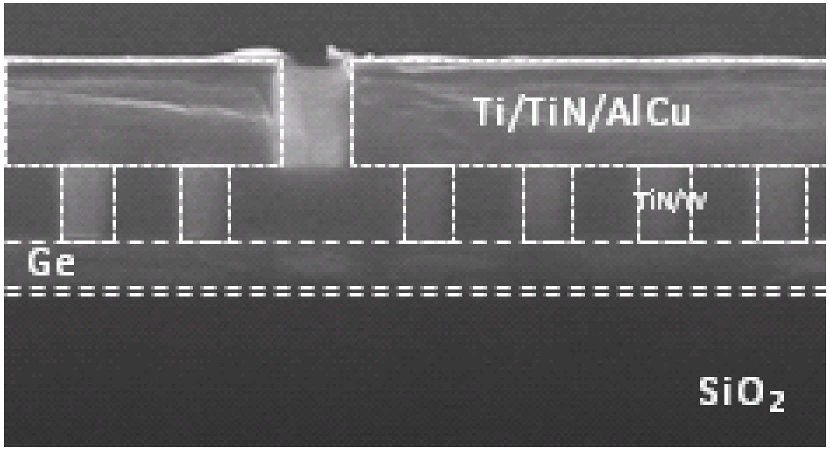
Y. Yamamoto et al., *Solid-State Electronics*, **60-1**, 2–6, (2011).

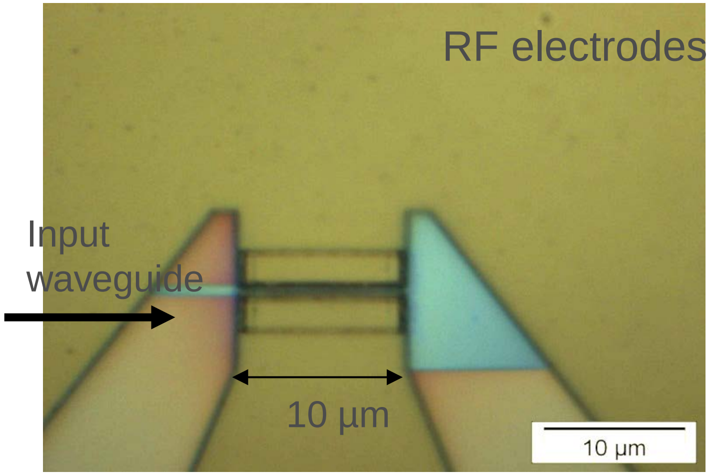
Device Fabrication: Contact and Metal

- Oxide encapsulation
- Planarization
- Contact definition
  - 0.4x0.4µm vias for metal filling (TiN/W)
  - Ti/TiN/AlCu pad defined by etching

Lateral







Circuit level integration

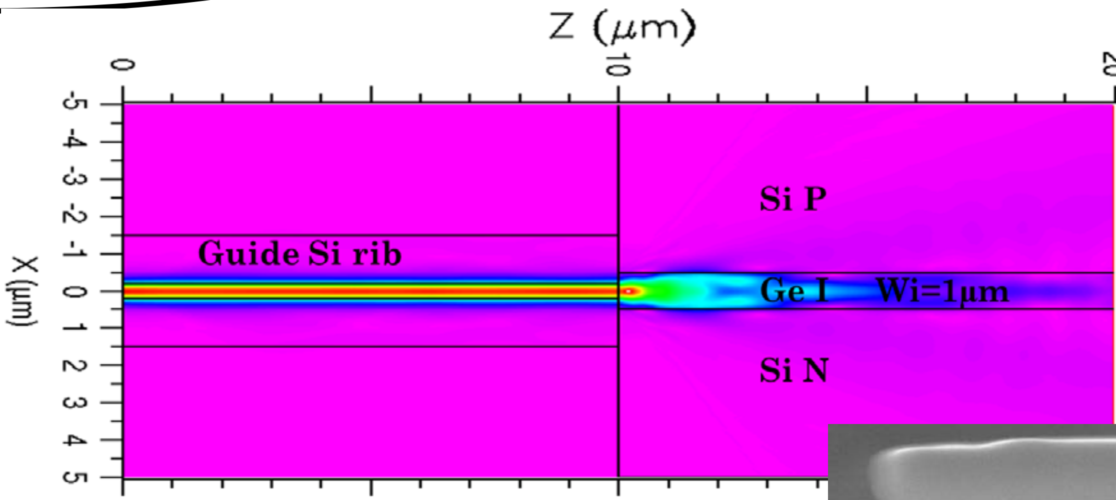
Source	Modulator	Photodetector
III-V on Si Hybrid laser	**PN, PIN in Si**	**PIN Ge on Si**
	Ion implantation in **Si**	Ion implantation in **Ge**
	Dopant activation for **Si**	Dopant activation for **Ge**
	Contacts on Si (silicide)	**Contacts on Ge**

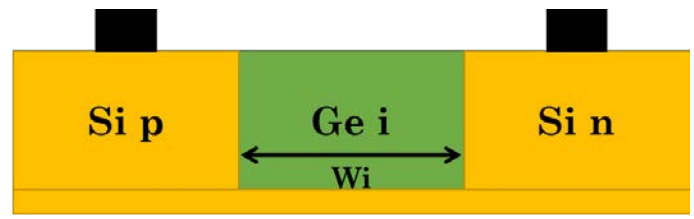
The full integration increases the fabrication complexity and the overall cost.

Double Si/Ge/Si heterojunction

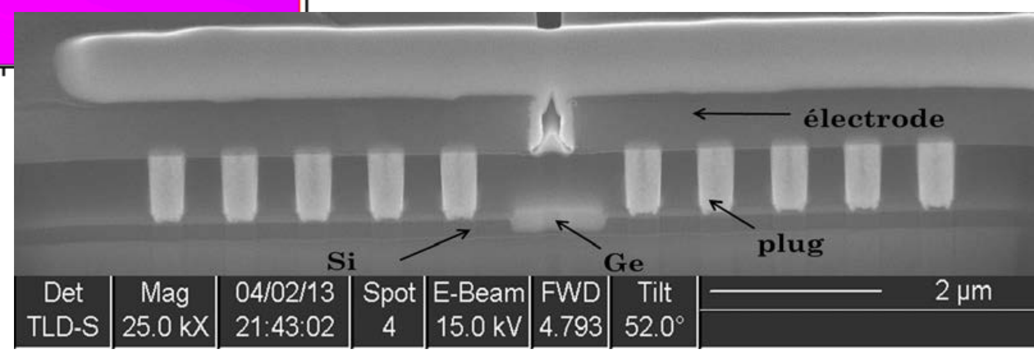
Aim: Use the same technological steps for modulators and detectors including doping, thermal annealing and contacts

p-i-n Si/Ge/Si Photodetector





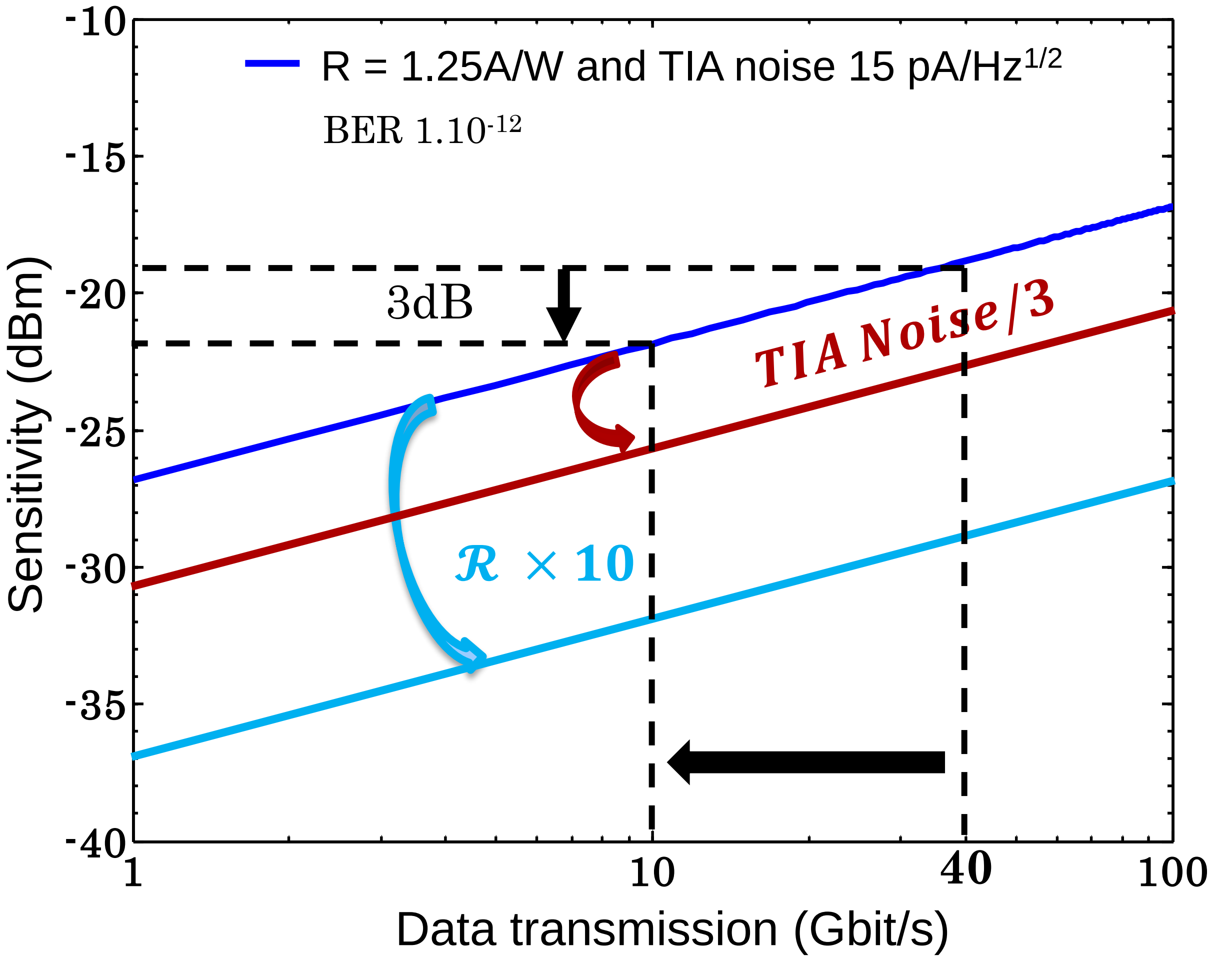
Wi = 1µm



$\mathcal{R}$~1.1 A/W @ 1550nm
Dark current <nA @ -1V
Bandwidth 18GHz @ -1V
30GHz @ -2V

How to improve the sensitivity of the receivers?

Sensitivity of photodetectors

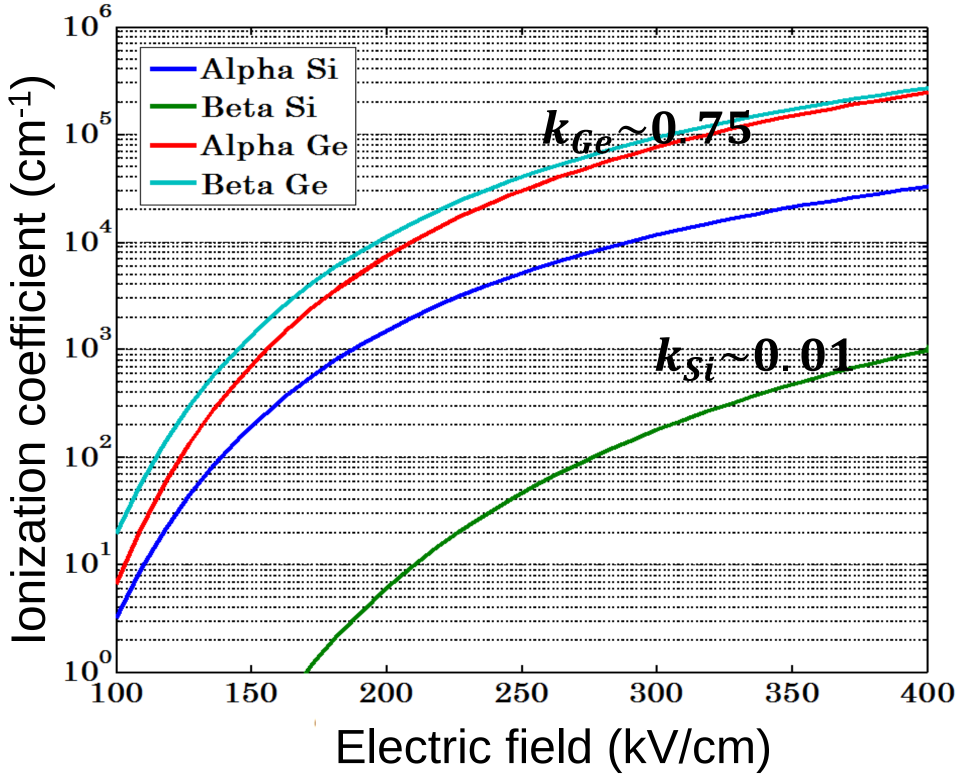


How to increase the sensitivity?

- λ Multiplexing
  - 40Gbits/s = 4*10Gbits/s
- Reduction of the TIA noise
- Increase the responsivity

Avalanche PD

Avalanche behaviour



α: Ionization coefficient of electrons
β : Ionization coefficient of holes

$$k = \frac{\beta}{\alpha} \text{ or } k = \frac{\alpha}{\beta}$$

At given multiplication region width:

- $M_{Ge} > M_{Si}$
- $V_{b\text{-}Ge} < V_{b\text{-}Si}$

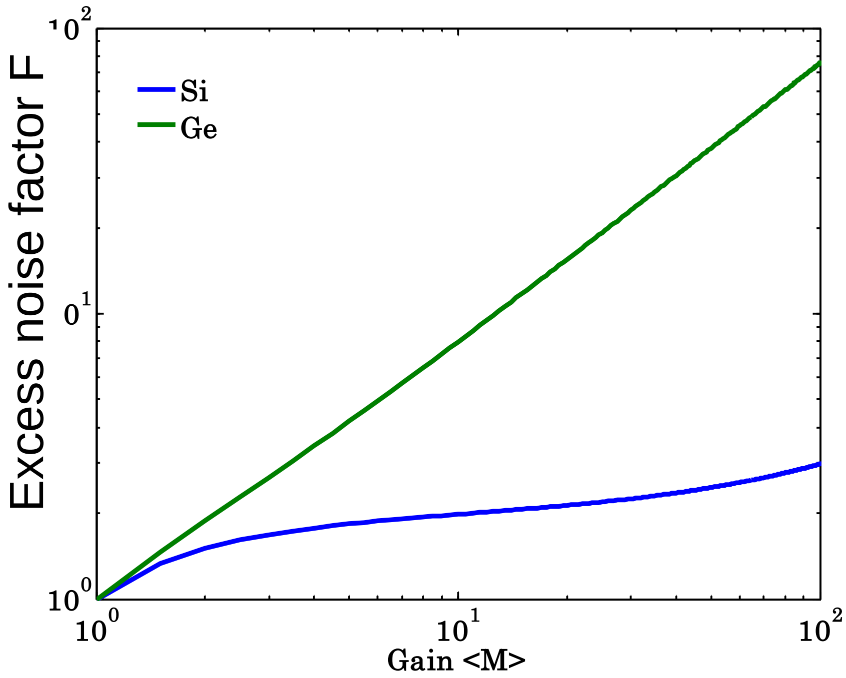
Avalanche behavior

Shot noise

$$\langle i_{sn}{}^2 \rangle^{1/2} = \sqrt{2q\left[\left(I_{photo} + I_{obs,m}\right)M^2F + I_{obs,nm}\right]\Delta f}$$

<u>Excess noise factor F</u> is defined as the ratio of the Gain variance on the mean square gain value

$$F(M) = \frac{\langle M^2 \rangle}{\langle M \rangle^2} = kM + (2 - 1/M)(1-k)$$



Ge in avalanche mode:
- **High Gain**
- **Low voltage**

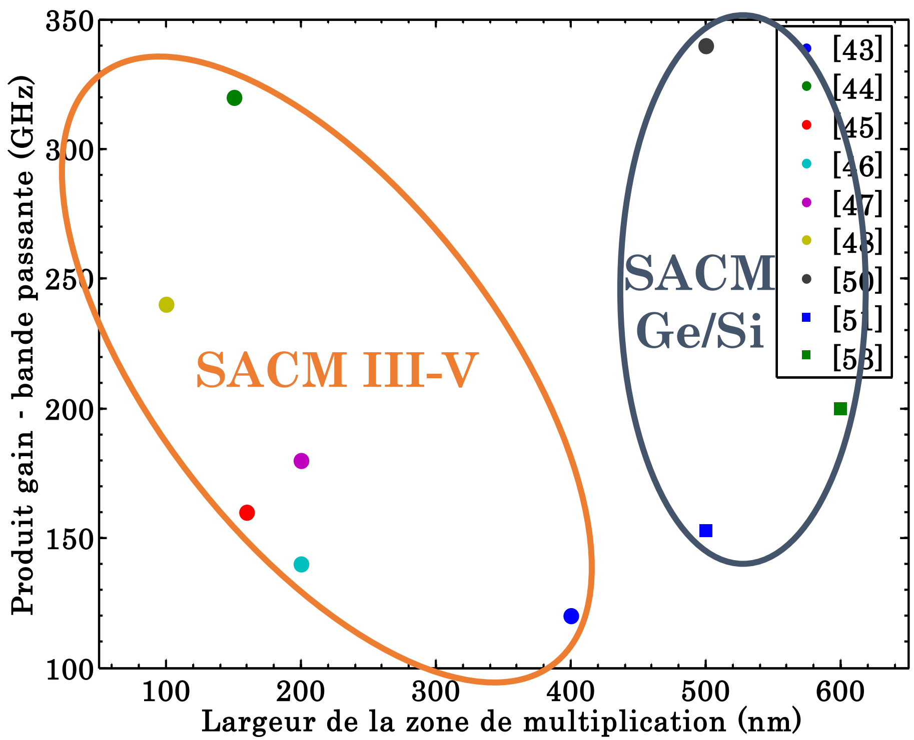
BUT
- **High multiplication noise**

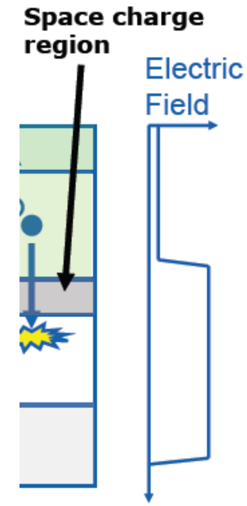
First Approach:

- Separate Absorption, Charge and Multiplication(SACM) APD
  - √ Ge for ab
  - √ Si for mul

Low multipl

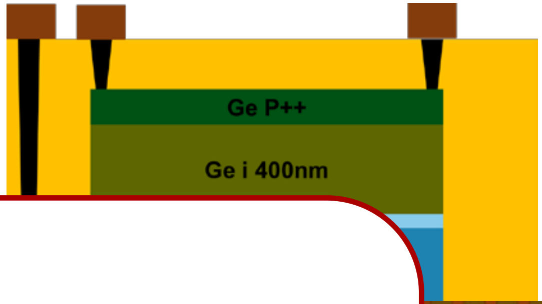
High Gain-B

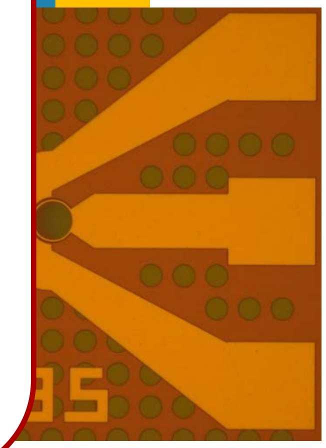




- Critical par
  - √ The char
    - Thickness
    - Doping

In-situ epitaxy and doping
→ Uniform doping in the charge layer
→ Good doping level and thickness controls



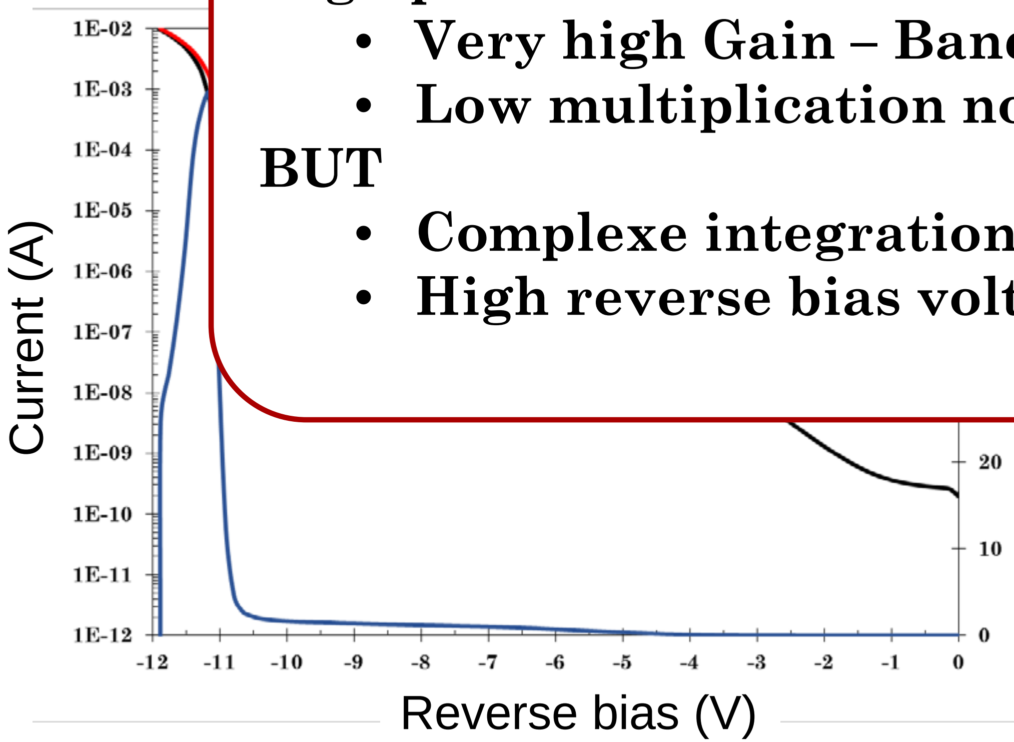


High preformances

- **Very high Gain – Bandewidth product**
- **Low multiplication noise**

BUT

- **Complexe integration**
- **High reverse bias voltage**



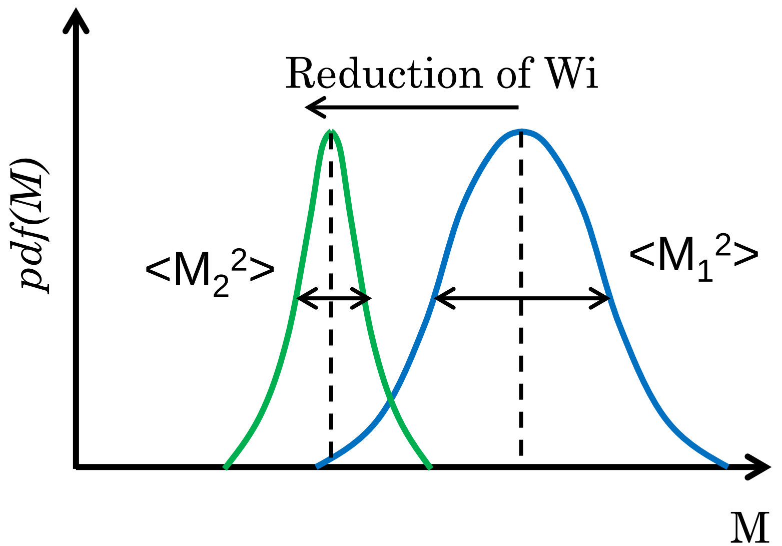
- **Gain – Bandewidth product: ~ 560GHz**
- **Avalanche voltage: ~ 11V**

Dead space: Minimum distance to induce ionization of carriers

D = E_{th}/qE $$d = \frac{E_{th}}{qE}$$

Reduction of Wi

- **Dead space is not neglecgible**
  d/Wi ~ 0.1
- **Reduction of the Excess Noise factor** $F(M) = \frac{\langle M^2 \rangle}{\langle M \rangle^2}$



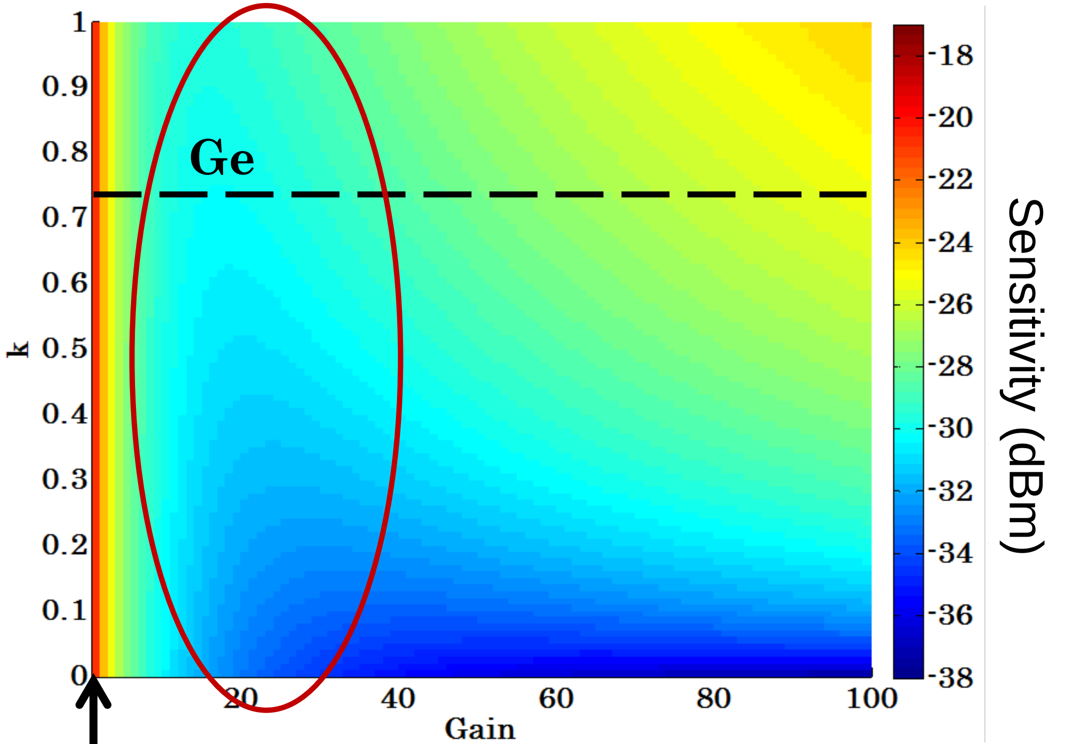
p-i-n avalanche photodiode: moderated gain and noise using « dead space » effect in Ge

In Germanium: *d* ~ 28 – 42nm for E ~300 – 200 kV/cm

d/Wi ~ 0.1 → Wi < 500nm

Sensitivity of p-i-n APD

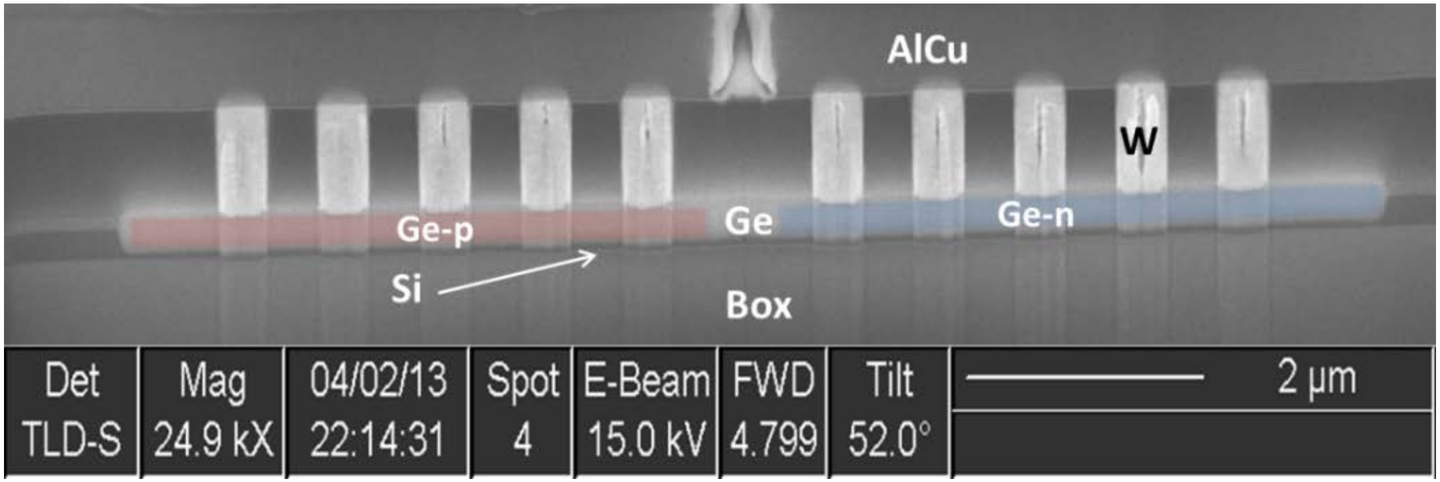
Sensitivity at 10Gbits/s for a BER=1.10^{-12} and a TIA noise of $15pA/Hz^{1/2}$



P-i-n Photodiode w/o gain (M=1)

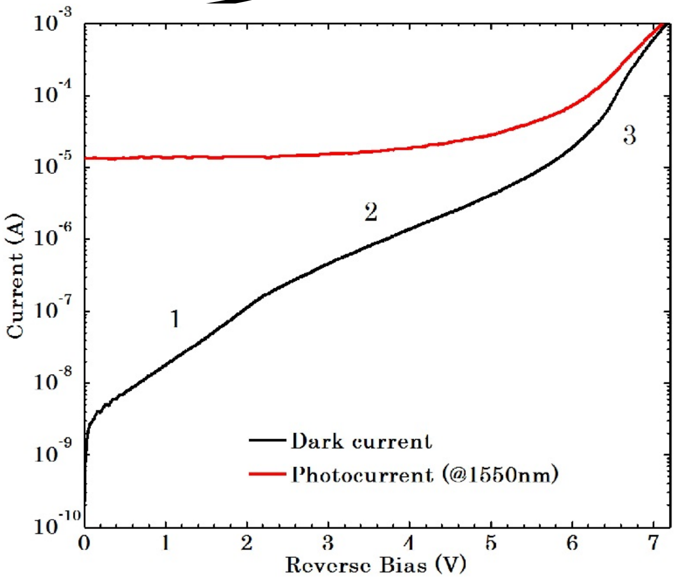
- **Even for *k=1* (the noisiest case) the sensitivity is improved**
- **The higher *k* factor, the lower optimal gain**

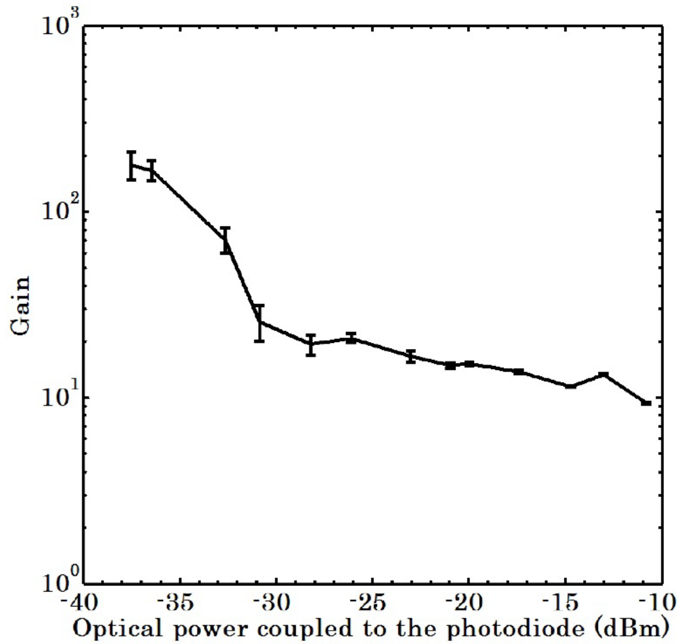
P-i-n APD receivers



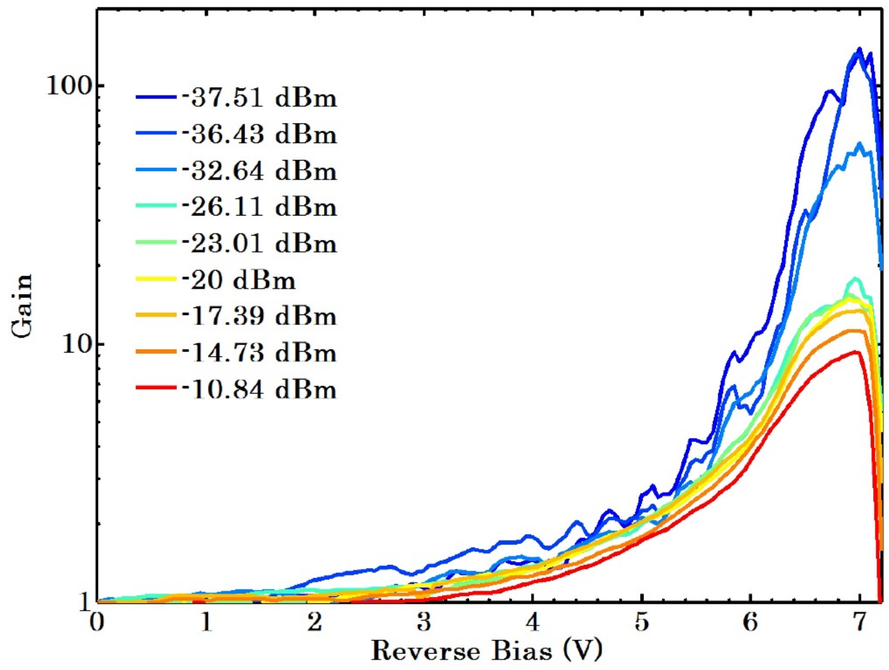
- **Classical p-i-n photodiode**
  - **Robust and reliable design**
  - **« Simple » Fabrication**
- **Low dark current**

DC characteristics





Wavelength: 1.55µm

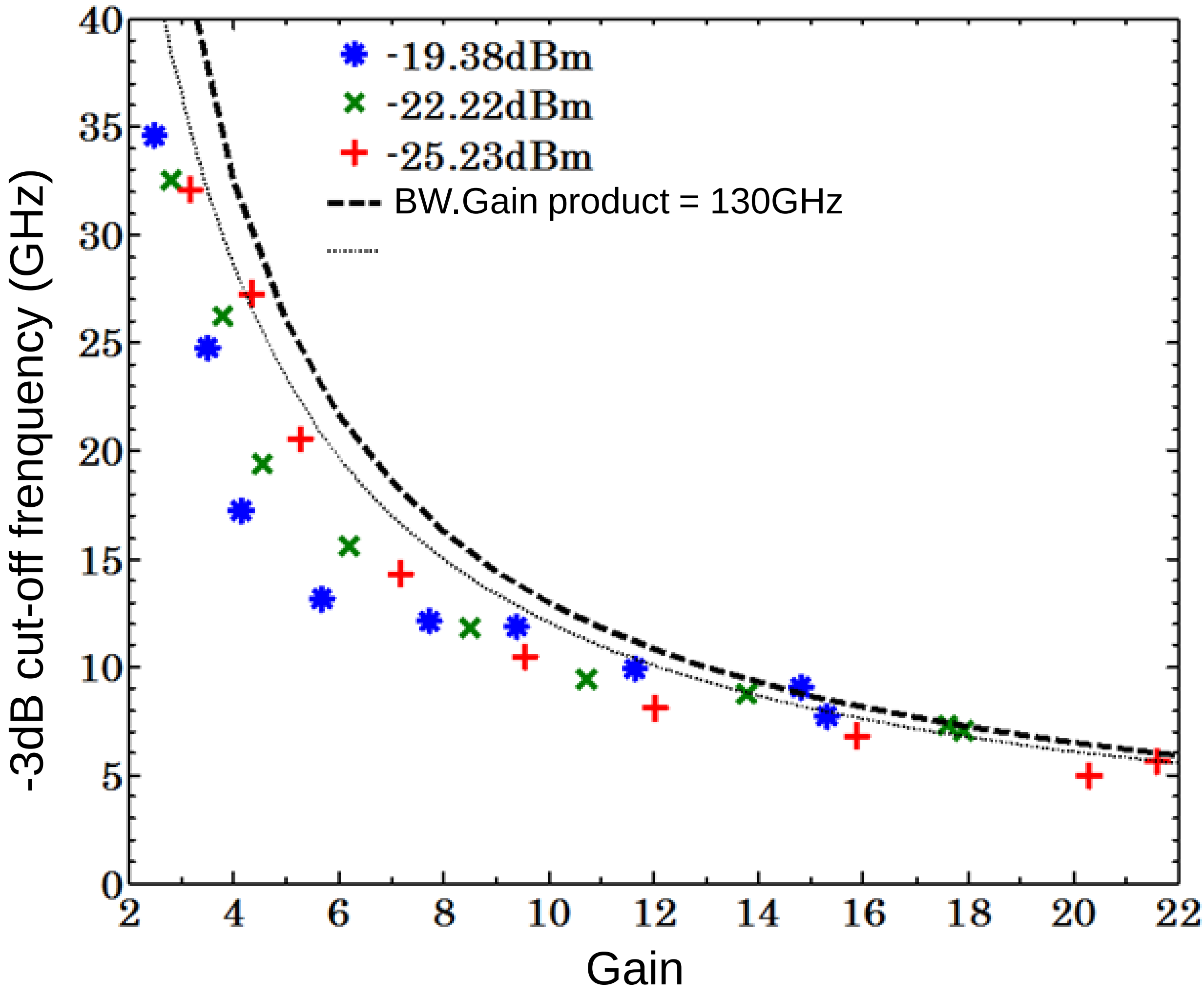


High gain achieved

- over 140 for -37.5dBm optical power coupled to the photodiode

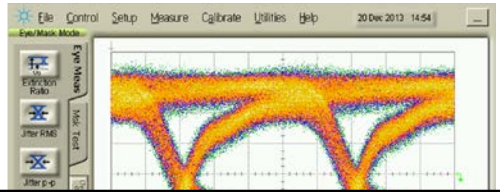
L. Virot et al., Nature Communications (2014)

RF characteristics

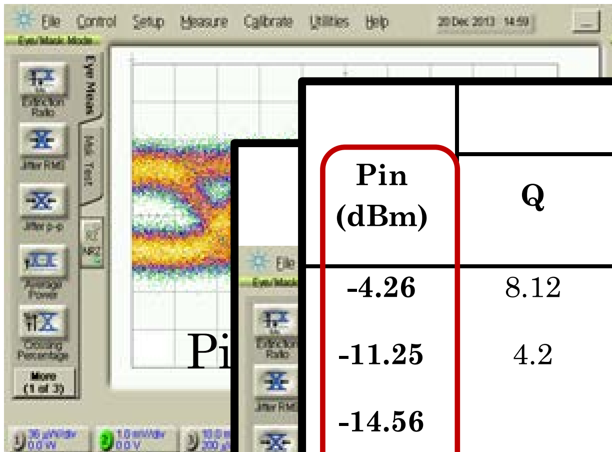


Eye diagrams without TIA

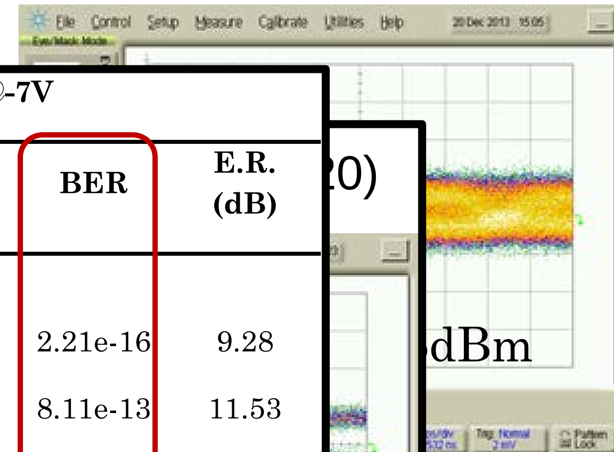
10GBit/s @ 0V (M=1)

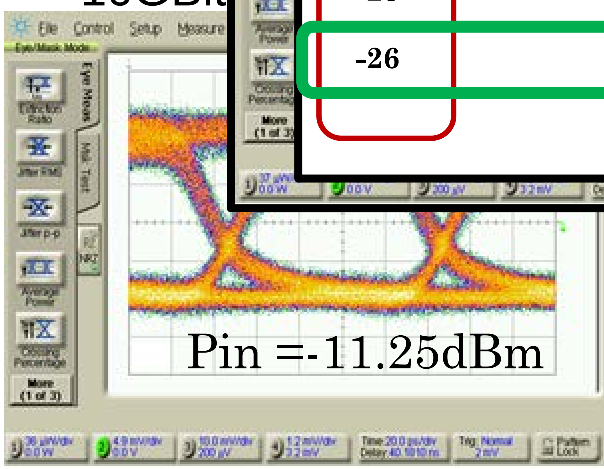


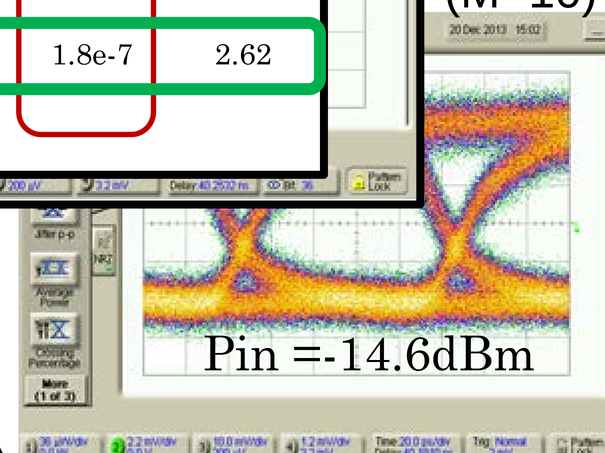
10GBit/s @ -2V (M=1)



10GBit/s @ -2V (M=1)

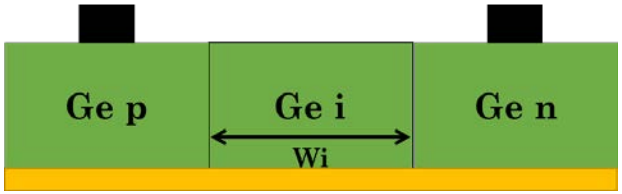






	M=1			@-7V			
Pin (dBm)	Q	BER	E.R. (dB)	M	Q	BER	E.R. (dB)
-4.26	8.12	2.42e-16	11.59				
-11.25	4.2	1.31e-5	4.72	10	8.13	2.21e-16	9.28
-14.56				11	7.06	8.11e-13	11.53
-23				15	6.94	1.9e-12	4.99
-26				20	5.09	1.8e-7	2.62

P-i-n APD receivers



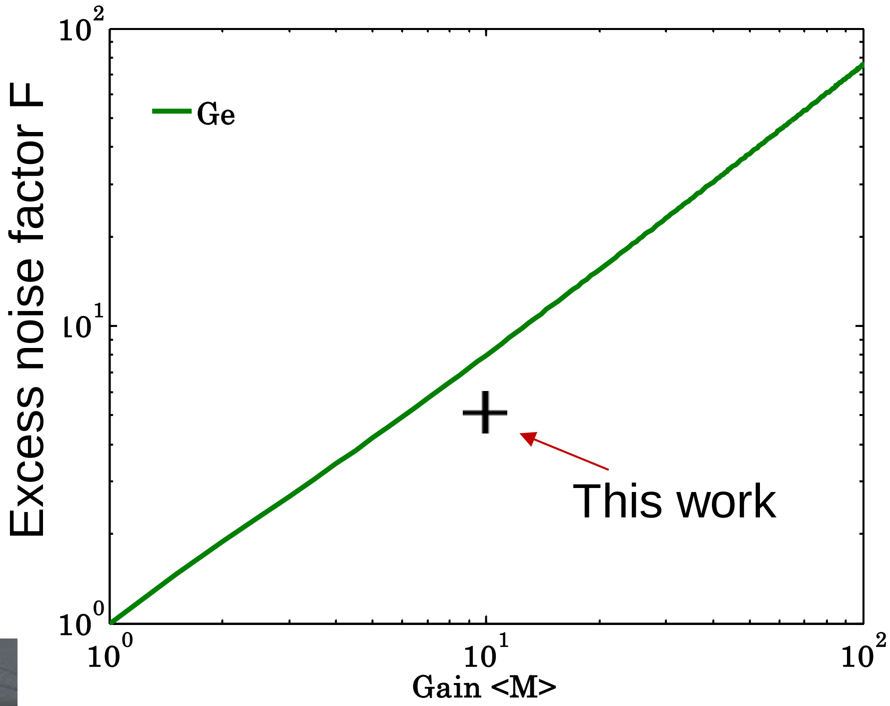
10Gbit/s eye diagram without TIA

Coupled optical power into Ge diode: -11.25dBm

Q = 4,2 → **M = 10** → **Q = 8,13**

$F_{-11.25dBm} = \sigma(M=10) / \sigma(M=1) = 5.24$

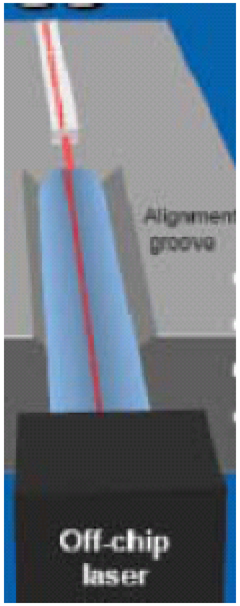
Reduction of the noise using « dead space » effect



Outline

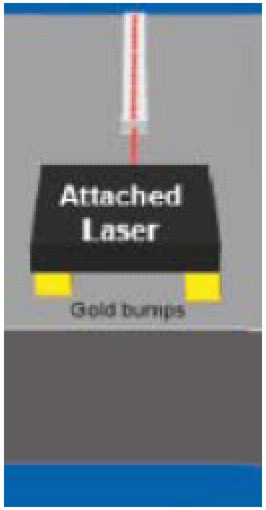
- Motivation
- Main building blocks in photonics
  - √ Light propagation
  - √ Optical modulation
  - √ Light detection
  - √ Light emission
    - ➢ The approaches to emit light on silicon
- Conclusion

Off-chip laser
Fiber attachement & alignment
High coupling losses
Very expensive
Non-integrated



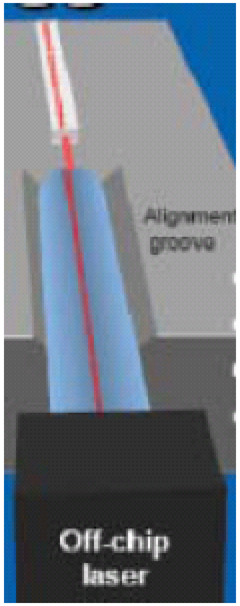
courtesy: Blas Garrido

Laser on silicon



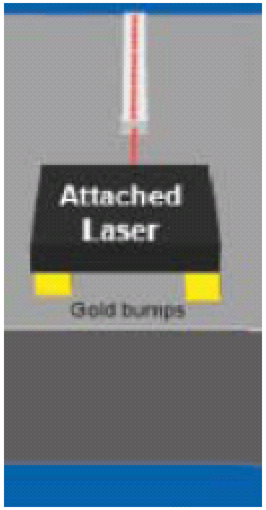
Attached laser
Tight alignment tolerances
Gold metal bonding
Expensive

Off-chip laser
Fiber attachement & alignment
High coupling losses
Very expensive
Non-integrated



courtesy: Blas Garrido

Laser on silicon



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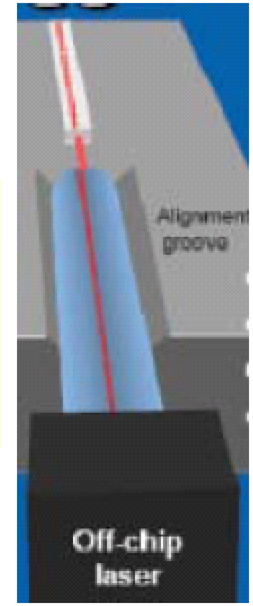
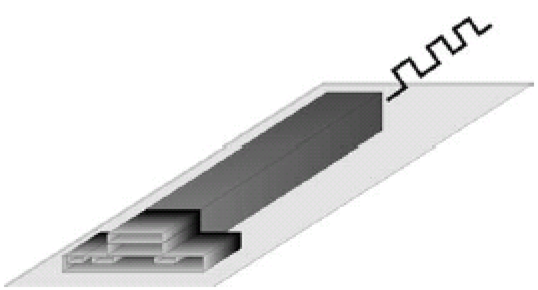
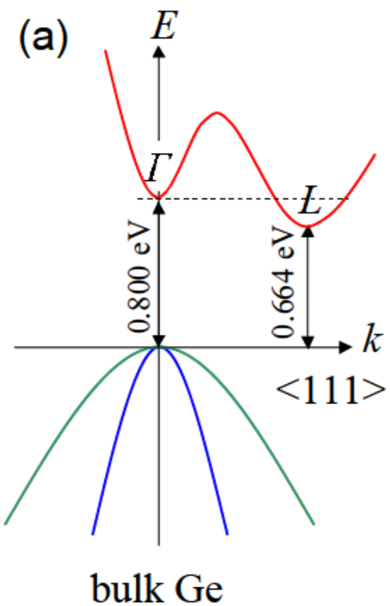


Monolithic laser Si compatible
Not any alignments
Highly integrable
Low cost
Electronic-photonic integration



courtesy: Blas Garrido

⇨ To indirect to “direct” bandgap SC



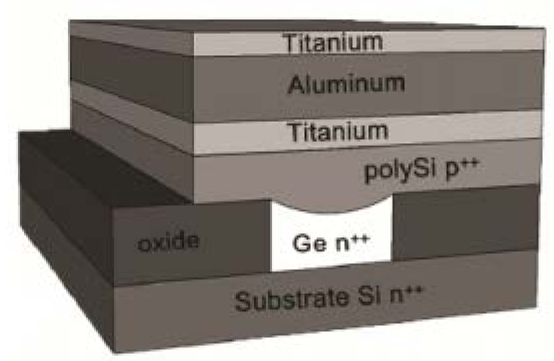
“The first Ge laser”; J. Liu, X. Sun, L.C. Kimerling, J. Michel : Presentation at Group IV photonics – San Francisco (September 2009).

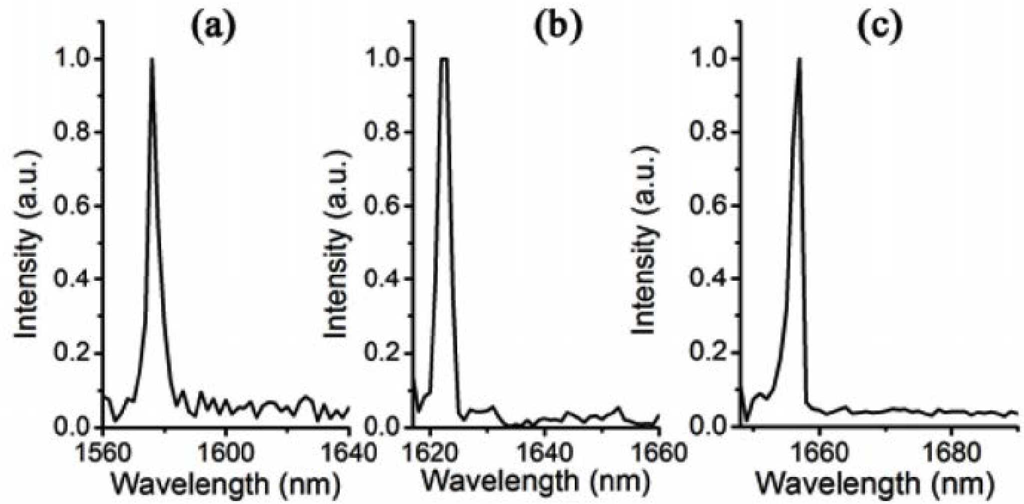
An electrically pumped germanium laser

Rodolfo E. Camacho-Aguilera,[1] Yan Cai,[1] Neil Patel,[1] Jonathan T. Bessette,[1] Marco Romagnoli,[1,2] Lionel C. Kimerling,[1] and Jurgen Michel[1,*]

[1]*Massachusetts Institute of Technology, 77 Massachusetts Ave., Cambridge, MA 02139, USA*
[2]*PhotonIC Corporation, 5800 Uplander Way, Los Angeles, CA 90230, USA*
**jmichel@mit.edu*

Abstract: Electrically pumped lasing from Germanium-on-Silicon pnn heterojunction diode structures is demonstrated. Room temperature multimode laser with 1mW output power is measured. Phosphorous doping in Germanium at a concentration over 4x10^{19}cm^{-3} is achieved. A Germanium gain spectrum of nearly 200nm is observed.

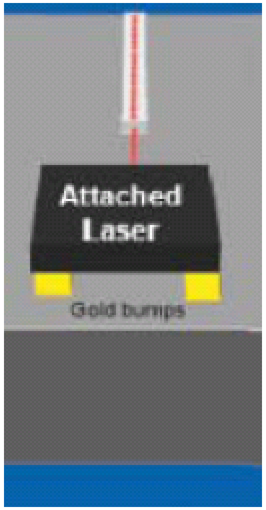




1576nm 1622nm 1656nm

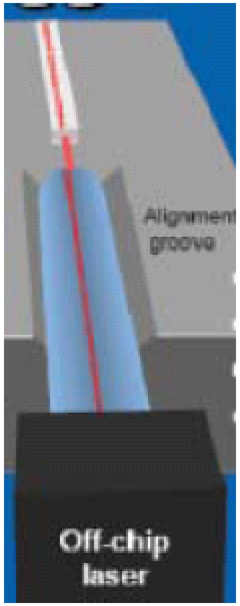
Rodolfo E. Camacho-Aguilera, et al. Opt. Express **20**, 11316-11320 (2012)

Laser on silicon



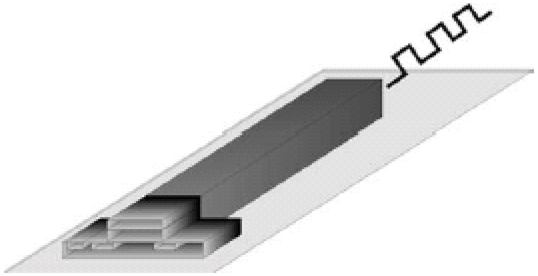
Attached laser
Tight alignment tolerances
Gold metal bonding
Expensive

Off-chip laser
Fiber attachement & alignment
High coupling losses
Very expensive
Non-integrated

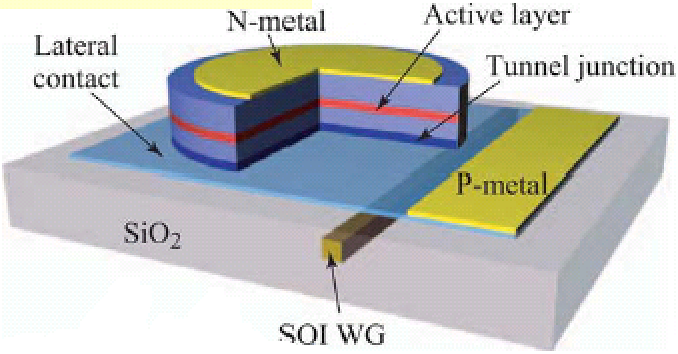


Monolithic laser Si compatible
Not any alignments
Highly integrable
Low cost
Electronic-photonic integration

Hybrid integrated laser
InP bonded laser to SOI CMOS
No alignment
Possibly to integrate
Moderate cost

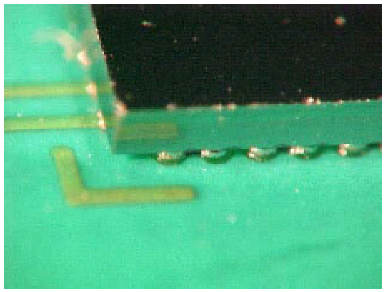


courtesy: Blas Garrido



III-V integration on silicon

- There are several ways to integrate III-V on SOI
  - Flip-chip integration of opto-electronic components



☺ most rugged technology
☺ testing of opto-electronic components in advance
☹ slow sequential process (alignment accuracy)
☹ low density of integration

  - Hetero-epitaxial growth of III-V on silicon

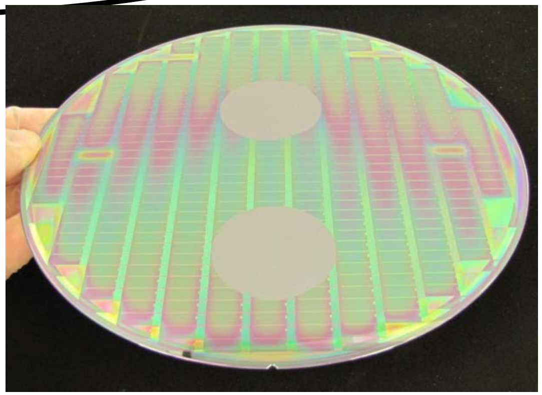
☺ collective process, high density of integration
☹ mismatch in lattice constant, CTE, polar/non-polar
☹ contamination and temperature budget

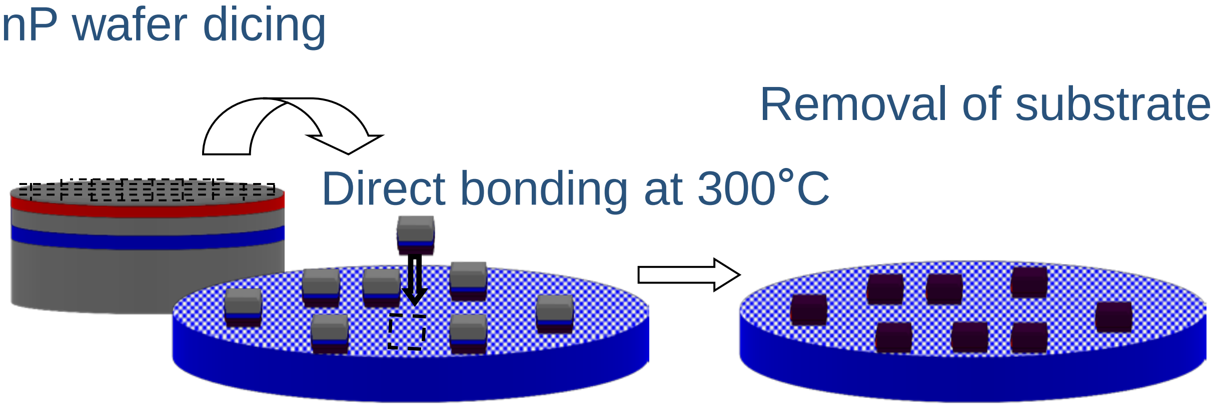
  - Bonding of III-V epitaxial layers

☺ sequential but fast integration process
☺ high density of integration, collective processing
☺ high quality epitaxial III-V layers

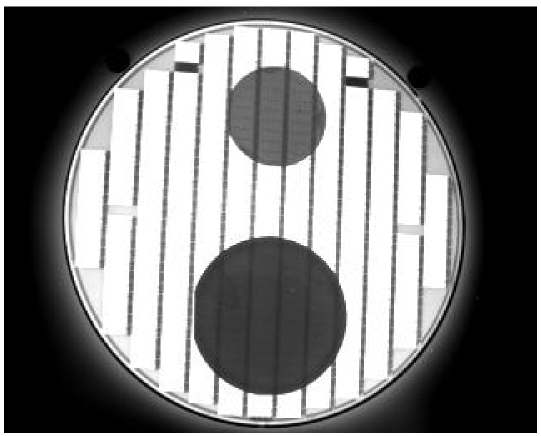
courtesy:GuntherRoelkens

Direct bonding of InP on structured SOI

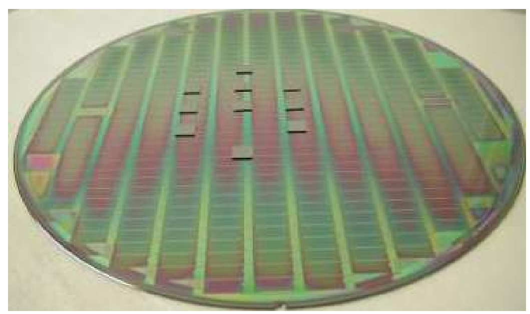


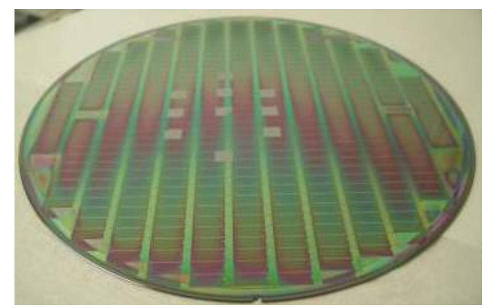


Optical image after substrate removal



IR image after bonding

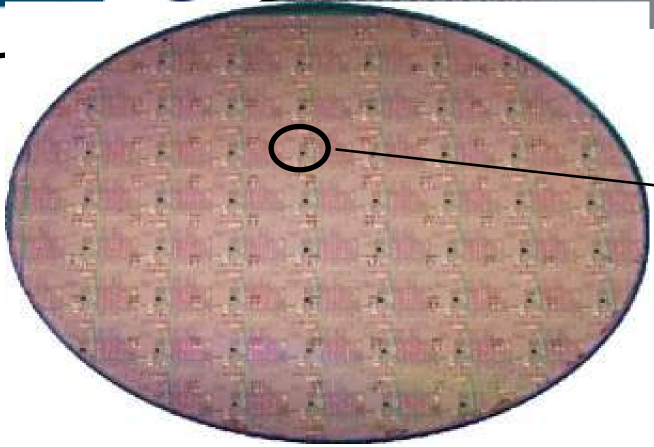


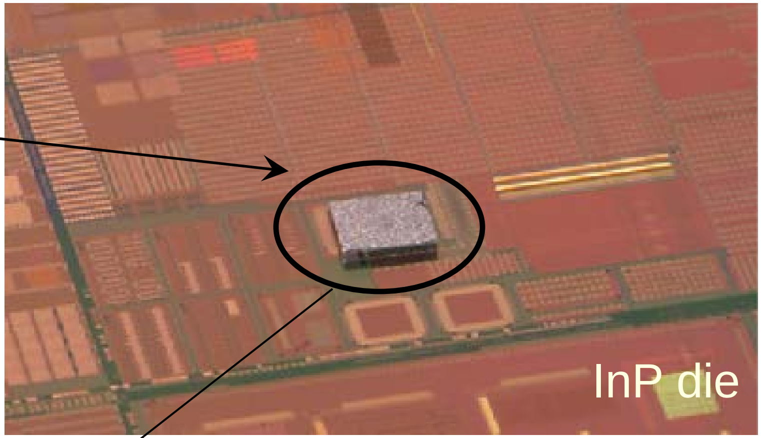


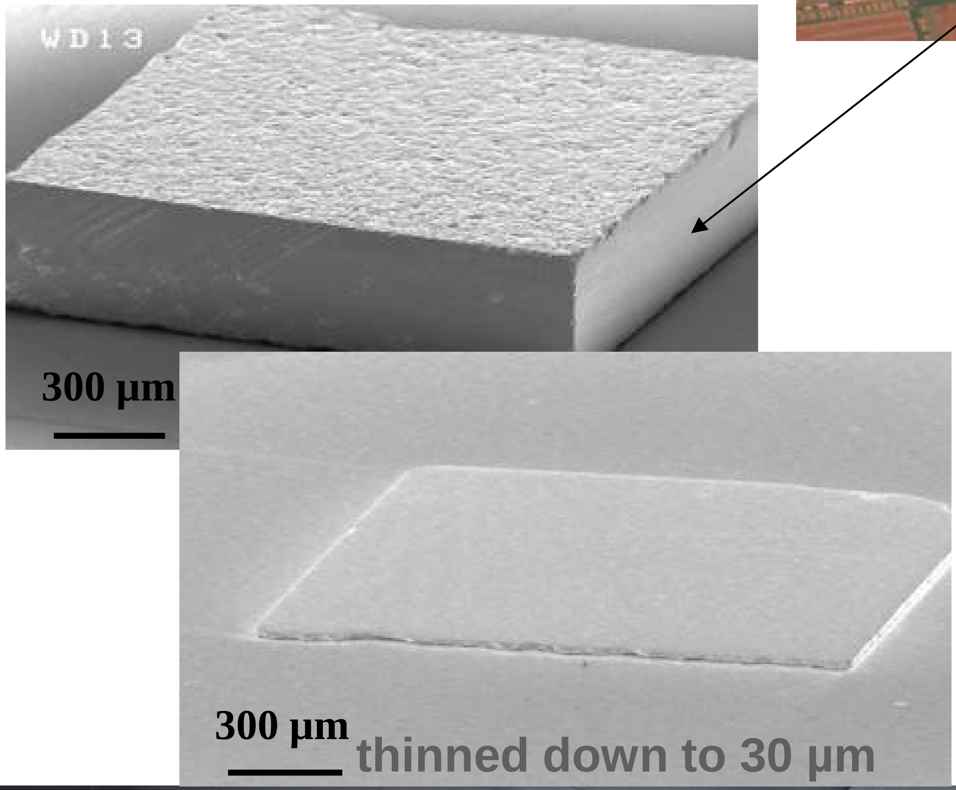
R&D use

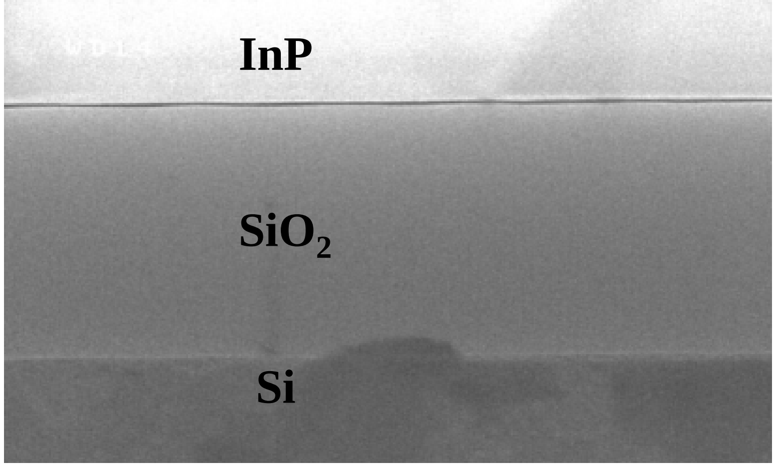
Industrial process

InP dies bonded on an EIC wafer



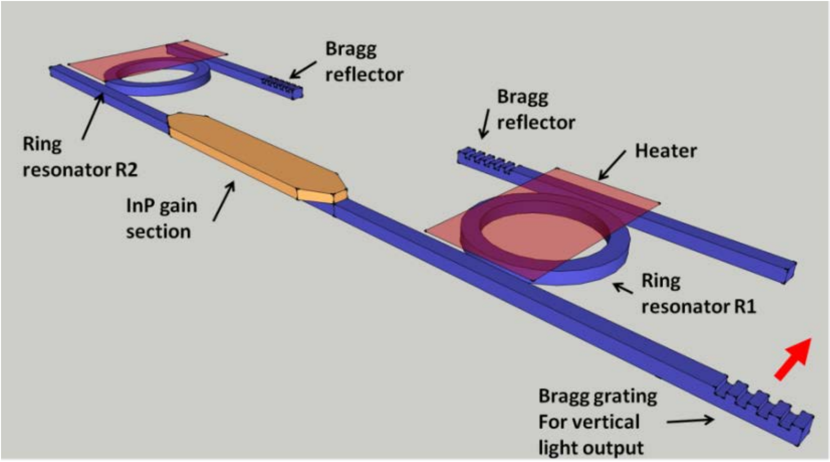


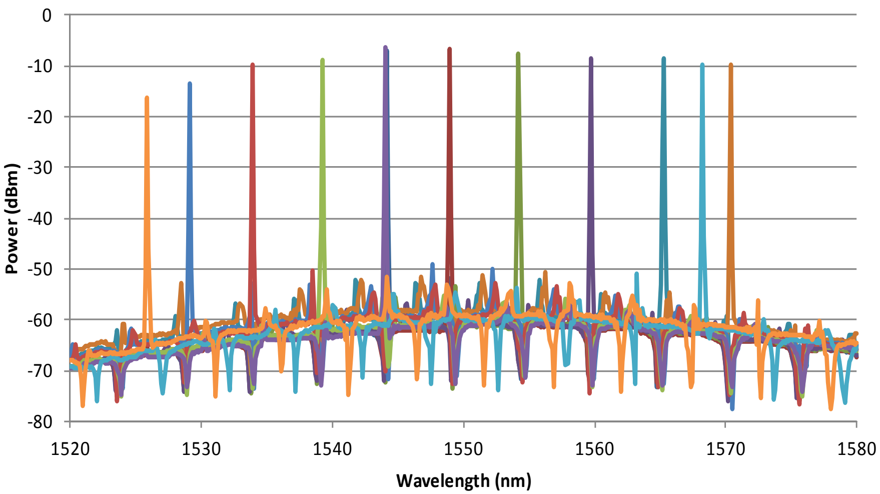




Bonding interface

courtesy: J-M Fédéli and L. Fulbert





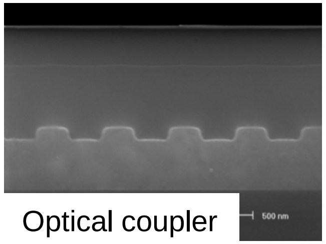
- 20 mA threshold at room temperature
- >45dB SMSR, tuning range 45nm

III-V lab

courtesy: G.H. Duan

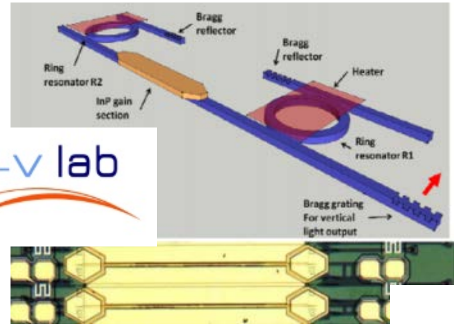
Silicon photonic building blocks

Off-chip III-V laser



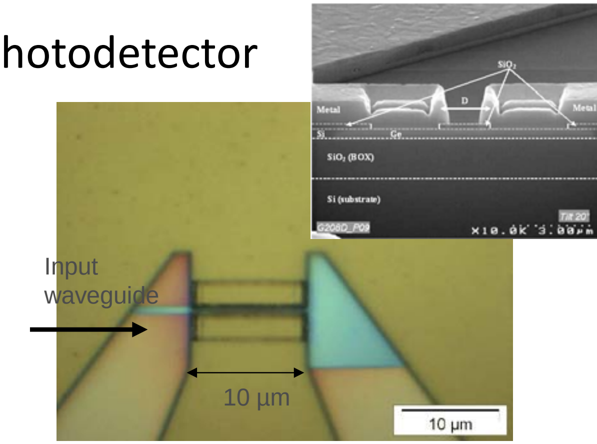
Optical coupler

On-chip III-V laser on Si



Germanium-based laser

photodetector

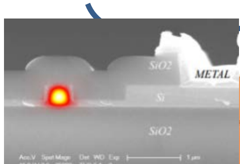


Emitter

Laser — Modulator

Receiver

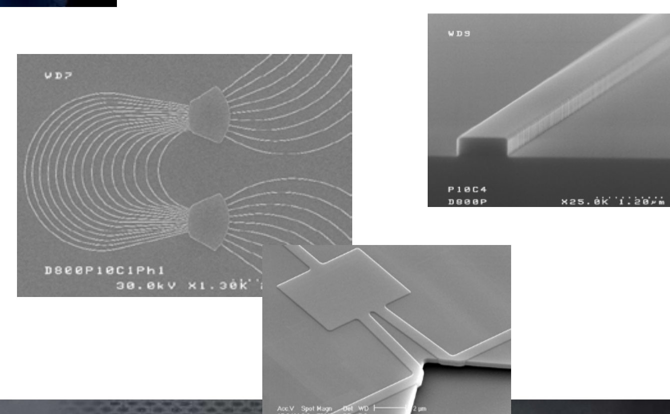
Detector



Si modulator

Bonded III-V EAM on Si

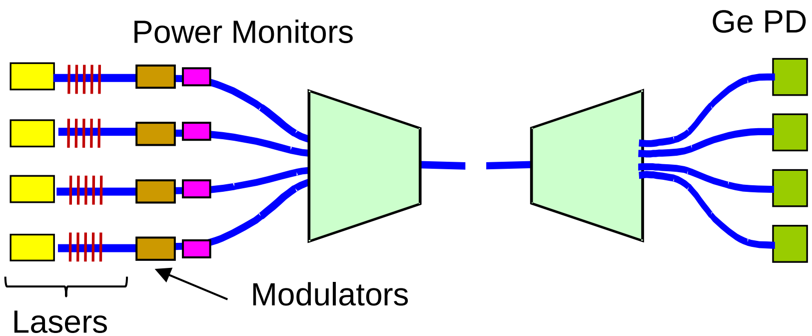
Ge-based modulator

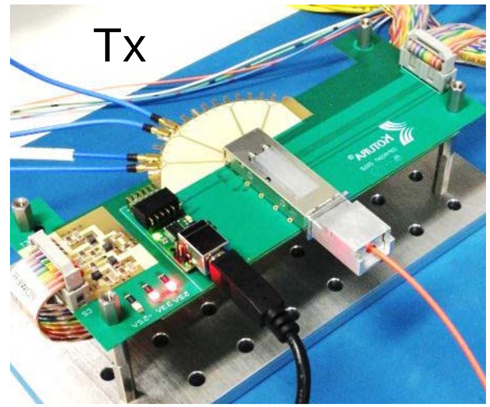


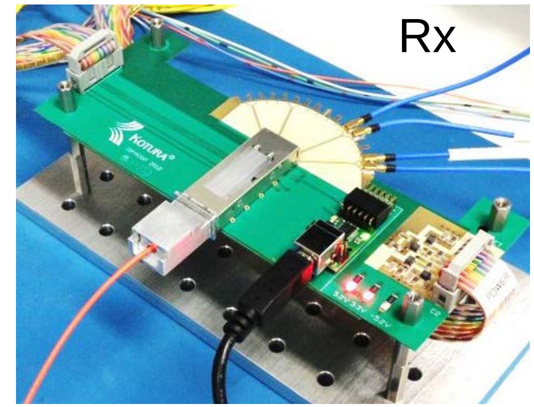
Outline

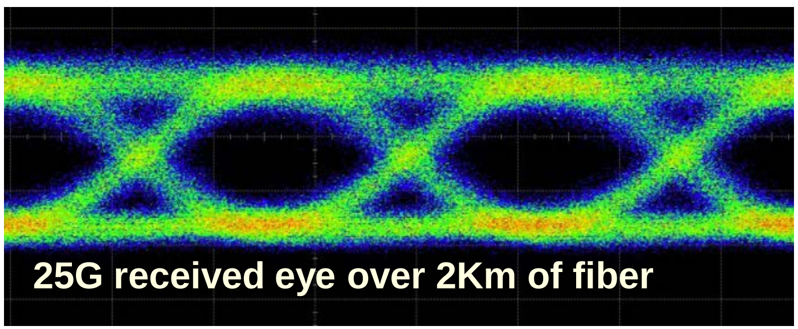
- Motivation
- Main building blocks in photonics
  - √ Light propagation
  - √ Optical modulation
  - √ Light detection
  - √ Light emission
    - ➢ The approaches
- Conclusion
  - √ Electronic-Photonic convergence
  - √ Silicon photonics: Ecosystem
  - √ Business

100GbE (4x25G) WDM in QSFP



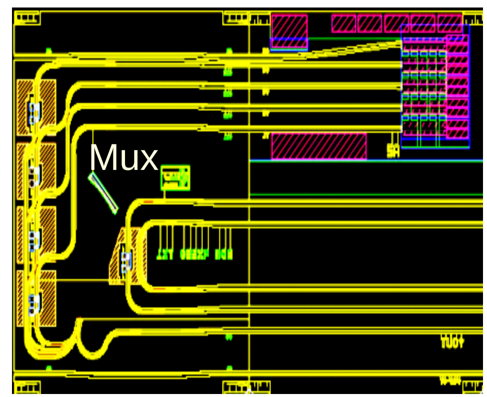


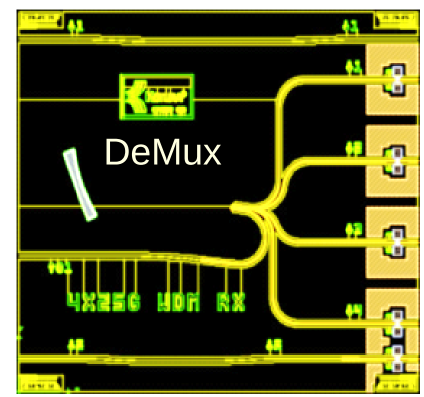




Laser bank

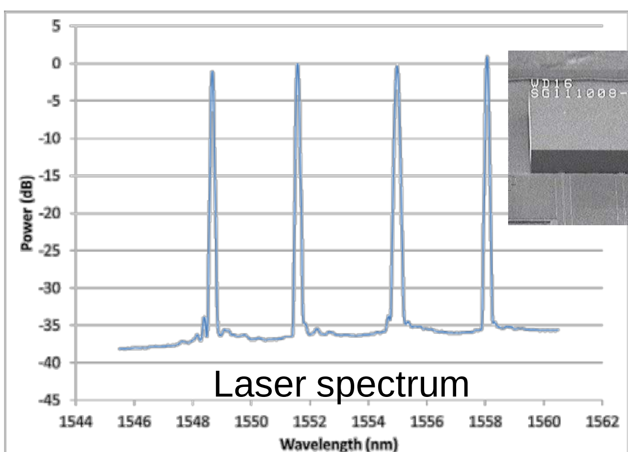
Modulators

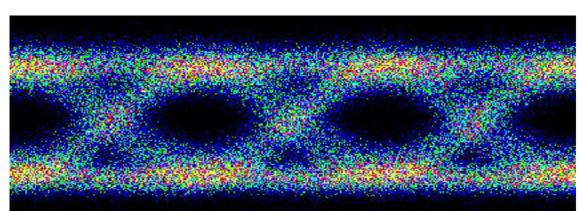




Ge PD bank

Quad Small Form-factor Pluggable



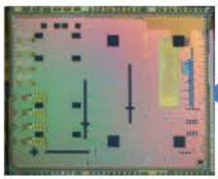


25G Transmit eye with low power drivers from **Oracle** (<70mW/ch)

Proposed Solutions for All Reaches

1310nm Parallel Solution

- 1 Laser
- 1 Chip
- Lowest cost at short reach
- Lowest power
- Ideal for short reach



0 to 30m: Active Optical Cable – Wavelength Agnostic

4x25G QSFP

Reach limited by deployment practicality of AOC, not by the optical transceiver

0 to 70m: Parallel Multi-Mode Fiber – 850nm to 1060nm

4x25G QSFP with MPO

0 to 1000m: Parallel Single Mode Fiber – 1310nm

4x25G QSFP with MPO

Longer Reach Possible

Embedded Optics with MPO

1310 nm WDM Solution

- 4 Lasers
- 1 Chip
- Lowest cost at long reach
- Reuse fiber plant
- Ideal for long reach

0 to 2000m: WDM Single Mode Fiber – 1310nm

4x25G QSFP with LC

Longer Reach Possible

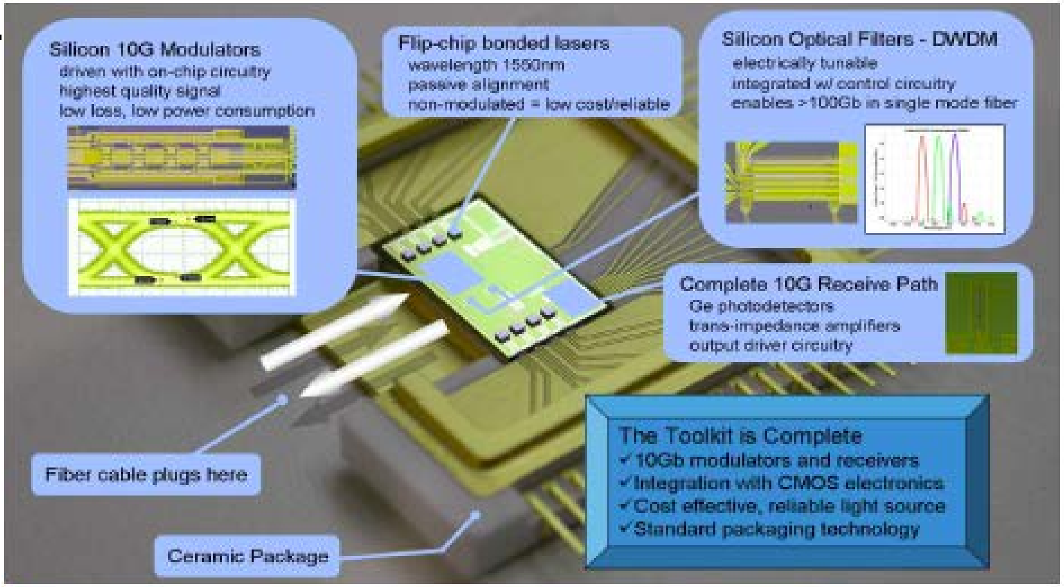
Embedded Optics with LC

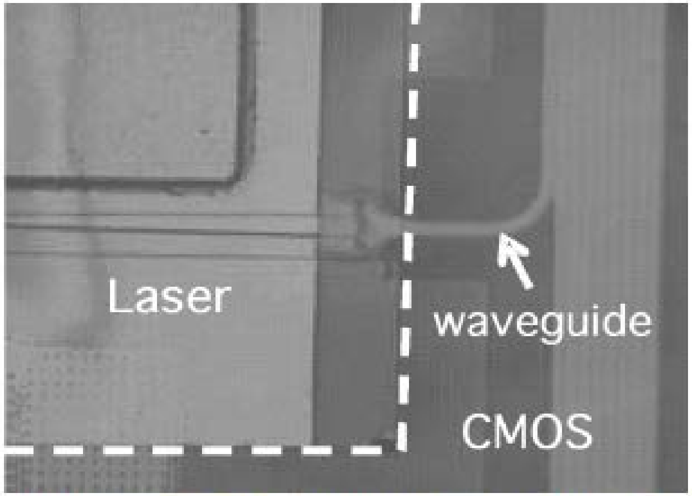
0 to 10,000m: WDM Single Mode Fiber – 1310nm

4x25G QSFP with LC

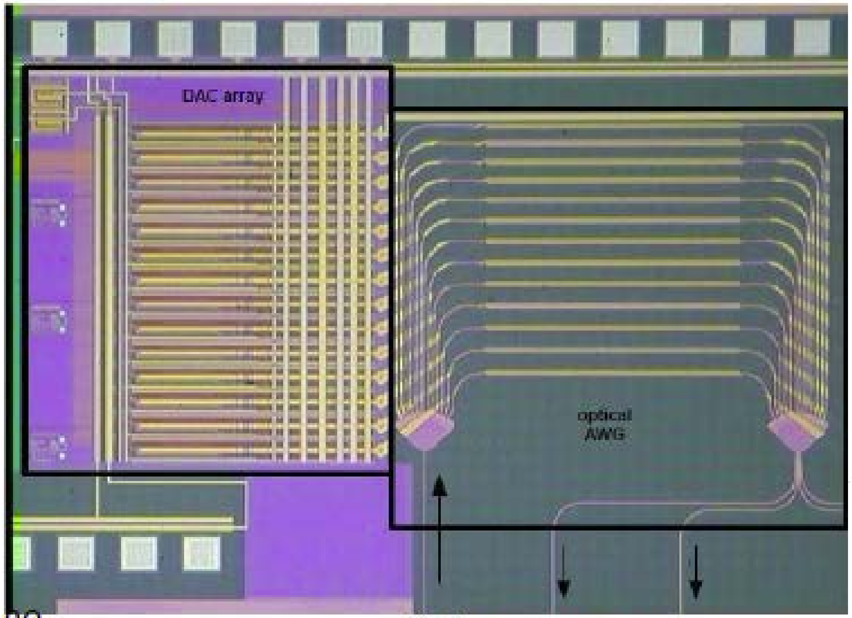
Embedded Optics with LC

Luxtera's 4 x 10 Gb/s Si Transceivers

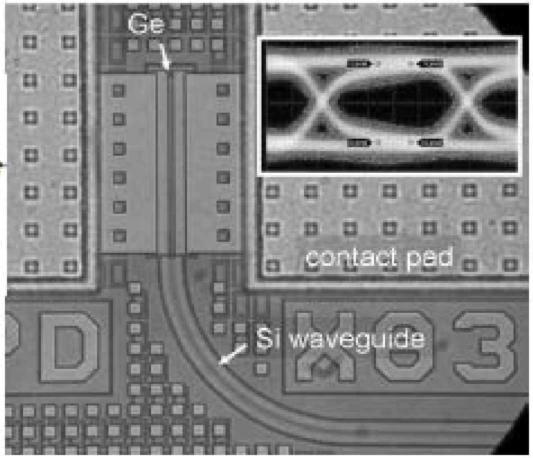




Top view of a flip-chipped laser on top of a CMOS die. The laser die is outlined by the dashed white lines.



A. Huang *et al.*, 2006 ISSCC



Germanium photodetector integrated into CMOS, shown with 10-Gbps eye

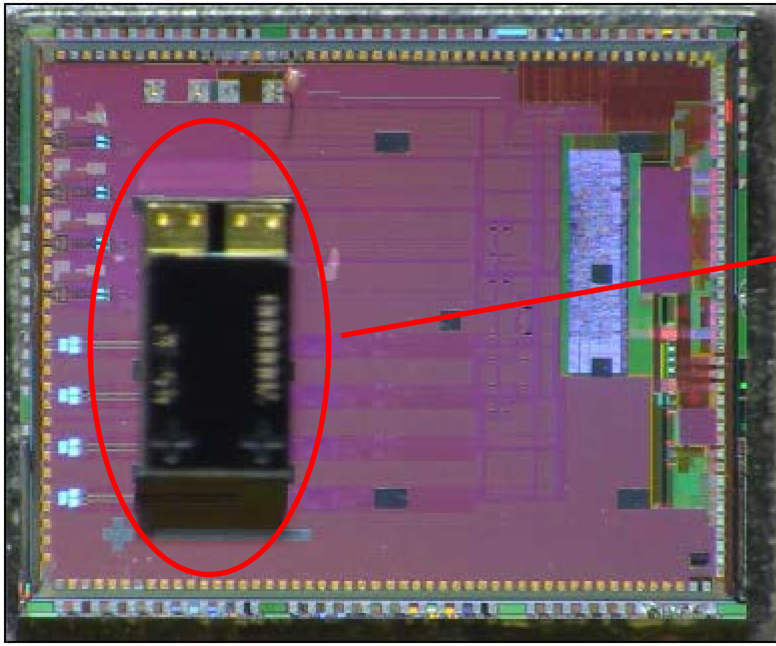
80

calibration light in

light out (more taps to the right)

Sasan Fathpour, CREOL

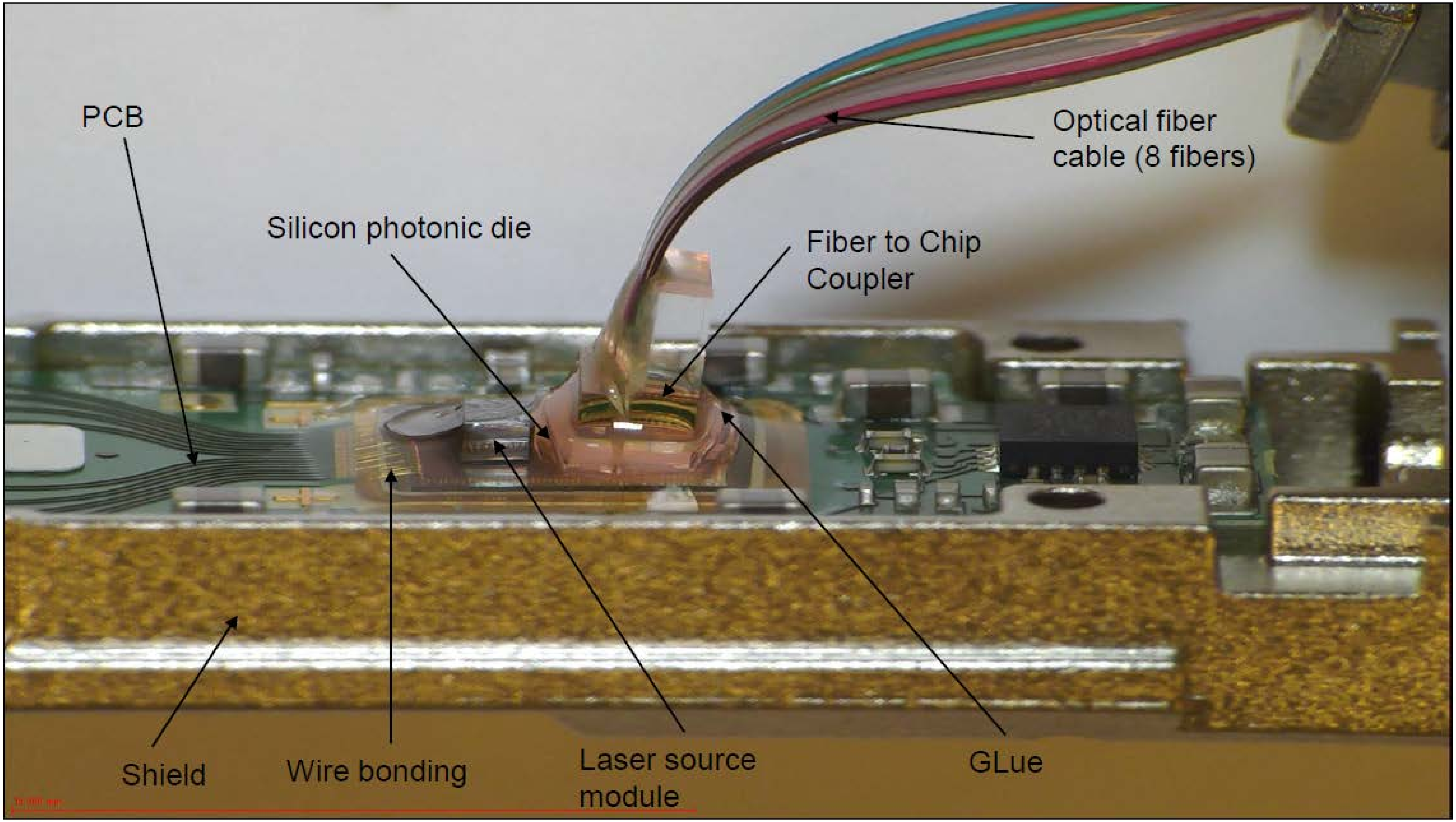
Molex' AOC with Luxtera Si Photonic Die



Silicon Photonic die

MEMS Laser Source

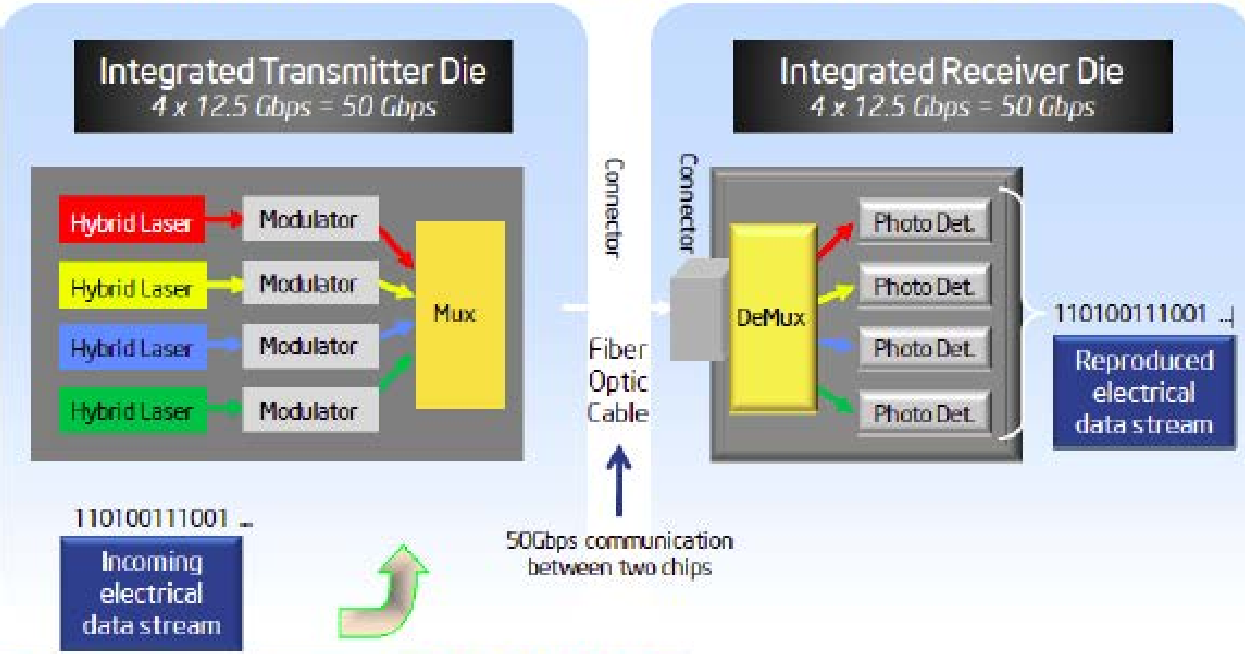
Fiber coupling



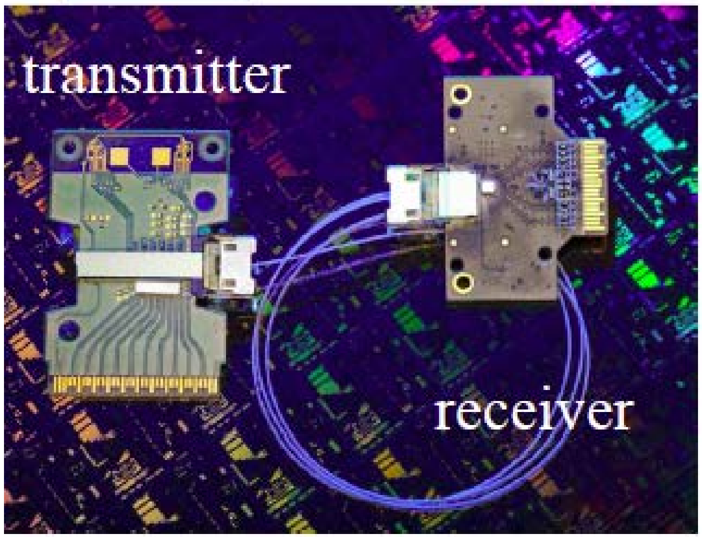
SYSTEMPlus CONSULTING

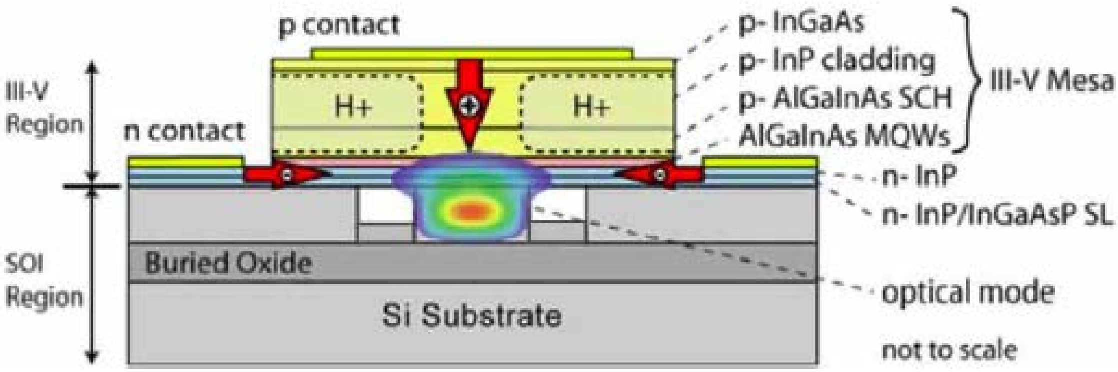
Optical fiber couplage – tilted view

Intel's 4 x 12.5 Gb/s Silicon Photonics Link



InP laser evanescently coupled into a Si WG





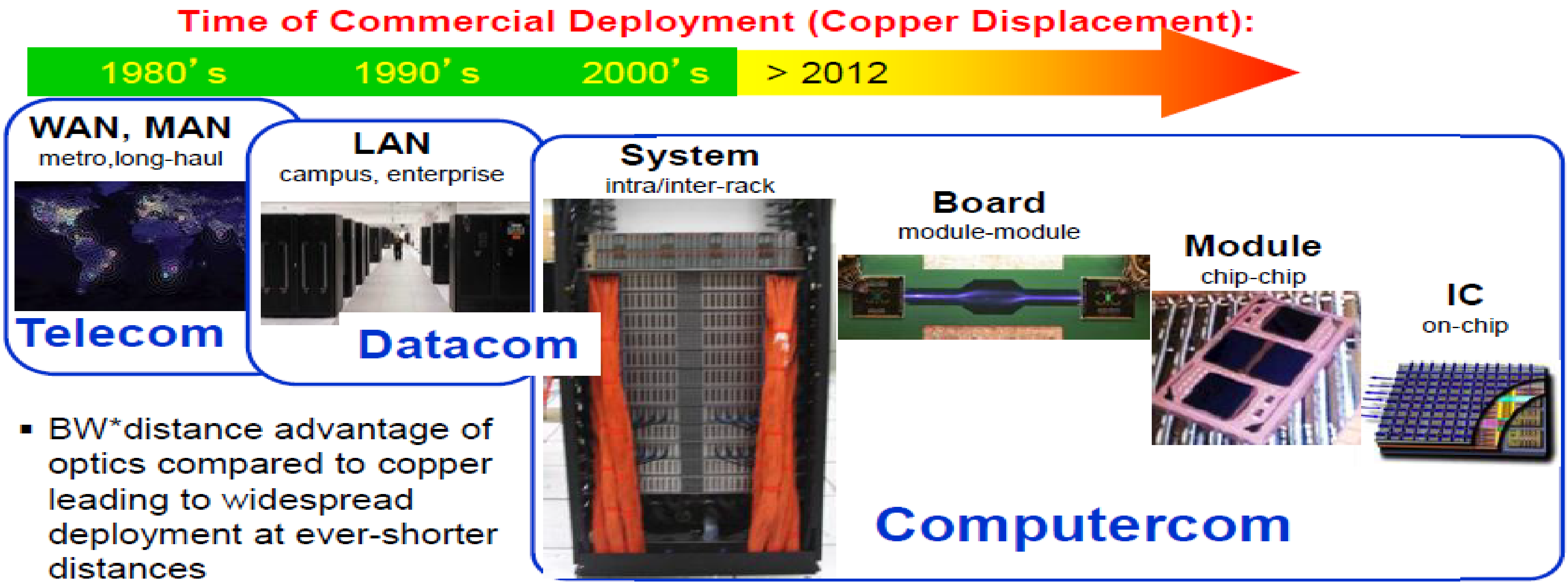
White Paper, Intel Labs, July 2010

W. Fang *et al.*, Opt. Express **14**, 9203-9210 (2006)

Evolution of optical interconnect

Evolution of Optical interconnects

IBM

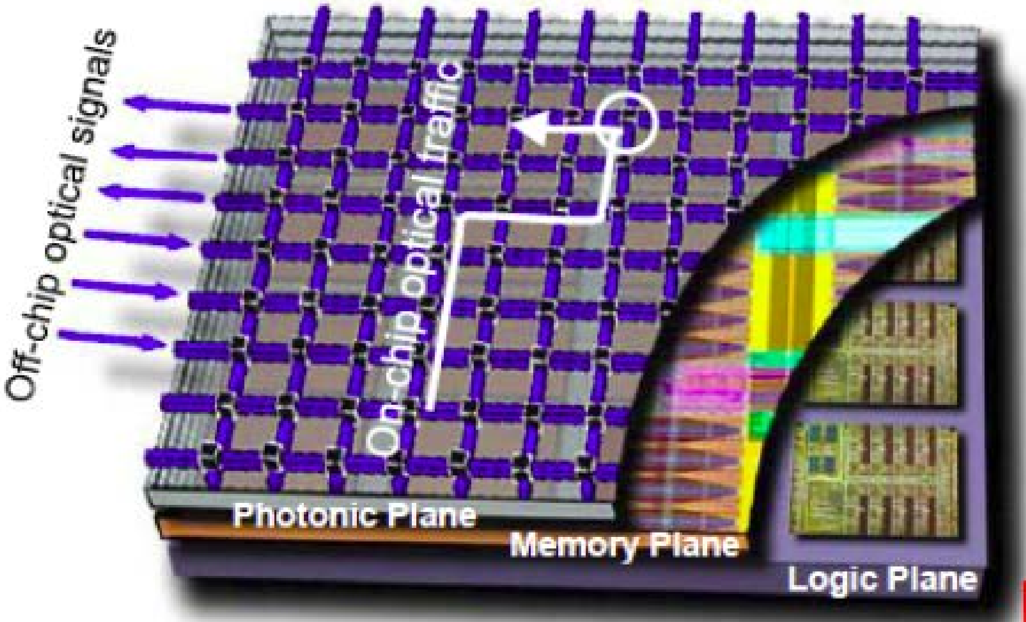


- BW*distance advantage of optics compared to copper leading to widespread deployment at ever-shorter distances
- As distances go down the number of links goes up putting pressure on power efficiency, density and cost

Increasing integration of Optics with
decreasing cost, decreasing power, increasing density

2020	1mW/Gb/s	$0.025/Gb/s

Vision for 2020 – Optically connected 3-D Supercomputer Chip



- 36 "Cell" 3-D chip
- Silicon photonics layer integrated with high performance logic and memory layers
- Layers separately optimized for performance and yield

Logic plane	~300 cores, ~5TF (36 "supercores")
Memory plane	~30GB eDRAM
Photonic plane	On-Chip Optical Network >20 Tbps (bidirectional) optical on-chip (between supercores) >20 Tbps optical off-chip

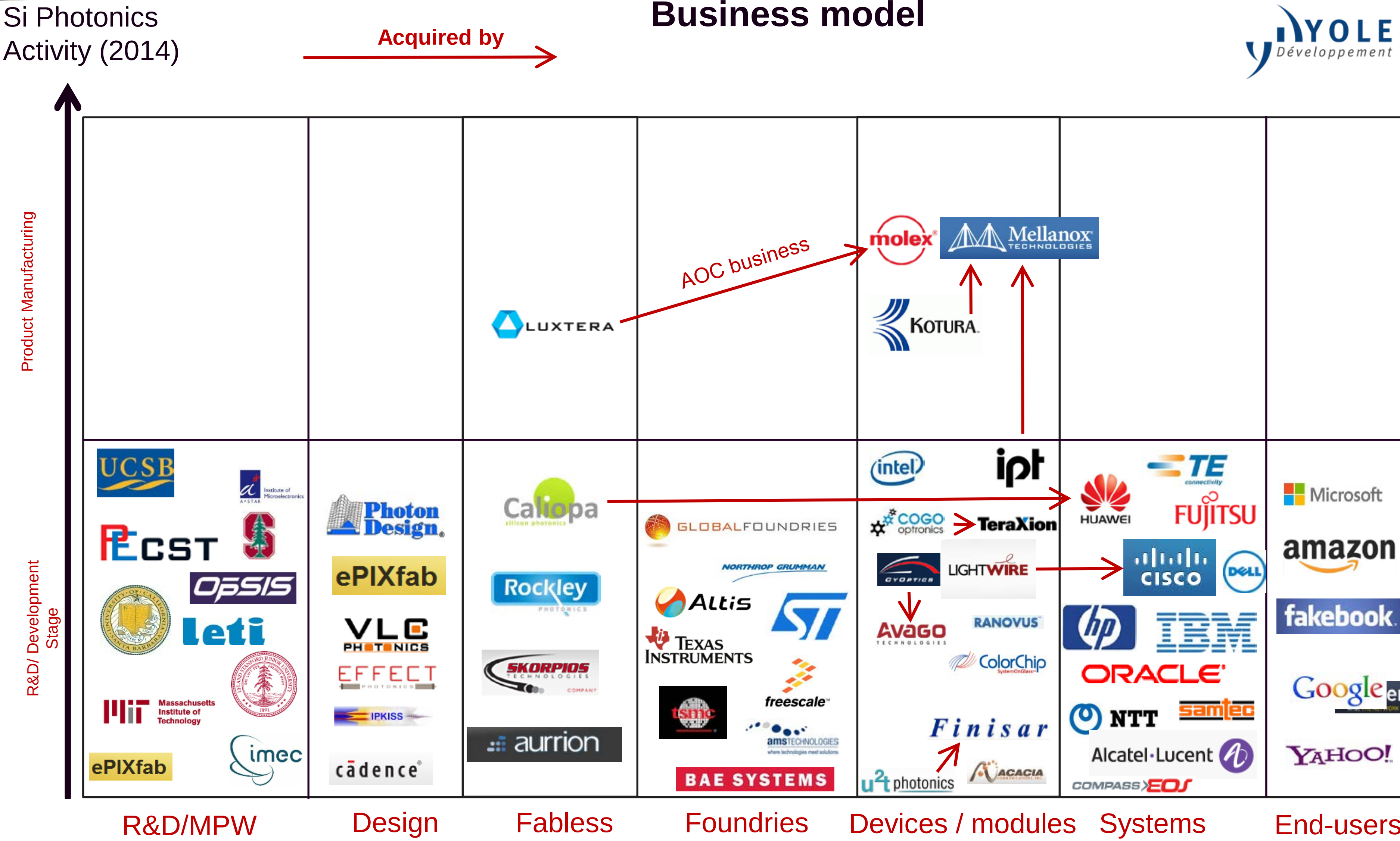
Photonic layer not only connects the multiple cores, but also routes the traffic

System level study:
IBM, Columbia, Cornell, UCSB

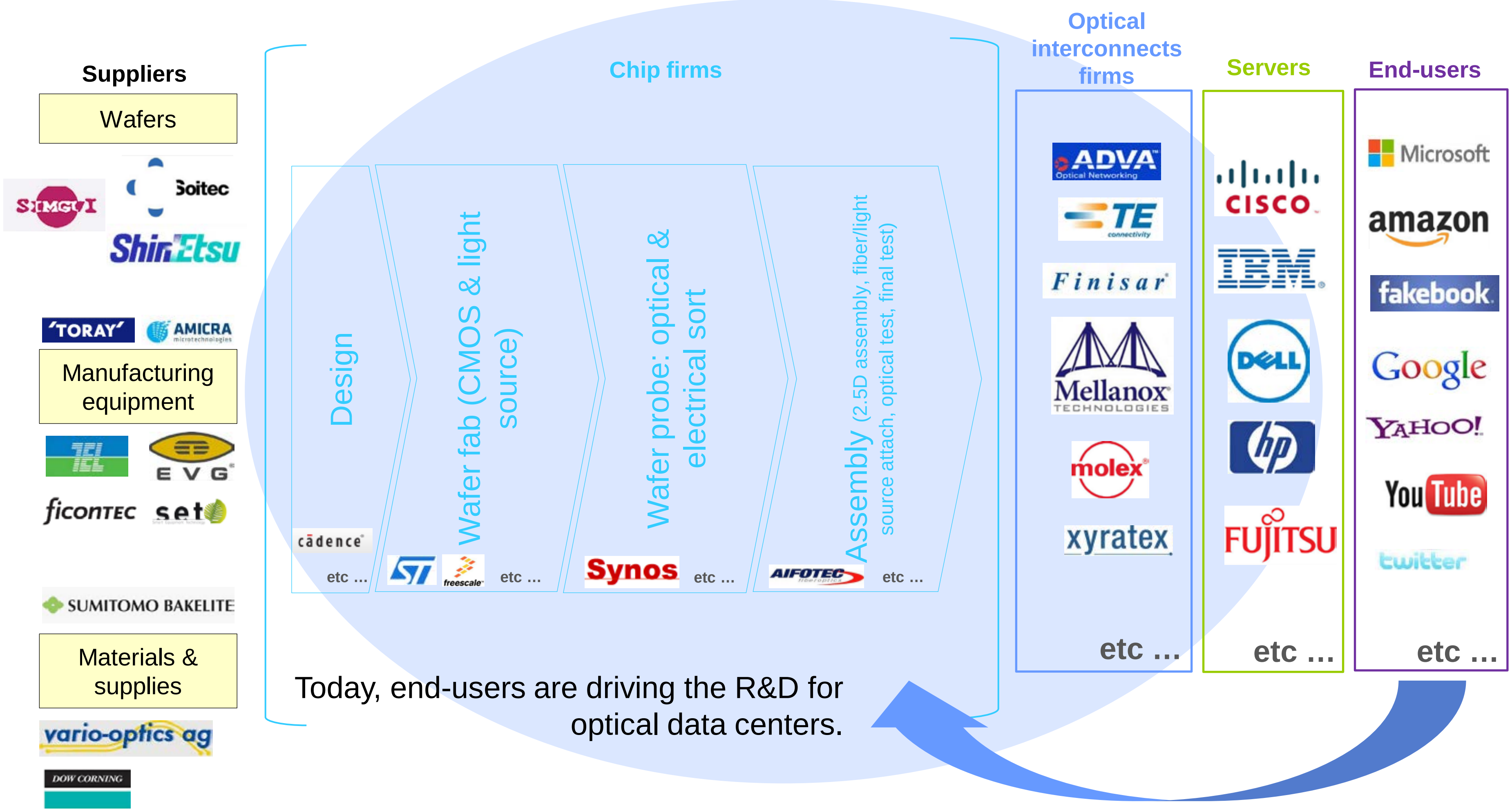
Courtesy of Jeff Kash

Business model

Si Photonics Activity (2014)



The Si Photonic supply chain



More than $1B invested worldwide by public fundings !

- **Strong investment from the European Commission**

  ✓ In the period 2002–2006, around **50 photonics research projects** were funded under the EU's 6th research framework program (FP6) for approximately **€130 million**.

  ✓ Since the beginning of FP7, **65 R&D photonic projects**, including organic photonics, have been selected so far with more than **€300 million** of EU funding.

  ⇒ **A total of €430 million invested by the European Commission e.g. US$ 580M**

- **Japan : JISSO program**
  ✓ $300M invested in 10 years

- **US : mainly DARPA programs**
  ✓ A $44M DARPA program involving Kotura, Oracle, Luxtera, various Universities (Stanford, San Diego)
  ✓ Orion also has a big program

Almost $1B transactions for photonics in datacenter!

Company	Date	Product	Transaction value	Acquirer	Rationale for transaction
Lightwire (US)	February 2010	Silicon CMOS optoelectronics interconnects / optical transceivers.	**US$271M**	**Cisco** (US)	To face with increasing traffic in data centers / service providers
Luxtera AOC line (US)	January 2011	AOC line	**US$20M**	**Molex** (US)	Luxtera may be changing strategy to become an IP licensing company. Molex had AOC product line for 12-channel AOCs with a product from Furukawa/Fitel based on a 1060nm InGaAs VCSEL.
COGO Optronics (CAN)	March 2013	InP modulators & lasers.	**Est. < $30M**	**TeraXion** (CAN)	To access 100Gb InP modulator technology.
Cyoptics (US)	April 2013	InP-based photonic components.	**US$400M**	**Avago** (US)	To strengthen products portfolio for 40Gb & 100Gb data centers applications.
Kotura (US)	May 2013	Si photonics & VOAs for data center.	**$82M**	**Mellanox** (US)	To access 100Gb optical engine for data centers.
IPTronics (US)	June 2013	IC for parallel optical interconnects (drivers).	**$47M**	**Mellanox** (US)	To access products / technologies for 100Gb optical engine.
Caliopa (BE)	September 2013	Si-based optical transceivers for datacoms.	**$20M**	**Huawei** (CHINA)	To develop European-based R&D in Si photonics.

TOTAL: ~US$900M
Est. 2013 Market < US$30M

AIM photonics

≈ 600 M$

Membership Status

Government

Department of Defense · Department of the Army · Department of the Air Force · Department of the Navy

NSF · NIST

Department of Energy · NASA

New York State

California State

Arizona State

Massachusetts State

Industry

Initial Emphasis

Tier 1

intel · United Technologies · GE · infinera

IBM · GLOBALFOUNDRIES · hp · cisco

ACACIA COMMUNICATIONS, INC.

LOCKHEED MARTIN · cadence

SYNOPSYS

Raytheon · Mentor Graphics

Tier 2

CORNING · aurrion · TE connectivity · IQE · LGS INNOVATIONS

Tier 3

4D · HARRIS · BOEING · Nistica · KEYSIGHT TECHNOLOGIES

NORTHROP GRUMMAN · samtec · AnalogPhotonics

NEAT

Photonics · Rockwell Collins · Adarza BioSystems · OPTIMAX · OptiPro · PHOTONICS

SYDOR OPTICS · JUNIPER NETWORKS · TEXAS INSTRUMENTS · NAVITAR · FREEDOM PHOTONICS · LaserMax · Micron · NEW SCALE TECHNOLOGIES Ingeniously small motion systems · Chiral Photonics

Academic

Tier 1

SUNY POLYTECHNIC INSTITUTE · UCSB · MIT Massachusetts Institute of Technology · COLUMBIA UNIVERSITY

UC DAVIS UNIVERSITY OF CALIFORNIA · RIT · UNIVERSITY of ROCHESTER · THE UNIVERSITY OF ARIZONA.

Tier 2

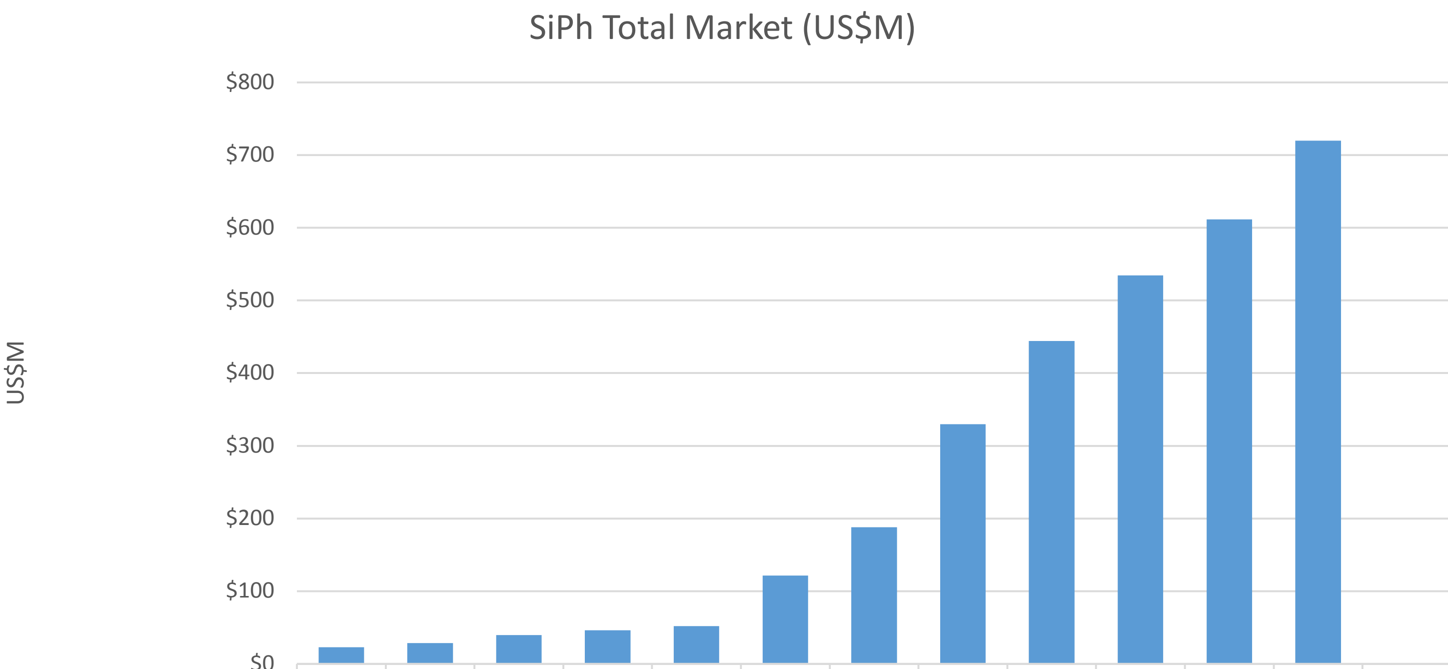
University of Delaware · Berkeley · UC San Diego

Caltech · BOSTON UNIVERSITY · University of Colorado

STANFORD UNIVERSITY · UNIVERSITY of VIRGINIA

- All Industry and Academic Tier 1 Members and potential Tier 1's received the Membership Agreement in October
- Feedback gathering /discussion/revision continue
- Targeting execution of Membership Agreements beginning by the EOY

Silicon photonics 2013-2014 market forecast in US$M



	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	CAGR
SiPh Total Market (US$M)	$23	$29	$39	$46	$52	$122	$188	$330	$444	$535	$612	$720	38%

- Silicon photonics devices market will grow from less than US$25M in 2013 to more than US$700M in 2024 with a 38% CAGR.
  - √ Emerging optical data centers from big Internet companies (Google, Facebook …) will be triggering the market growth in 2018 (see following slides).

A broad range of application

SEMICONDUCTOR ENGINEERING

Home > **Low Power-High Performance** > Photonics Moves Closer To Chip

LOW POWER-HIGH PERFORMANCE

Photonics Moves Closer To Chip

20 211 38

Government, private funding ramps up as semiconductor industry looks for faster low-power solutions.

JUNE 20TH, 2016 - BY: **ED SPERLING**

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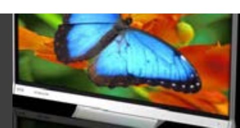
Sensor applications



Home wiring and Consumer Applications

In-cabinet communication

Acknowledgments

- Eric Cassan – Univ. Paris Sud
- Delphine Marris-Morini – Univ. Paris Sud

- Jean Louis Malinge – Ex CEO of KOTURA (USA)

- References
  - √ Handbook of Silicon Photonics – CRC Press
  - √ Yole report

  - √ Few figures, slides, illustrations provided from International school presentations: W. Bogaerts, G. Reed, L. Pavesi, J-M. Fédéli,

Acknowledgements: Funding and collaborations

National Research Agency

NANO2017-ST

NanoDesign
IDEX Paris-Saclay

COSMICC

CmOs Solutions for Mid-board Integrated transceivers with breakthrough Connectivity at ultra-low Cost

HELIOS

Photonics Electronics functional integration on CMOS

Plat4M

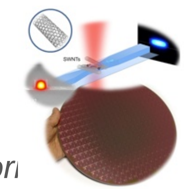
photonic libraries and technology for manufacturing

SASER

Safe and Secure European Routing

CARTOON

Carbon nanotube photonic devices on silicon



MIDEX

Mid refractive Index contrast Si photonics platforı

ERC Consolidator POPSTAR
grant agreement No 647342

ERC Starting InsPIRE
grant agreement No 647342

University of Tokyo