General Outline

- ✓ ULSI technologies: manufacturing
- ✓ Radiation effects in devices and technologies
- ✓ Radiation Hardness-By-Design (HBD) techniques for ASICs
- ✓ 130nm technology node for High Energy Physics: vendor, properties, radiation effects

Hardness-By-Design (HBD) techniques

Outline

- ✓ Foreword
- ✓ TID: Total Ionizing Dose
  - TID and scaling
  - Solutions
- ✓ SEEs: Single Event Effects
  - SEEs and scaling
  - Solutions
- ✓ Summary & Conclusion

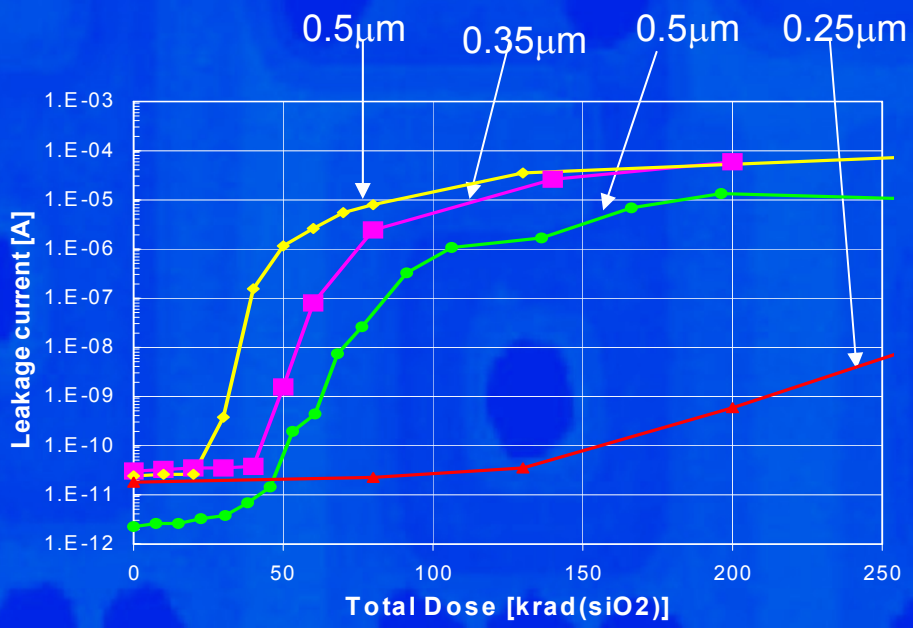
Foreword

- ✓ What we will be talking about:
  - ASICs (application-specific ICs)
  - CMOS technologies only
  - Effects: TID, SEU, SEL

  - How to conceive ASICs able of surviving to and functioning in a radiation environment

Is it a problem for me?

- ✓ Which TID can be considered as “safe”?
- ✓ Is there a dependence on design (logic vs analog, …)?
- ✓ Is there variability with time (different results for different production lots)?
- ✓ Is there a technological dependence on the TID tolerance?



Risk management

- ✓ As seen before, there are many variables influencing the final radiation hardness of an IC
- ✓ The “safer” the circuit is designed, the more “expensive” it is (area, performance, complexity, …)
- ✓ Risk reduction comes at some cost

- ✓ In the following, a procedure to RELIABLY designing radiation tolerant ASICs is presented. It reposes on physics, not on specific process recipes, hence it gives very predictable results.

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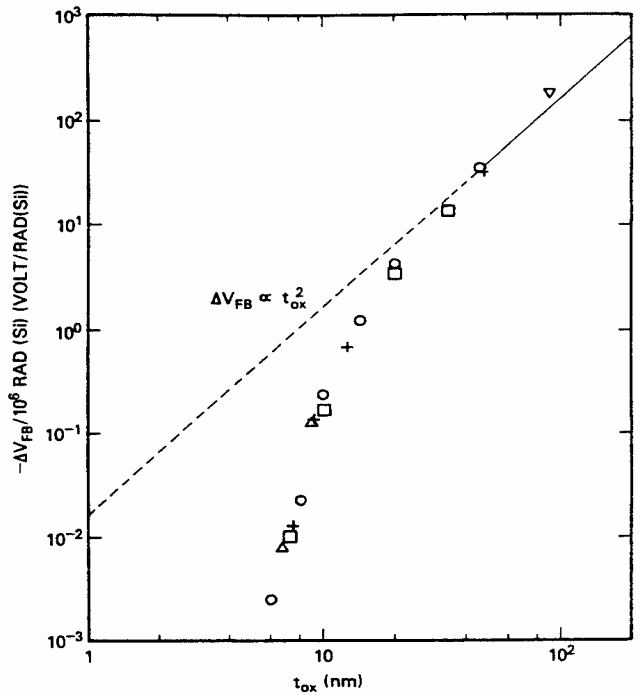
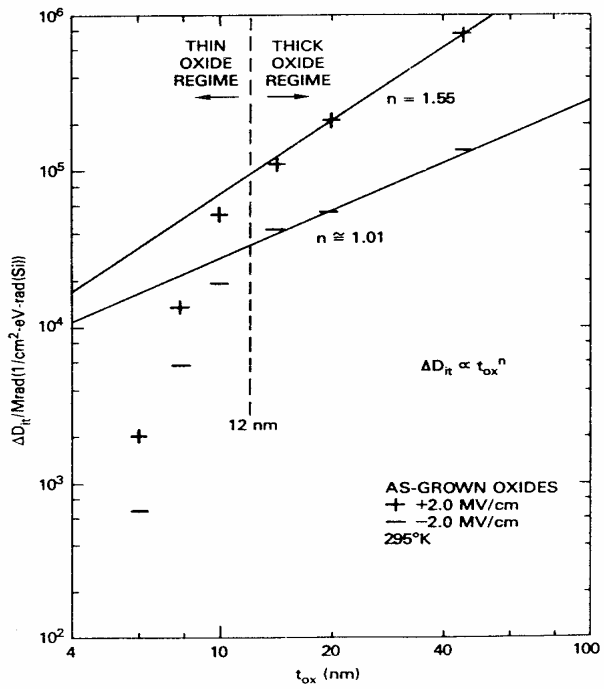
Radiation effects and t_{ox} scaling

Damage decreases with gate oxide thickness

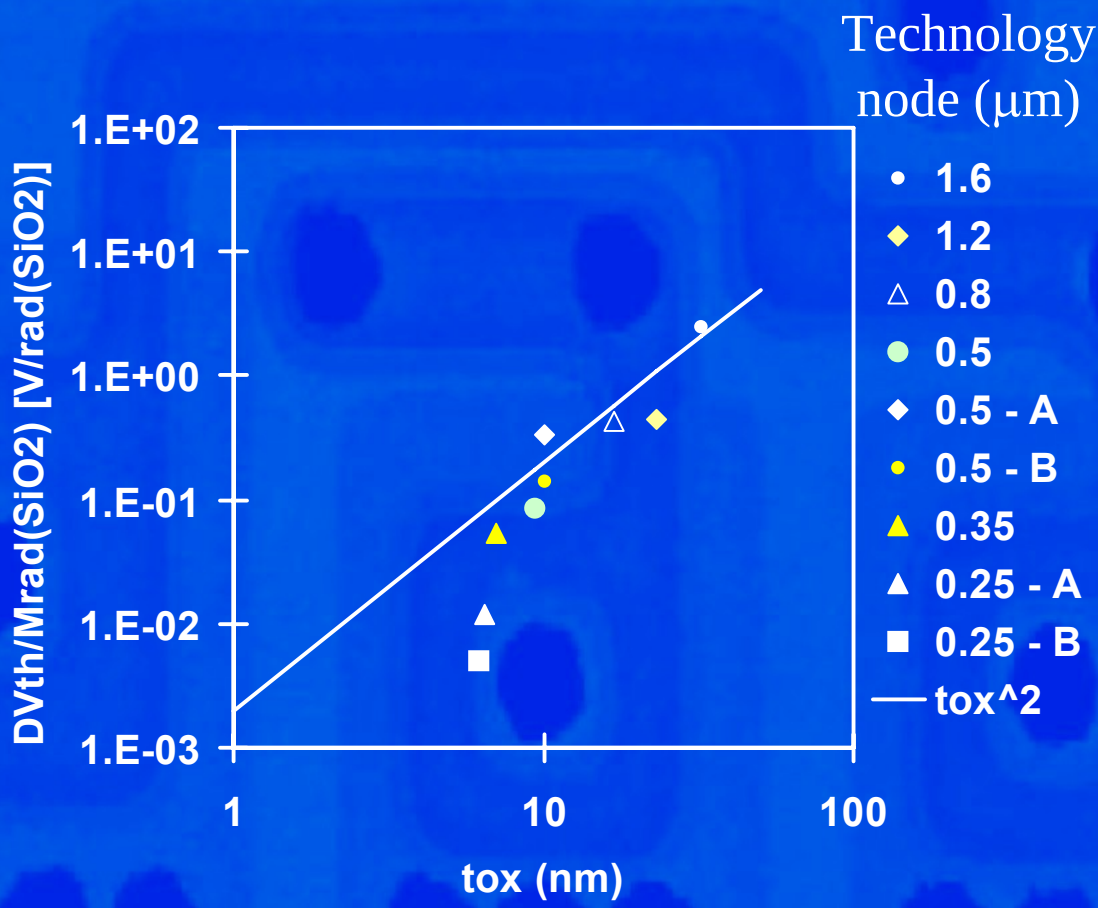




N.S. Saks et al., IEEE TNS, Dec. 1984 and Dec. 1986

Tendency confirmed

- ✓ Gate oxides in commercial CMOS technologies did follow the curve drawn by Saks and co-workers!



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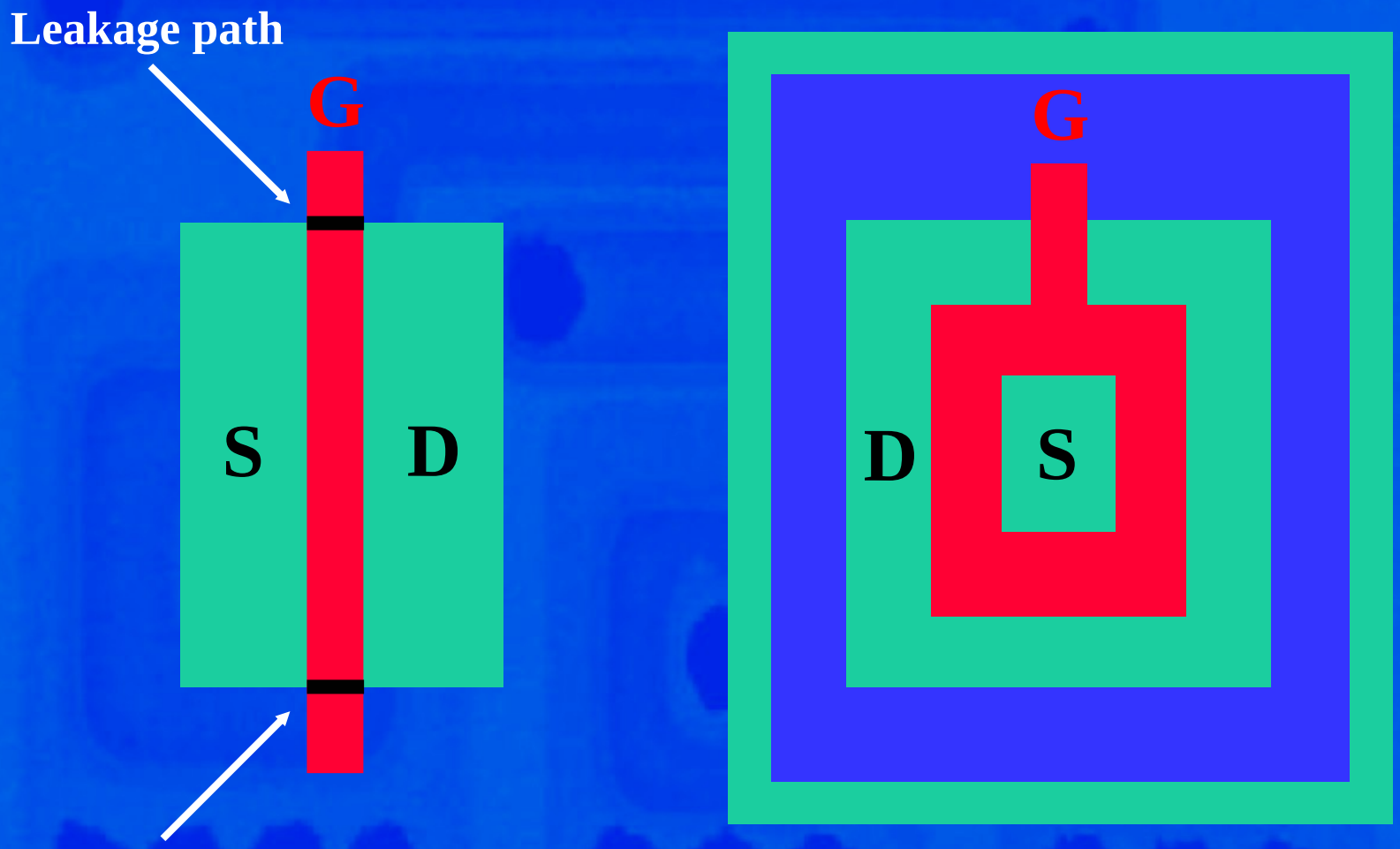
Radiation hard CMOS processes

- ✓ “Usual solution”: technology hardening
- ✓ TID hardness is guaranteed

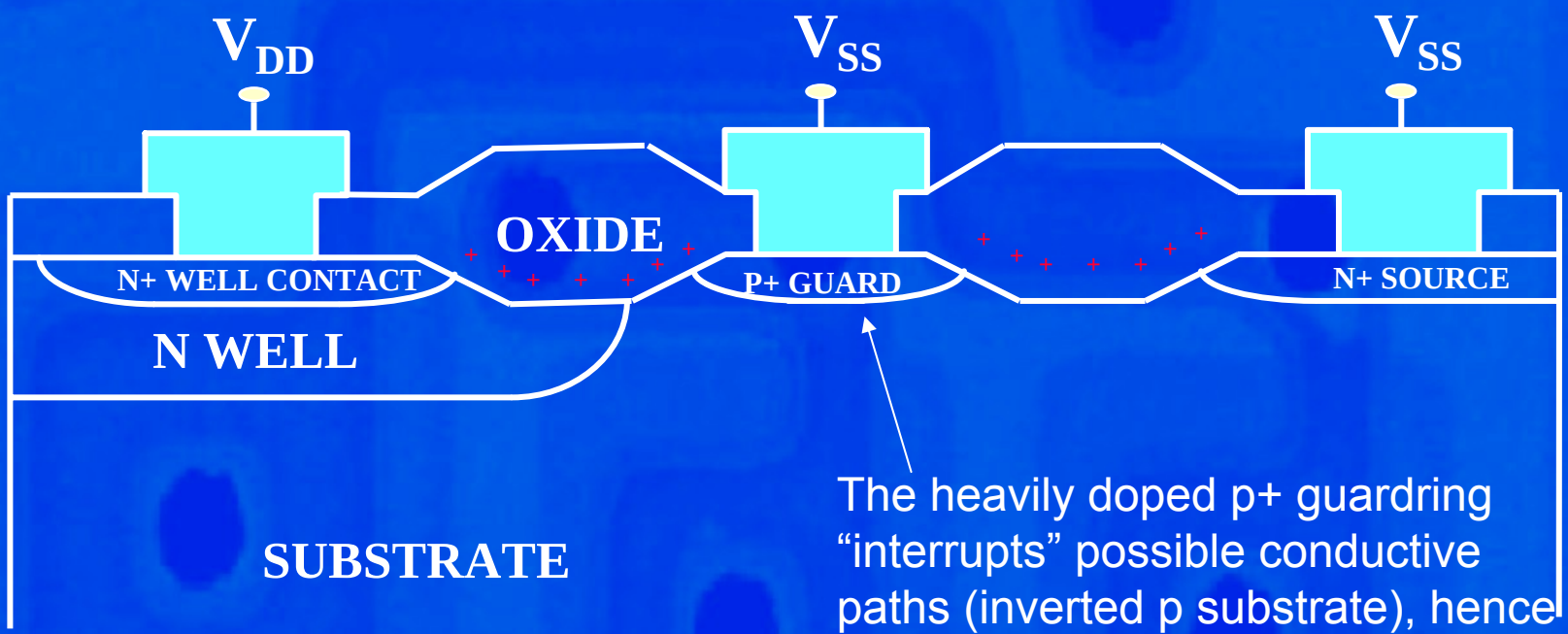
but

- ✓ Low volume in fabs => yield can be low, and unreliable radiation performance for large quantities
- ✓ Cost is very high
- ✓ Very limited number of processes still available today, and risk of unavailability in the long run
- ✓ Analog performance often not very good

Radiation-tolerant layout (ELT)



Function of the guardring

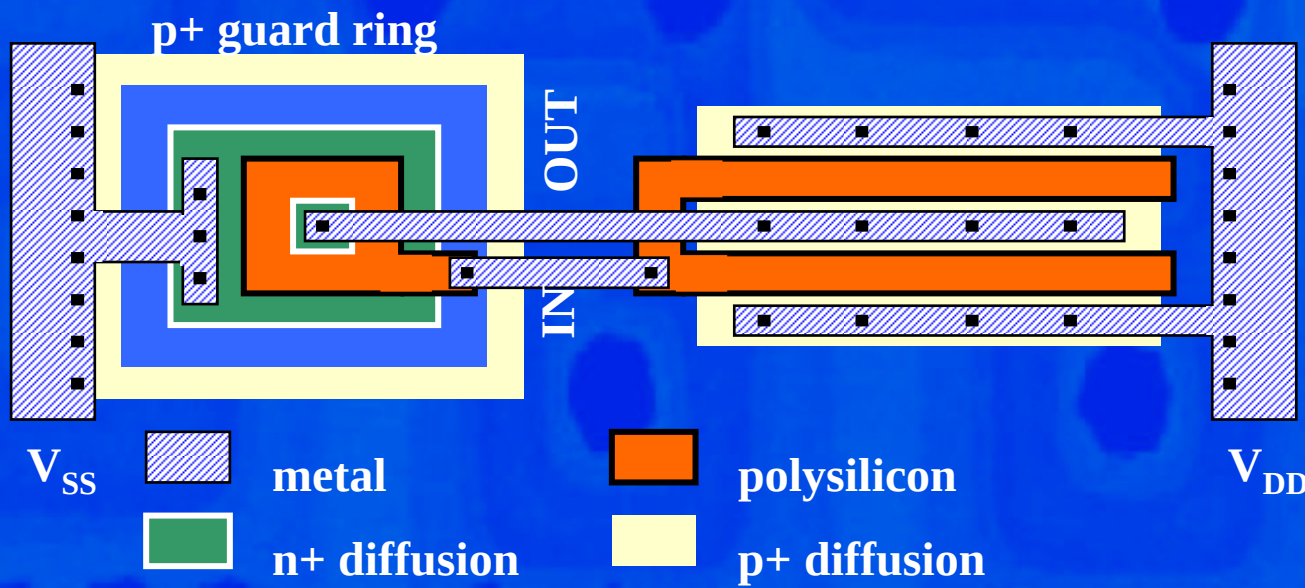


The heavily doped p+ guardring "interrupts" possible conductive paths (inverted p substrate), hence preventing inter-device leakage currents

Radiation tolerant approach

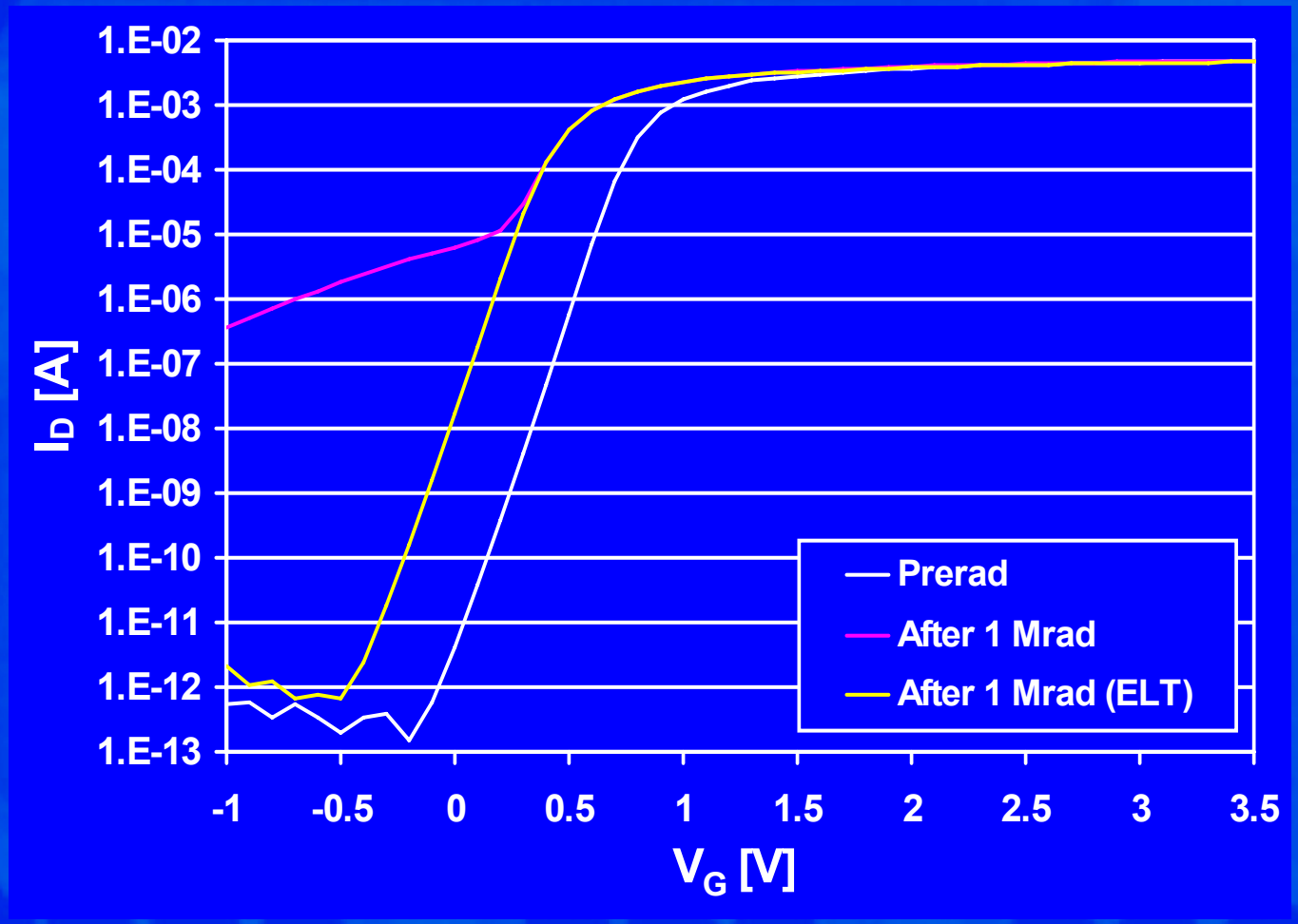
$$\Delta V_{th} \propto t_{ox}^{n} + \text{ELT's and guard rings} = \text{TID Radiation Tolerance}$$

Example layout for an inverter



Effectiveness of ELTs

0.7 μm technology - W/L = 2000/1.5



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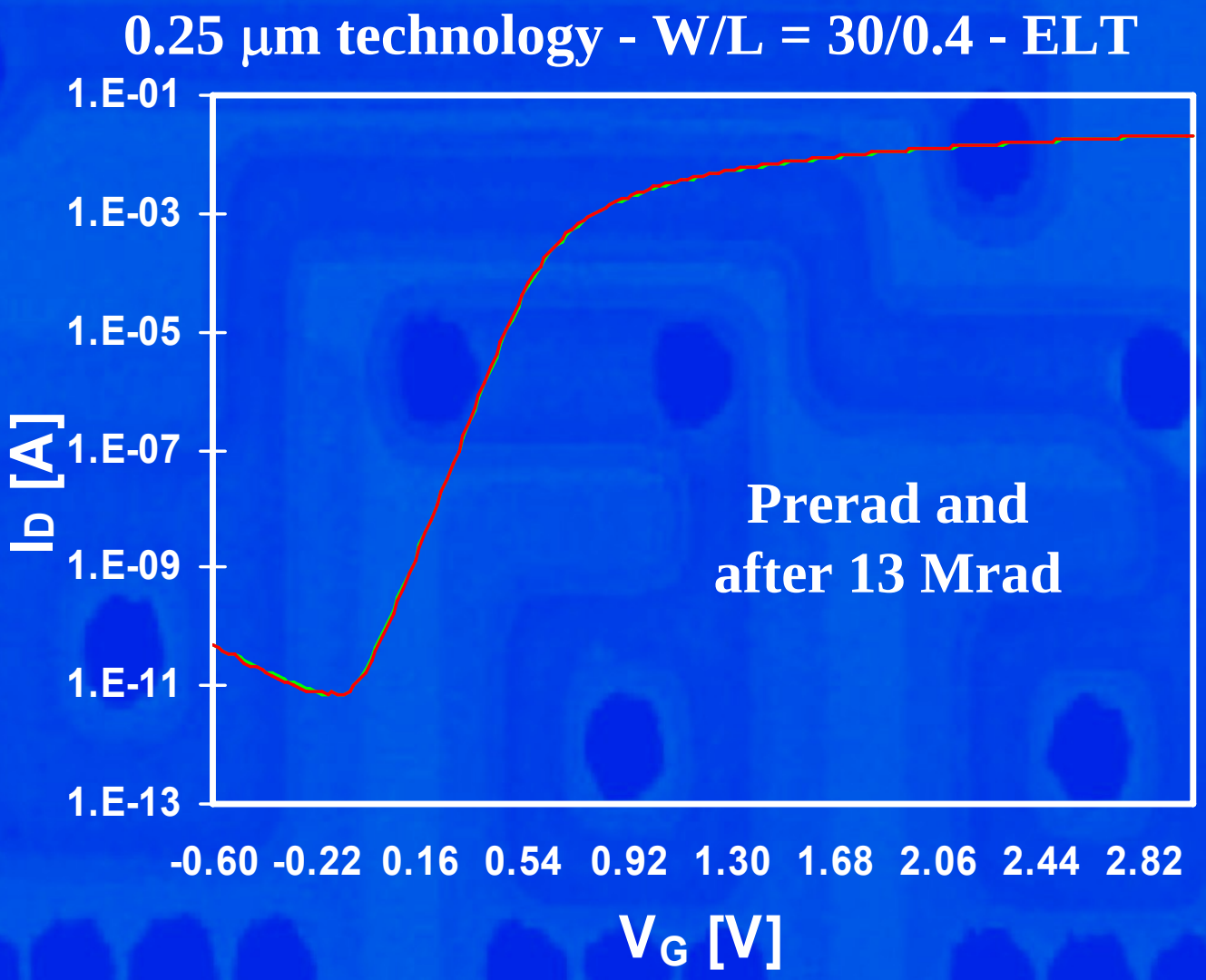
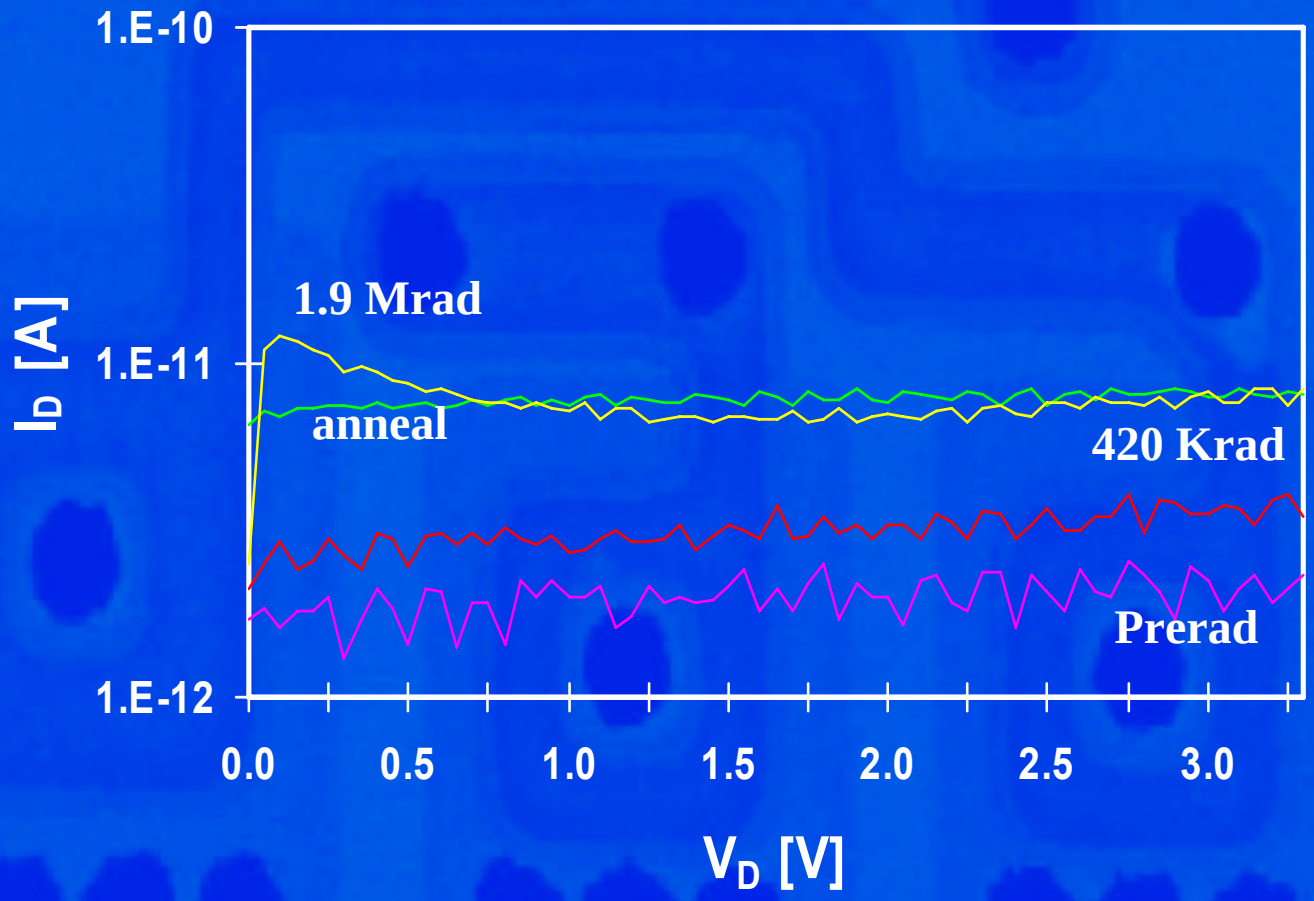


Field oxide leakage

FOXFET 14.4/2.6 without gate, with guardring
0.5 μm technology



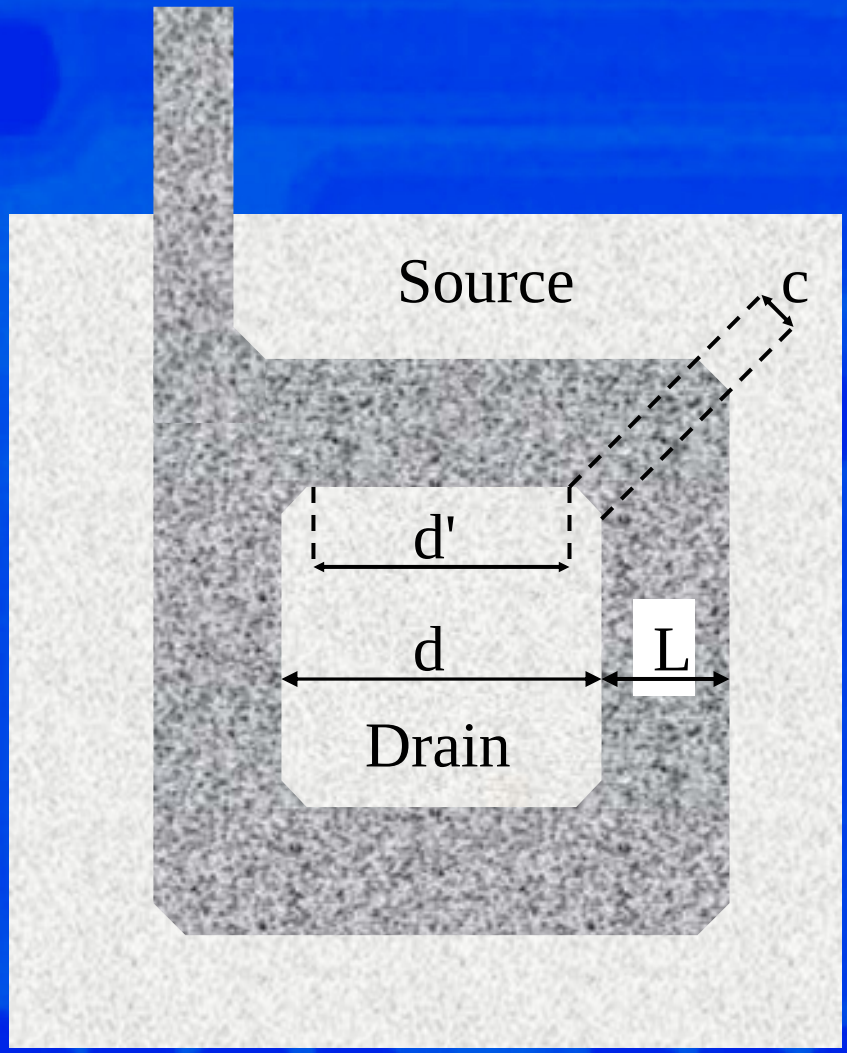
Advantages of this approach

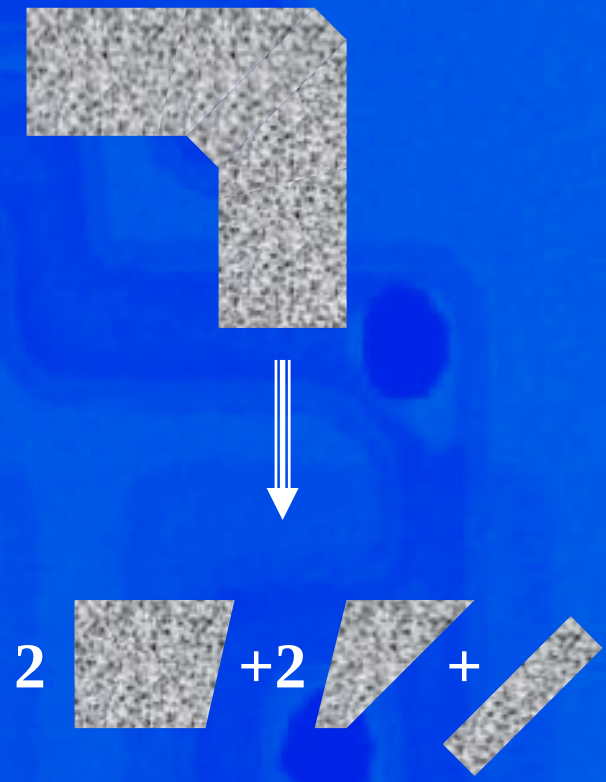
- ✓ Relies on physics (thickness of gate oxide): not process-dependent
- ✓ Allows for using state-of-the-art technologies:
  - Low power
  - High performance
  - High throughput, high yield, short turnaround times
  - Low cost

Difficulties for this approach

- ✓ Peculiar ELT behaviour
  - Modeling of ELT (size W/L?)
  - Limitation in aspect ratio
  - Asymmetry
- ✓ Lack of commercial library for digital design
- ✓ Loss of density
- ✓ Yield and reliability???

Modeling of ELTs (1)





Modeling of ELTs (2)

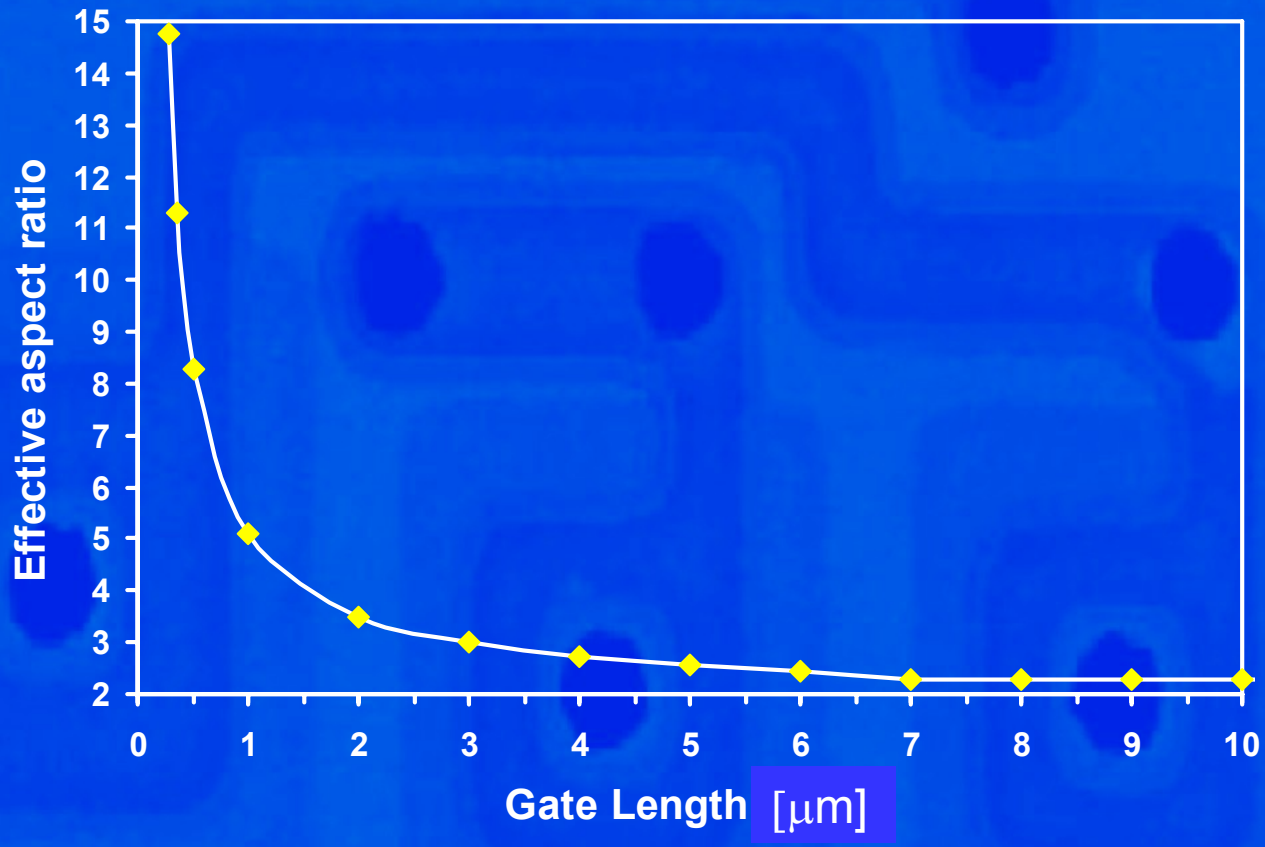
$$\left(\frac{W}{L}\right)_{eff} = 4\,\frac{2\alpha}{\ln\dfrac{d'}{d' - 2\alpha L_{eff}}} + 2K\,\frac{1-\alpha}{1.13\cdot\ln\dfrac{1}{\alpha}} + 3\,\frac{\dfrac{d-d'}{2}}{L_{eff}}$$

L_{drawn}	Estimated $(W/L)_{eff}$	Extracted $(W/L)_{eff}$
0.28	14.8	15
0.36	11.3	11.2
0.5	8.3	8.3
1	5.1	5.2
3	3	3.2
5	2.6	2.6

- ✓ 1 shape only supported (size of “c” fixed)
- ✓ Custom routines and layers integrated in design kit for extraction/design checking/computation

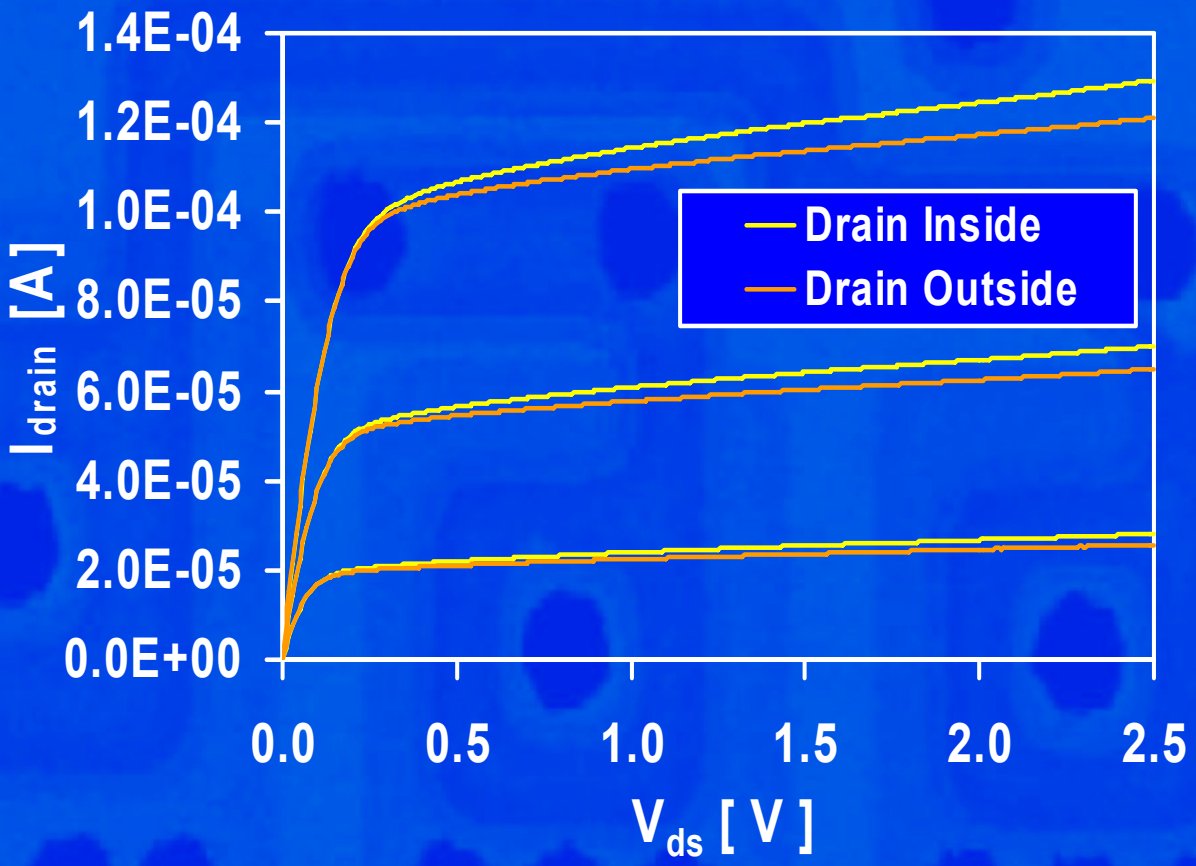
Limitation in the aspect ratio

Aspect ratio = W/L

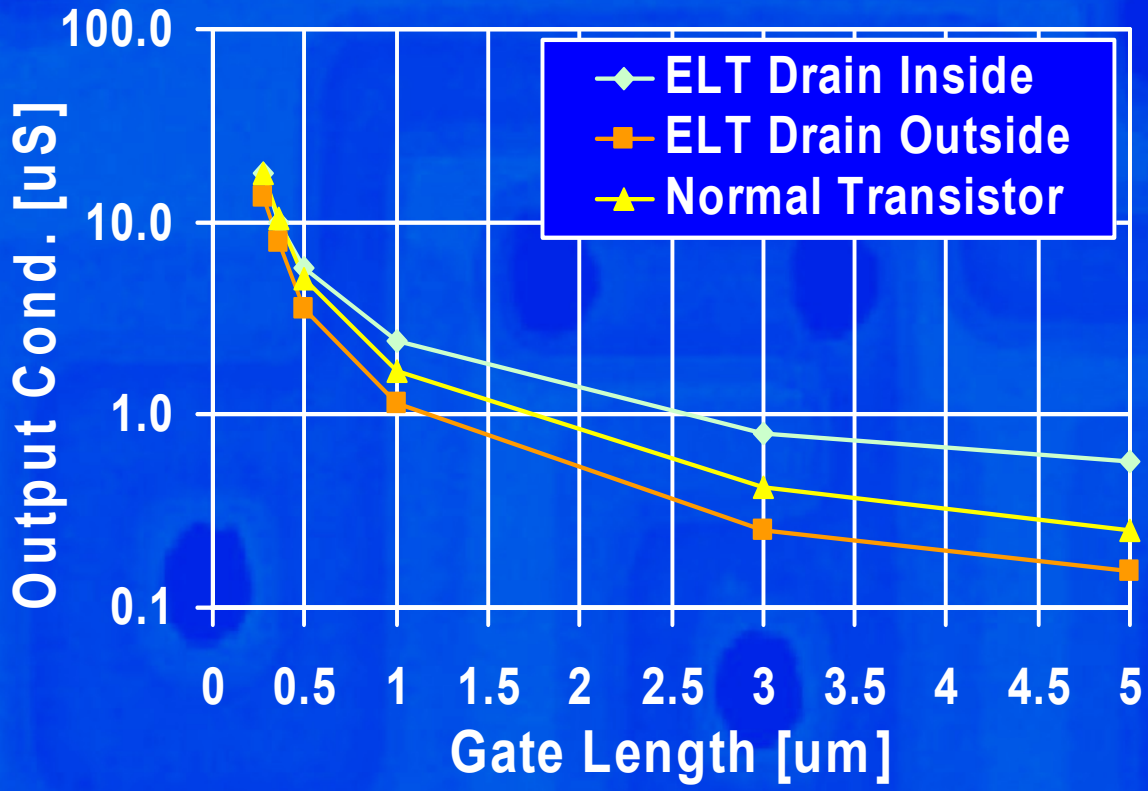


Asymmetry (1)

L = 0.28 μm G_{DI} = 11.9 μS G_{DO} = 9.6 μS

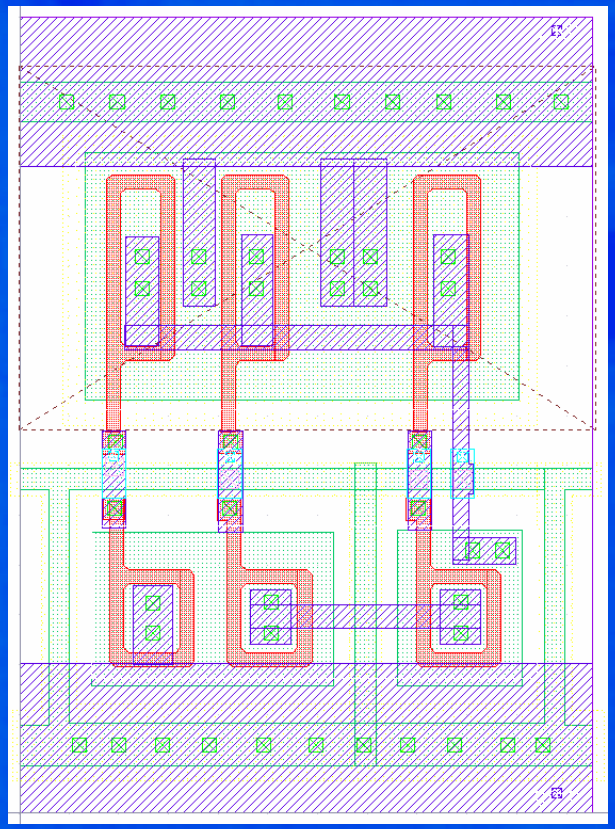


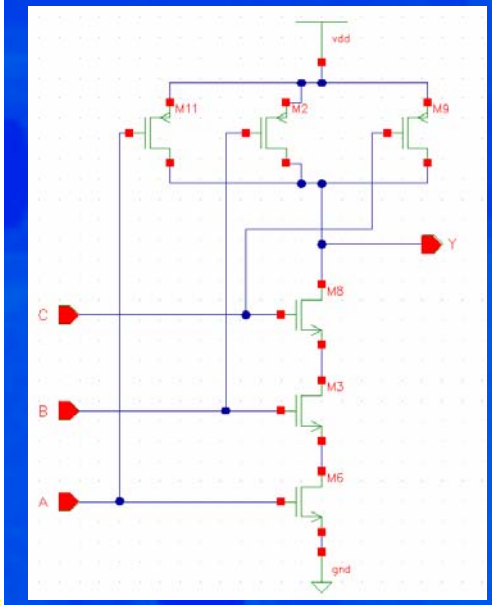
Asymmetry (2)



L (μm)	$\Delta G/G_{DI}$
0.28	19 %
0.36	23 %
0.5	33 %
1	53 %
3	70 %
5	75 %

Lack of commercial library (1)





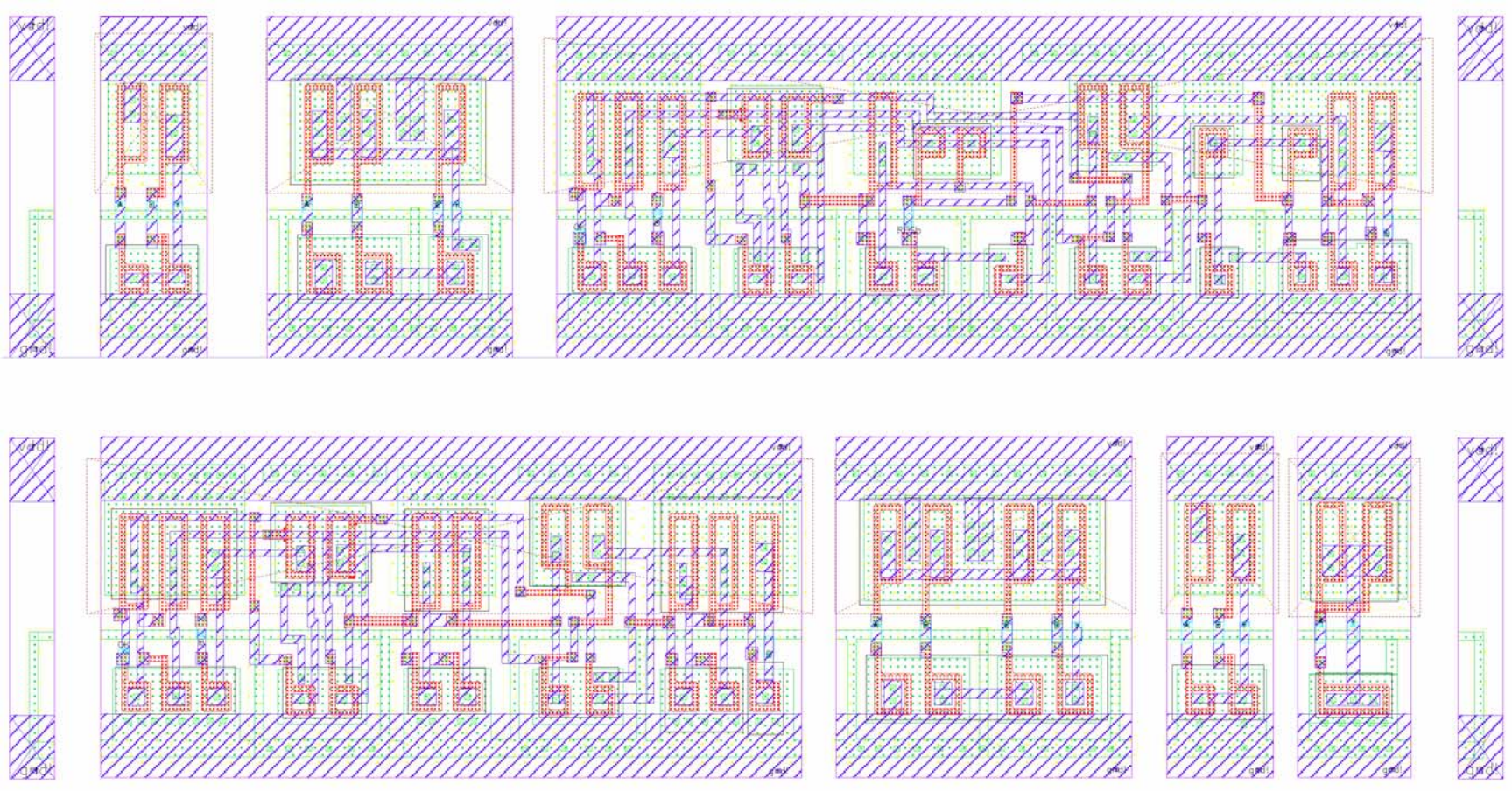
NAND3

Radiation tolerant design :

- Use of enclosed NMOS transistors
- Use of guard rings to isolate all n^+ diffusions at different potentials (including n-wells)

Lack of commercial library (2)

- ✓ Example of core cells



Lack of commercial library (3)

CERNLIB Digital Standard Cells

Core Logic	Cell Name	Trans. count	Size (µm) 16x	Area (µm²)
Boolean				
Inverter 1X Drive	E_Inv1	2	3	48
Inverter 2X Drive	E_Inv2	3	5	80
Inverter 4X Drive	E_Inv4	6	9	144
Inverter 8X Drive	E_Inv8	10	17	272
2 Input NAND	E_Nand2	4	7	112
3 Input NAND	E_Nand3	6	12	192
4 Input NAND	E_Nand4	8	14	224
2 Input NOR	E_Nor2	4	5	80
3 Input NOR	E_Nor3	6	11	176
4 Input NOR	E_Nor4	8	21	336
2 Input XNOR	E_Xnor2	12	18	288
Complex Gates				
2-Wide 2-Input AND-OR	E_AO22	10	16	256
2-Wide 2-Input AND-OR-INVERT	E_AOI22	8	13	208
2-Wide 2-Input OR-AND-INVERT	E_OAI22	8	12	192
Multiplexers				
2-Input MUX	E_Mux2	12	18	288
4-Input MUX	E_Mux4	28	40	640
Buffers				
Buffer X4 Drive	E_Buf4	8	11	176
Buffer X8 Drive	E_Buf8	16	26	416
Simple Cells				
Logic 0	LOGIC0	2	3	48
Logic 1	LOGIC1	2	3	48
Adders				
1-bit Half Adder	E_HAD1	18	27	432
1-bit Full Adder	E_FAD1	34	45	720
Flip Flops				
Static D FLIP-FLOP	E_dff	24	33	528
Static D FLIP-FLOP with Reset	E_dff_R	28	41	656
Static D FLIP-FLOP with Set	E_dff_S	28	41	656
Static D FLIP-FLOP with Set & Re	E_dff_SR	32	47	752
Static D Flip Flop with Scan	E_dff_SR_SC	40	59	944
Dynamic TSPC D FLIP FLOP	E_TSPC	11	19	304
Latches				
D-Latch	E_LD	18	25	400
D-Latch with Reset	E_LDR	21	29	464

I/O Logic	Cell Name	Trans. count	Size (µm) 458x	Area (µm²)
Output Pads				
8mA Drive Standard	OB8mA	16	115	51865
16mA Drive Standard	OB16mA	26	115	51865
20mA Drive Standard	OB20mA	34	115	51865
8mA Drive with Slew Rate control	OBSR8mA	14	115	51865
16mA Drive with Slew Rate control	OBSR16mA	30	115	51865
20mA Drive with Slew Rate control	OBSR20mA	38	115	51865
Input Pads				
CMOS Inverter Input	IB1	6	115	51865
Simple PAD	INPAD	0	115	51865
LVDS I/O Pads				
LVDS TX	LVDStx	33	235	105985
LVDS RX	LVDSrx	18	235	105985
I²C interface I/O Pads				
20mA Open Drain Output	OD20mA	9	115	51865
Bidirectional with 20mA Open Drain	IOD20mA	17	115	51865
Power Pads				
VDD for periphery & core	VDD	0	115	51865
VDD for periphery	VDD_CORE	0	115	51865
VDD for core	VDD_PERI	0	115	51865
VSS for periphery & core	VSS	0	115	51865
VSS for periphery	VSS_CORE	0	115	51865
VSS for core	VSS_PERI	0	115	51865
Corner for I/O periphery	CORNER	0	115	51865
Guard-ring cells				
Endcap Cell Left	CAPL	0	115	51865
Endcap Cell Reft	CAPR	0	115	51865
Filler Cell	FILLERCELL	0	115	51865

- ✓ List of Library Standard Cells

Existing libraries

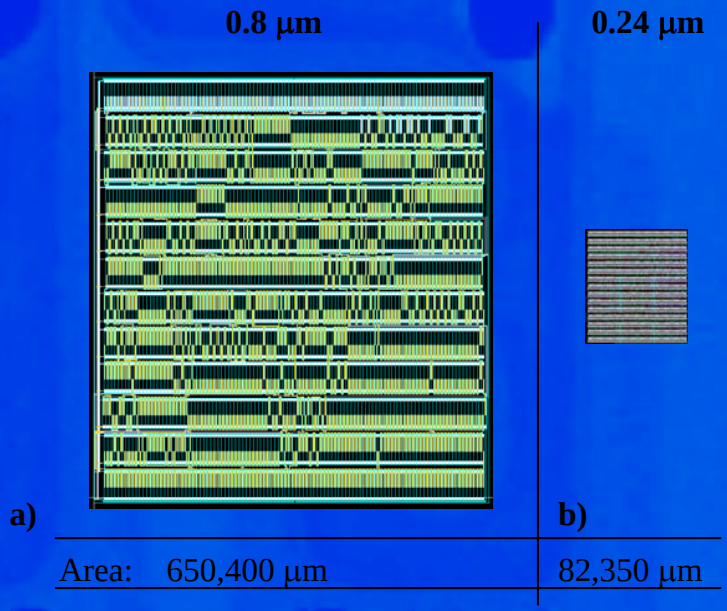
- ✓ List is not exclusive:
  - CERN in 0.25μm
    - "Daughter" libraries in PSI, LBL, Fermilab
  - IMEC (for ESA) in 0.18μm
  - Mission Research Corporation (for Aerospace Corporation) in 0.18μm

Loss of density

- ✓ Radiation Tolerant techniques introduce a ~70% layout area overhead

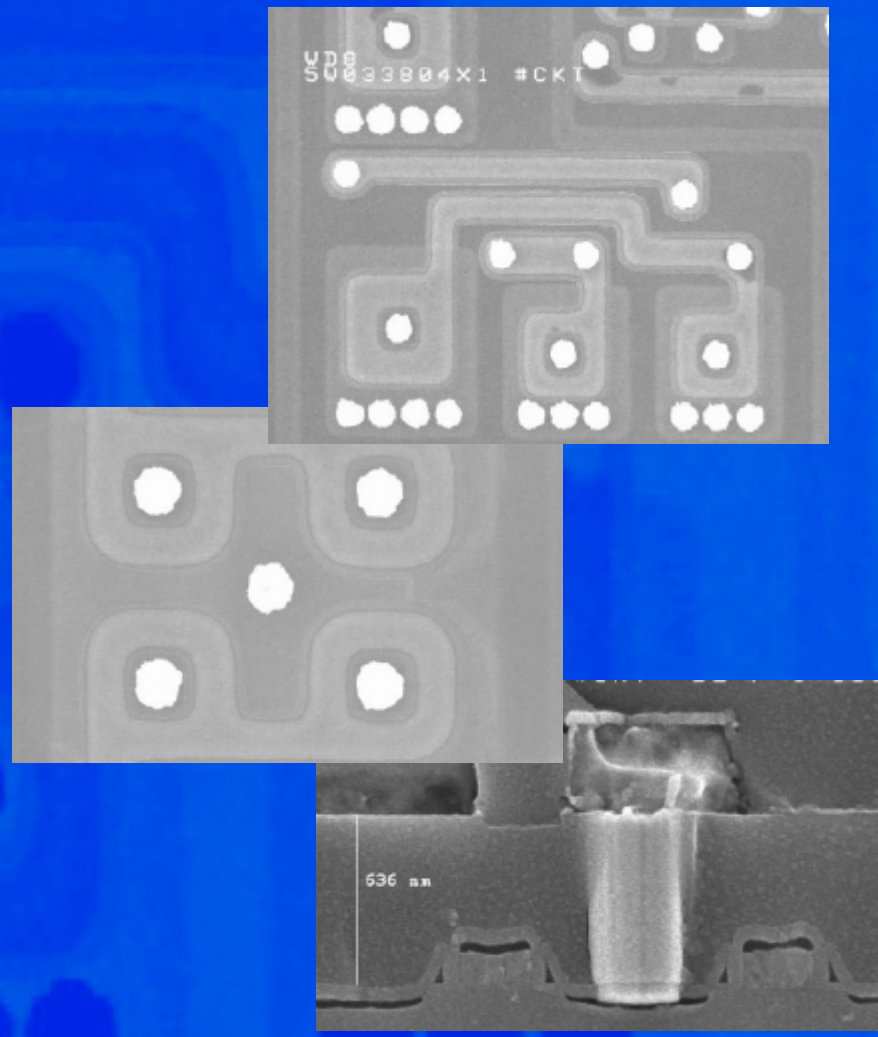
	Standard	Rad-Tol	Penalty
Inverter	33.6 μm^2	50.9 μm^2	34 %
2-in NAND	46.0 μm^2	119.0 μm^2	61 %
2-in NOR	47.8 μm^2	80.0 μm^2	41 %
Static D-F/F	153.0 μm^2	533.1 μm^2	71 %
Static D-F/F SR	188.1 μm^2	572.0 μm^2	75 %

- ✓ Gate density is 8 times larger when compared to a 0.8μm technology
  - Example: ring oscillator with 1280 inverters in 0.8 and 0.25mm technologies (0.25 uses the CERN radtol library)



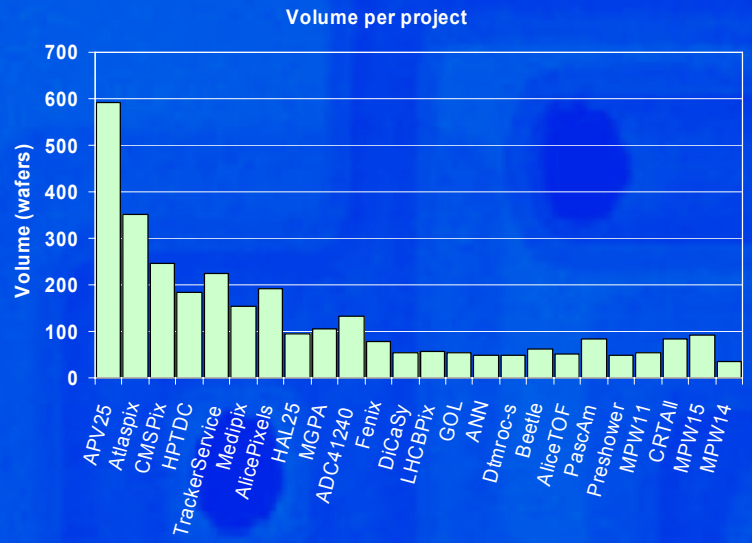
Yield and reliability?

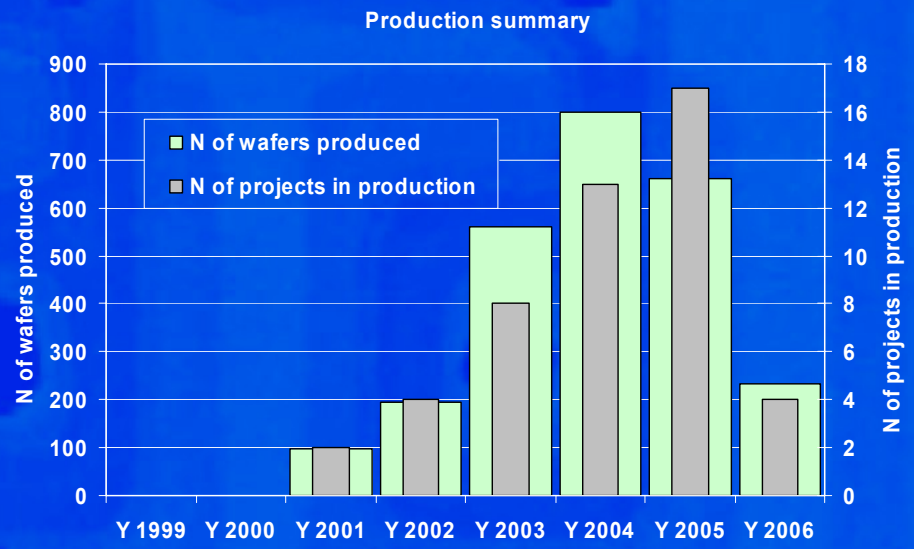
- ✓ Construction analysis performed on several chips
- ✓ Circuits produced, qualified and tested in thousands (100 different designs!)
- ✓ No concern on yield or reliability found yet…



“Large” scale production

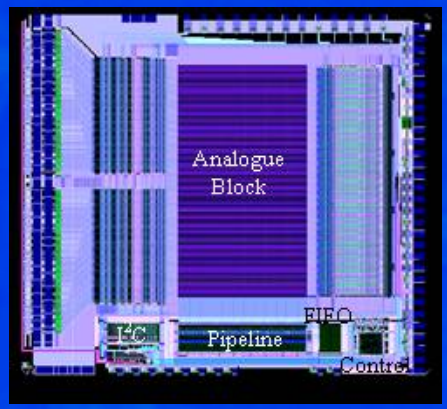
- ✓ Relatively large number of project in production, for quantities up to almost 600 wafers (200mm size). Total production in excess of 3000 wafers.

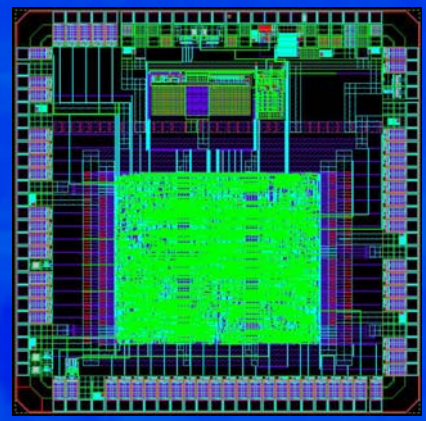




ASICs examples

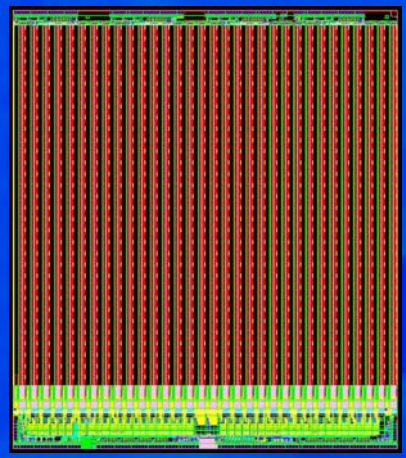
- ✓ APV25: readout of Silicon tracker detector of the CMS experiment
- ✓ 128 channels, analog output

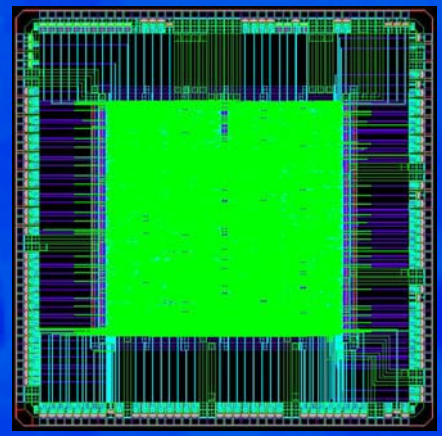




- ✓ GOL, optical link driver (serializer + laser driver) @ 1.6 Gbit/s

- ✓ Alice Pixel1, readout of silicon pixel detector of the ALICE experiment
- ✓ 2.1cm^2, 8000 analog channels, 13M transistors

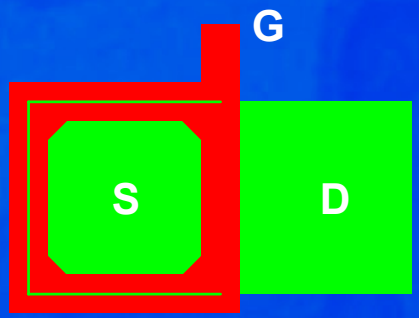




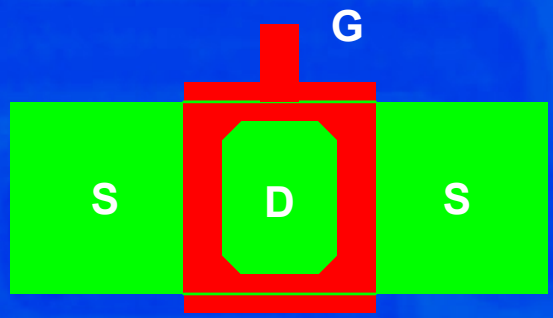
- ✓ CCU, control chip for the CMS tracker detector (fully digital chip, 120kgates)

Other edgeless designs

- ✓ Other “edgeless” transistor designs are possible !

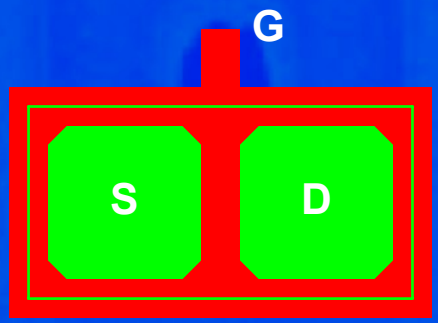


Ringed Source

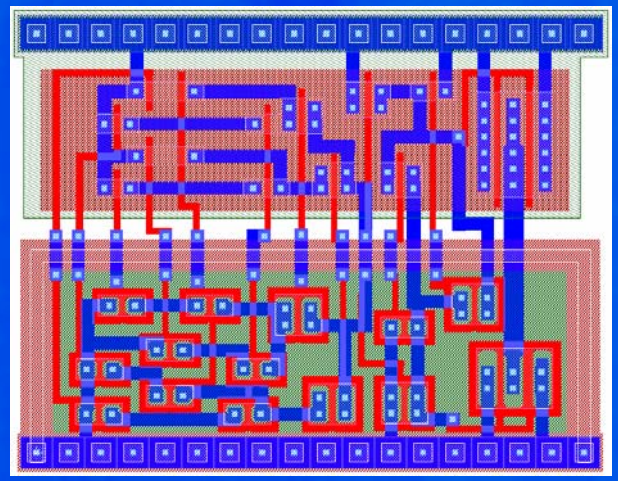


Ringed Interdigitated

from D.Mavis, MRC



Butterfly



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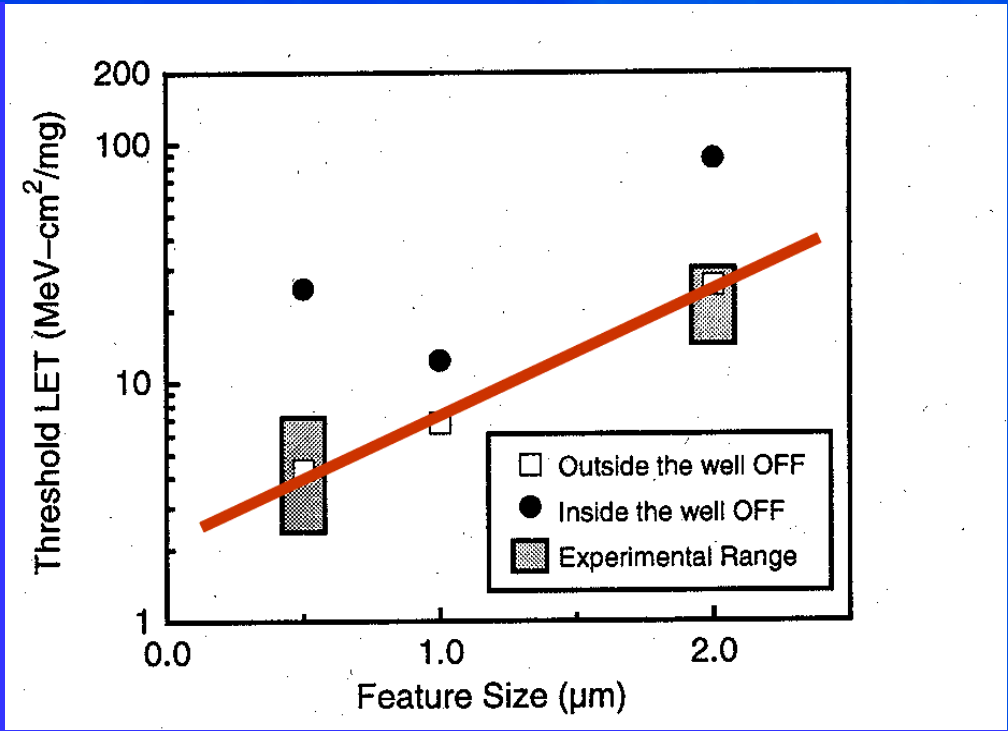
SEU and scaling: forecast

- V_{DD} reduced
- Node C reduced
- New mechanisms for SEU



P.E. Dodd et al., IEEE TNS, Dec. 1996

From the above, it looks like the SEU problem worsens with scaling

SEU and scaling: reality

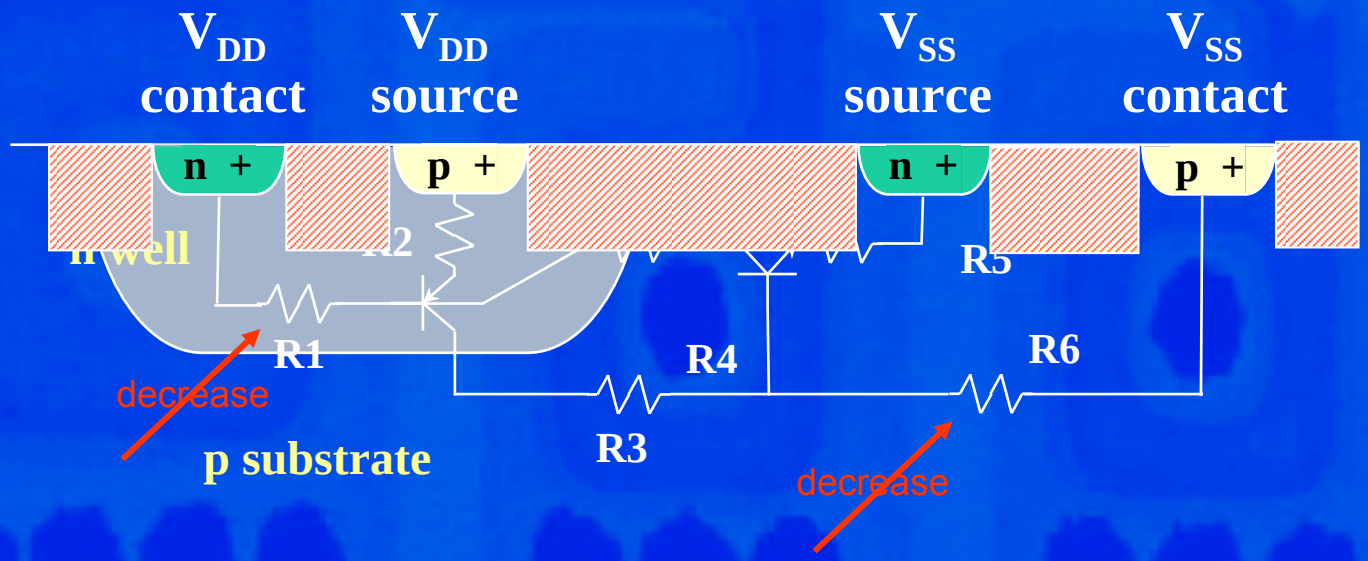
- ✓ All sources agree: DRAM sensitivity has been scaling down (cell area scaling has outpaced the decrease in stored charge).
- ✓ Picture somewhat less clear for SRAMs
- ✓ P.Hazuka et al (work funded by Intel) developed a model to predict SER scaling with Lg. The results suggest that the per-bit sensitivity decreases –at least- linearly with Lg
- ✓ Overall: FIT/MB decreases, but FIT/chip increases

- ✓ Not only Vdd and node capacitance have to be taken into account: sensitive area and charge collection efficiency are also important and change with technology generation!

SEL and scaling

- ✓ Retrograde wells
- ✓ Trench isolation
- ✓ V_{DD} reduced

All these issues help in preventing SEL, but they might not be always effective



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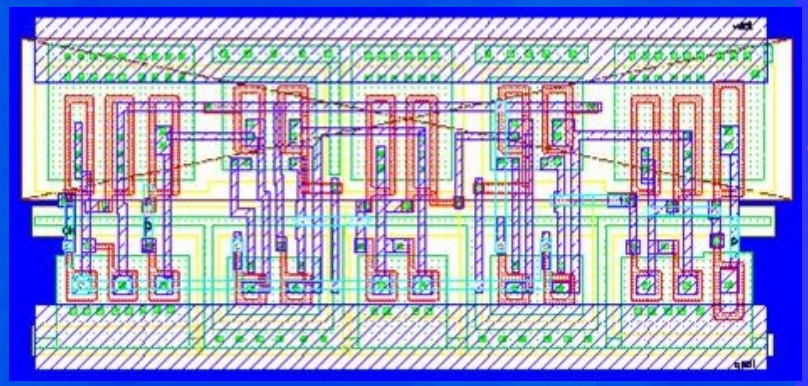
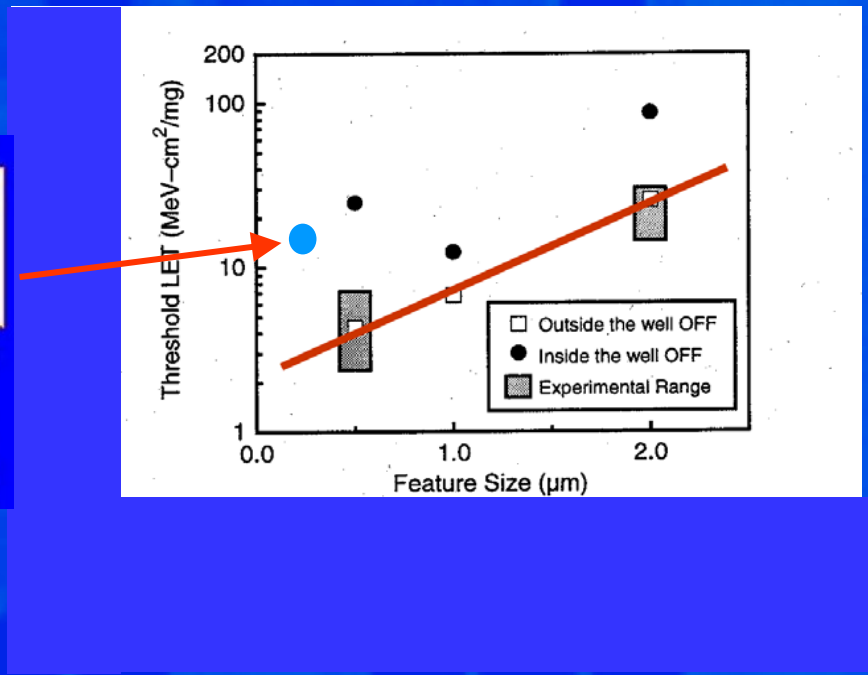
Solutions: SEU

- ✓ Technology level: epitaxial substrates, SOI,…
- ✓ Cell design: SEU-tolerant FFs or memories
- ✓ Redundancy
  - Triple Modular Redundancy (TMR): triplication and voting
  - Encoding (EDAC)
- ✓ Always to be considered at system level

Cell design (1)

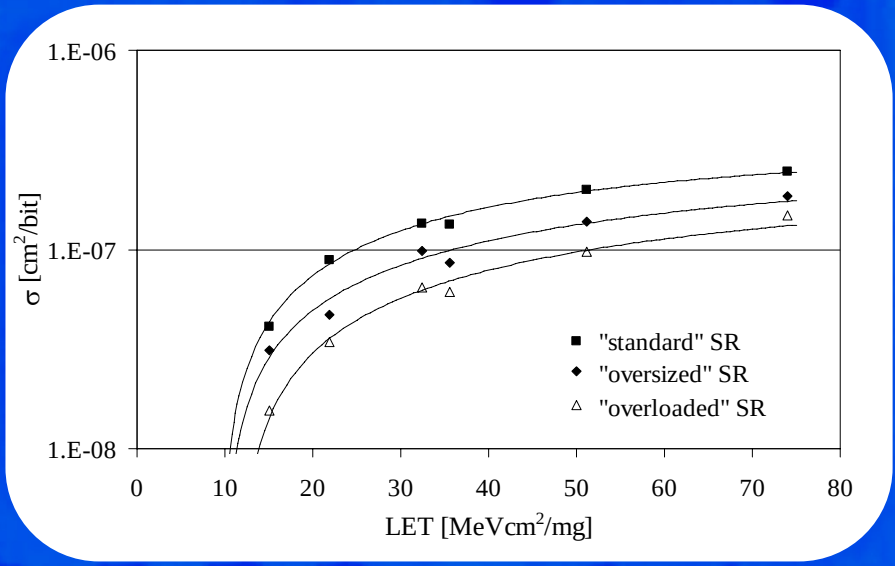
- ✓ Increase the critical charge by increasing the node capacitance:
  - Design larger transistors – also more driving strength





Cell design (2)

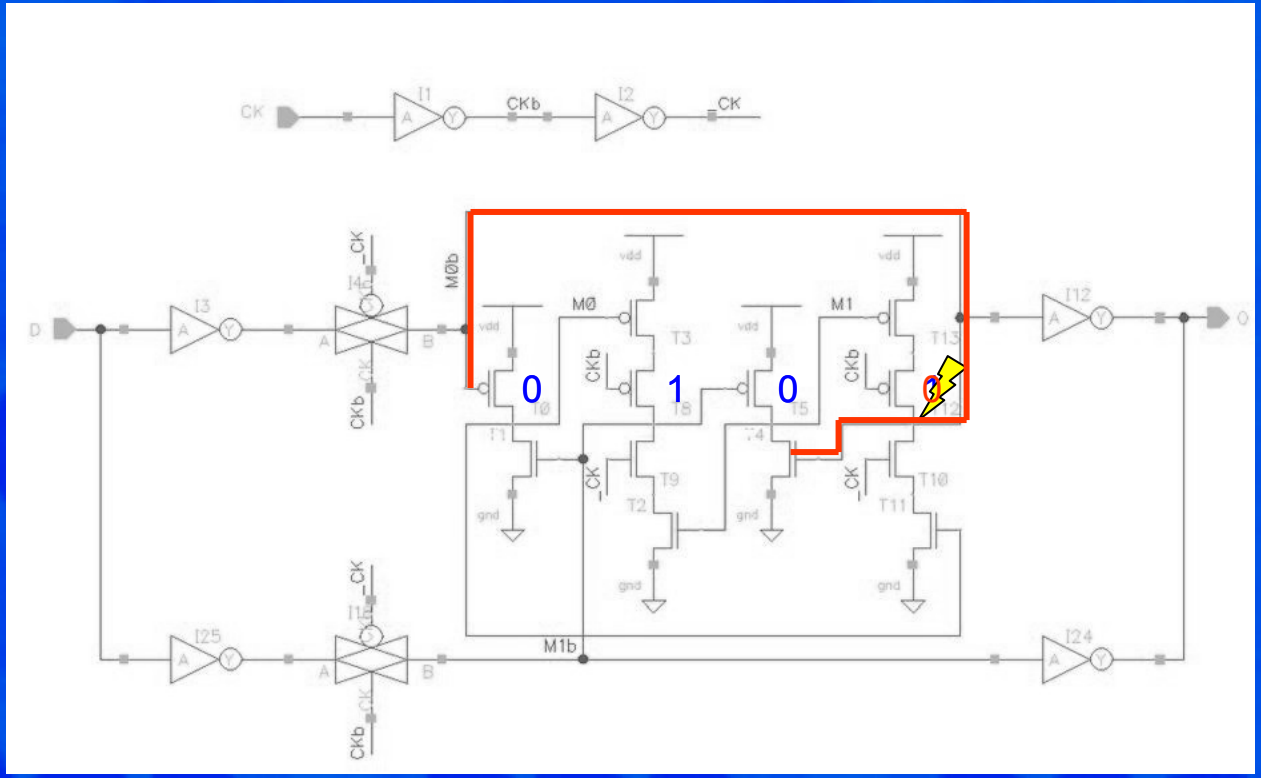
- ✓ Increase the critical charge by increasing the node capacitance:
  - Add “extra” capacitors
    - Metal/metal to avoid loosing space



Upset rates in proton environment:
- twofold decrease for the “oversized”
- tenfold decrease for the “overloaded”

Cell design (3)

- ✓ DICE (Dual Interlock Cell)
- ✓ Dual Interlock ensures SEU protection against hit on one node
- ✓ Writing in the cell requires access to 2 nodes



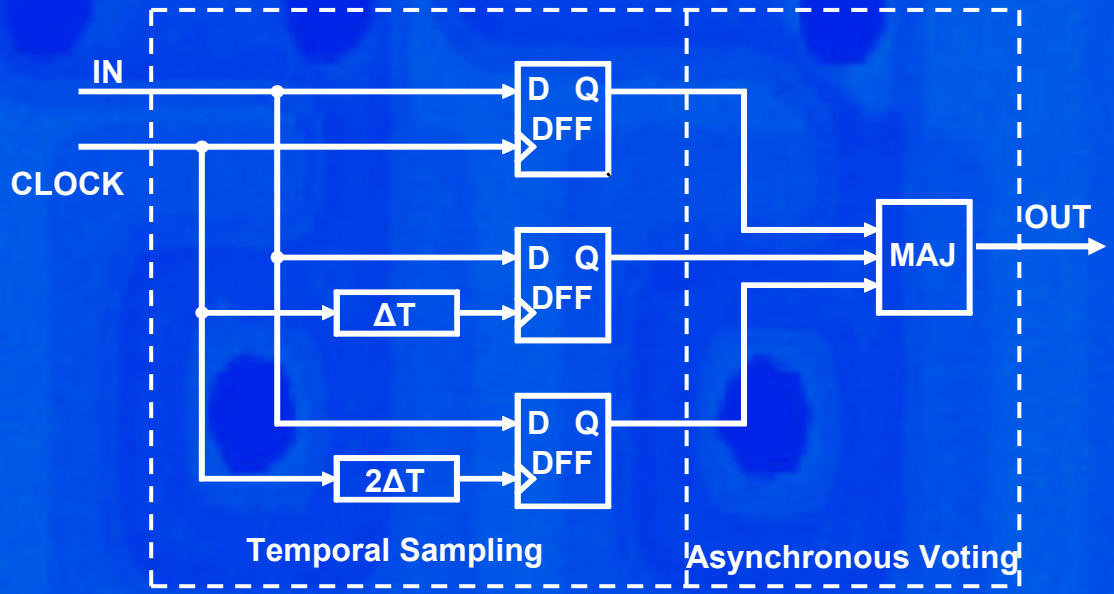
Cell design (4)

- ✓ DICE cell weakness:
  - Recovery time needed after SEU
    - Output glitch
    - A rising edge of the clock during recovery time can store wrong data in the following pipeline stage
  - Local clock buffers
  - Charge collection by multiple nodes is not negligible! (in 90nm technology, just 10x SEU rate improvement)

Cell design (5)

- ✓ Use special cell architectures
  - Temporal sampling with internal clock delays (after Mavis) effective against digital SET

• Transient can only be captured by 1 latch
• Sensitive to transients on clock line
• Many variations to this concept exist (one can delay data instead of clock, for instance)

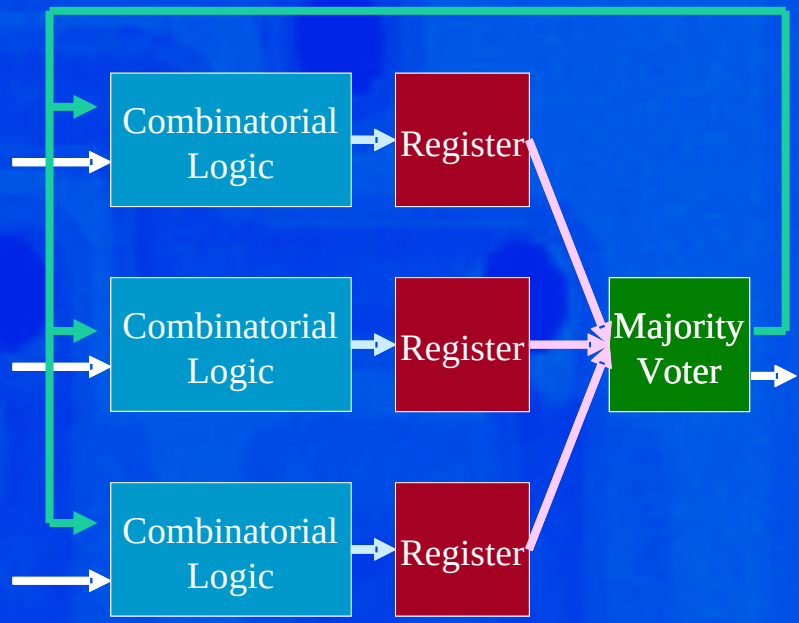


Solutions: SEU

- ✓ Technology level: epitaxial substrates, SOI,…
- ✓ Cell design: SEU-tolerant FFs or memories
- ✓ Redundancy
  - Triple Modular Redundancy (TMR): triplication and voting
  - Encoding (EDAC)
- ✓ Always to be considered at system level

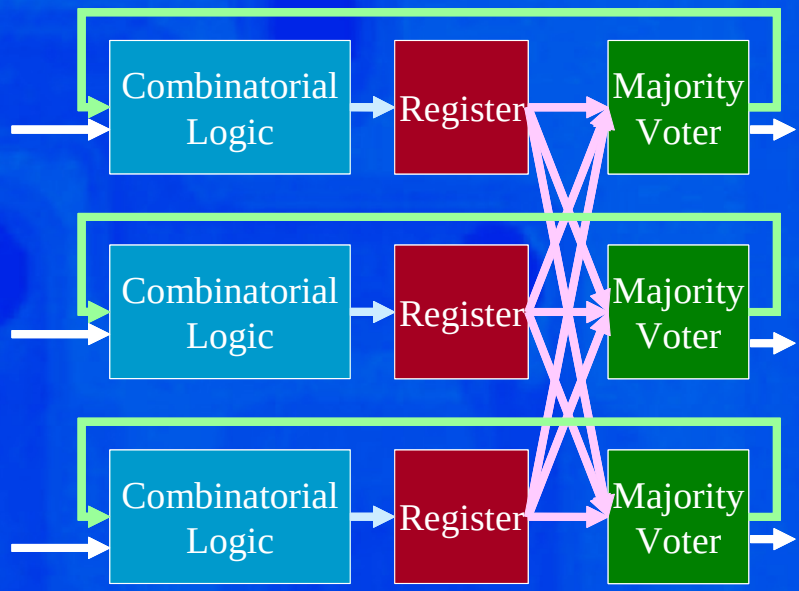
Redundancy: TMR (1)

- Triplication with 1 voter
  - The state machine is instantiated 3 times, with 1 voter
  - An SEU can corrupt the output of one of the blocks, but majority voting restores the correct state
  - An error in the voter instead corrupts the state!



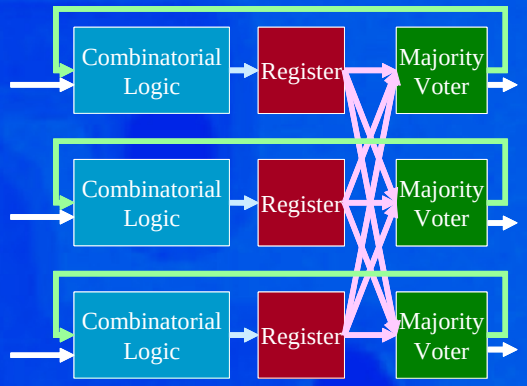
Redundancy: TMR (2)

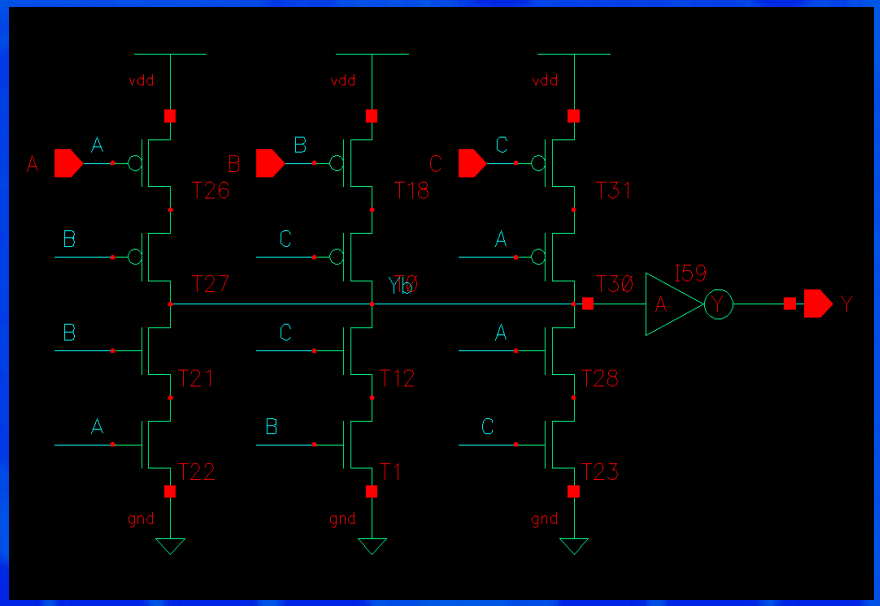
- Triplication with 3 voters
  - The state machine is instantiated 3 times, with 3 voters
  - An SEU can corrupt the output of one of the blocks, but majority voting restores the correct state
  - An error in one of the voters is also restored
  - This seems a lot of additional transistors, but sometimes the designer can find more “compact solutions”. This is shown in the following example.



Example of TMR in registers (1)

- ✓ A majority voter can necessitate a large number of transistors. Since 3 voters are required to protect the data from errors in the voter, the overall area penalty can be very large!
- ✓ One compact solution for the voter is in the schematic below:

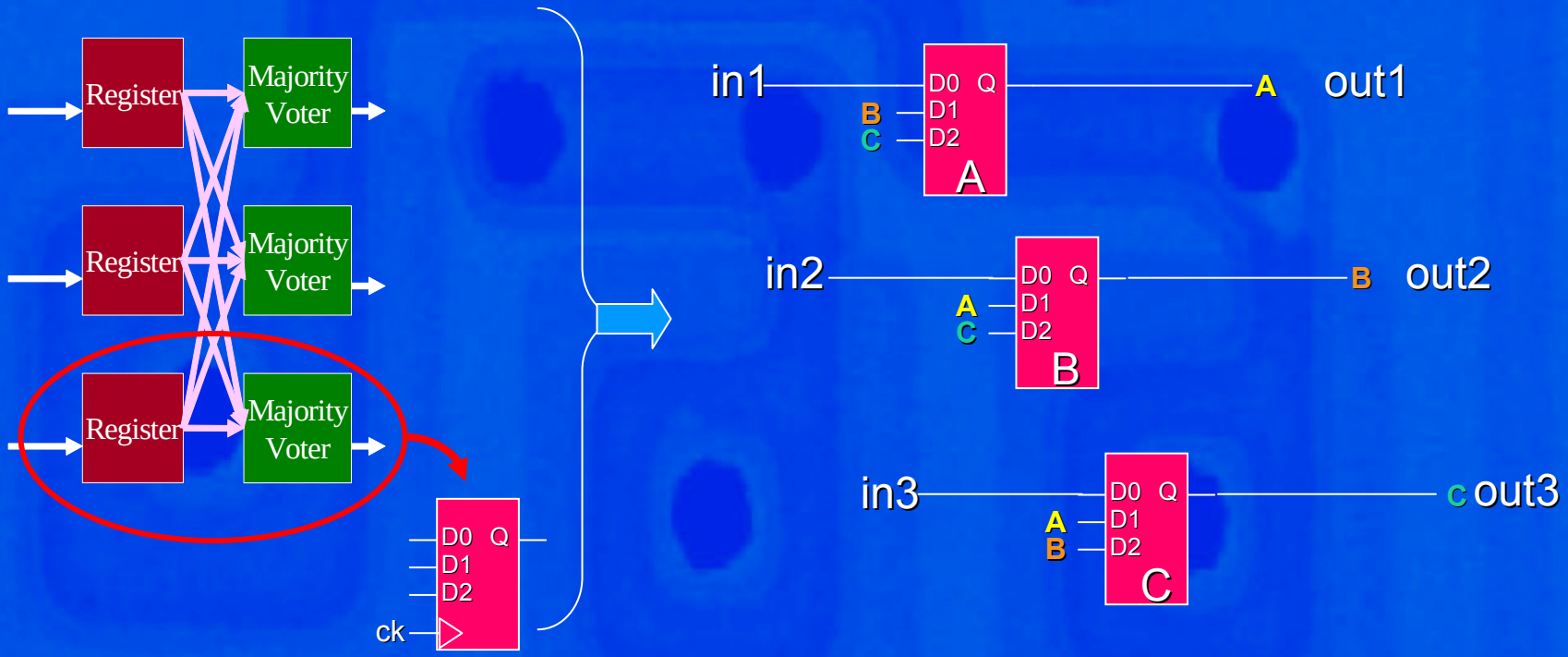




- ✓ Very compact layout
- ✓ 14 transistors (better than XOR+MUX style)
- ✓ Fast
  - 2 logic levels only
  - Possible to save the inverter (2 transistors less)
- ✓ Still 3 voters are needed, for a minimum of 36 transistors

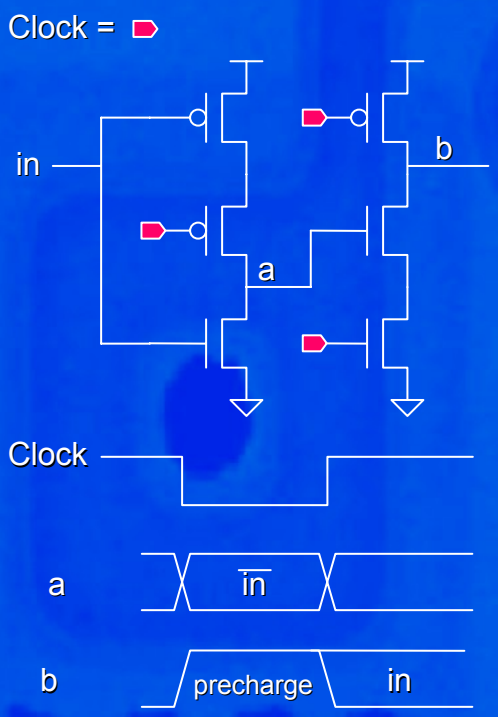
Example of TMR in registers (2)

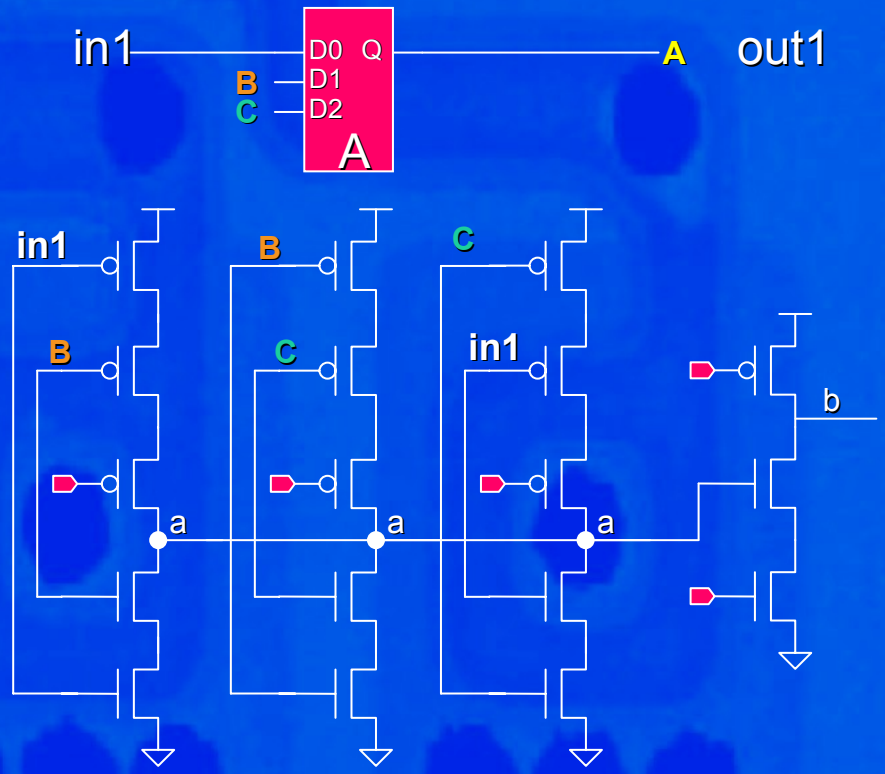
- ✓ To save some transistors, it is possible to merge the voter in the register, and make a single cell
- ✓ Each “super cell” will then have 3 inputs and 1 output with merged connections between them



Example of TMR in registers (3)

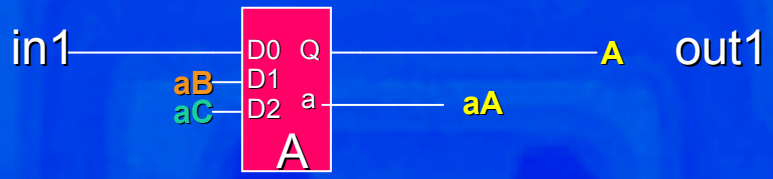
- ✓ Merging of the voter can be done at different levels
- ✓ The example below, for a dynamic FF, illustrates it. The first part of the FF cell is shown in the left picture, with its timing diagram.
- ✓ A first level of merging is achieved by integrating the voter in the input inverter, as shown in the right picture. This does not really save transistors with respect to a separate voter

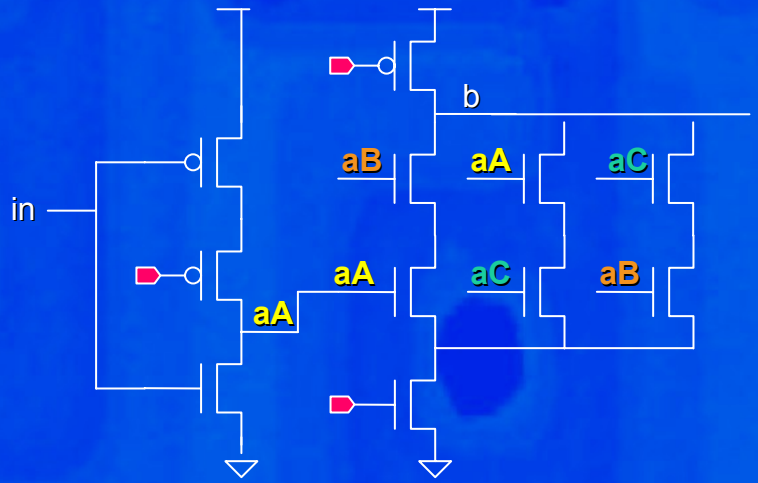




Example of TMR in registers (4)

- ✓ A “deeper” merging, where the voter is moved inside the FF, leads to considerable area saving





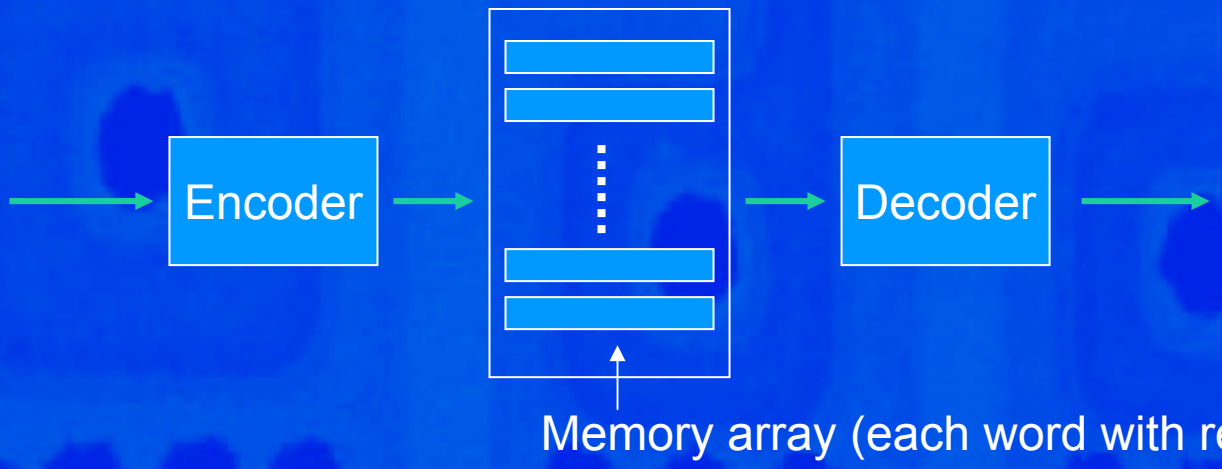
This integration of the voter in the cell “only” costs 5 additional transistors! For 3 “super cells”, the penalty for the voter decreases from 36 to 15 transistors!

Solutions: SEU

- ✓ Technology level: epitaxial substrates, SOI,…
- ✓ Cell design: SEU-tolerant FFs or memories
- ✓ Redundancy
  - Triple Modular Redundancy (TMR): triplication and voting
  - Encoding (EDAC)
- ✓ Always to be considered at system level

Redundancy: encoding (1)

- ✓ Adding redundant information (bits) and encoding-decoding
  - Used for data transmission and for memories
  - Requires complex encoding-decoding logic
  - Several different codes can be used (Hamming, Reed-Solomon, BCH, etc.)



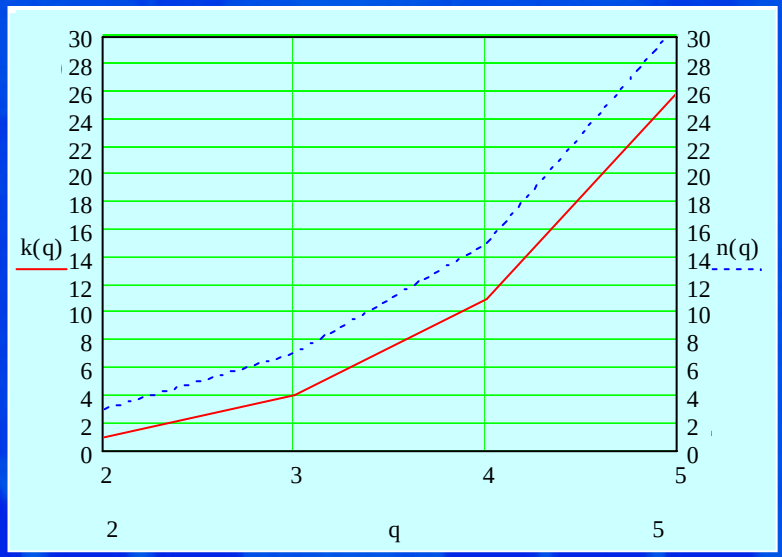
Redundancy: encoding (2)

- ✓ Example: Hamming encoding (1950)

k = number of message bits
q = number of check (parity) bits
n = number of word bits

Minimum distance between words = 3
⇒All valid words in the code differ AT LEAST by 3 bits
⇒It can be used for single error correction, double error detection

$n = k+q \qquad n \leq 2^q-1$



Redundancy: encoding (3)

- ✓ Example: Hamming encoding (1950)

Example of encoding for k = 8 q = 4 n = 12

Encode in a way requiring “as easy as possible” encoding/decoding logic

1. Check bits in powers of 2 positions in the word (position 1,2,4,8)
2. Other word bits are the message bits
3. Each check bit computes the parity for some of the word bits:
   - Position 1: check 1 bit, skip 1 bit, etc. (bits 1,3,5,7,9,11)
   - Position 2: check 2 bits, skip 2 bits, etc. (bits 2,3,6,7,10,11)
   - Position 4: check 4 bits, skip 4 bits, etc. (bits 4,5,6,7,12)
   - Position 8: check 8 bits, skip 8 bits, etc. (bits 8,9,10,11,12)

Word to encode: 10101010

word	.1	.1	1	.1	0	1	0	0	1	0	1	0
position	1	2	3	4	5	6	7	8	9	10	11	12

Redundancy: encoding (4)

- ✓ Example: Hamming encoding (1950)

Word to encode: 10101010

Encoded word	1	1	1	1	0	1	0	0	1	0	1	0
position	1	2	3	4	5	6	7	8	9	10	11	12
SEU changes to	1	1	1	1	0	0	0	0	1	0	1	0

Check the parity bits in the received word:

Position 1: OK
Position 2: wrong
Position 4: wrong
Position 8: OK

The position of wrong bit is the sum of the wrong positions, that is Position 6!

Outline

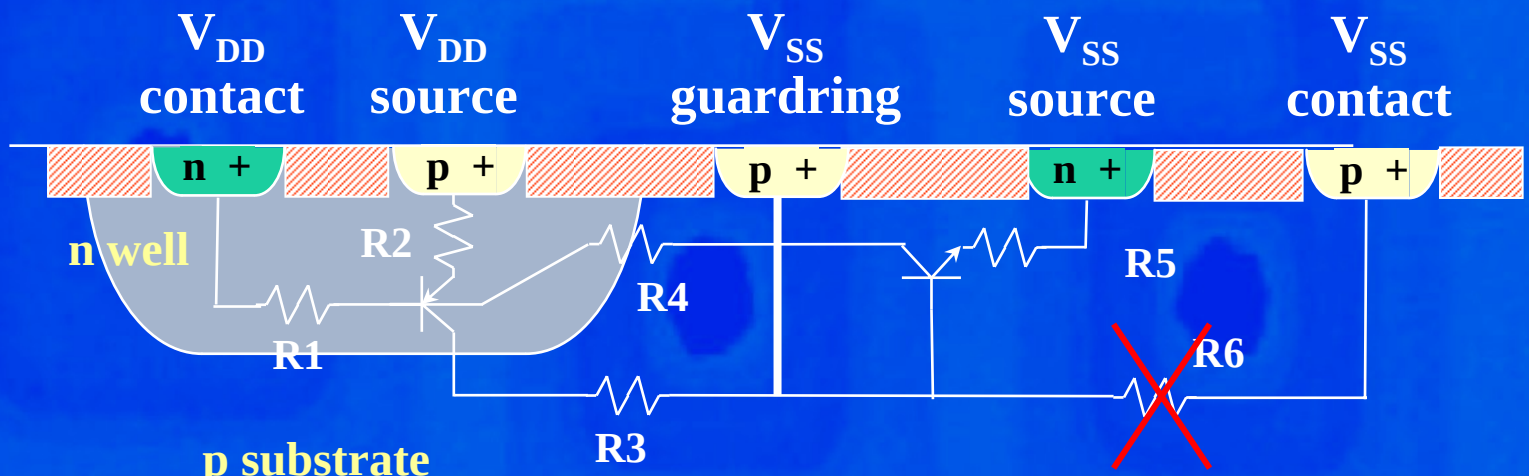
- ✓ Foreword: CMOS technologies
- ✓ TID: Total Ionizing Dose
  - Effects (reminder)
  - Solutions
  - Trends in state-of-the-art technologies
- ✓ SEEs: Single Event Effects
  - Effects (reminder)
  - SEEs and scaling
  - Solutions
    - SEU
    - SEL
- ✓ Conclusion

Reducing SEL sensitivity

The best solution is to decrease the gain of the parasitic pnpn structure.
Technological and layout solution can help in that respect:

Technological => use of epitaxial substrates and retrograde wells
=> use of trench instead of junction isolation

Layout => increase the distance between complementary devices
=> use guardrings
=> use lots of substrate and well contacts



Hardness-By-Design (HBD) techniques

Outline

- ✓ Foreword
- ✓ TID: Total Ionizing Dose
  - TID and scaling
  - Solutions
- ✓ SEEs: Single Event Effects
  - SEEs and scaling
  - Solutions
- ✓ Summary & Conclusion

Summary & Conclusion

- ✓ In state-of-the-art commercial-grade CMOS technologies, reliable radiation tolerance can be achieved with HBD techniques
- ✓ If “natural” TID is insufficient, the use of ELTs and guardrings can “upgrade” it – large effort needed mainly for digital design
- ✓ SEU rates can be decreased with proper engineering (study of environment, introduction of tolerant cells, redundancy, encoding, etc.) and should always be considered at the system level
- ✓ SEL – already unlikely – can be further controlled by careful layout

Further reading

- ✓ On Enclosed Transistor Layout:
  - Ph.D. thesis describing results in 0.25μm technology:
  - G.Anelli, “Conception et caractérisation de circuits intégrés résistants aux radiations pour les détecteurs de particules du LHC en technologies CMOS submicroniques profondes“, Ph.D. Thesis at the Politechnic School of Grenoble (INPG), France, December 2000, availeble on the web at the URL: http://rd49.web.cern.ch/RD49/RD49Docs/anelli/these.html
  - Paper containing all references on the work done at CERN on this subject: F.Faccio, “Radiation Issues in the new generation of high energy physics experiments”, Int. Journal of High Speed Electronics and Systems, Vol.14, No.2 (2004) 379-399
- ✓ On SEU-tolerant Cells:
  - Increased capacitance:
    - F.Faccio et al., “Single Event Effects in Static and Dynamic Registers in a 0.25mm CMOS Technology”, IEEE Trans. Nucl. Science, Vol.46, No.6, pp.1434-1439, December 1999
    - F.Faccio et al., “SEU effects in registers and in a Dual-Ported Static RAM designed in a 0.25mm CMOS technology for applications in the LHC”, in the proceedings of the Fifth Workshop on Electronics for LHC Experiments, Snowmass, September 20-24, 1999, pp.571-575 (CERN 99-09, CERN/LHCC/99-33, 29 October 1999)
    - P.Roche, F.Jacquet, C.Caillat, J.P.Schoellkopf, "An Alpha Immune and Ultra Low Neutron SER High Density SRAM", proceedings of *IRPS 2004*, pp671-672, April 2004
  - Special SEU-tolerant cells:
    - R.Velazco et al., “2 CMOS Memory Cells Suitable for the Design of SEU-Tolerant VLSI Circuits”, IEEE Trans. Nucl. Science, Vol.41, No.6, p.2229, December 1994
    - T.Calin et al., “Upset Hardened Memory Design for Submicron CMOS Technology”, IEEE Trans. Nucl. Science, Vol.43, No.6, p.2874, December 1996
    - M.N.Liu et al., “Low power SEU immune CMOS memory circuits”, IEEE Trans. Nucl. Science, Vol.39, No.6, p.1679, December 1992
    - J.Canaris, S.Whitaker, “Circuit techniques for the radiation environment of Space”, IEEE 1995 Custom Integrated Circuits Conference, p.77
    - P.Eaton, D.Mavis et al., “Single Event Transient Pulsewidth Measurements Using a Variable Temporal Latch Technique”, IEEE Trans. Nucl. Science, Vol.51, no.6, p.3365, December 2004
- ✓ On TMR and encoding:
  - Paper comparing techniques and containing references, to be used as a starting research point: S.Niranjan, J.F.Frenzel, “A comparison of Fault-Tolerant State Machine Architectures for Space-Borne Electronics”, IEEE Trans. On Reliability, Vol.45, No1, p.109, March 1996

General Outline

- ✓ ULSI technologies: manufacturing
- ✓ Radiation effects in devices and technologies
- ✓ Radiation Hardness-By-Design (HBD) techniques for ASICs
- ✓ 130nm technology node for High Energy Physics: vendor, properties, radiation effects

130nm technology node for HEP

Outline

- ✓ The 130nm technology node
- ✓ Radiation effects in samples from different Foundries
- ✓ CERN Foundry Service in 130nm
  - Specific features
  - Radiation effects
  - Design Kits

The 130nm technology node

- ✓ In production since 2000-2001
- ✓ Still available via “brokers” (Europractice, MOSIS, CMP), but not all versions
- ✓ General common features:
  - “still” available in 200mm wafers (8 inches)
  - 8 levels of copper metallization
  - Logic and analog/RF versions with different devices available
  - 2 oxide thicknesses (core 2-2.2nm and I/O for operation to 2.5V), thin oxides that should be radiation tolerant
  - Wide range of transistors (different dopings)
  - Effective minimum L 0.08-0.09 um
  - Integration achievable of the order of 200kgates/mm^2
  - Very wide range of IP blocks generally available from either the Foundry or third parties
  - Large number of masks, and expensive => NRE between 2.5 and 5 times more expensive than “our” 250nm
  - Projected availability to around 2018

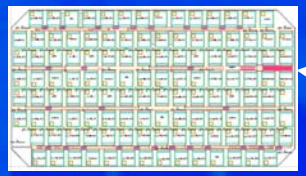
130nm technology node for HEP

Outline

- ✓ The 130nm technology node
- ✓ Radiation effects in samples from different Foundries
  - Core transistors (ELT, linear layout)
  - I/O transistors (ELT, linear layout)
- ✓ CERN Foundry Service in 130nm
  - Specific features
  - Radiation effects
  - Design Kits

Aim and experimental details

- ✓ AIM: Understanding the natural radiation tolerance of the 130nm node. Testing samples from different Foundries allows to check if observed results are common properties or specific of just “one” particular process
- ✓ Samples from 3 commercial 130nm CMOS processes have been tested
- ✓ Some are Process Monitoring Devices (PMD) from foundry, some custom-designed test ICs
- ✓ NMOS and PMOS transistors, core and I/O devices (different oxide thickness), FOXFETs
- ✓ Testing done at probe station – no bonding required (transistors are extremely fragile and gate oxide can be damaged by bonding)
- ✓ Irradiation with X-rays at CERN up to 100-200Mrad, under worst case static bias



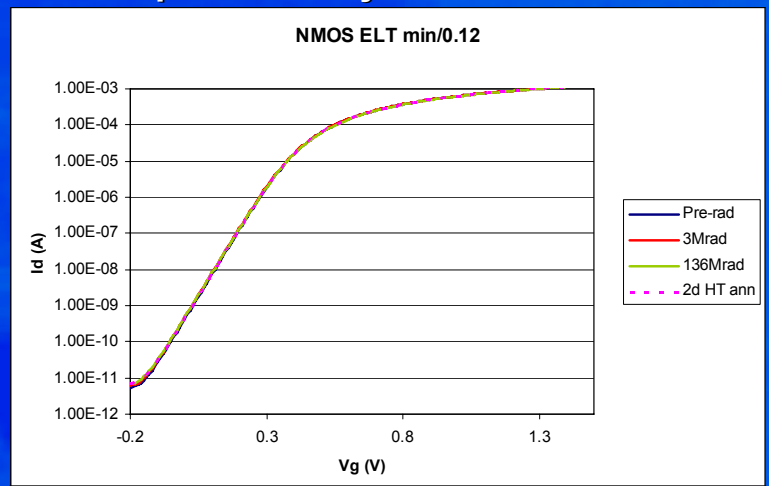
Custom-developed test IC

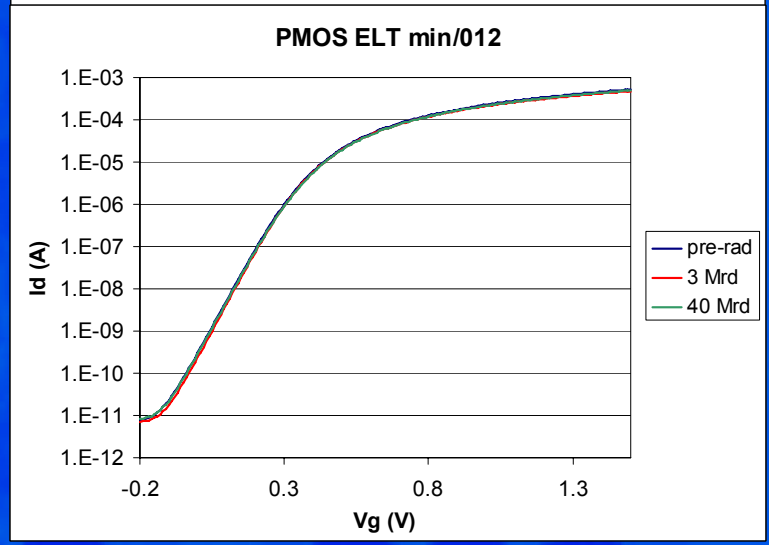
The CERN X-ray facility

Core NMOS transistors, enclosed (ELT)

- ✓ The radiation hardness of the gate oxide is such that practically no effect is observed – verified for 2 foundries (A up to 140Mrad, B up to 30Mrad). Id=f(Vgs) curves drop on top of each other after any TID step (see figures)
- ✓ ELT transistors are suitable for SHLC applications: are they really needed?

Example: Foundry A



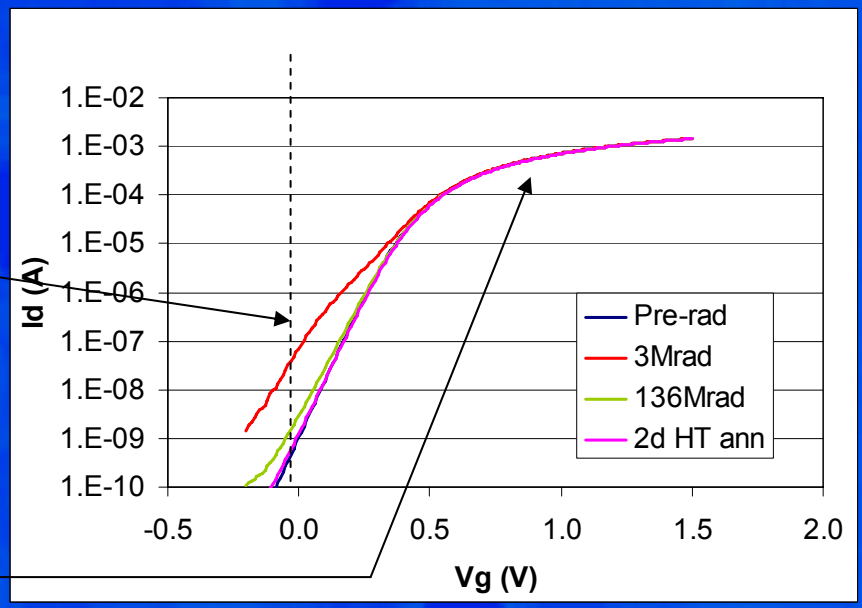


Core NMOS transistors, linear layout (1)

- ✓ Wide transistors

(W > 1μm):

- When the transistor is off or in the weak inversion regime:
  - Leakage current appears (for all transistor sizes)
  - Weak inversion curve is distorted
- When the transistor is in strong inversion:
  - No significant change in characteristics



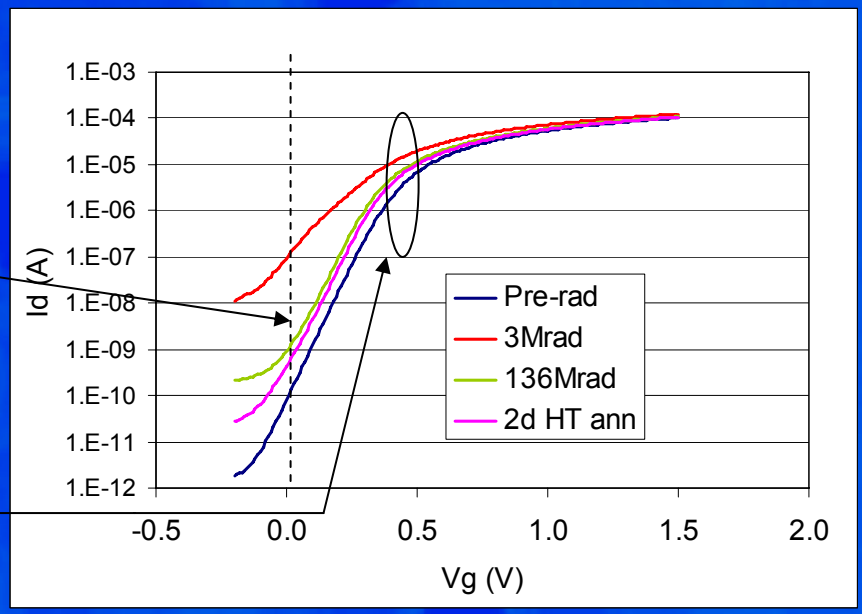
Core NMOS transistors, linear layout (2)

- ✓ Narrow transistors

(W < 0.8μm):

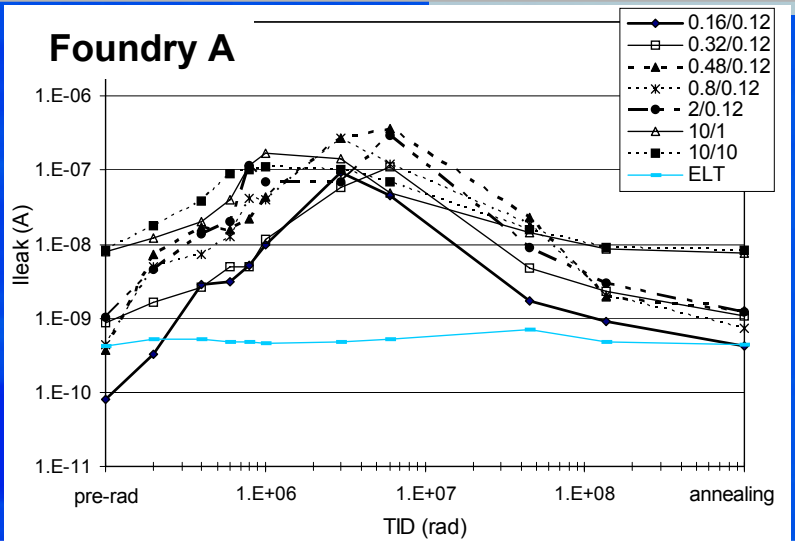
- When the transistor is off or in the weak inversion regime:
  - Leakage current appears (for all transistor sizes)
  - Weak inversion curve is distorted
- Additionally, a Vth shift (decrease) appears for narrow channel transistors
- The narrower the transistor, the larger the Vth shift. This effect has been called Radiation-Induced Narrow Channel Effect (RINCE)

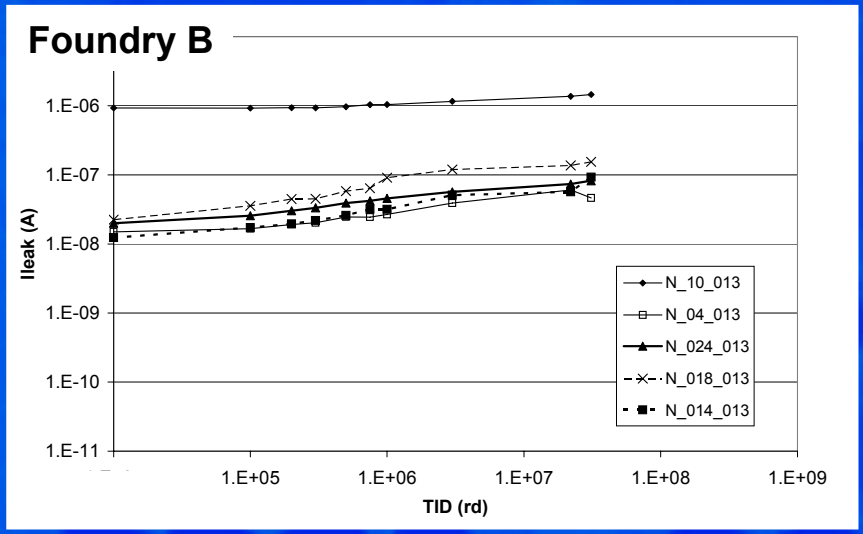
Foundry A, 0.16/0.12

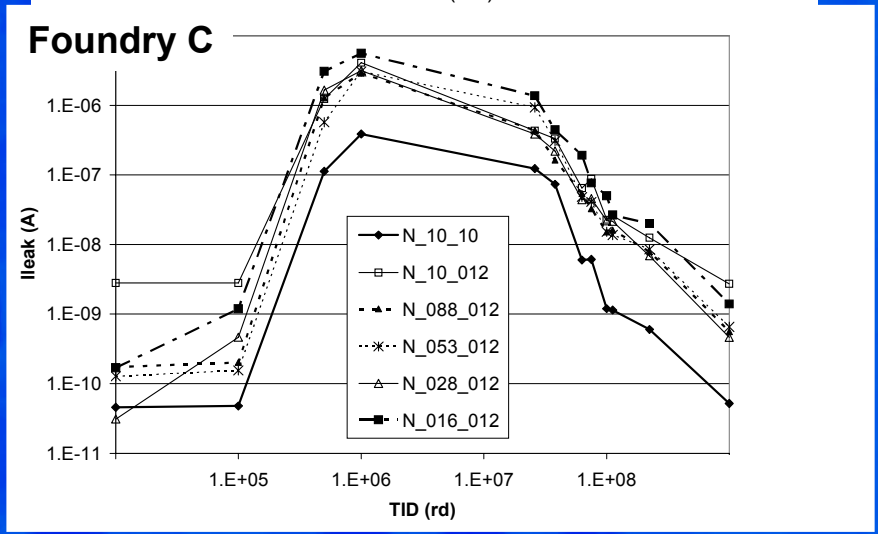


Core NMOS transistors, linear layout (3)

- ✓ Let's observe the effect on the **leakage current**
  - Peak in leakage at a TID of 1-5Mrad (A and B), similar for all transistor sizes
  - Peaking dependent on dose rate and temperature, difficult to estimate in real environment
  - Different in the 3 technologies

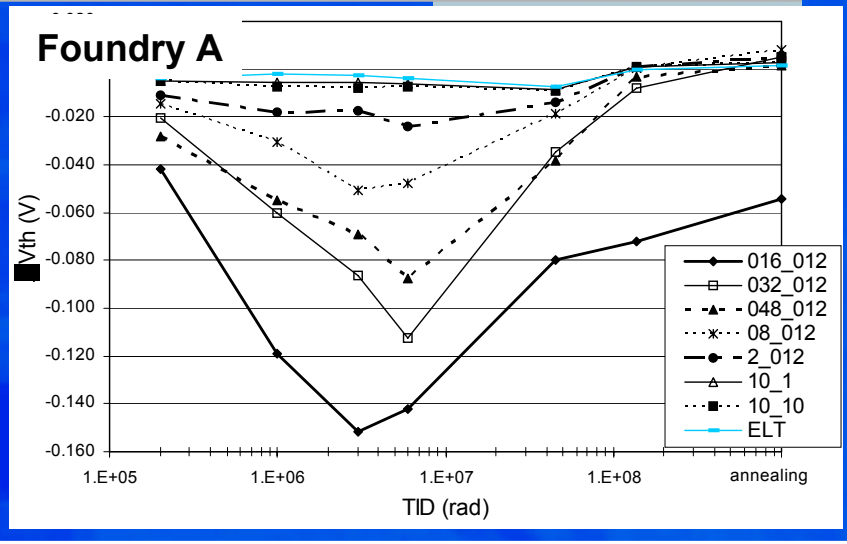


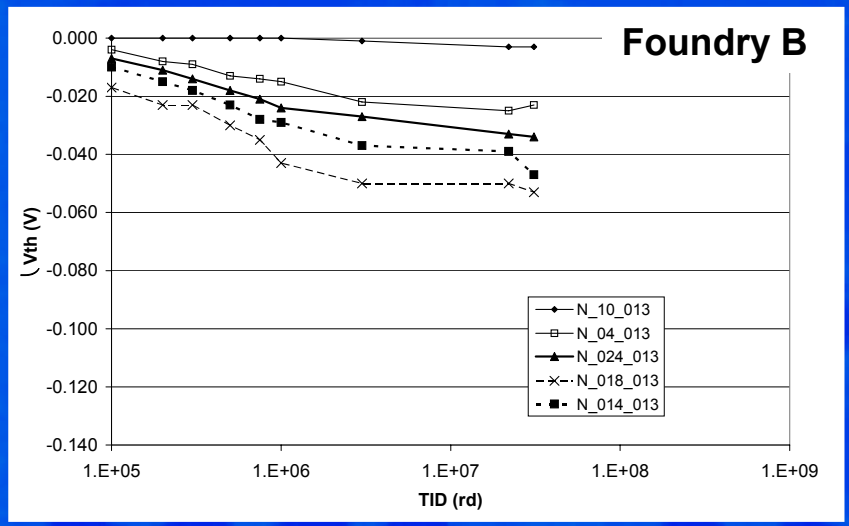


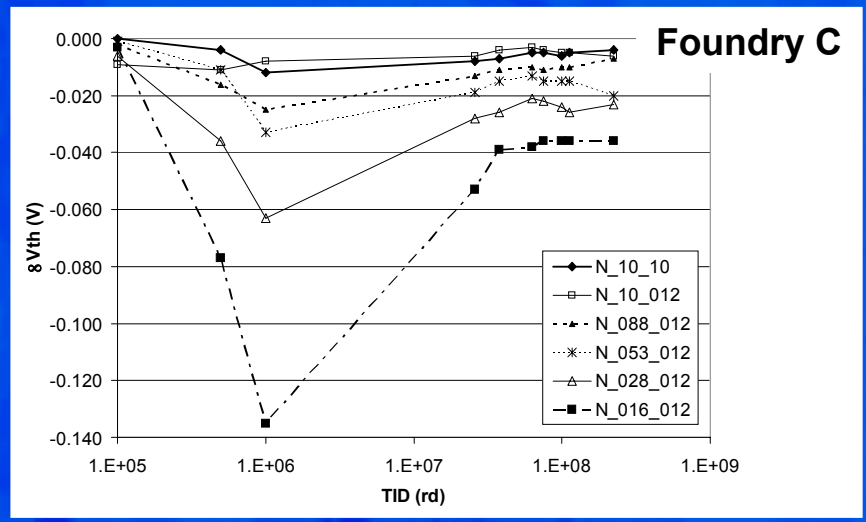


Core NMOS transistors, linear layout (4)

- Let's observe the effect on the **threshold voltage**
  - Peak in Vth shift at a TID of 1-5Mrad (A and C)
  - The narrower the transistor, the larger the Vth shift (RINCE)
  - Peaking dependent on dose rate and temperature, difficult to estimate in real environment
  - Sample from Foundry B different!

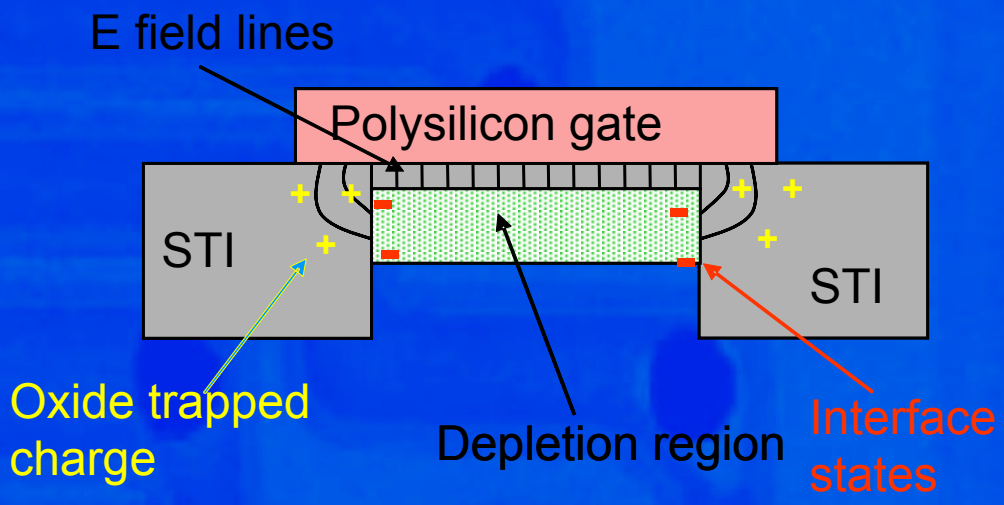


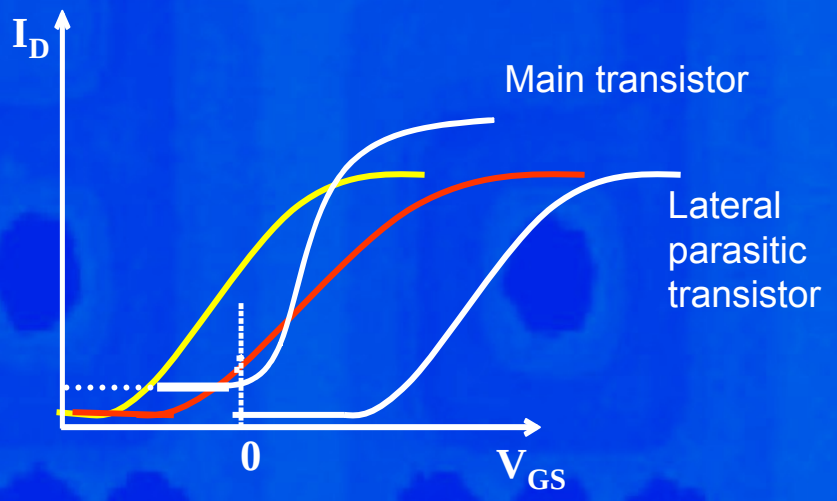




Radiation-induced edge effects - NMOS

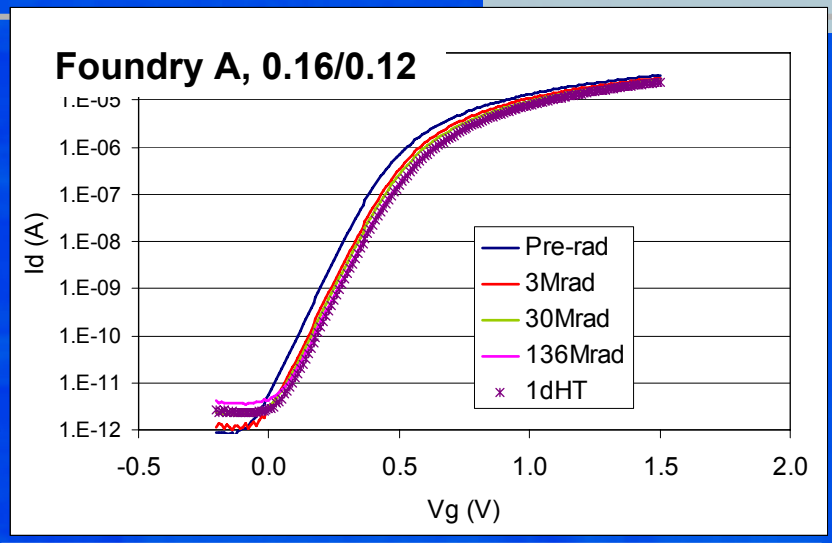
- The peak at 1-5Mrd in the leakage and Vth can be explained by the different evolution of charge trapped in the bulk of the lateral STI (positive) and in the interface states at the interface between STI oxide and silicon (negative)
- At the beginning of irradiation, charge trapped in the oxide dominates. With further TID, interface states eventually dominate. The relative contribution will depend on T, dose rate, etc.
- The narrower the transistor, the more important the influence of the charge trapped in the lateral STI and interface on the full depletion region => the more relevant the radiation effects => RINCE

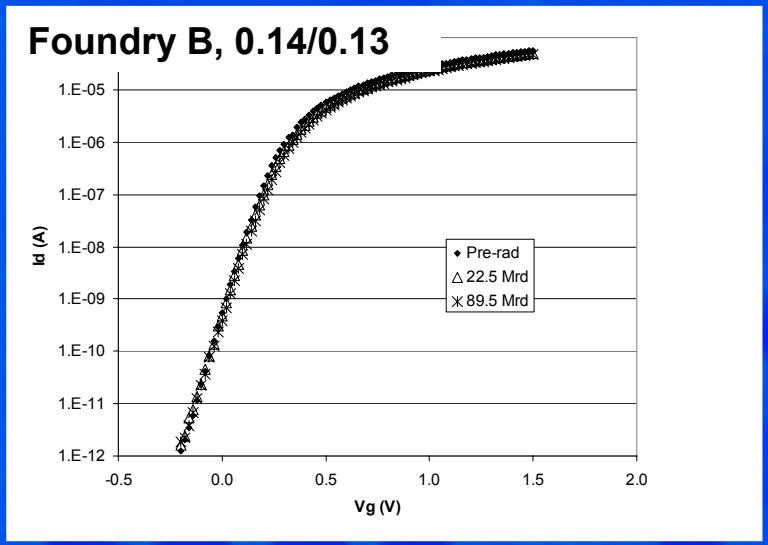


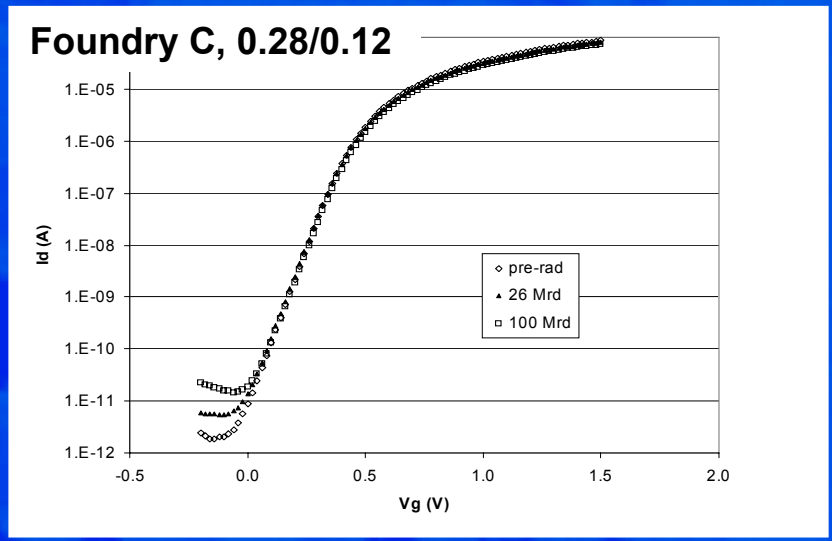


Core PMOS transistors, linear layout (1)

- ✓ No change in the weak inversion regime, no leakage
- ✓ An apparent Vth shift (decrease) for narrow channel transistors, more visible in samples from Foundry A
  - The narrower the transistor, the larger the Vth shift (RINCE)

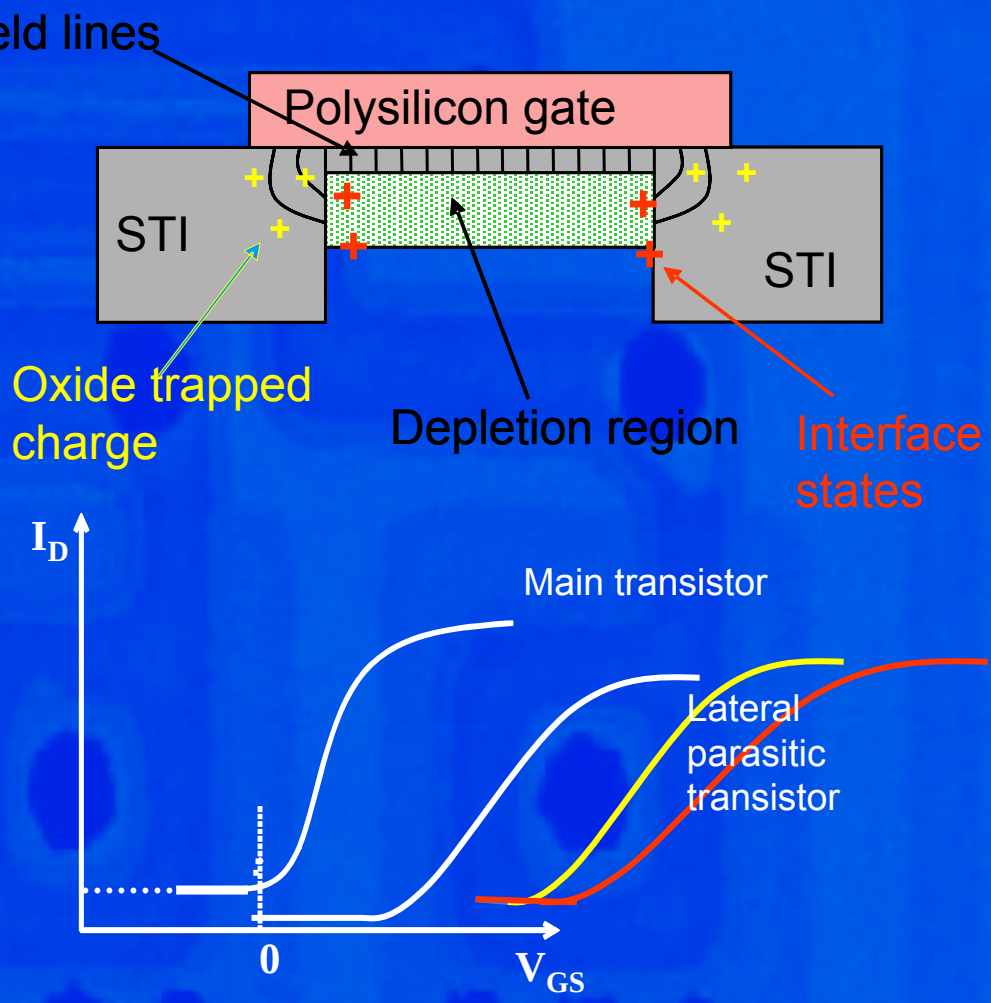






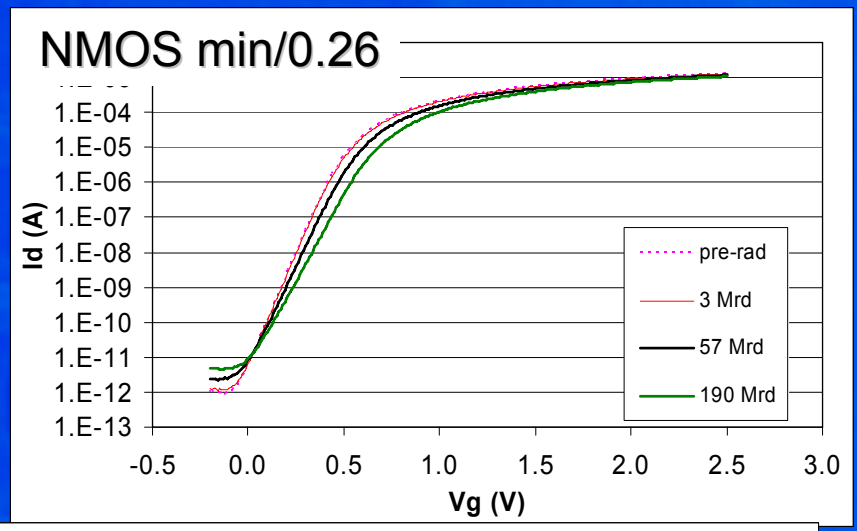
Radiation-induced edge effects - PMOS

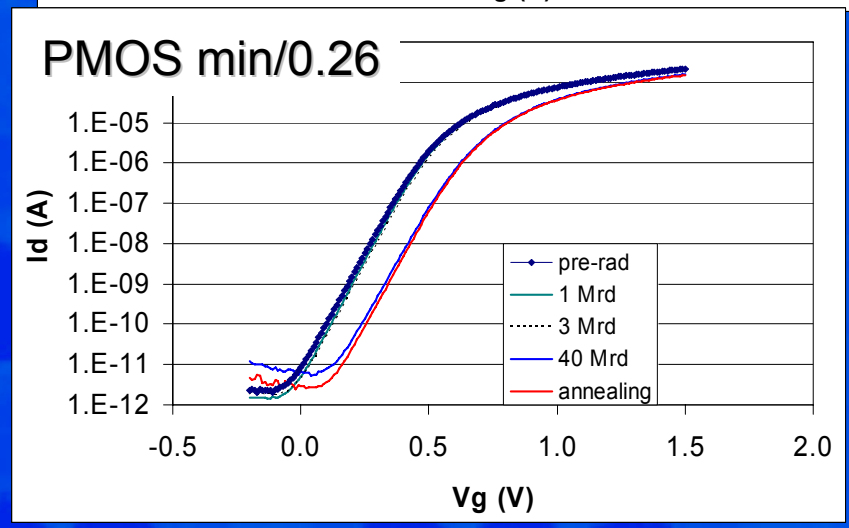
• IN PMOS, the charge trapped in both oxide traps and interface states are positive. Therefore, the threshold voltage of the lateral "parasitic" increases steadily and no leakage or deformation of the Id=f(Vgs) curve in weak inversion is observed.
• Nevertheless, in narrow transistors the charge trapped laterally can influence the electric field in the whole depletion region, inducing and apparent Vth shift.
•The narrower the transistor, the more important the influence of the charge trapped in the lateral STI and interface on the full depletion region => the more relevant the radiation effects => RINCE



I/O transistors, ELT

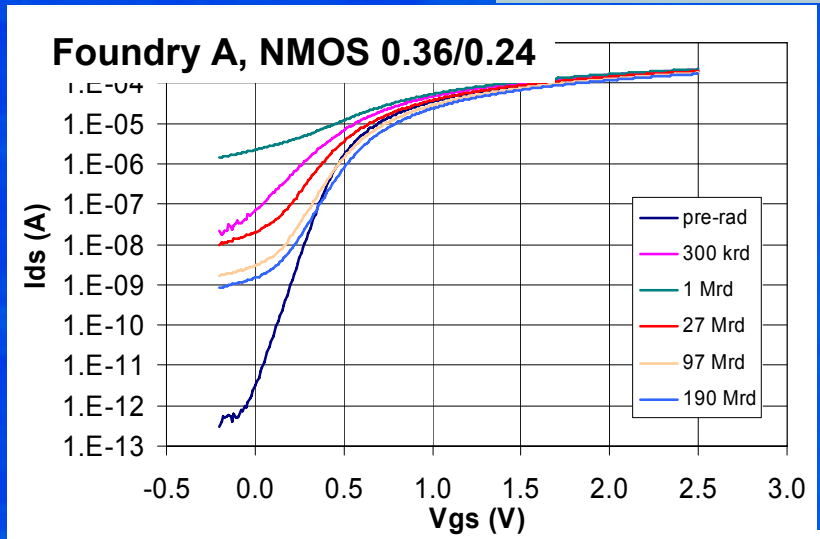
- ✓ Non-negligible effect on the Vth, especially for PFETs
- ✓ Shift larger than what observed in 250nm node in the past…

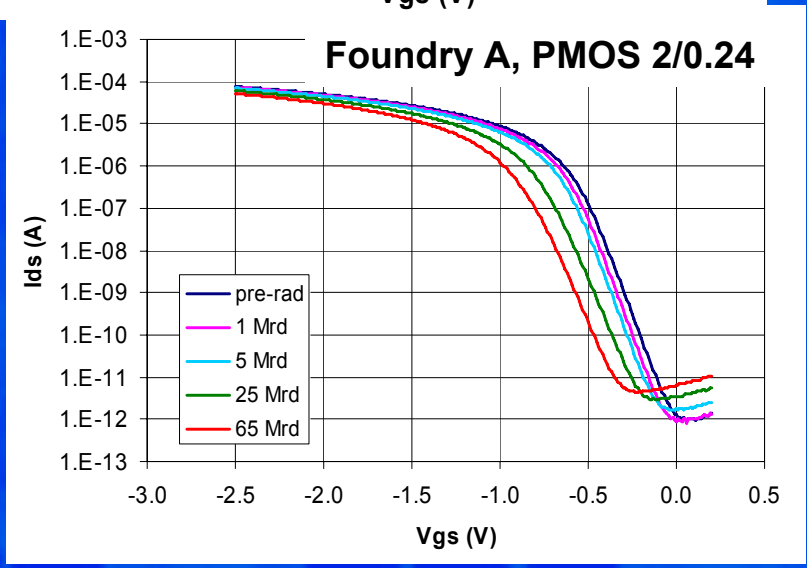




I/O transistors, linear layout

- ✓ Same qualitative effects as for core transistors, but larger impact on transistor parameters
  - Peak degradation at 1-5Mrd observed as well
  - RINCE observed as well
- ✓ Results different for different Foundries, but for all leakage in NMOS starts already at 50-100krad





130nm technology node for HEP

Outline

- ✓ The 130nm technology node
- ✓ Radiation effects in samples from different Foundries
- ✓ CERN Foundry Service in 130nm
  - Specific features
  - Radiation effects
  - Design Kits

Selected Foundry Services supplier

- ✓ Competitive tendering has taken place in 2006 (CERN rules for “frame contracts”)
- ✓ One Foundry has been selected to supply the serviceContract is for 130nm (and beyond) CMOS and BiCMOS
- ✓ CERN will organize MPWs and engineering runs as already provided in the 250nm node
- ✓ In the absence of sufficient demand, MPW service is now accessible via a broker. CERN organizes “grouped” access via the broker, since there is a minimum area to be purchased ($10mm^2$). Grouping allows users to prototype small chips for reasonable charges

130nm technology node for HEP

Outline

- ✓ The 130nm technology node
- ✓ Radiation effects in samples from different Foundries
- ✓ CERN Foundry Service in 130nm
  - Specific features
  - Radiation effects
  - Design Kits

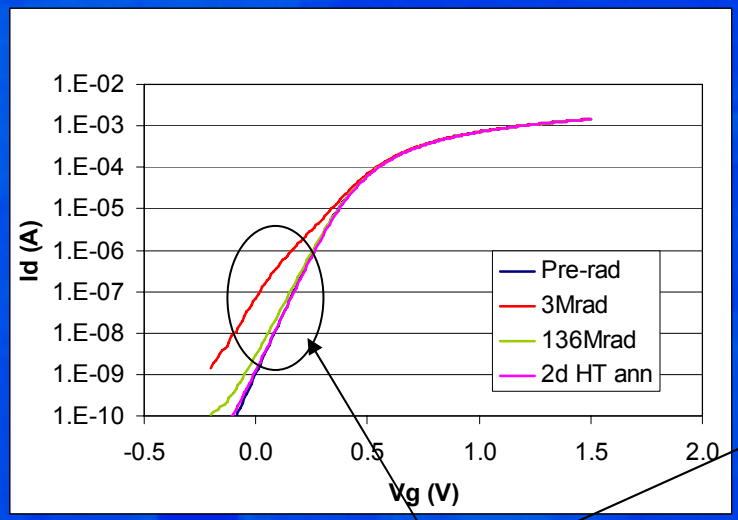
Natural radiation tolerance and its stability

- ✓ The use of ELTs and guardring renders the ASICs tolerant to TID safely and reliably – but the cost is performance (power, area) and effort (custom library)
- ✓ Can we rely on the “natural” tolerance of the technology, such that “standard” layout can satisfy our TID tolerance requirements?
- ✓ The question is complex and answers will be elaborated in the following few slides…
- ✓ NB: Radiation tests have been performed on this technology over time. Available hardware from Q1-2002 to Q1-2006 (4 samples at different times). In this time frame, the process went through final development and then production phase, possibly with significant changes. Nevertheless, radiation performance is very comparable!

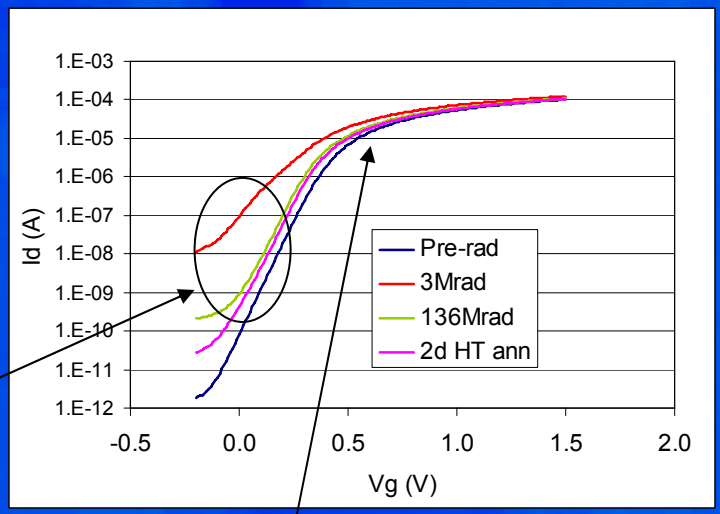
Core NMOS transistors

REMINDER of main effects:

Wide transistor (W>0.8um)



Narrow transistor (W>0.8um)



Leakage and “distortion” of weak inversion slope => all sizes

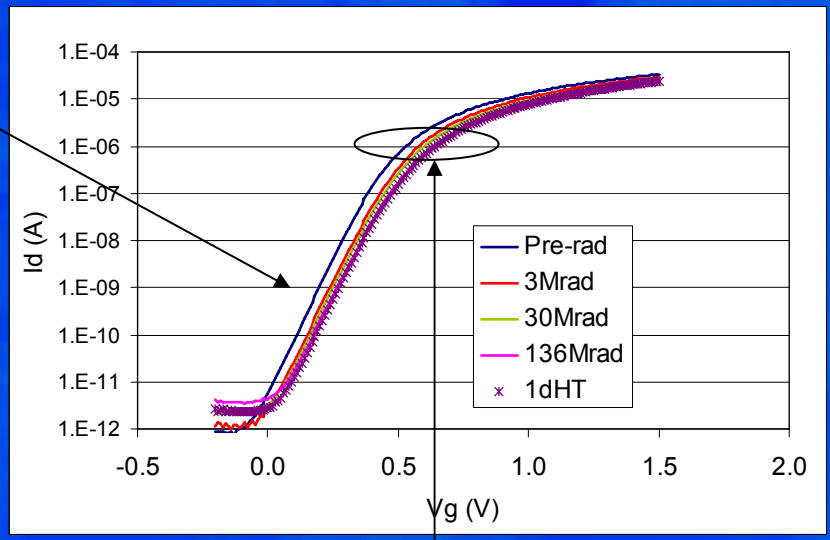
Influence on “main” transistor also in strong inversion => narrow transistors (RINCE)

There is NO sharp frontier between “narrow” and “wide”! RINCEs will be increasingly pronounced for narrower transistors…

Core PMOS transistors

REMINDER of main effects:

NO leakage or distortion of weak inversion curve

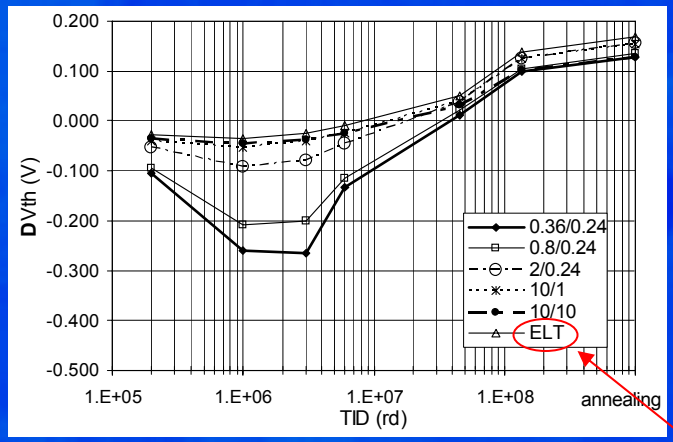


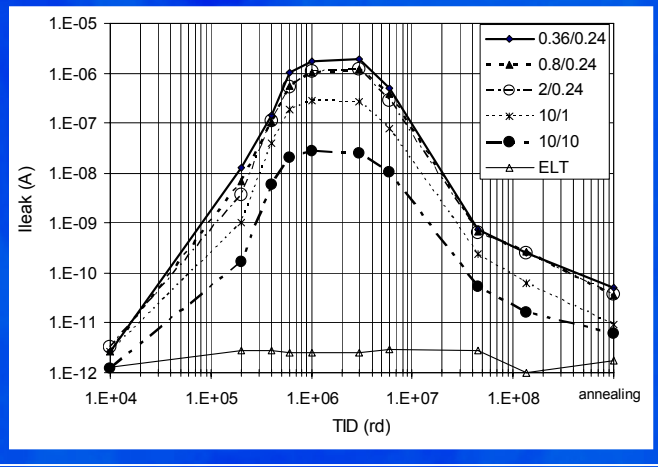
Slight Vth shift for the narrowest transistors only (0.16-0.3um)

I/O transistors

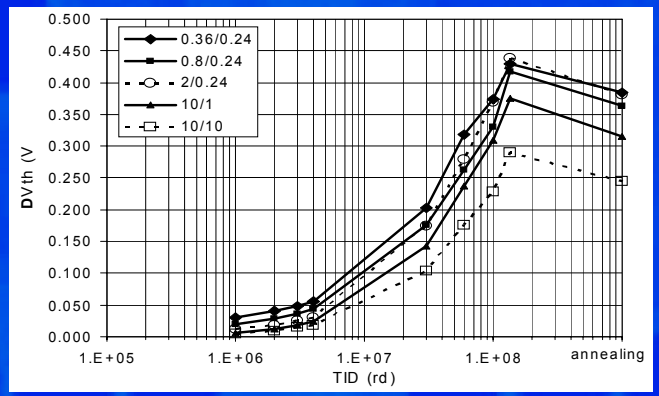
- ✓ Results qualitatively similar to Core FETs, but the impact of damage is more important

NMOS





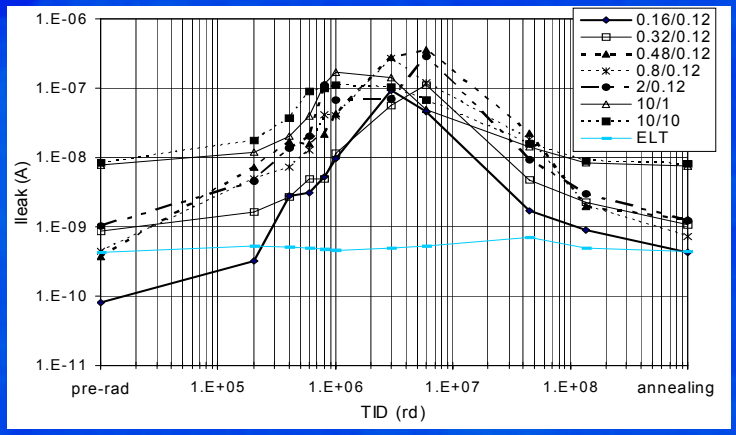
PMOS



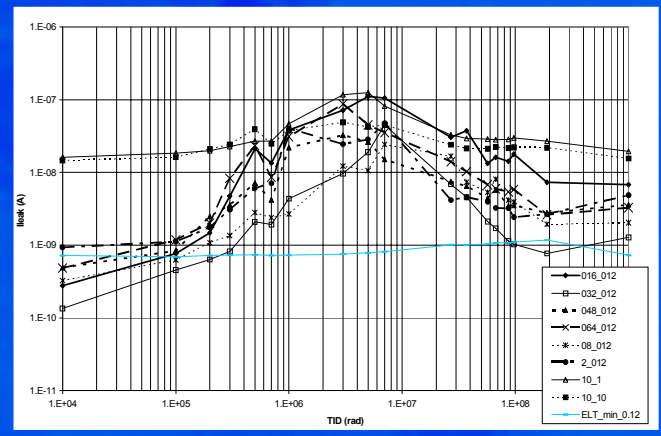
Notice that the radiation effects are important ALSO for ELTs (also for PMOS, not shown here)

Radiation-stability of Core NMOS FETs

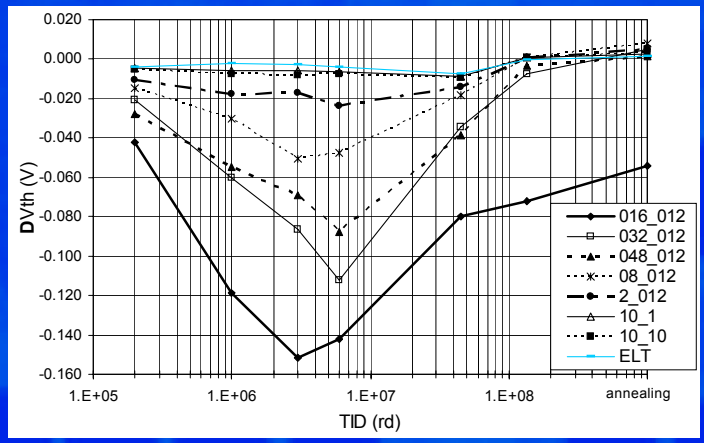
Exactly the same “test structure” was integrated in 2 runs (about 16 months apart). Results are compared here for the leakage current and Vth shift. They are well comparable (charts use the same scales)

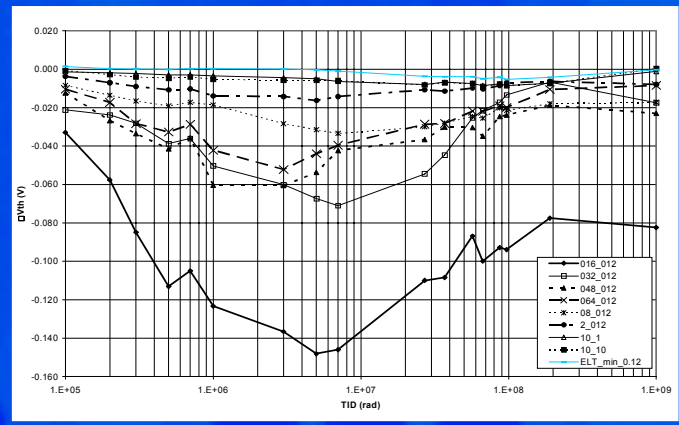


Run “CuTe2”



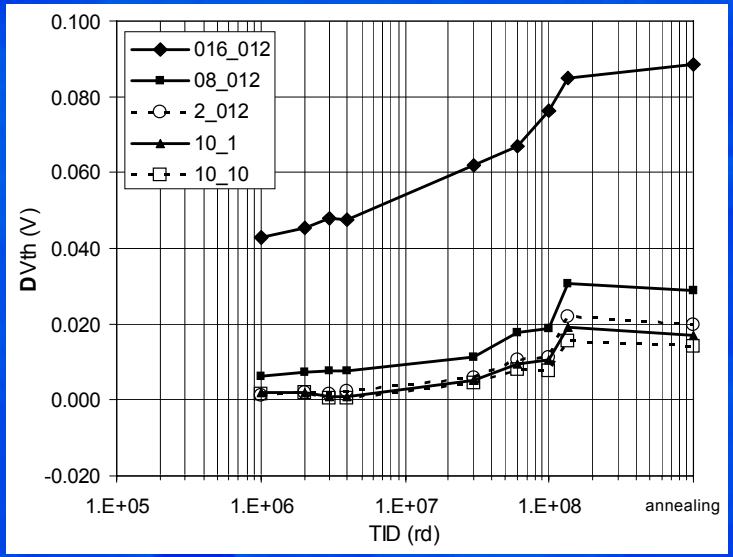
Run “CuTe3”



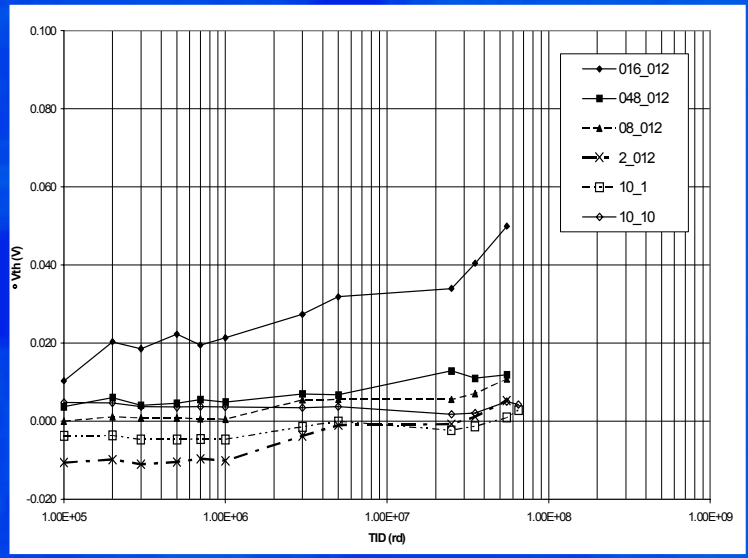


Radiation-stability of Core PMOS FETs

Exactly the same “test structure” was integrated in 2 runs (about 16 months apart). Results are compared here for the Vth shift. They are well comparable (charts use the same scales)



Run “CuTe2”

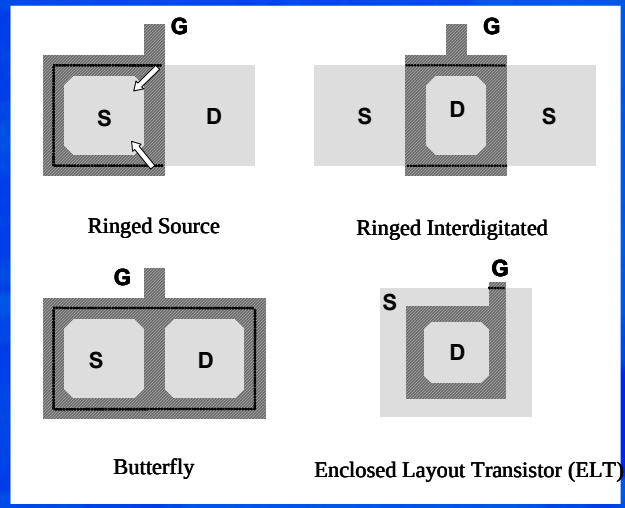


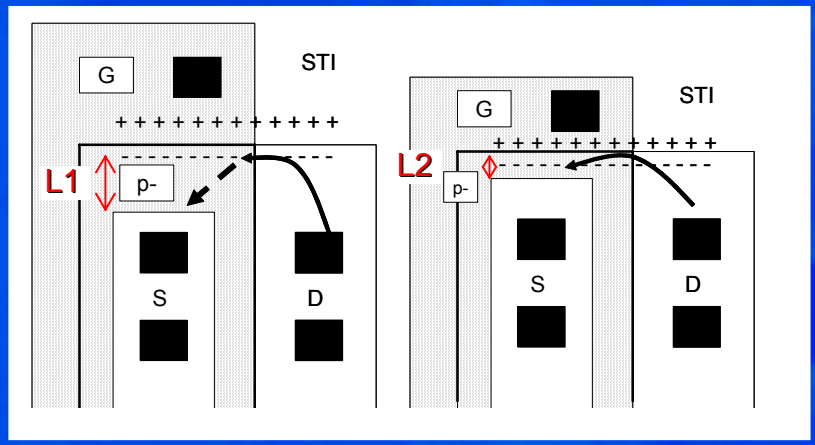
Run “CuTe3”

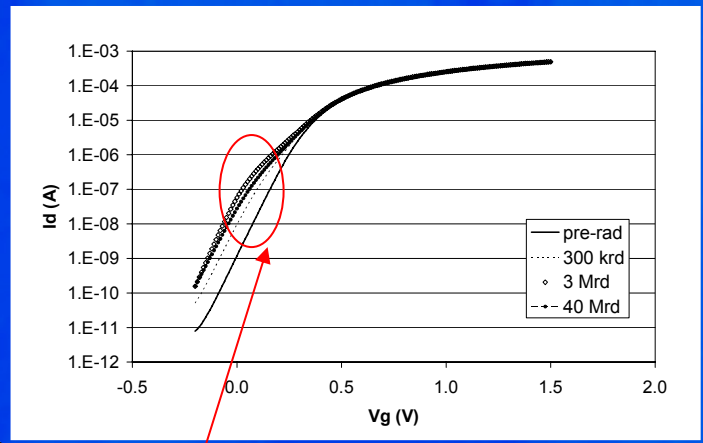
Results were very comparable for all other devices measured (I/O transistors, resistors, FOXFETs). **CONCLUSION**: the radiation tolerance does not seem to vary significantly with time, and to be sensitive to small process changes or fluctuations in the processing procedure.

Ringed layout

Alternative shapes for “hardness by design” based on ringed layout are not very attractive anymore in the 130nm technology node.
Influence of charge trapped in the STI can influence the inversion condition of the p- diffusion under the ring, and leakage can still appear (unless the overlap of gate on p- is very large)



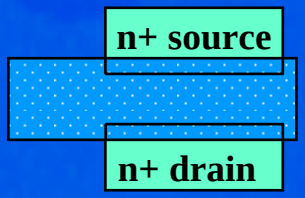


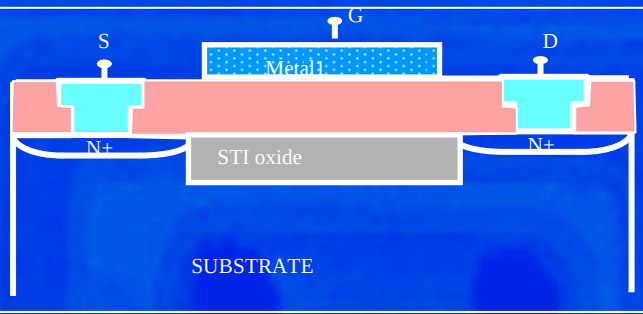


If overlap region L gets small (like L2), inversion in the p- under the poly can occur under the influence of the electric field induced by the charge trapped in the STI (indicated with + in the drawings). Therefore Leakage appears

Inter-device leakage

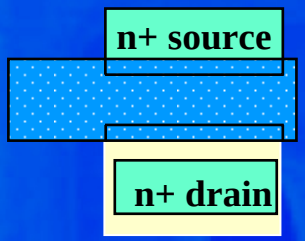
Measurements based mainly on FOXFETs (only p-doped substrate is relevant).
Diffusions/n-wells always at minimum distance compatible with design rules.

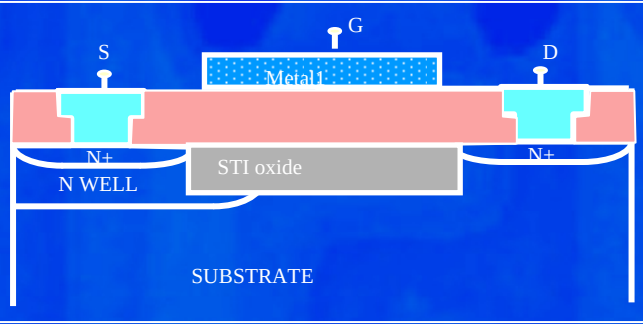




Between n+ diffusions

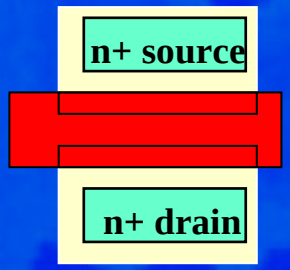
This FOXFET simulates the situation where two neighbor NMOS FETs have terminals at different potential

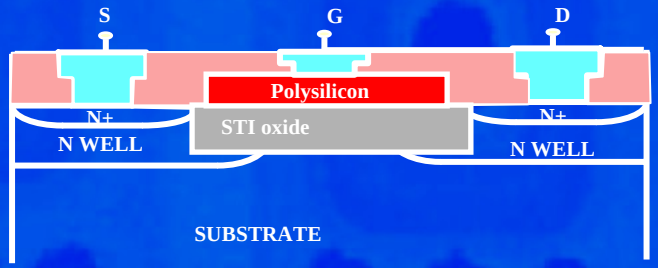




Between nwell and n+ diff

This FOXFET simulates the situation where an n-well at Vdd is close to an NMOS FET with diffusion at gnd (common case for logic circuits)

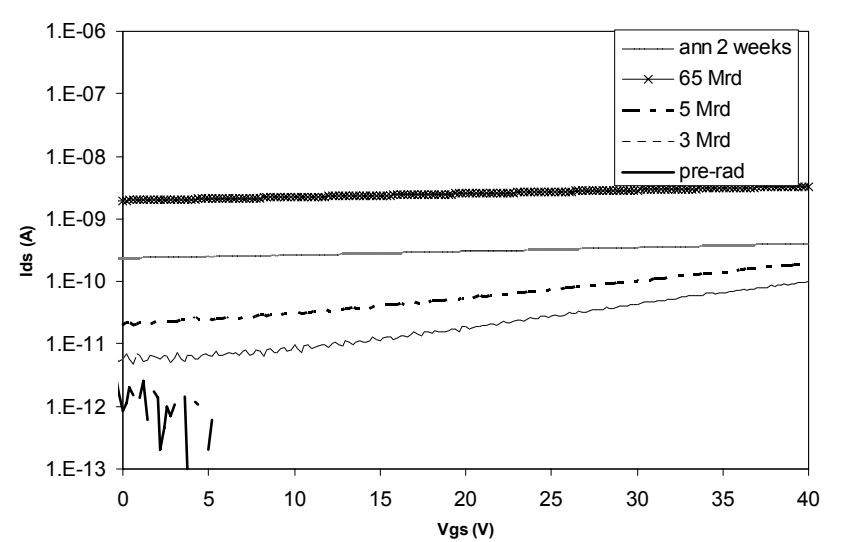




Between nwells

This FOXFET simulates the situation where two n-wells at different potential are close to each other (this happens only in analog, and seldom)

Leakage between NFETs



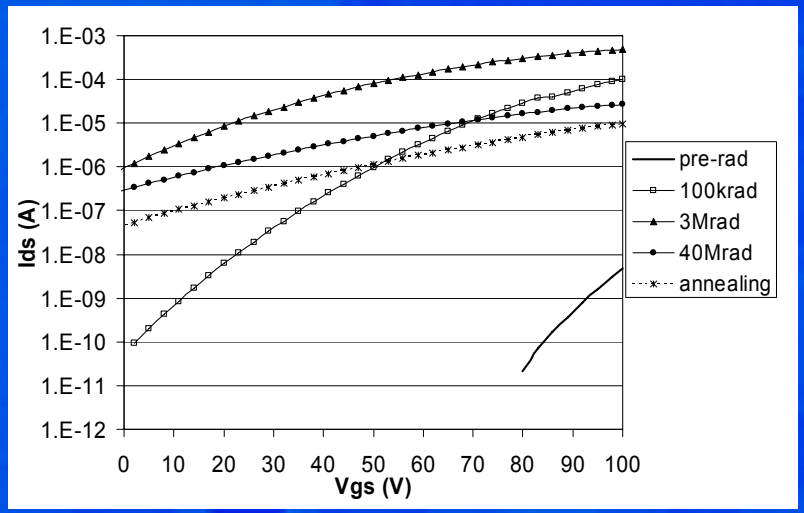
FOXFET with W=200um
Vgs=2.5V during irradiation

Leakage increases, but stays in the nA range.
This should not impact digital circuits (if their size is not in the 10^6 NFETs)
For analog design, issue only for very low current applications

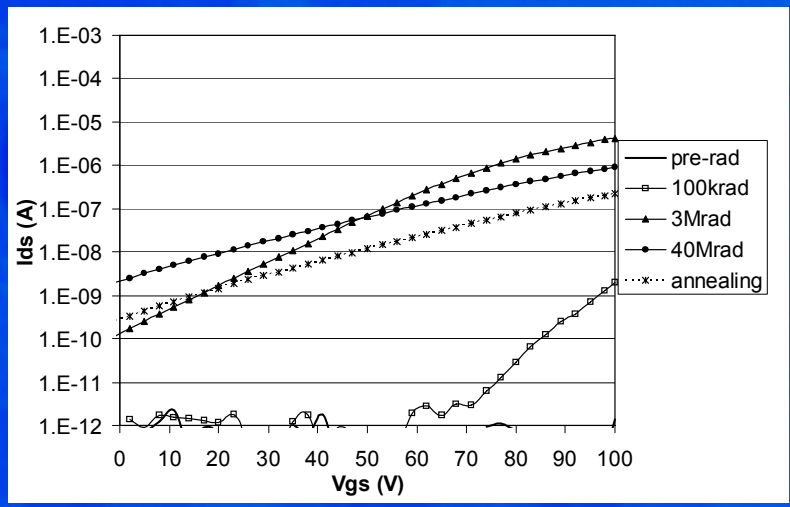
Leakage NFET-Nwell (1)

FOXFET with W=200um
Vgs=2.5V during irradiation

L = minimum allowed

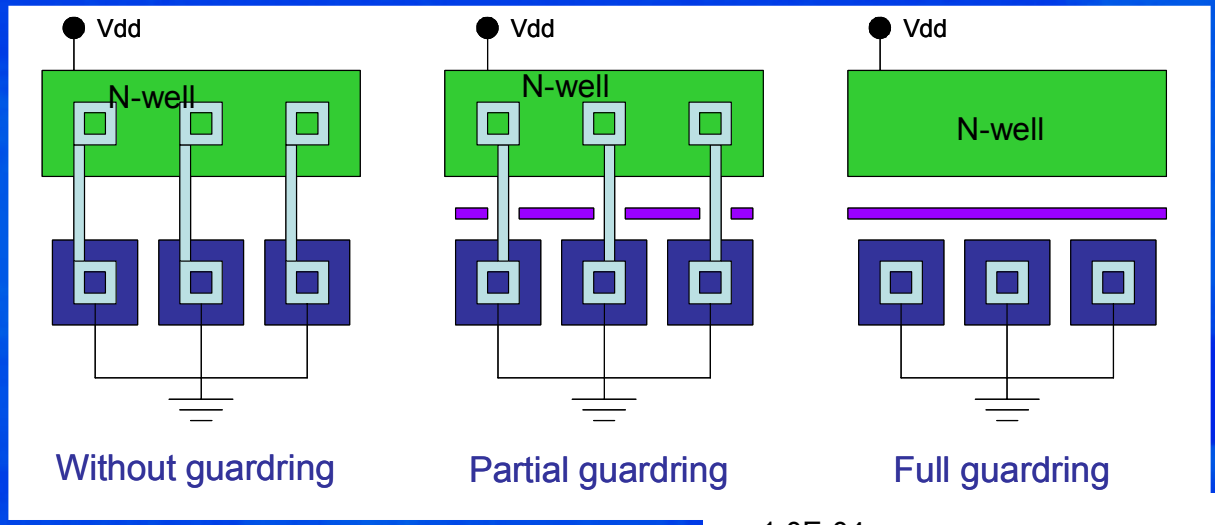


L = twice minimum allowed



The leakage level measured should not compromise the functionality of digital circuits (if their size is below a few 100.000 gates) even if space is left at minimum. Leakage peaks at about 3Mrd – as for NMOS leakage! Analog designers should be careful to this possible source of failure.

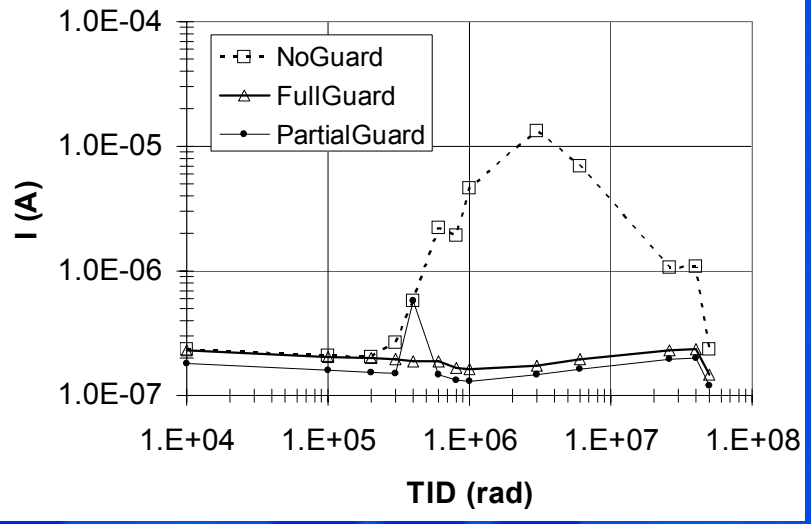
Leakage NFET-Nwell (2)



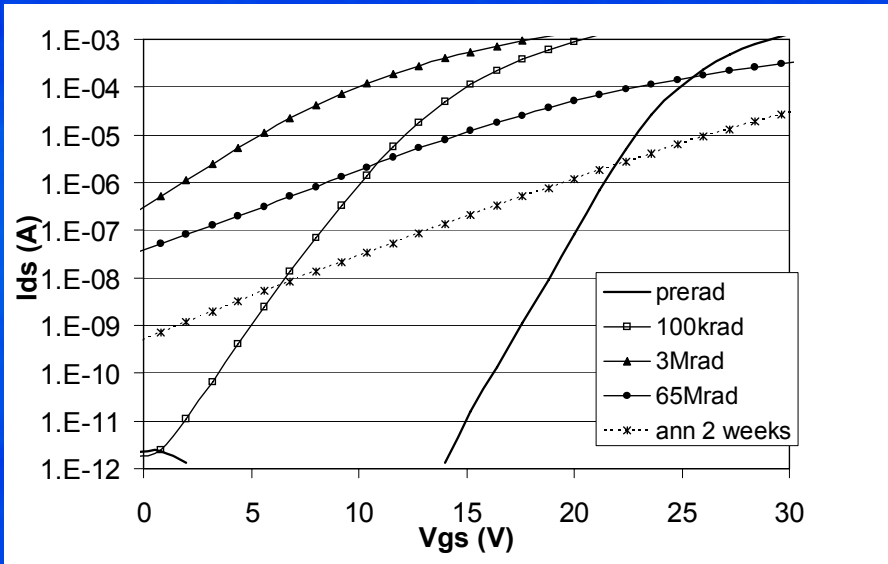
Three layout approaches have been tested in small logic blocks:

- -Standard (no separation)
- -Full p+ guardring
- -Guardring only where possible (without cutting poly connections between N and PFETs)

Irradiation results show that partial guardring is good enough to improve tolerance considerably



Leakage Nwell-Nwell

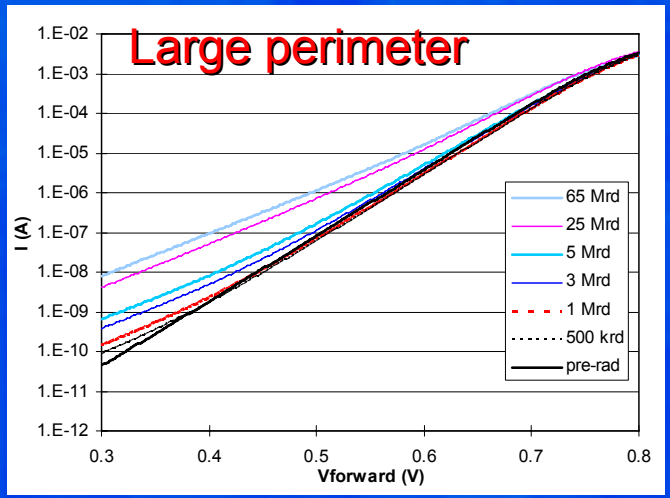


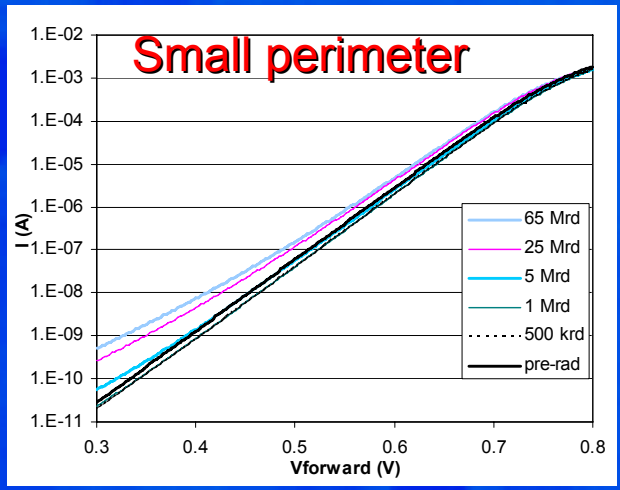
FOXFET with W=200um
Vgs=2.5V during irradiation

The leakage increase is maximum at about 3Mrd (as for NFET leakage!). This leakage has to be considered when designing analog circuits – especially when using N-well resistors or triple-well transistors.

Forward-biased diodes

Devices typically used in bandgap reference voltage circuits.
Two different layout used for the same area of diffusion (STI-bound):
-Small perimeter (one large diffusion)
-Large perimeter (parallel of large number of narrow fingers).
Irradiation performed under direct bias = 0.7V





Use the smallest perimeter possible in all cases, and at largest injection level!

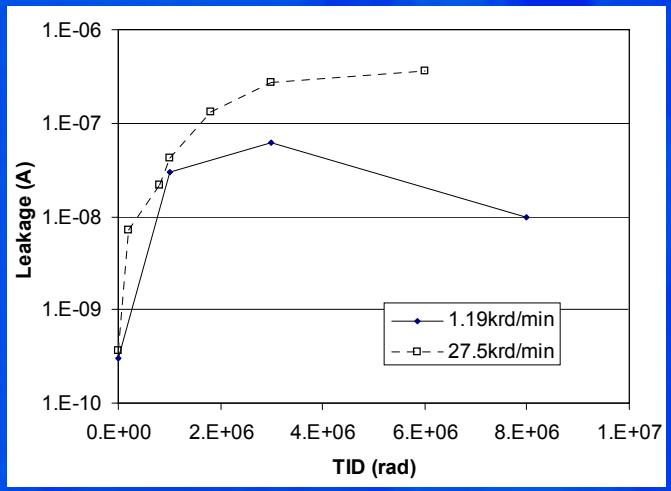
Diffusion resistors

- ✓ Two n+ diffusion resistors designed and measured:
  - Minimum width, nominal R=15.03 KΩ
  - W=1.5um, nominal R = 2.52 KΩ
- ✓ Measured values 17.12 and 2.52 KΩ (tolerance on minimum width is larger!)
- ✓ Irradiated up to 65Mrd, with changes of the order of 1%

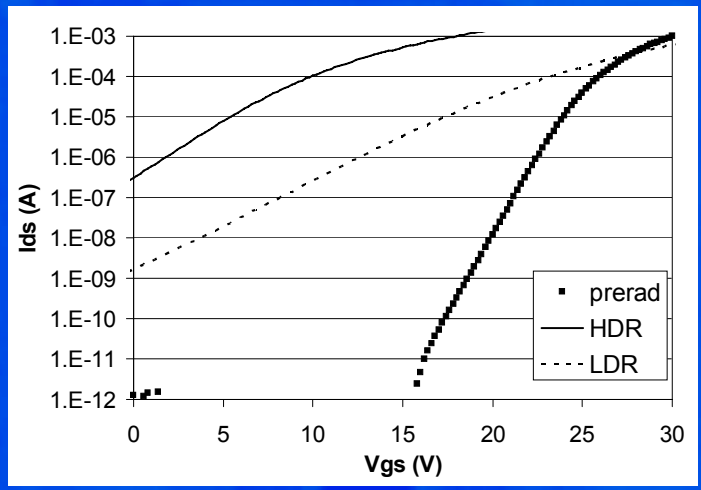
Why all previous results are worst case (1)

1. Relevance of dose rate

All results shown refer to high “laboratory” dose rates typically above 20krd/min. In real applications, the dose rates will be 2-3 orders of magnitude below. Since the radiation response is governed by the combination of oxide trapped charge and interface states, the overall damage depends on temperature and dose rate.



0.48/0.12 NFET leakage at different dose rates: the increase is considerably smaller, and reaches the peak value at lower TIDs, for the smaller dose rate

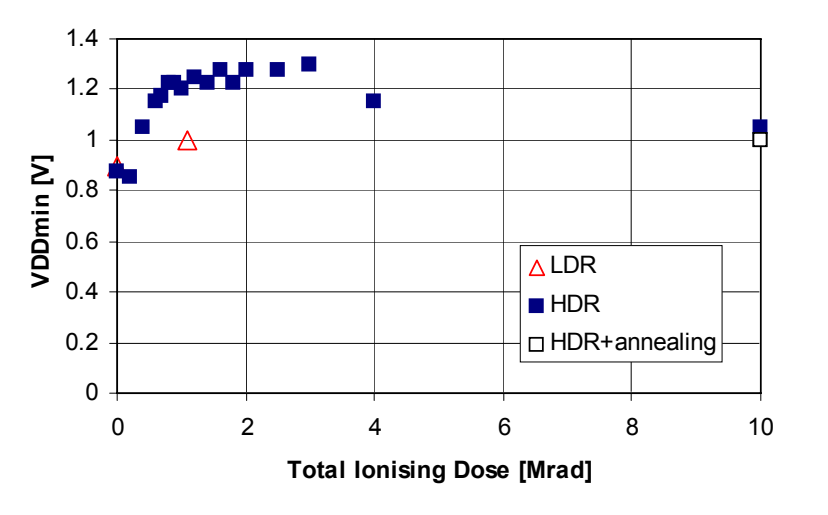


Current of FOXFETs with n-wells (size=200/min) at two very different dose rates: 24.4krd/min (HDR) and 65rd/min (LDR). Again, current is much smaller at low dose rate.

Why all previous results are worst case (2)

1. Relevance of dose rate

All results shown refer to high “laboratory” dose rates typically above 20krd/min. In real applications, the dose rates will be 2-3 orders of magnitude below. Since the radiation response is governed by the combination of oxide trapped charge and interface states, the overall damage depends on temperature and dose rate.



TEST circuit: 16kbit SRAM designed with a memory generator (commercial design, no ELT or guardring, and dense layout).

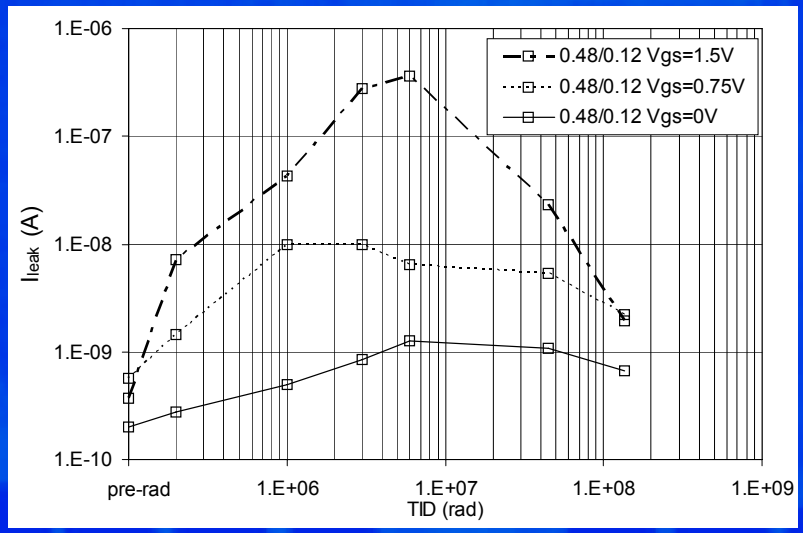
VDDmin is the minimum supply voltage for error-free functionality at 10MHz. Before irradiation, VDDmin is about 875mV. With irradiation at 24.4krd/min (HDR), VDDmin increases and peaks at 1-6Mrd, to decrease when the TID reaches 10Mrd. With irradiation at 65rd/min (LDR), the increase in VDDmin is very marginal.

Why all previous results are worst case (3)

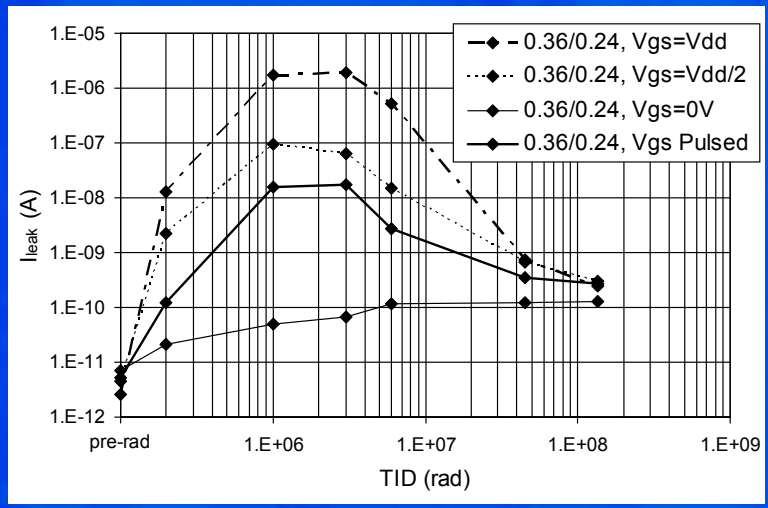
1. Relevance of applied bias

All results shown on NFETs and FOXFETs have been obtained with DC "worst case" bias:
-NFETs: all terminals grounded except gate at Vdd (1.5V)
-FOXFETs: all terminal grounded except gate at 2.5V
Bias has an important influence on the degradation, as shown in the results below from M.Silvestri (Dept. of Information Engineering, University of Padova, Italy): the radiation-induced increase in leakage depends strongly on applied bias.

Core NFETs



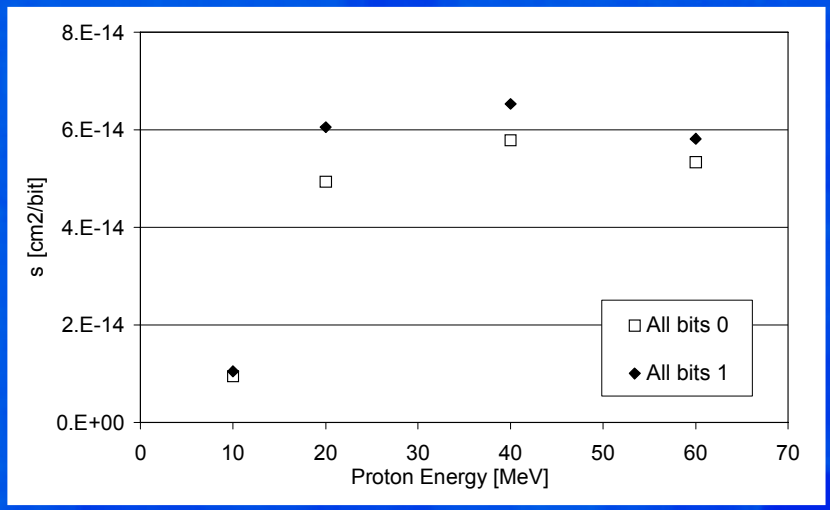
I/O NFETs



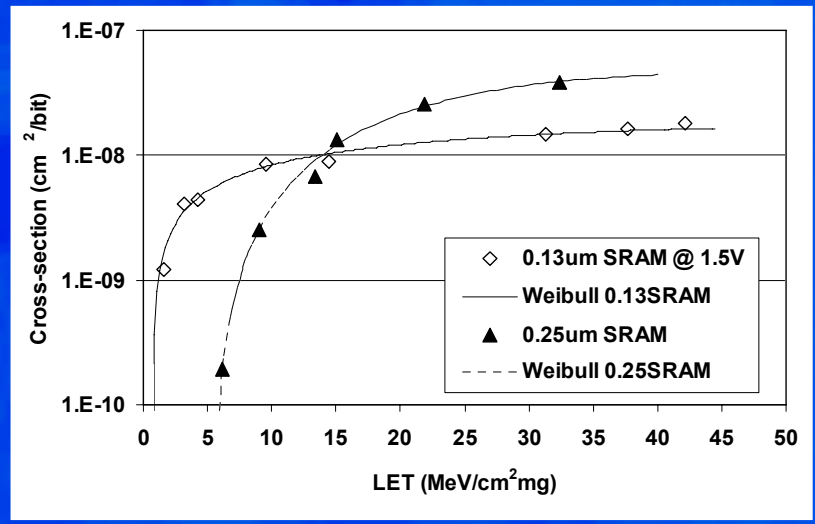
Pulsed=digital-like (1MHz, 50% duty cycle)

Single Event Upset

Sensitivity has been tested twice:
-With protons on a sample provided by the foundry (16k x 16 SRAM) in 2001
-With heavy ions on a 16kbit SRAM designed using the commercial memory generator
-No SEL ever observed



Foundry sample irradiated with mono-energetic protons. The cross-section curve has been obtained with Vdd=1.5V, and shows no significant difference for “all 1” or “all 0” patterns, and large sensitivity at low energy



Custom SRAM irradiated with Heavy Ions, and compared to the cross-section measured for the SRAM in the “CERN Radiation-Tolerant” library in 0.25um. The 130nm SRAM has a much lower LET threshold. In an LHC-like environment, this translates in increased sensitivity (15-30 times larger!).

Summary for designers (1)

- ✓ Analog design
  - Core FETs ok, however
    - Avoid narrow transistors (RINCE)
    - Use ELTs for devices in weak/moderate inversion
  - Isolation
    - Neighbor NFETs: ok unless very small current
    - Nwells surrounded by guardring if the Nwell is sensitive to leakage (small current) and if neighbor NFETs are sensitive to small leakage
    - Generally enclose with guardrings nodes sensitive to small leakage currents
  - Diodes
    - Use forward-biased diodes with max perimeter/area ratio and at max injection
  - I/O FETs are quite sensitive to TID, expect large leakage and Vth shifts

Summary for designers (2)

- ✓ Digital design
  - Core gates
    - Use of the commercial library cells should be OK unless the circuit requires the ultimate performance from the technology. This still needs to be confirmed by a real demonstrator.
    - If custom cells needed, same recommendation as for analog design
  - I/O cells
    - The suitability of using the commercial library cells still has to be assessed – only 1 test on few cells has been made so far (result good, but not very representative)

Summary for designers (3)

- ✓ Single Event Effects
  - SEU
    - The sensitivity is larger than for the 0.25um technology, and mitigation techniques are required for SLHC applications
  - SEL
    - No evidence in any test, and very unlikely due to technology (dopings, STI) and voltage supply. Nevertheless, limit resistance to Vdd and Gnd by placing always lots of contacts across the circuit.
  - SEGR
    - Although this should not be an issue, sensitivity will be tested later in 2007 (with an heavy ion irradiation on dedicated test structures).

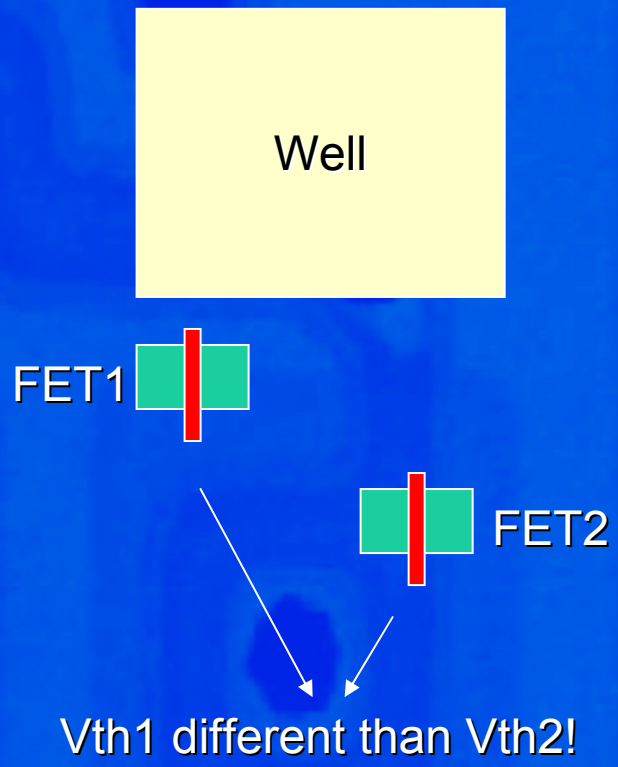
130nm technology node for HEP

Outline

- ✓ The 130nm technology node
- ✓ Radiation effects in samples from different Foundries
- ✓ CERN Foundry Service in 130nm
  - Specific features
  - Radiation effects
  - Design Kits

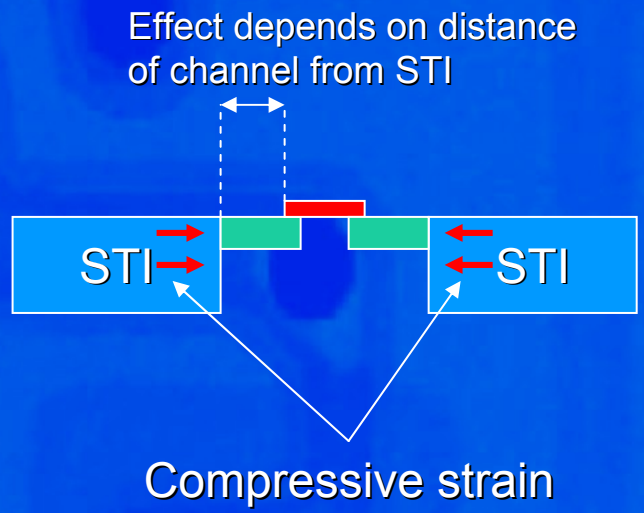
Well proximity effect

- ✓ High energy well implants result in significant scattering of dopants at the well edge, increasing the net doping level and hence threshold voltage for FETs near a well edge
  - The effect is modeled by 1 parameter (which is extracted for post-layout simulations), for estimation – simulation will not be very precise, and it will not depend on the specific layout
  - The use of good design practices for sensitive devices is necessary – place the sensitive devices far from the wells



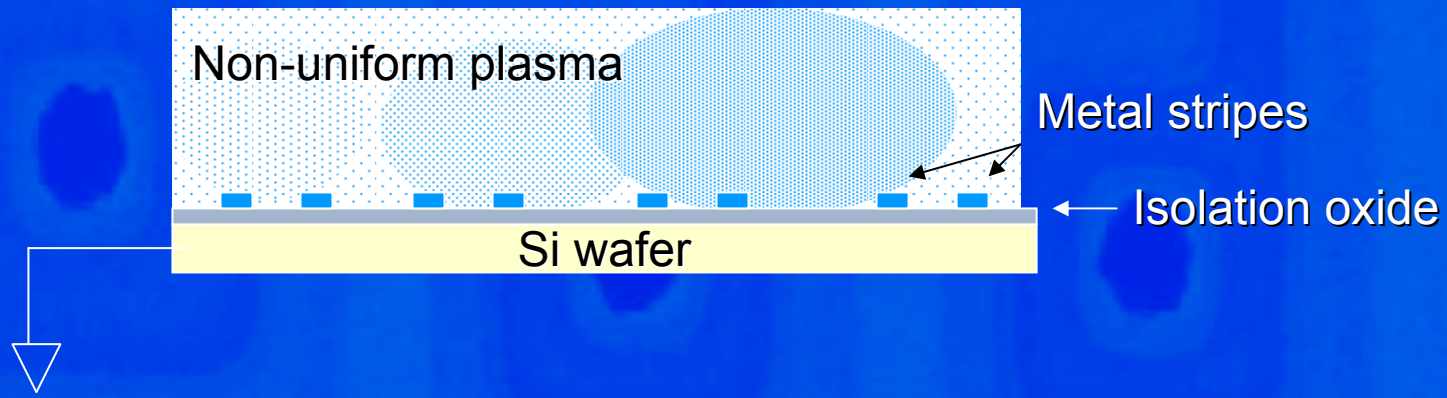
Isolation-induced stress

- ✓ STI induces compressive strain in silicon, which alters mobility of FETs
  - Ids increases for NFETs, decreases for PFETs
  - This effect is modeled for simulation purposes with two parameters, which can be hand calculated (geometric size to measure in the layout)
  - Extraction from layout is fully supported for post-layout simulation



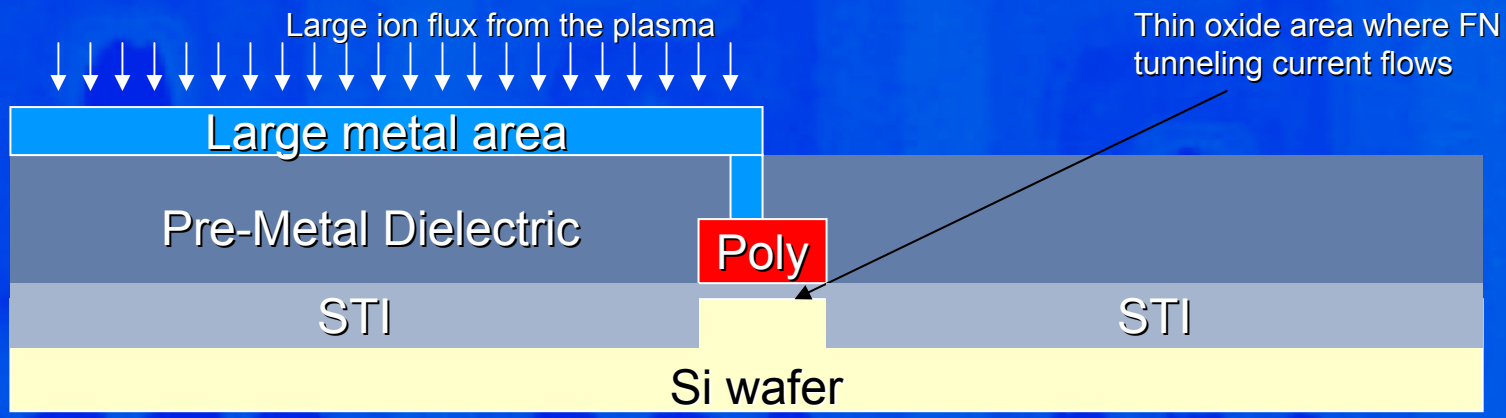
Gate damage due to plasma charging (1)

- ✓ Many processes step for wafer manufacturing take place in a plasma
- ✓ Isolated metal stripes in a non-uniform plasma get charged at different potentials. The wafers substrate is at one only potential (typically grounded), and an electric field builds up in the oxide isolating the metal from the substrate
- ✓ In the absence of any current from substrate to metal, large voltage differences can be reached – exceeding breakdown of the isolation oxide if this is thin (such as the gate oxide)



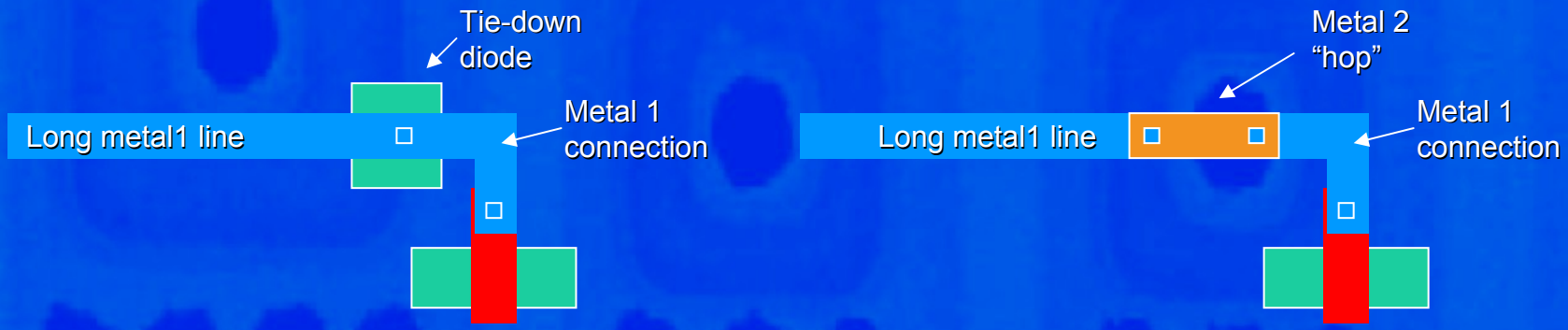
Gate damage due to plasma charging (2)

- ✓ Before the voltage differences reaches breakdown, a current starts flowing across the thin oxide (Fowler-Nordheim tunneling). Current is from electrons injected from substrate to metal
- ✓ This current roughly needs to compensate for flux of positive ions on metal from the plasma. The larger the flux, the larger the current required
- ✓ If large area of metal is exposed to ions, the flux on the metal is large. If the metal is connected to a small area of thin oxide, the FN tunneling current per unit area needs to be large => large voltage across the gate oxide THIS IS CALLED AN ANTENNA!
- ✓ This condition leads to damage to the gate oxide, with consequences on the transistor performance => Vth shift, gate dielectric leakage and increased oxide reliability failure



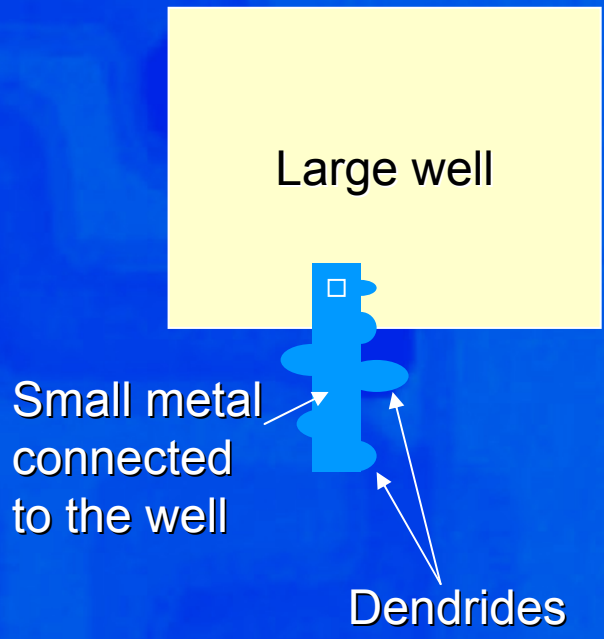
Gate damage due to plasma charging (3)

- ✓ To avoid damage, Design Rules limit the allowable ratio of PC/Metal to thin oxide area. This applies individually to all metal layers (it is not cumulative across layers)
- ✓ Solutions to avoid damage:
  - Add “tie-down” diodes, connected via M1 to the PC (in this case, the limit ratio from the design rules still applies but the tie-down diode area sums – with multiplication coefficient – to the thin oxide area). At wafer processing temperatures, diodes are very conductive and allow current to flow from metal to substrate
  - Introduce “hops” to next metal level. Before the “hop”, only the area of the metal already connected to the thin oxide counts for the antenna. When processing the next metal level, only the (small) area of the “hop” counts for antenna.



Copper dendride formation

- ✓ This is a complex effect that can take place during processing of copper metal layers
  - Potential differences built across wells (n and p- wells) can generate currents in the solutions where processing related to a copper metal layer is taking place
  - The induced currents will form “dendrides” around the copper metal line connected to the well, which can lead to shorts to neighbor lines in the same metal level
- ✓ To prevent this to happen, Design Rules have been introduced
  - Ratio of metal to well area has to be large

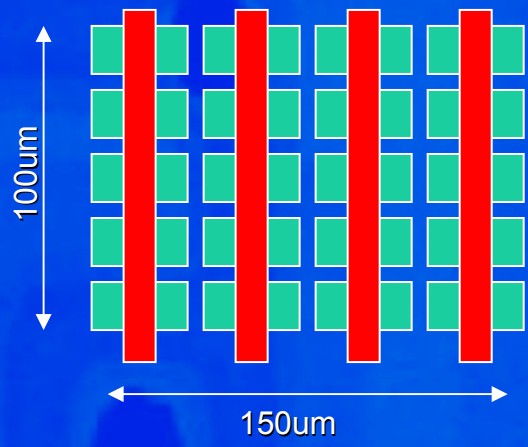


Pattern Density

- ✓ STRICT requirements exist for density of each of the following layers: RX (active area), PC (poly), all metals
- ✓ Requirements are both for the full chip (global rules) and for any small area of it (local rules)
  - Global rules set the limit – upper and lower density – for the full chip
  - Local rules set the limit – upper and lower density – for areas about 100um wide stepped by about 50um across the full design
- ✓ After tape-out, automatic routine at the Foundry will fill in all layers (“filling”), and produce holes in copper layers (“cheesing”). This is unavoidable
- ✓ Some consequences:
  - It is not possible to place “exclude” shapes over area where filling is not wanted. To prevent random metal shapes to be placed over sensitive portion of the design (for instance, where matching is important), cover the sensitive area with uniform metal
  - Some designs that produce excessive local density CAN NOT be manufactured. Example: regions with too large usage of RX. This error is spotted by running a check that predictively estimates the final densities after filling.

Example:

Large array of large transistors (for instance, a large current mirror)



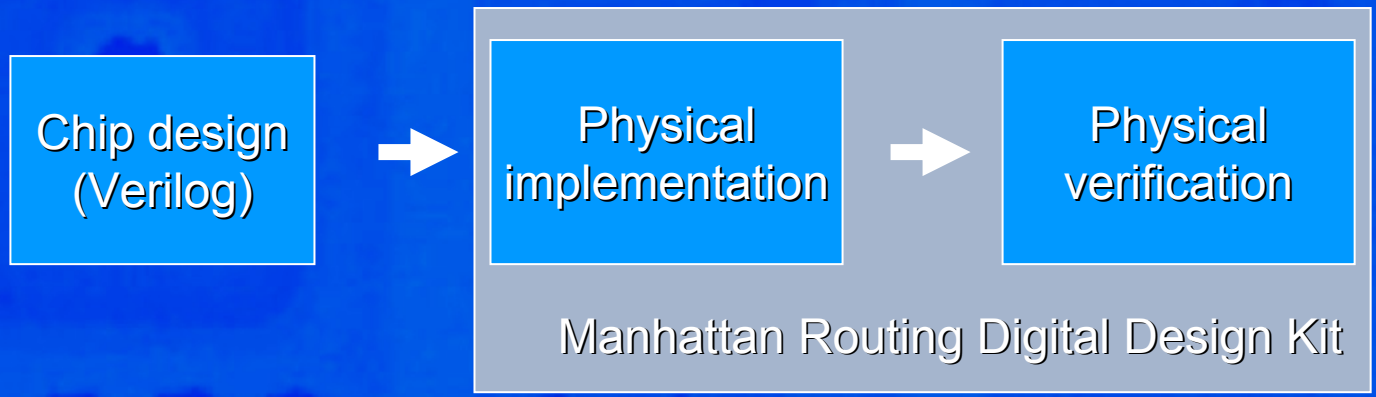
Local RX density migh be eccessive here!
The design HAS to be modified or it will be rejected from fabrication!

Check procedure before tape-out

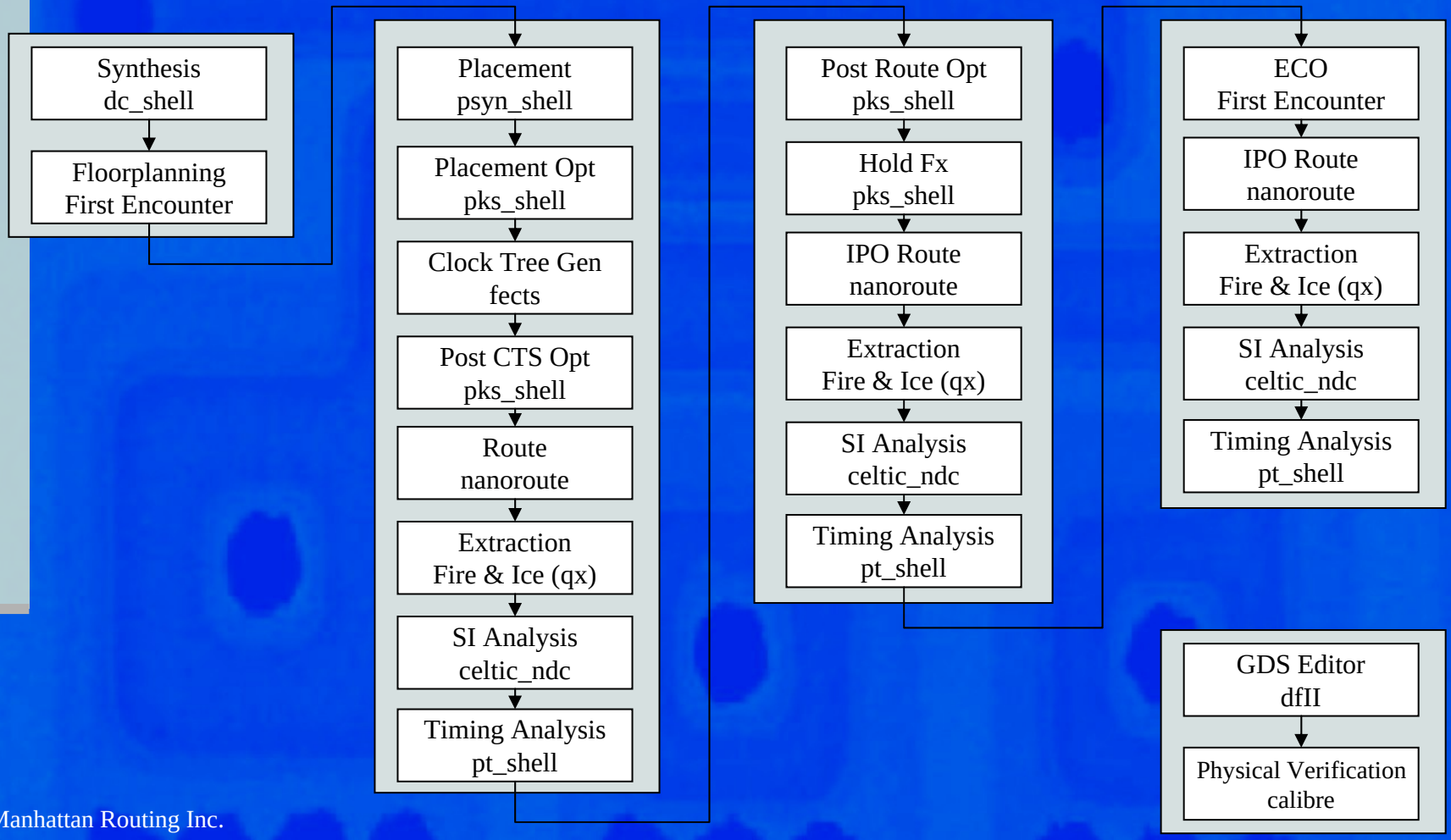
- ✓ Due to antenna, dendride formation, filling and other complex rules, the checking procedure before tape-out requires several steps just for Design Rule Check (DRC)
  - Check “ground rules” (GR), or rules mainly related to geometrical requirements
  - Check floating gates and antennas to ensure rules related to plasma damage and dendride formation are satisfied
  - Check global density
  - Check (predictively) local density – the design can be filled at the Foundry to meet all local density requirements
- ✓ All these checks can be performed with Assura (Diva has very limited use for checking). Calibre should also be able to do the job, but we have no experience with it
- ✓ NB: procedure to get “waivers” as we were used with the quarter micron is now much heavier and given the complexity of the technology the risk is also higher

Digital design flow

- ✓ The complexity of the technology, its high performance, and the need for minimizing expensive prototyping cycles drives the need for sophisticated tools for digital design
- ✓ A full library is available from a commercial supplier, but how to merge it with the foundry design kit in an optimized and standard design flow?
- ✓ The task of rationalizing the digital design flow and to providing a common platform for design tools has been outsourced to Manhattan Routing Inc. (MRE)



The MRE Digital Design Flow in detail



Manhattan Routing Inc.

User point of view

- ✓ The design flow uses specific tools
- ✓ Users shall use the same tools, and the appropriate versions of those, to be able to run the flow correctly
  - Tools and versions used in the latest release of the Design Kit (V1.3):

Tool	Version
CADENCE DFII	IC5.1.4.1
First Encounter	4.1.USR5
Fire & Ice	SEV_3.2
Prime Time	X-2005.12-SP2
CeltIC	TSI42_USR1
Calibre	2004.3_9
Synopsys DC, PC	2004.6.SP1
CADENCE Incisive Simulator	IUS_5.7

- ✓ 1-week courses with limited attendance (10 people) are organized periodically at CERN. 3 such courses have already been given by MRE personnel, and another one is planned

130nm technology node for HEP

Summary

- ✓ CERN will offer a Foundry Service, as already done in the 250nm node, for the 130nm
- ✓ both CMOS (mixed-signal) and BiCMOS (with SiGe HBTs) can be offered
- ✓ Radiation tolerance of the CMOS technology:
  - It has been tested extensively, and a dedicated HBD digital library does not seem needed
  - A set of recommendation to the use of the technology for designs that have to operate in a radiation environment is available
  - The stability of the natural radiation tolerance will be monitored frequently
- ✓ Cadence-based PDK is available
- ✓ Digital library is available
- ✓ Both PDK and library are distributed within a “Design Kit” from Manhattan Routing Inc., together with a Design Flow for complex digital design
- ✓ CERN-organized MPW runs will start as soon as demand for silicon is sufficient to bring price to competitive level. In the meanwhile, frequent runs are accessible via a broker (CERN can act as contact for such runs)