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Ultra-thin Tracking Detectors for ILC and Other Applications

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Outline

- Short introduction to semiconductor (tracking) detectors
- Ultra-thin, high-precision trackers for ILC and other applications
  - Monolithic CMOS Pixel Sensors
  - SOI detectors
- New trends: Vertical Integration (3D electronics)
- Conclusions

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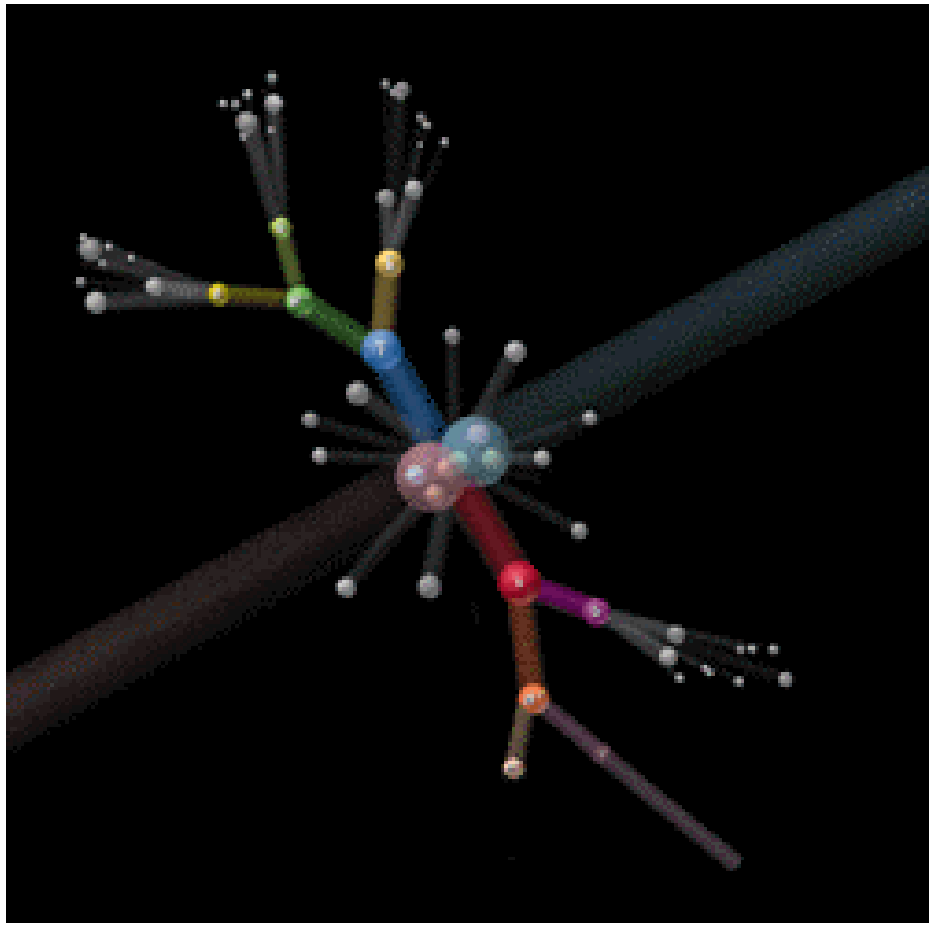
Physics motivation for vertex detectors in particle physics experiments: identification and tracking of short living particles

Vertex reconstruction is used for the following:

- lifetime
- quark mixing
- B-tagging
- top physics
- background suppression



For this application, the spatial resolution is THE factor of merit!

Typical Tracking Detector Characteristics

Detector Type	Spatial Resolution
Drift Chambers	~100 μm
MSGC	~30 μm
Silicon Detectors	2-15 μm
Nuclear Emulsion	1 μm

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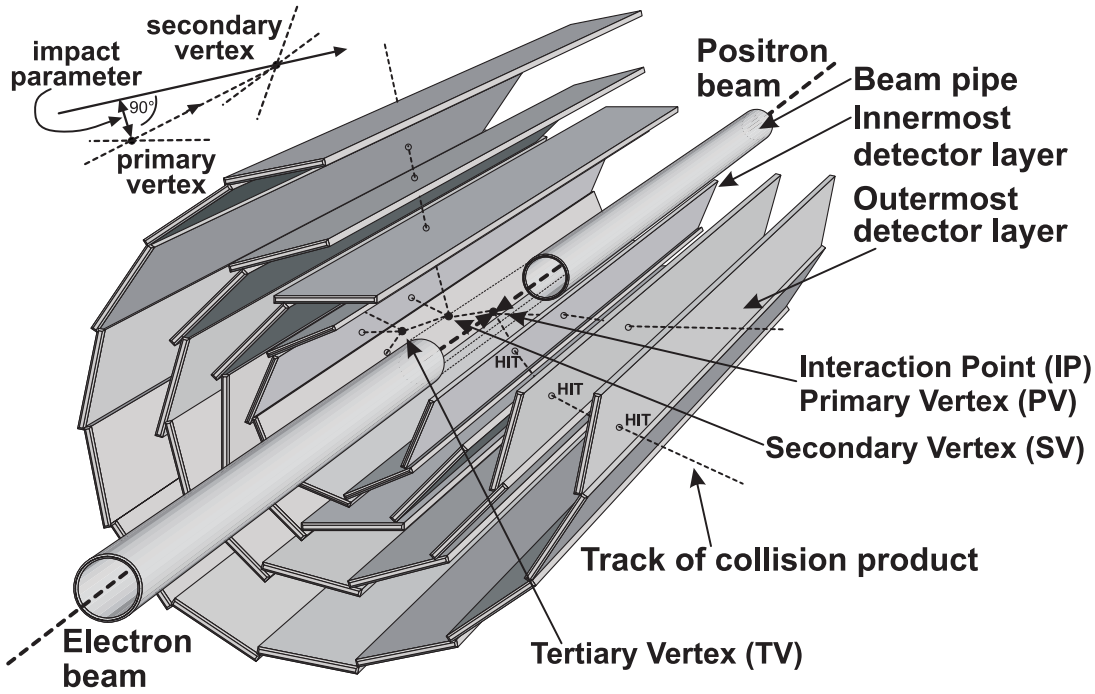
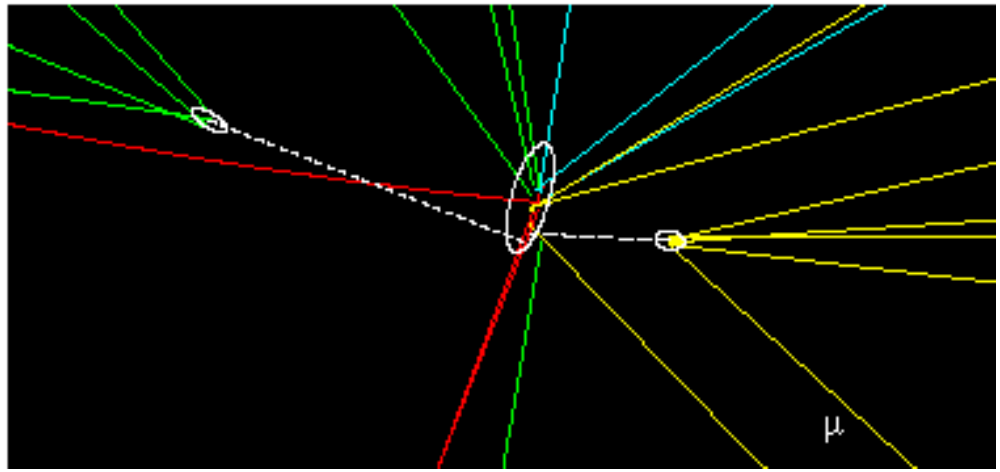
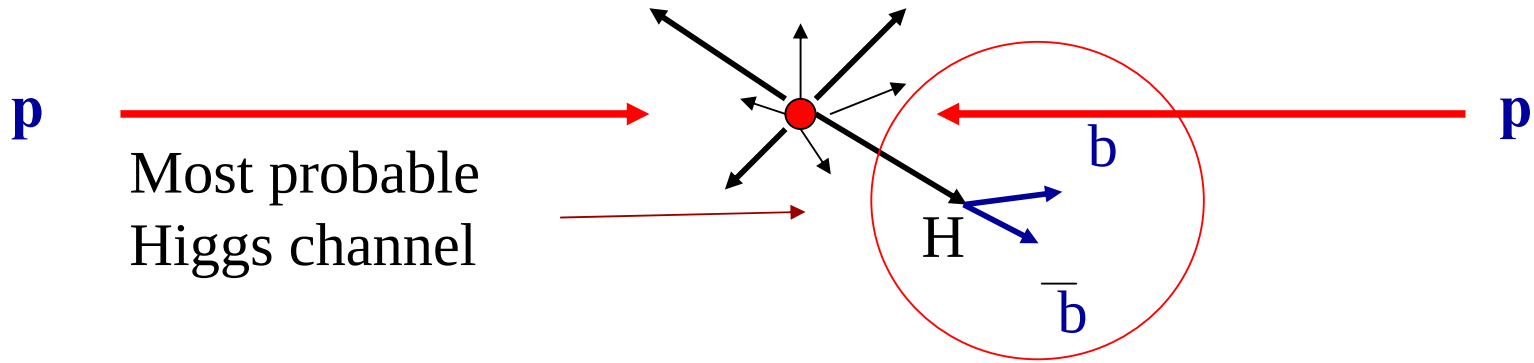
Vertex detector based on silicon detectors



Was it there already??



Event display shows a b candidate reconstructed in the ALEPH vertex detector.



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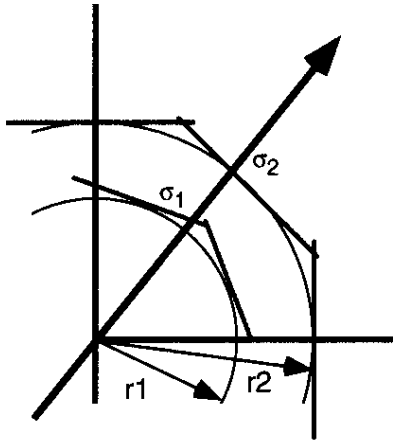
Impact Parameter Resolution

Without Multiple Scattering



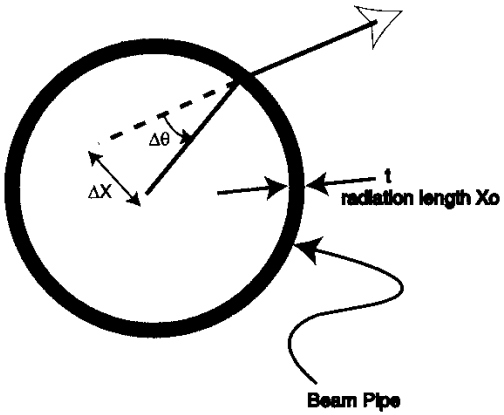
$$\sigma_I^{\,2} = \sigma_1^{\,2} + \frac{r_1^2}{(r_2^2 - r_1^2)}\sigma_2^{\,2}$$

So we want:

-small r_1, large r_2

-small σ_1, σ_2

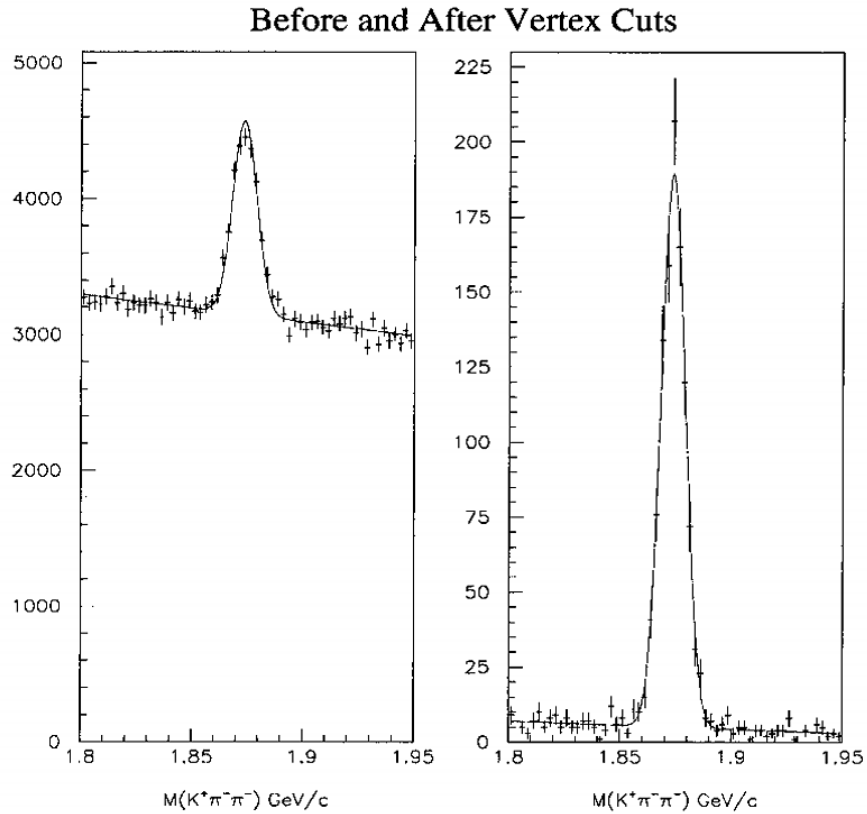
With Multiple Scattering



$$\Delta\theta \propto \frac{15}{P\beta}\sqrt{\frac{t}{X_0}}$$

$$\Delta X \propto \frac{r}{P\beta}\sqrt{\frac{t}{X_0}} \approx \frac{r}{P\beta}\sqrt{tZ^2\rho}$$

Example of background suppression



7σ vertex cut from beam spot.

Thin, low Z, highly segmented detector → silicon sensors!

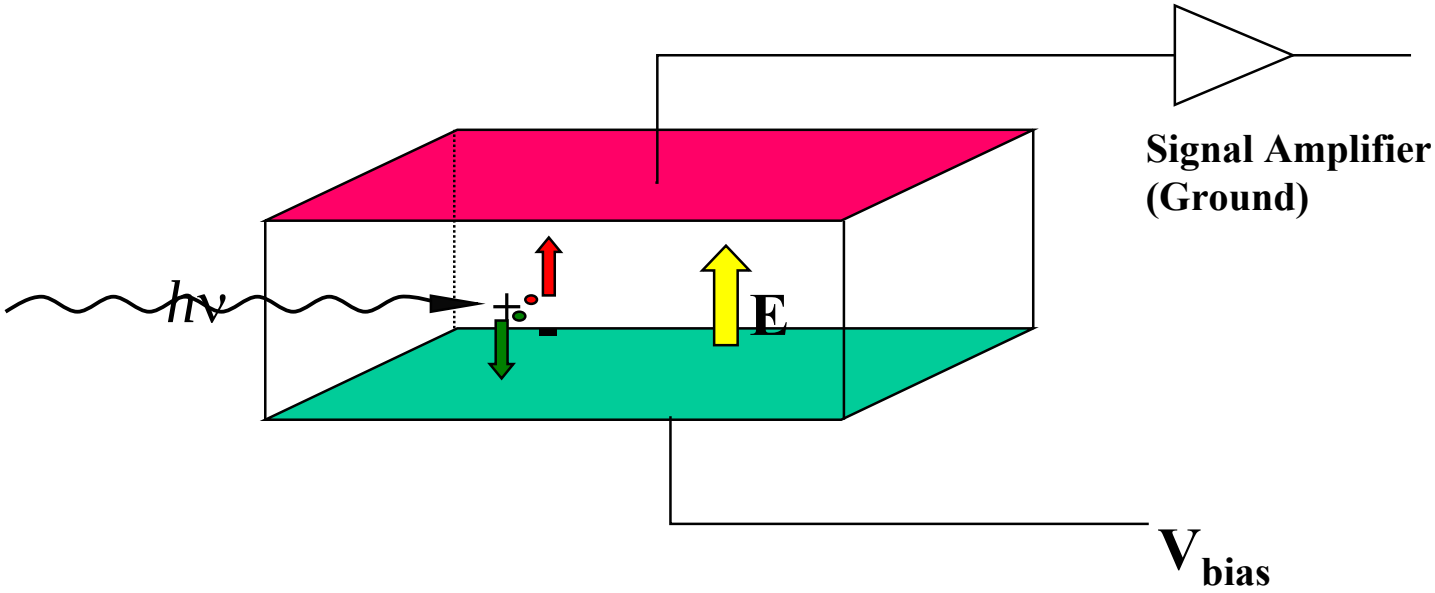
The Generic Semiconductor Radiation Detector

In general, the following steps must take place in the process of Ionising Radiation detection :

- **Radiation Interaction with the detector active medium : transfer of a part of initial radiation energy to the detector (OR total absorption with total energy transfer).**
- **Charge Carriers Creation inside detector : effective use of absorbed energy.**
- **Efficient Charge Carriers Transport across detector volume using internal electric field : useful signal (electric current pulse) generation.**
- **Amplification and processing of a primary signal with the help of an (external) electronic circuits : interface with data acquisition/storage system.**

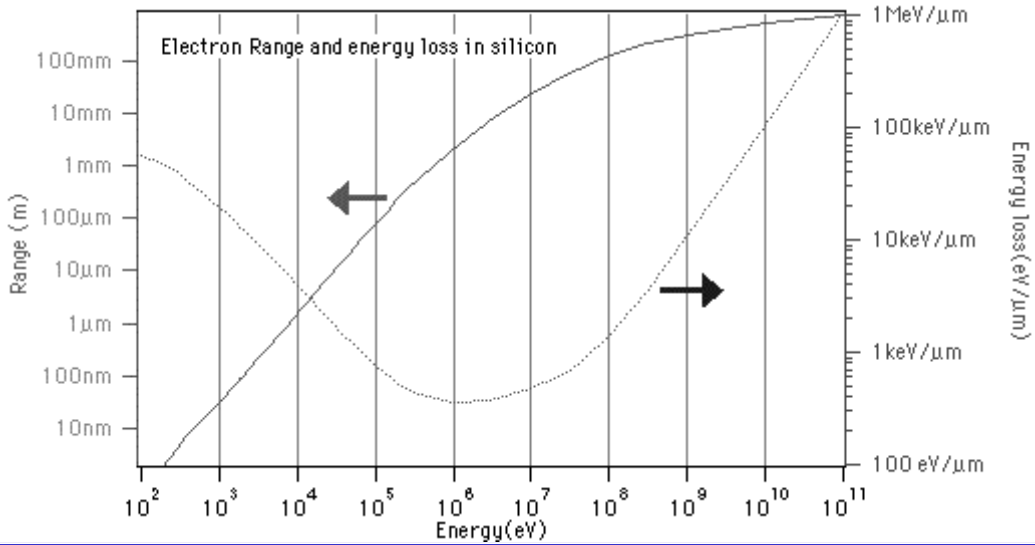
In consequence, good ionising radiation detector should optimise all above steps...

The Generic Semiconductor Radiation Detector



Shape of a Radiation-Generated Cloud

- Visible and UV light: single e-h pair
- X-Rays: "point" interaction, $N_{e-h} = E_X/3.6$ eV
- α particle: short, dense track (Bragg curve)
- β radiation: low density (close to MIP), scattered path
- High-energy particles: uniform low density track (MIP)
- Non-relativistic charged particle: $dE/dX \sim z^2/E$



Choice of detector material for tracker : silicon!

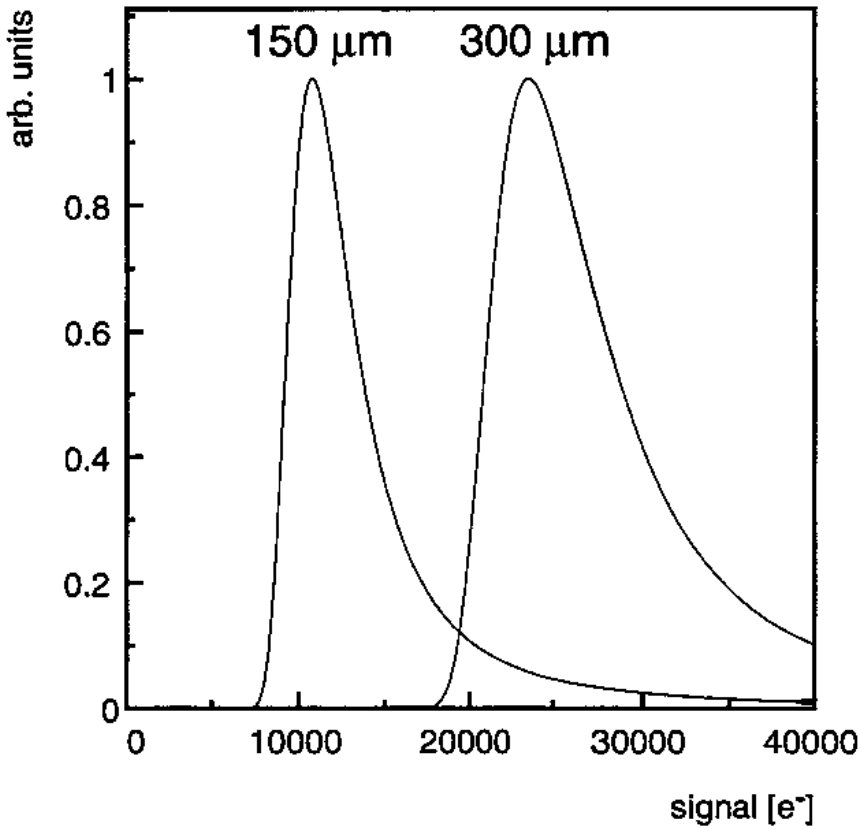
Bethe-Bloch equation applied for silicon and for minimum-ionising particles (γ~3.5) gives:

dE/dx = 39 keV/100μm

-an energy deposition of ~3.6 eV will produce an e-h pair in silicon

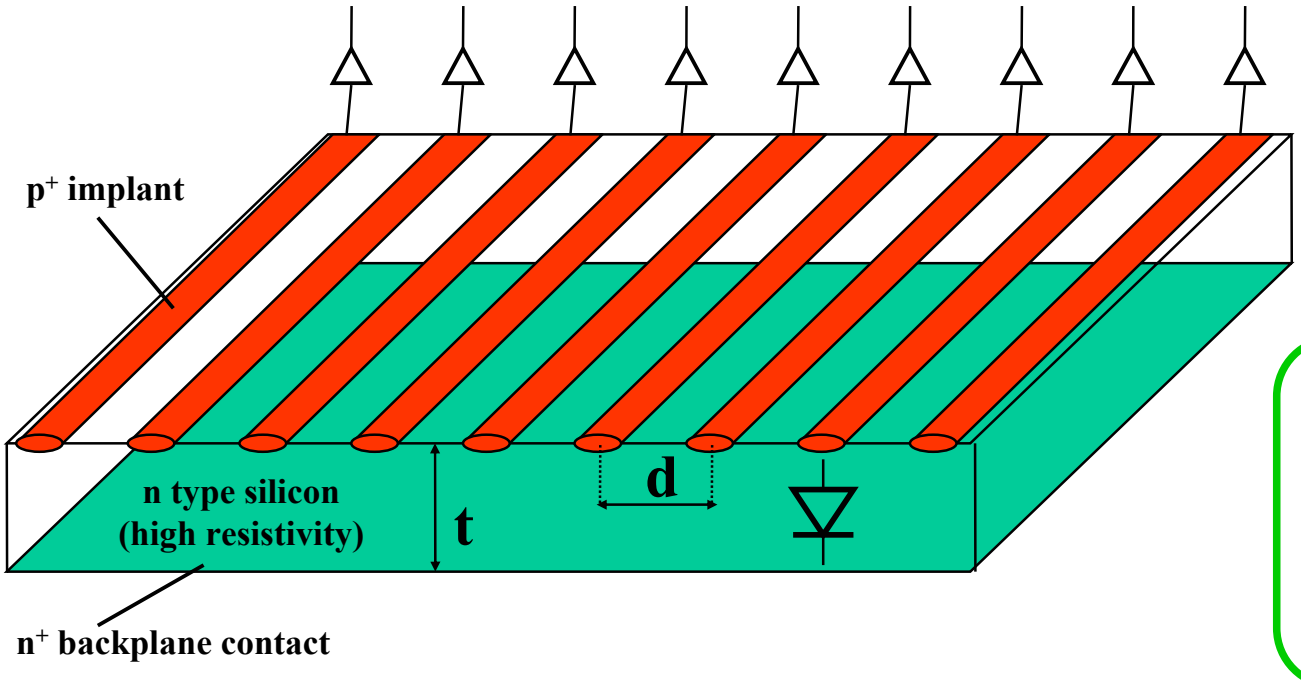
-minimum-ionising particle will produce ~10 000 e-h pairs traversing 100 μm of silicon

- because of Landau fluctuation : E_{peak} ~7300 e-h pairs per 100 μm of silicon



Landau distribution (calculated) for a 300μm and a 150μm thick silicon detector.

Semiconductor Position Sensitive Detectors: Single Sided Microstrip Detector



To be measured:

-hit position

- signal amplitude

Single sided microstrip detector

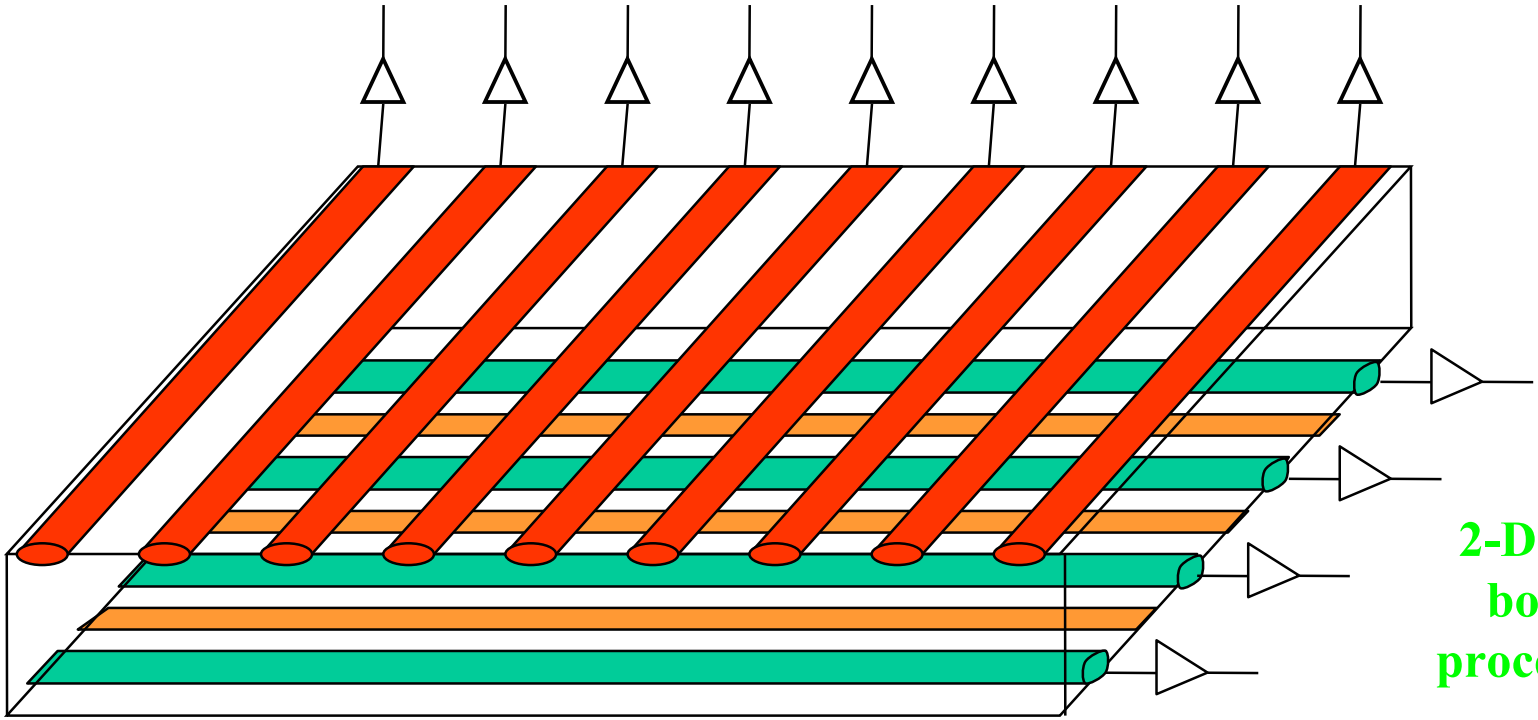
Typical parameters : t~300μm, d~50 μm, size ~10x10 cm

Spatial Resolution is the Factor of Merit : $\sigma \approx d/\sqrt{12}$

σ = 1.3 μm has been demonstrated

σ ~ d/2 (S/N)$^{-1}$
If analog readout

Semiconductor Position Sensitive Detectors: Double Sided Microstrip Detector



2-D Information, but both sides must be processed and read out

Problem of n-strips isolation!

Problem with multihits!

Semiconductor Position Sensitive Detectors: Hybrid Pixel Detector

A pixel detector is a single sided detector segmented in both directions.

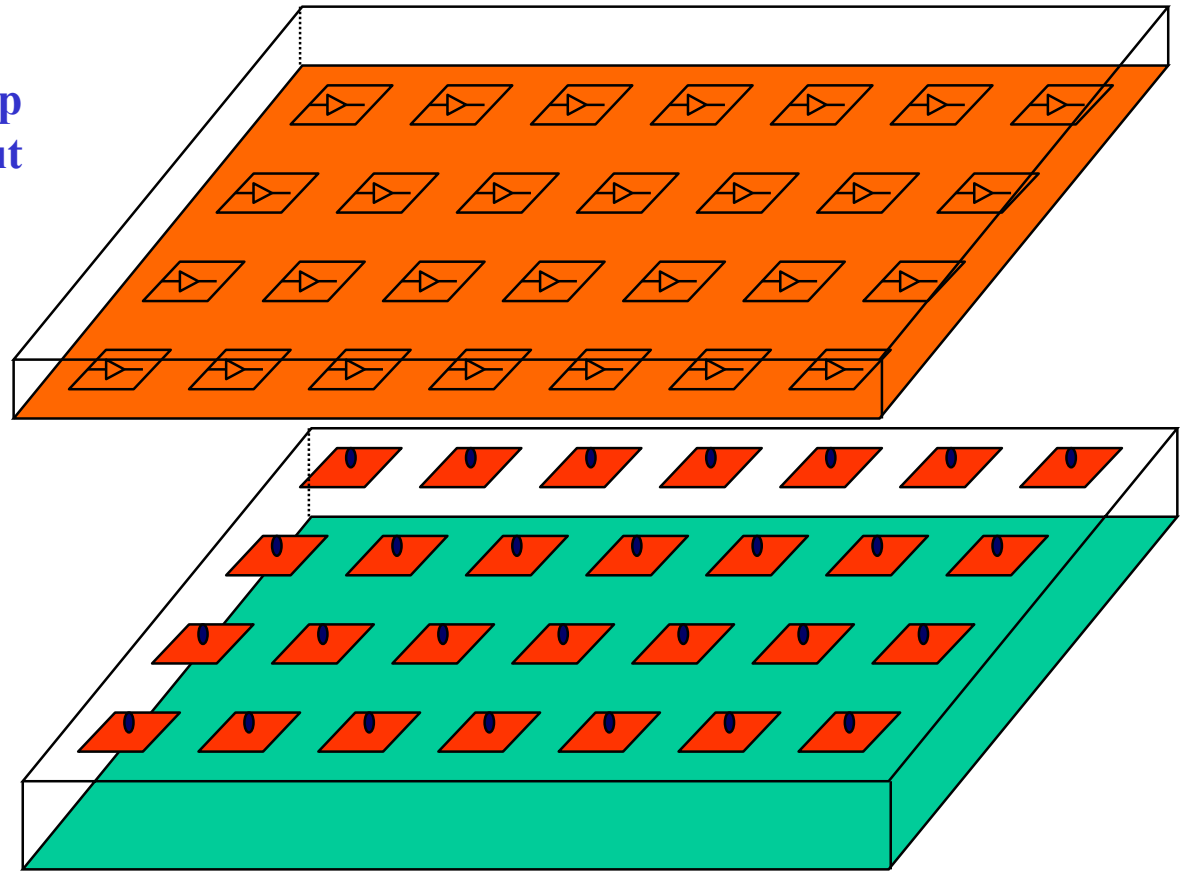
The readout chip is mounted directly on top of the pixels, each pixel has it's own readout amplifier. Metal micro balls (Bump bonding) are used to provide electrical connection between two wafers. This is relatively complicated and expensive procedure!

To be measured:

-hit position

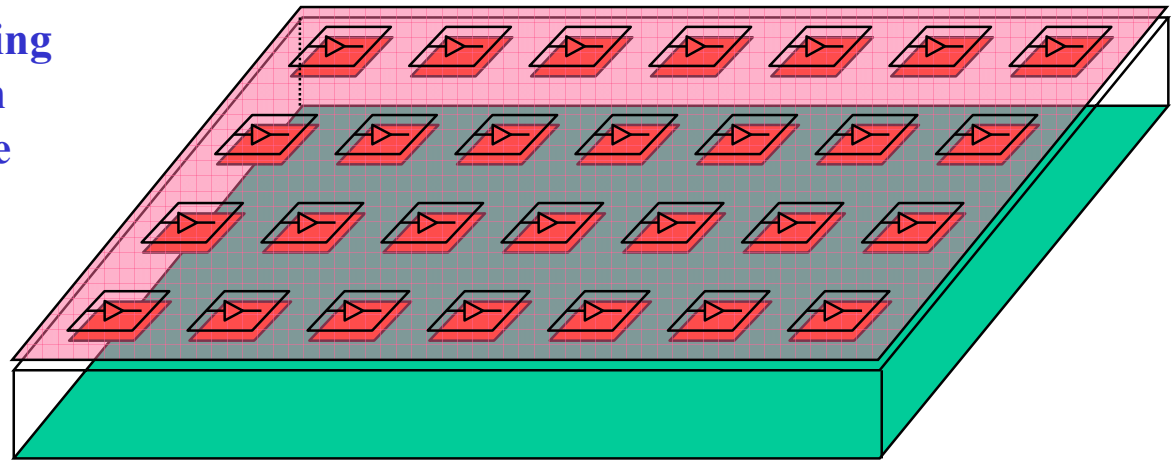
-hit arrival time

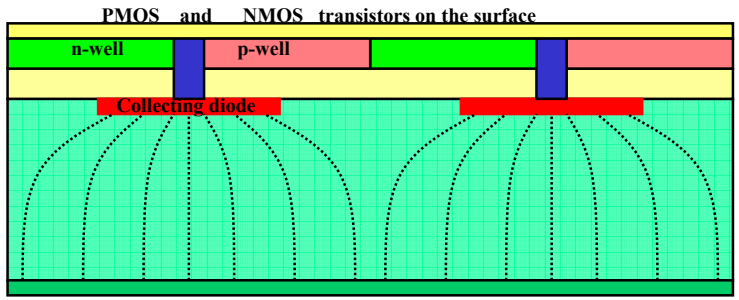
- signal amplitude



Semiconductor Position Sensitive Detectors: Monolithic Pixel Detector

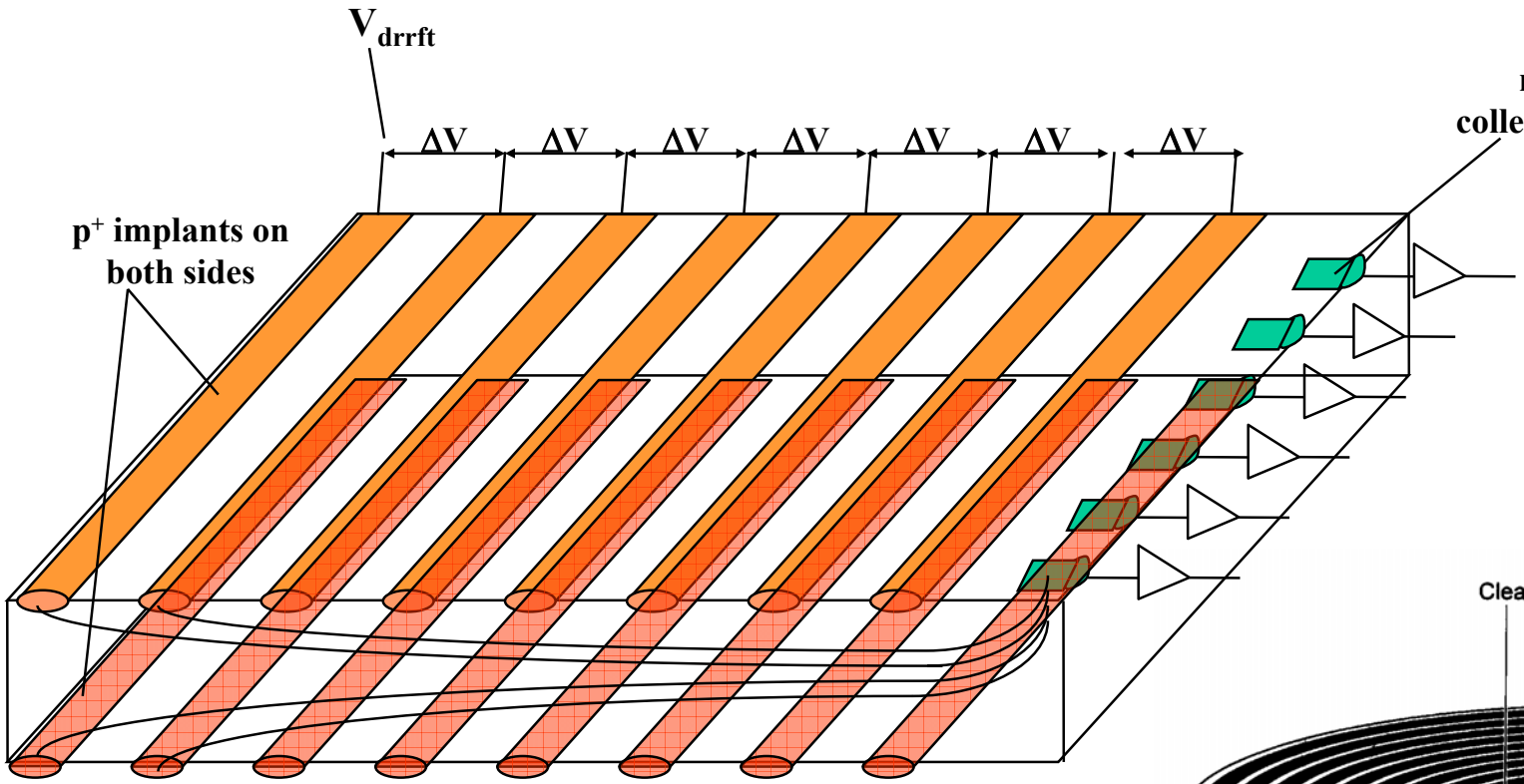
Both detector elements and readout electronics are integrated on the same (silicon) wafer, using slightly (?) more complicated process. High granularity, low noise, thin detectors can be fabricated this way.





Example of possible monolithic detector implementation:
SOI CMOS + High Resistively handling wafer

Semiconductor Position Sensitive Detectors: Silicon Drift Detector (SDD)

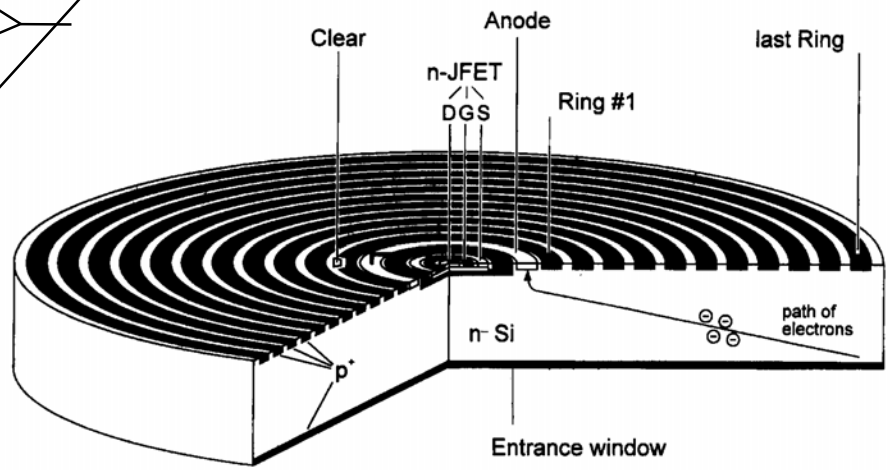


To be measured:

-hit position

- arrival time

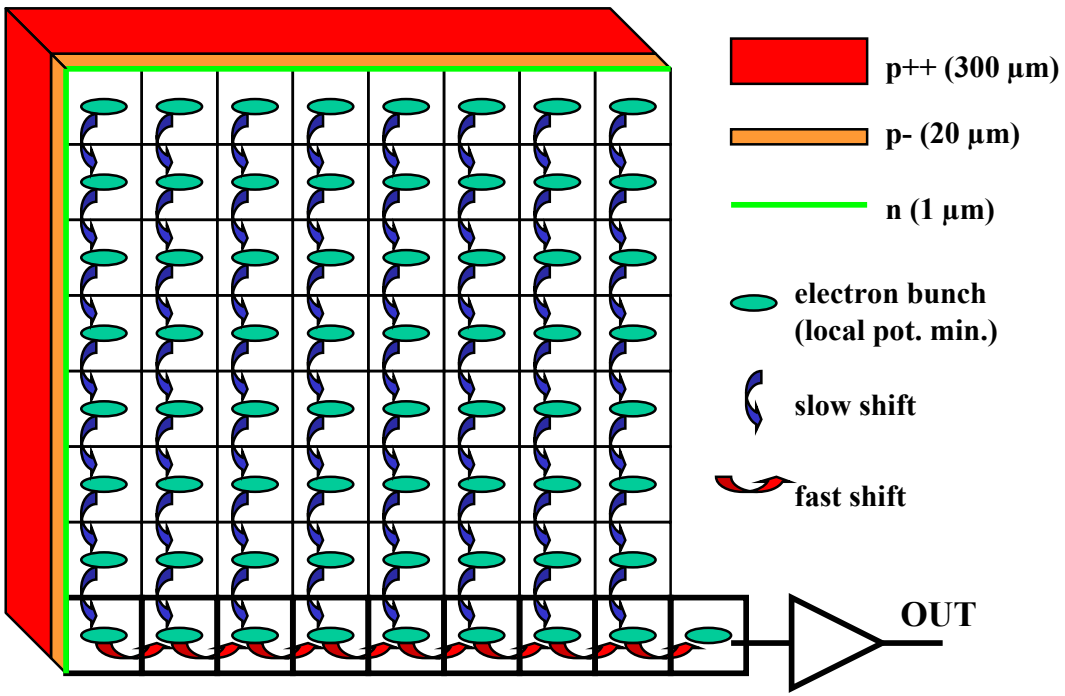
- signal amplitude

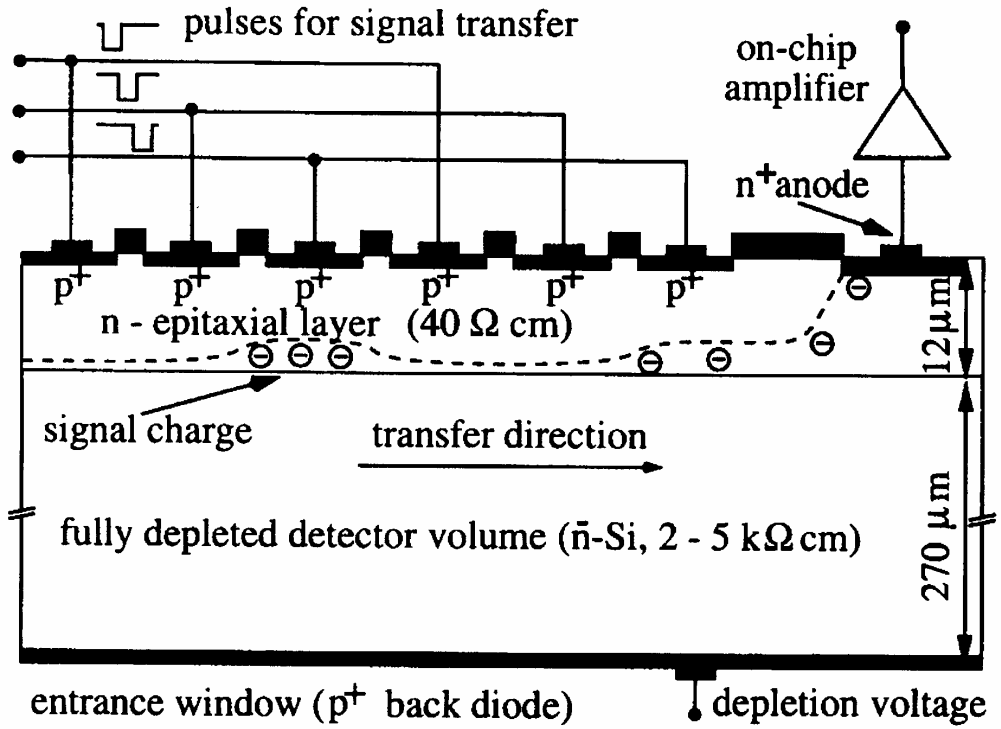


Silicon Drift Chamber used as photodetector

Semiconductor Position Sensitive Detectors: Charge Coupled Device (CCD)

An imaging CCD consist firstly of a square matrix of potential wells, so the charge signal generated below the silicon surface can be accumulated, building up an image. Secondly, by manipulating clock voltages in the parallel register charge can be transferred in parallel from one row to the next and into linear register in the bottom of the matrix. Then the linear register is read out, cell after cell. Thus the CCD image is converted from a 2-D charge pattern to a serial train of pulses.





Fully depleted pn-CCD with integrated on-chip first amplification stage
(P.Hall et al., SPIE, 3114: 126-133, 1977C)

DEPFET Pixel Sensor for X-rays

- can be back illuminated, can have a fill factor of 1, can be made very large (all pros of CCD)
- does not need a charge transfer, no out-of-time events, every pixel is xy-addressable (all pros of APS)
- in addition, can have a non destructive multiple readout to reach very low noise figures

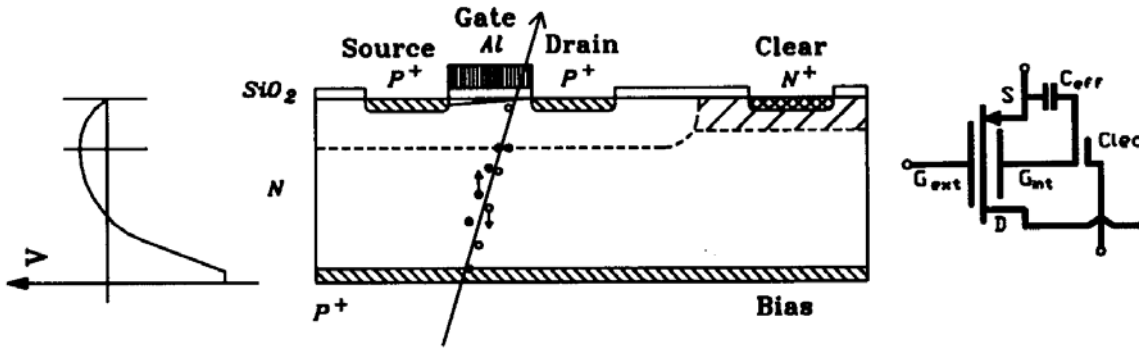
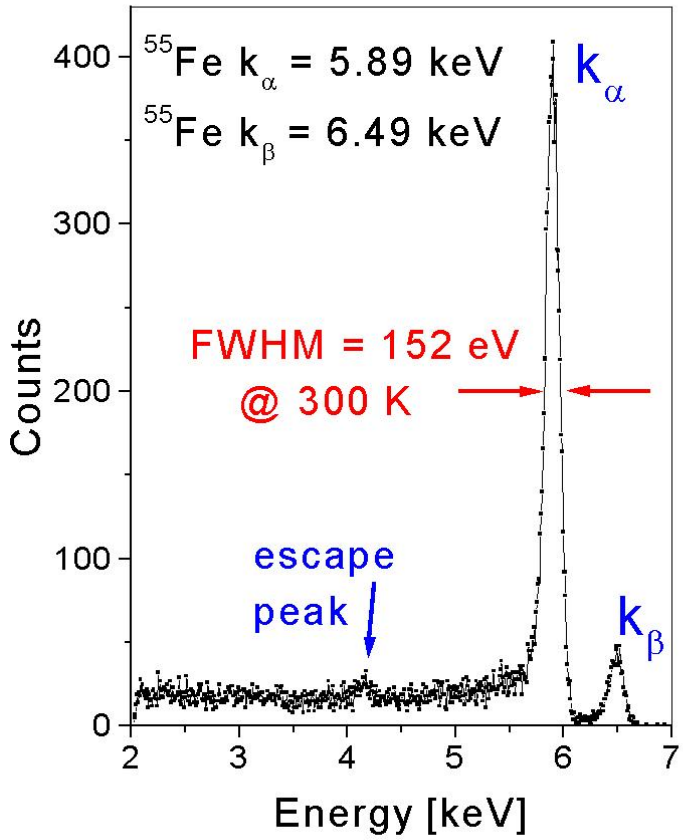


Figure 1. *The DEPFET structure and device symbol*

J.Kemmer, G.Lutz et al. NIM A 288 (1990) 92

Device concept:
combination of FET transistor with sideward depletion (drift chamber)



DEPFET : excellent noise figures (9 electrons rms.) at room temperature!

Microelectronics for trackers (silicon detectors) in France

- CPPM: hybrid pixels for ATLAS (DMILL → IBM 0.25)
- IPHC (CRN, LEPSI, IRES): microstrip readout for STAR (AMS 1.2) and ALICE (IBM 0.25),
- IPHC and DAPNIA: monolithic pixels for STAR, EUDET, CBM and ILC
- IPNHE: microstrips for ILC

→ 1.93% / layer

Ultra thin detectors for future particle physics experiments

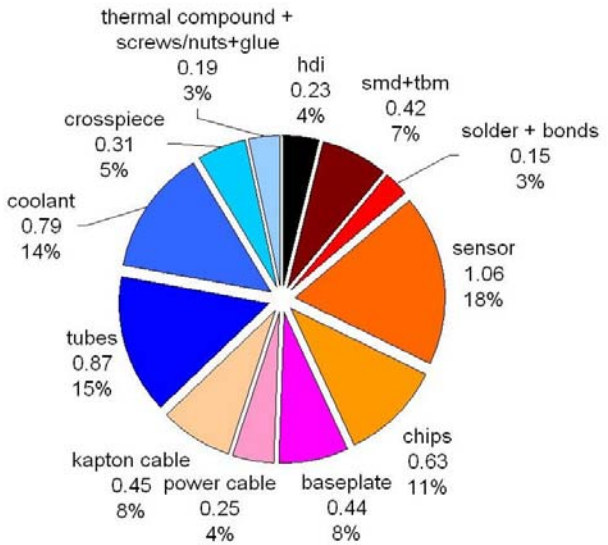
Example: Microvertex Detector for ILC

- **Key issuses:**
  - **measure impact parameter for each track**
  - **space point resolution < 5 μm**
  - **smallest possible inner radius $r_i \approx 15$ mm**
  - **transparency: ≈ 0.1% X_0 per layer**
    = 100 μm of silicon
  - **stand alone tracking capability**
  - **full coverage $|\cos \Theta| < 0.98$**
  - **modest power consumption < 100 W**

- **Five layers of pixel detectors plus forward disks**
  - **pixel size O(20×20 μm²)**
  - **10^9 channels**

- **Note: wrt. the LHC pixel detectors**
  - **1/5 r_i**
  - **1/30 pixel area**
  - **1/30 thickness**

Material budget for 3 Layers of CMS pixels at η = 0

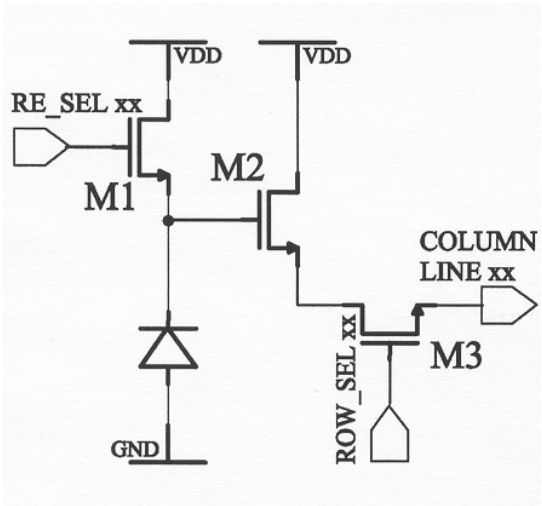


X/X_0 = 5.79% for 3 barrel pixel layers
→ 1.93% / layer

In order to be thin, reduce power!

CMOS Active Pixel Sensors for radiation (light) imaging: late 80's (?)

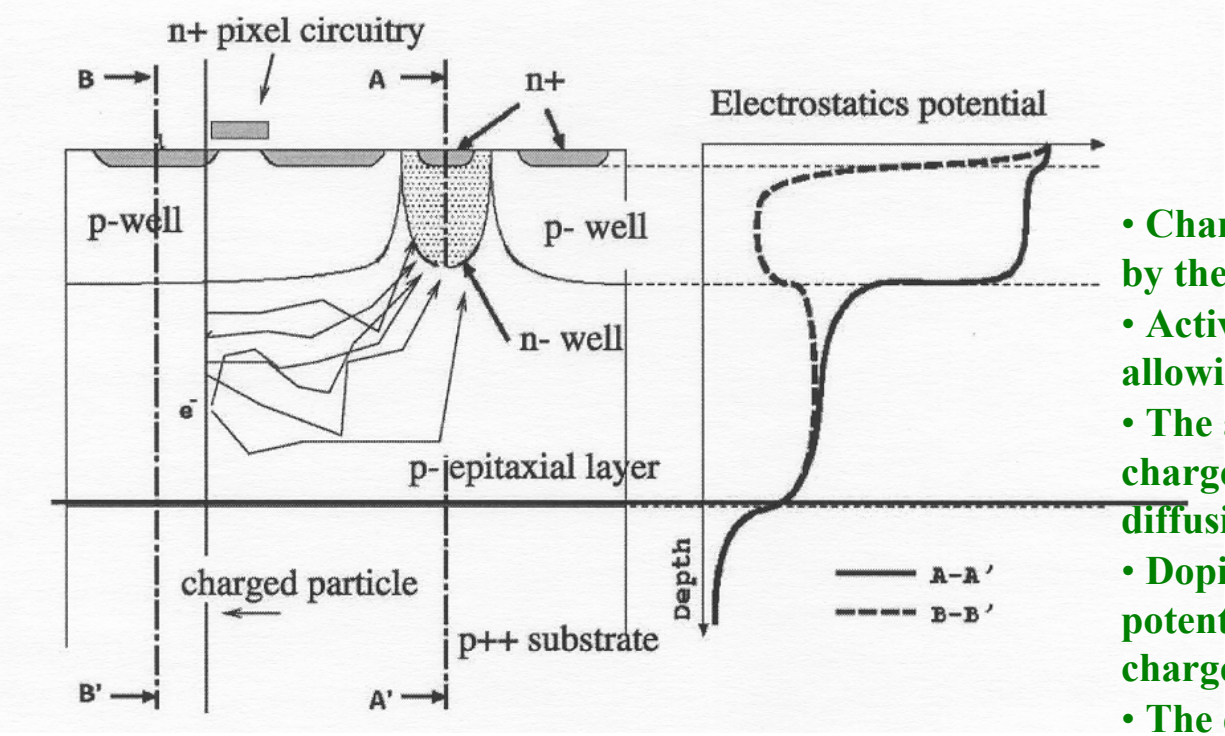
E. R. Fossum, "CMOS image sensors :electronic camera-on-a-chip", IEEE Trans. On Electron Devices 44 (10) (1997)



Basic pixel electronics schemes (photodiode, 3 or 4 transistors, transfer gate…) : all this elements are still bases of today's digital cameras

From digital cameras to particle tracking: use of an epitaxy layer as a detector active medium

B. Dierickx, G. Meynants, D. Scheffer "Near 100% fill factor CMOS active pixel sensor", Proc. of the IEEE CCD&AIS Workshop, Brugge, 1997



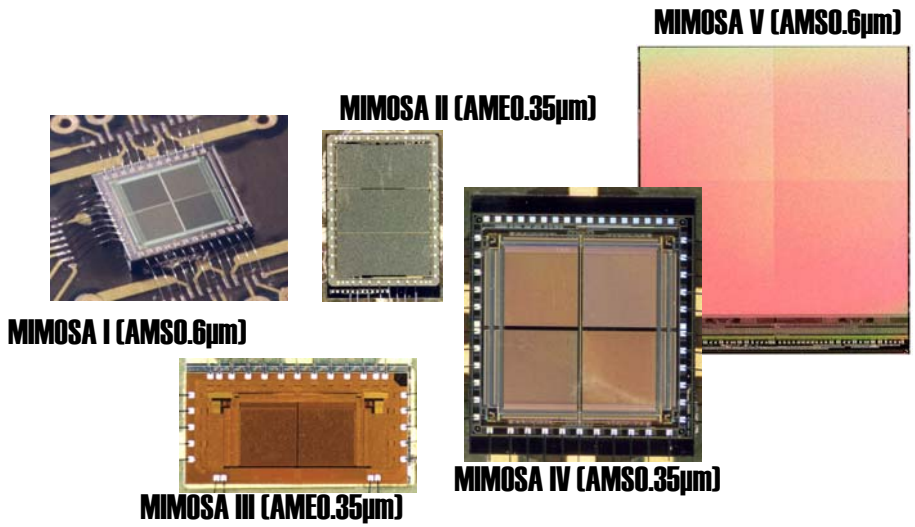
Twin - tub (double well), CMOS process with epitaxial layer

- **Charge generated by the impinging particle is collected by the n-well/p-epi diode.**
- **Active volume is underneath the readout electronics allowing a 100% fill factor.**
- **The active volume is NOT fully depleted: the effective charge collection is achieved through the thermal diffusion mechanism.**
- **Doping gradient ($P^{++}_{substrate} - P^{-}_{epi} - P^{+}_{well}$) results in a potential minimum in the middle of epitaxy layer, limiting charge spread (2D instead of 3D)**
- **The device can be fabricated using almost any standard, cost-effective and easily available CMOS process**

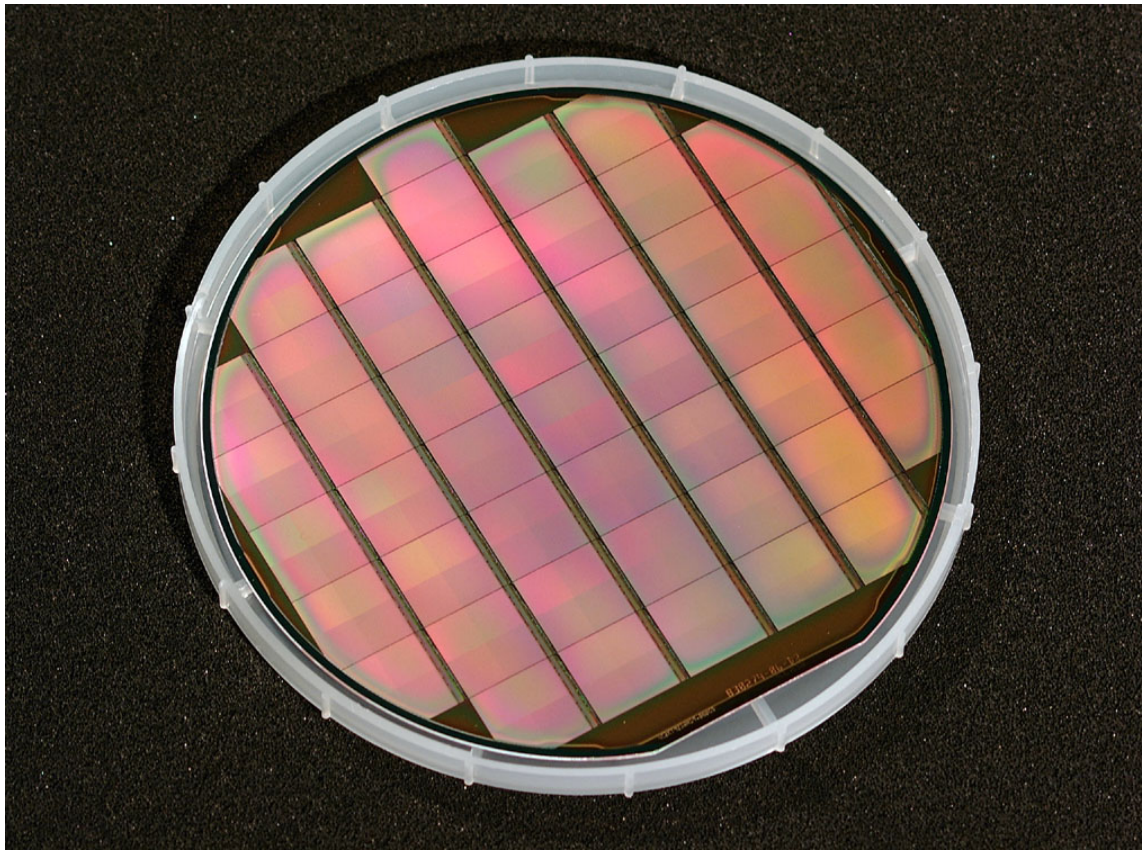
Beginning of MAPS activity at Strasbourg: 1999

Dierickx idea brought to us by R. Turchetta with his own proposition to use it for particle tracking, bought (and financed) by M. Winter from IReS and implemented by LEPSI team (B. Casadei, C. Colledani. W.Dulinski …) backed by a young PhD student from Cracow: G. Deptuch

"Big Bang" → long series of MIMOSA *(Minimum Ionising Particle MOS Active Pixel Sensor)* chips…



Wafer scale MAPS prototype example: Mimosa5 (10^6 pixels) in AMS-0.6 µm CMOS process (2003)



Six inch wafer hosts 33 sensors, 1.7×1.9 cm² each

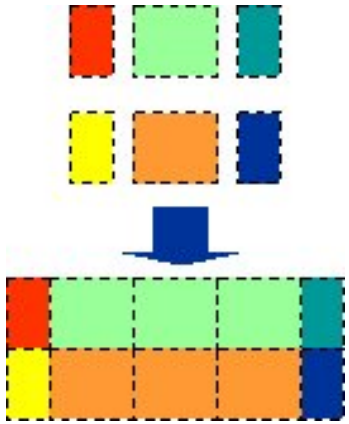
Maximum allowed size of a circuit in a standard CMOS process: ~20x20 mm² (reticle)

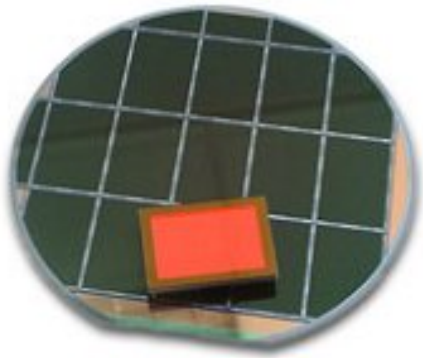
Reticle stitching is needed, in order to get a larger device (a ladder, ~10x2 cm²)

MIMOSA5

Each reticle is an independent circuit. Periphery logic and bonding pads layout along one side. Simplified stitching of up to 7 reticles in one direction. Still some problems with a yield (~30-40%) but it can be solved (according to some digital imager suppliers).

Real stitching, as offered by TOWER Semiconductor Ltd. The way to fabricate monolithic ladders?





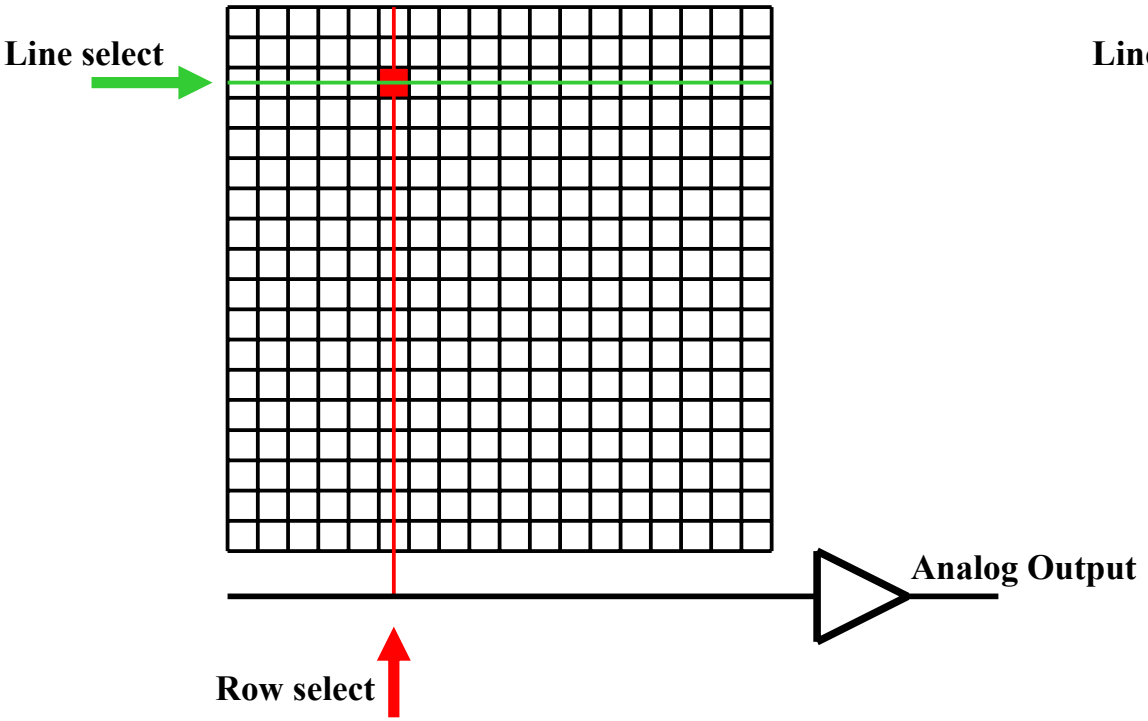
Kodak Professional 14 Mpixel Camera

Signal processing: Correlated Double Sampling

in case of serial (slow) and column-parallel (fast) readout

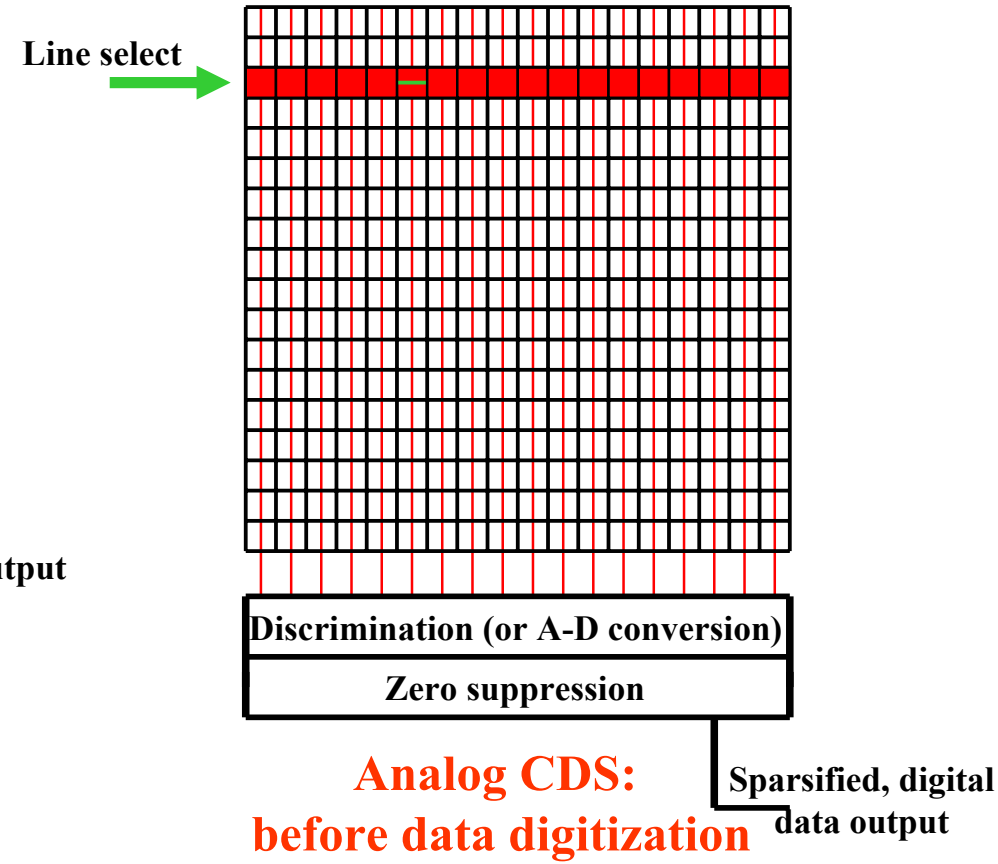
CDS: Signal = Sample(t_1) – Sample (t_0); t_1-t_0 is the integration time

Serial (pixel-by-pixel) readout



Digital CDS:
after data digitization

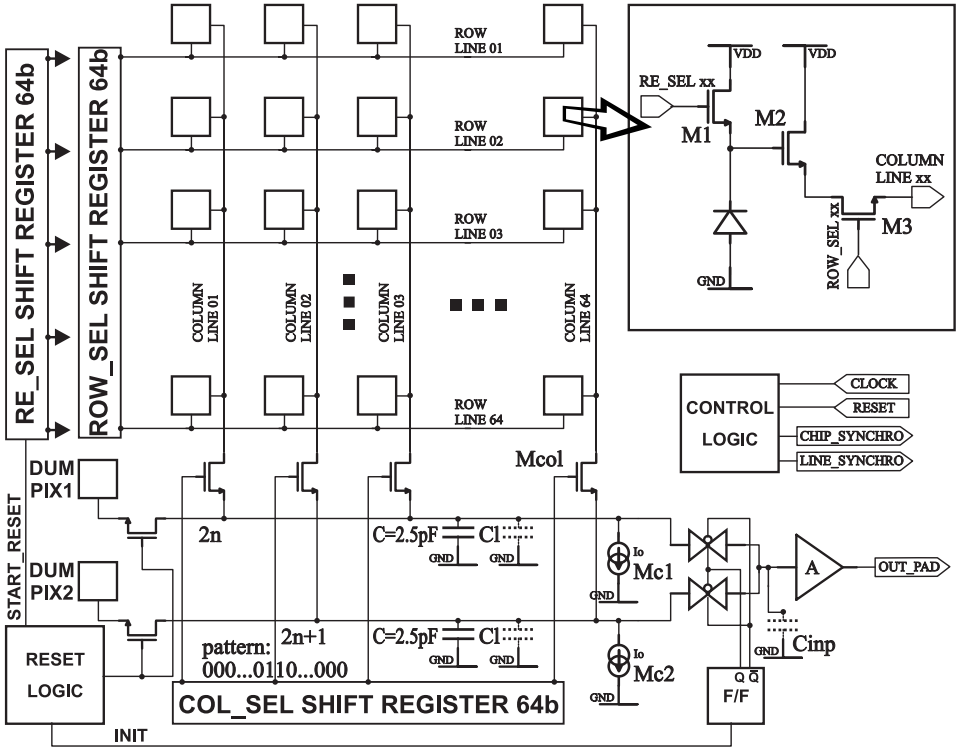
Column parallel (line-by-line) readout



Analog CDS:
before data digitization

CDS is very efficient (and the only effective?) way of removing the inter-pixel pedestal spread, which is at least order of magnitude higher than the signal

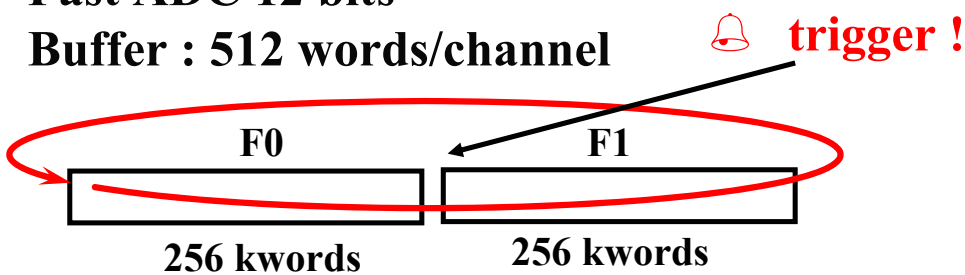
The simplest readout electronics: diode + 3 transistors/pixel



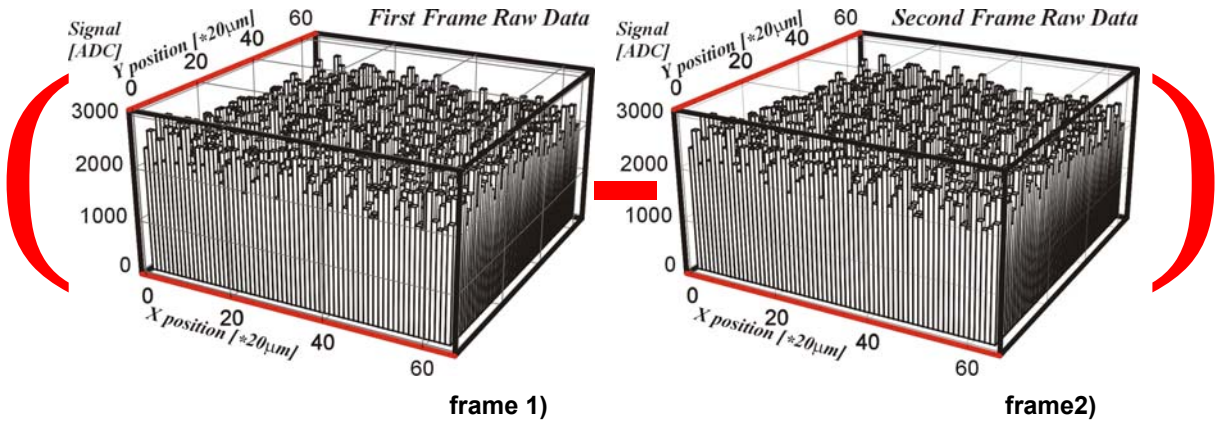
1. Reset in order to inverse bias
2. Continuous serial addressing and readout (digitisation) of all pixels
3. Keeping two successive frames in external circular buffer
4. Following reset when needed (removing integrated dark current)
5. After trigger (or in a real time)), simple data processing in order to recognise hits

Fast ADC 12 bits

Buffer : 512 words/channel



Data processing: (Digital) Correlated Double Sampling



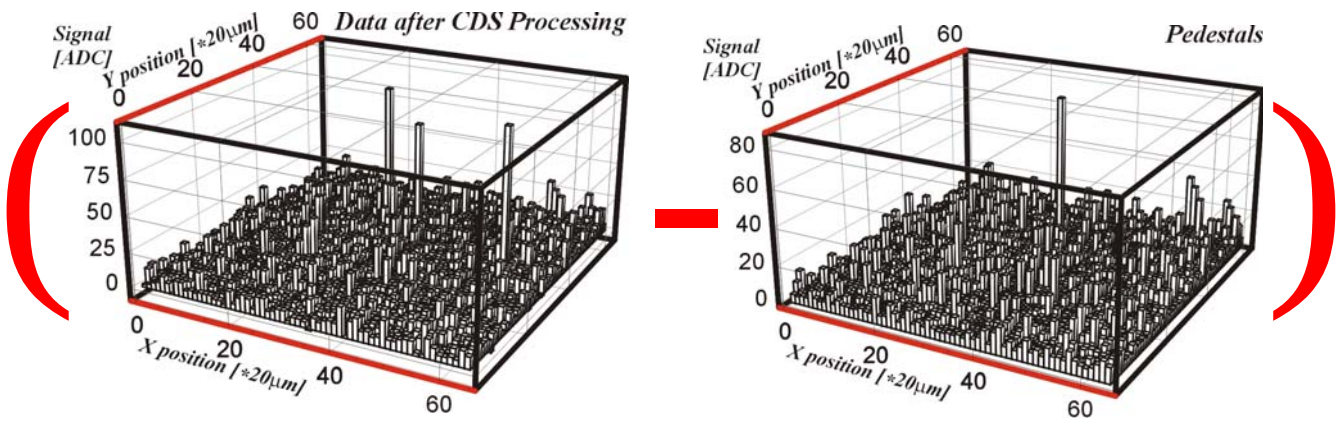
frame 1) frame2)

(frame2 - frame1) subtraction

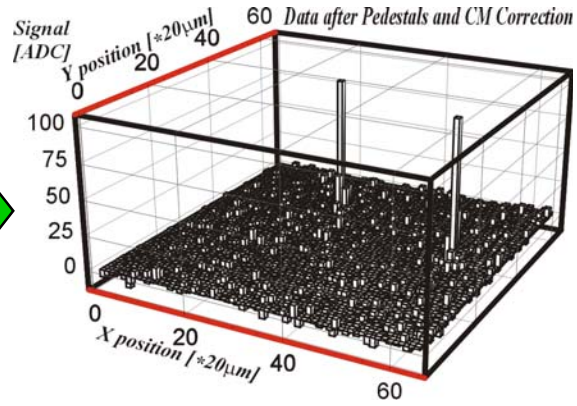
Useful signal on top of Fixed Pattern DC level

Fixed Pattern dispersion: ~100 mV

Typical signal amplitude: ~1mV



frame2 – frame1) **Pedestal (dark current) subtraction**



Hit candidates!

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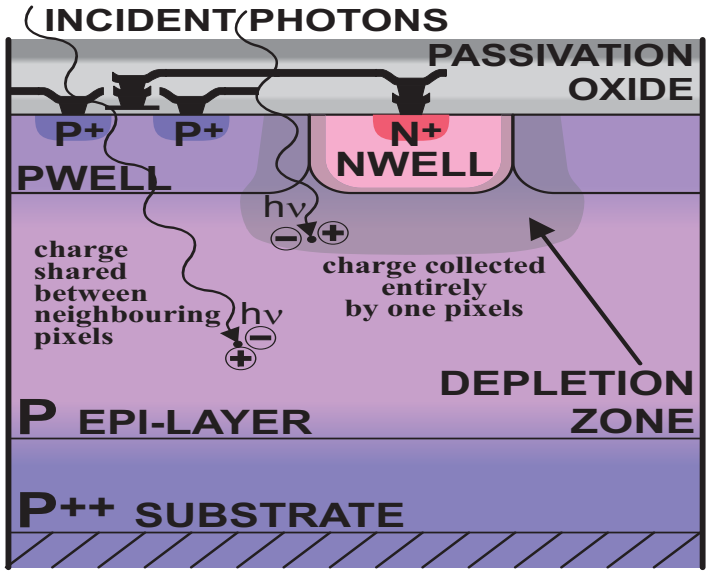
Calibration of the conversion gain - with soft X-rays

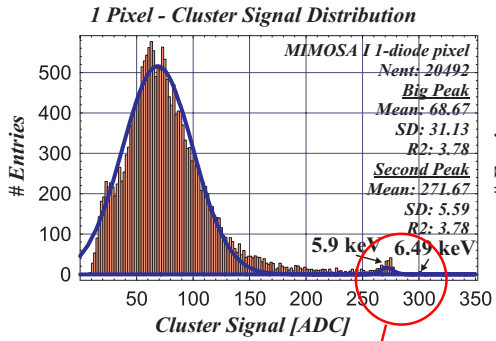
•Calibration methods:

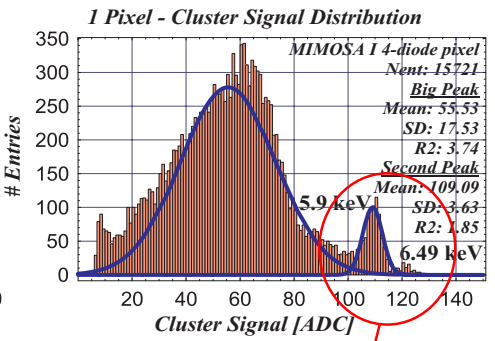
Emission spectra of a low energy X-ray source e.g. iron ^{55}Fe emitting 5.9 keV photons.

very high detection efficiency even for thin detection volumes - μ =140 cm^2/g, constant number of charge carriers about 1640 e/h pairs per one 5.9 keV photon



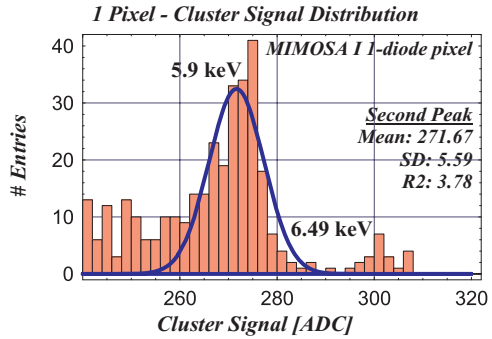
The ' warmest ' colour represents the lowest potential in the device

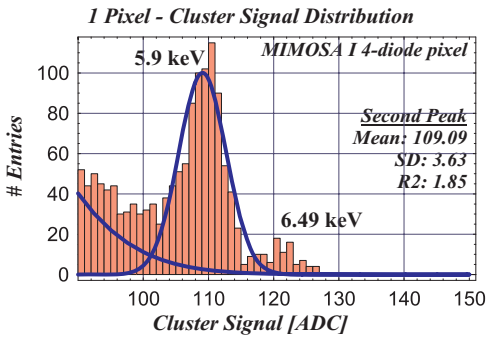




MIMOSA I (14 µm EPI) configuration with single diode in one pixel

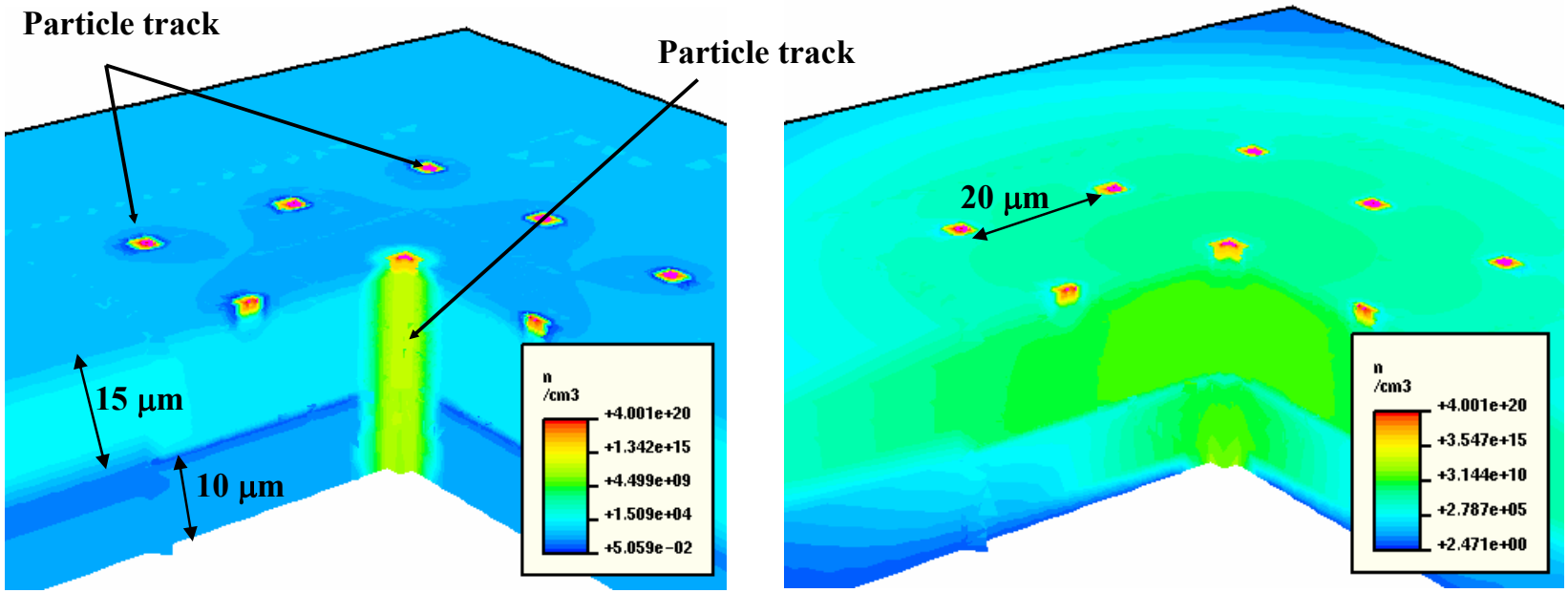
MIMOSA I (14 µm EPI) configuration with four diodes in one pixel





MIMOSA I CMOS 0.6 µm	1 diode – 14.6 µV/e$^-$	4 diode – 6.0 µV/e$^-$
	ENC = 14 e$^-$ @1.6 ms f. rate	ENC = 30 e$^-$ @1.6 ms f. rate
MIMOSA II CMOS 0.35 µm	1 diode rad. tol.– 22.9 µV/e$^-$	2 diode rad. tol.– 17.5 µV/e$^-$
	ENC = 12 e$^-$ @0.8 ms f. rate	ENC = 14 e$^-$ @0.8 ms f. rate

Simulation of physics process (ISE – TCAD)



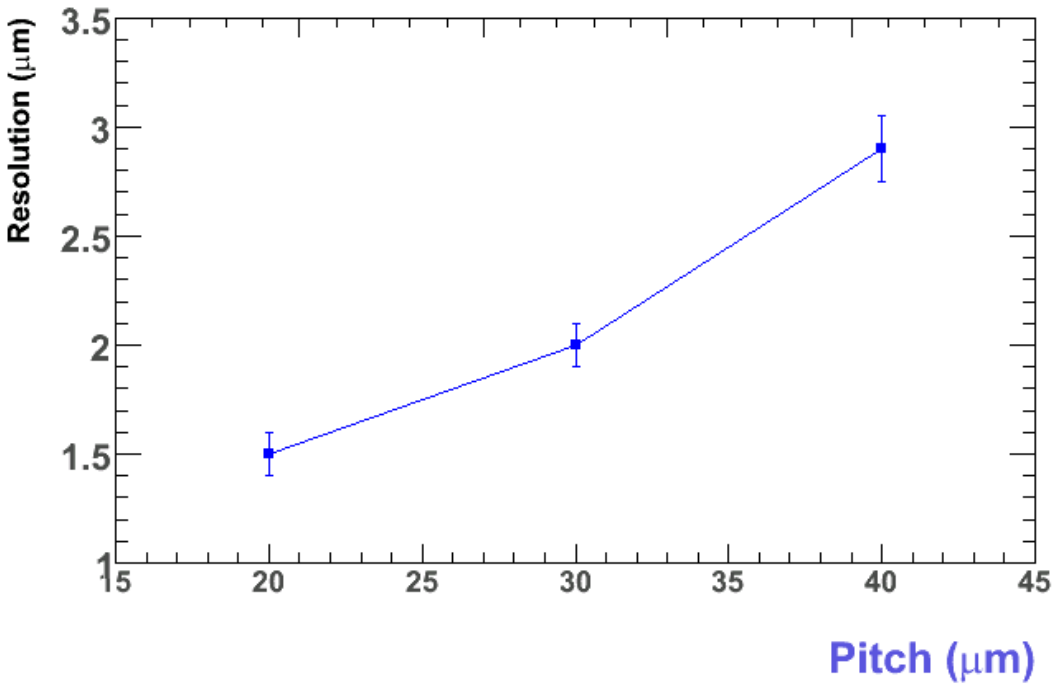
τ = 0 ns Carrier concentration τ = 25 ns

- The charge collection efficiency examined using the mixed mode device and circuit simulator DESSIS-ISE from the ISE-TCAD package,
- The charge collection is traced as a relaxation process of achieving the equilibrium state after introducing an excess charge emulating passage of the ionising particle
- The device is described in three dimensions by a mesh generated using the analytical description of doping profiles and the boundary definition corresponding to the real device,
- Different detector parameters, including the thickness of the epitaxial layer, the size of a pixel and collecting diodes and number of diodes per pixel, were investigated.

Mimosa9 (various pitch) beam tests results (THE reference)

AMS 0.35 µm CMOS OPTO process

- Advanced mixed-signal polycide gate CMOS: 4 metal, 2 poly, high-res poly, 3.3V and 5V gates
- Optimized N-well diode leakage current
- 14 µm epi substrate (20 µm possible)
- Availability through multi-project submissions, with a reasonable pricing (< 1 k€/mm^2). In production, the price is of few k€ per 8 inch wafer.



Signal in the seed pixel: down to few tens of electrons

But: ENC ~10 electrons, so S/N comfortable

Efficiency >99.5%, for the fake hit rate ~10^{-5}

Excellent spatial resolution!

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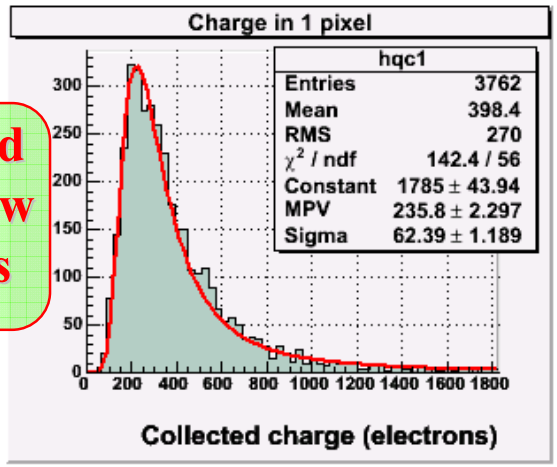
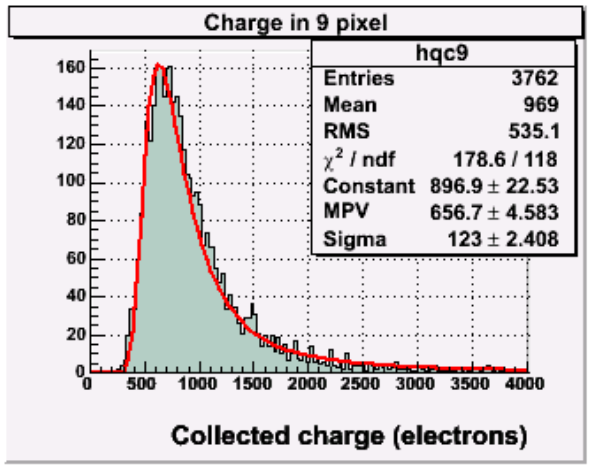
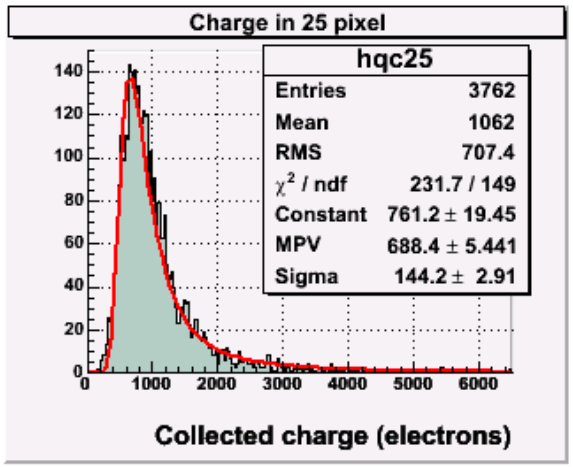
A "typical" example from the beam tests: 30µm pitch array, 20°C

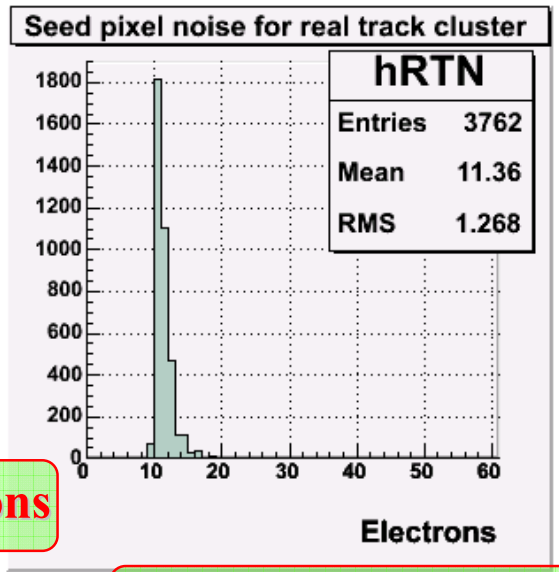
M9 ; run 9534; Pl 10, dist 90; Gain 7.200; eff 99.810 +- 0.070; Seed 6.0; Neigh 4.0

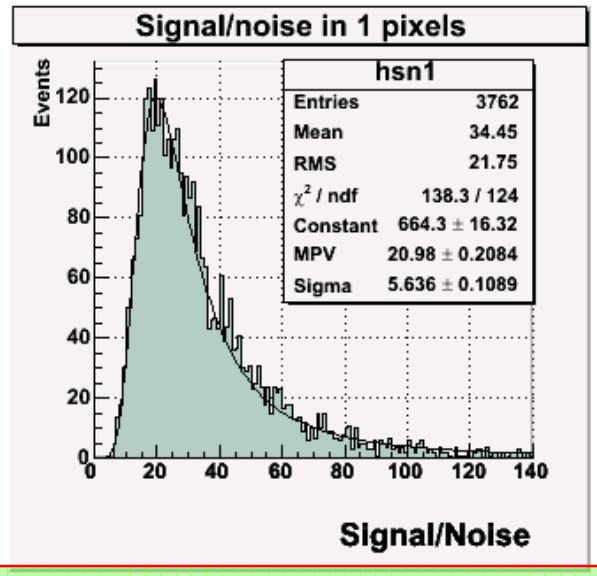
Signal in the seed pixel: down to few tens of electrons

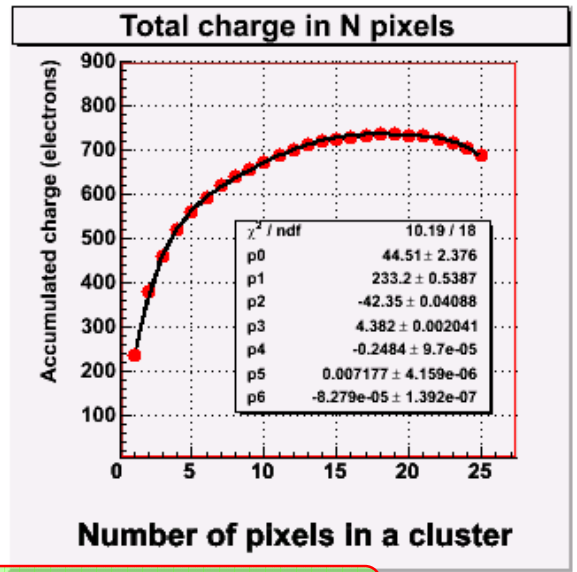












ENC: ~10 electrons

Efficiency >99%, spatial resolution: down to 1.5 µm

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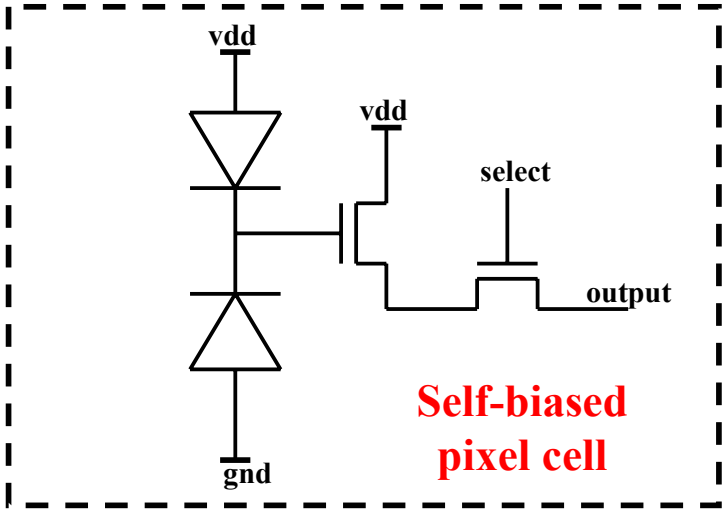
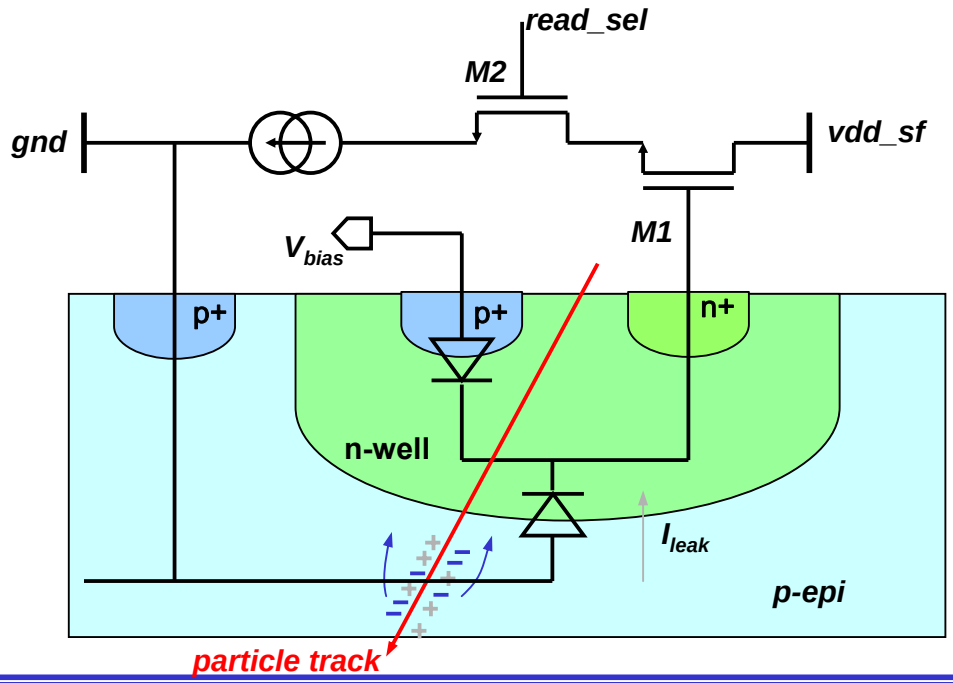
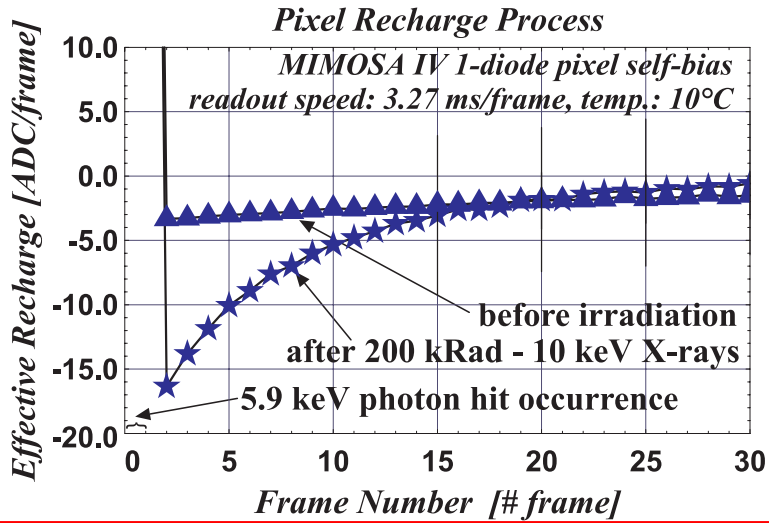
Modified sensing elements: self-biasing diode



DC level stabilization

RESET transistor replaced by a forward-biased diode, equivalent of a ~TeraOhm resistor for a ~fA (typical) leakage current





Typical RC constant: tens of ms (even after irradiation)

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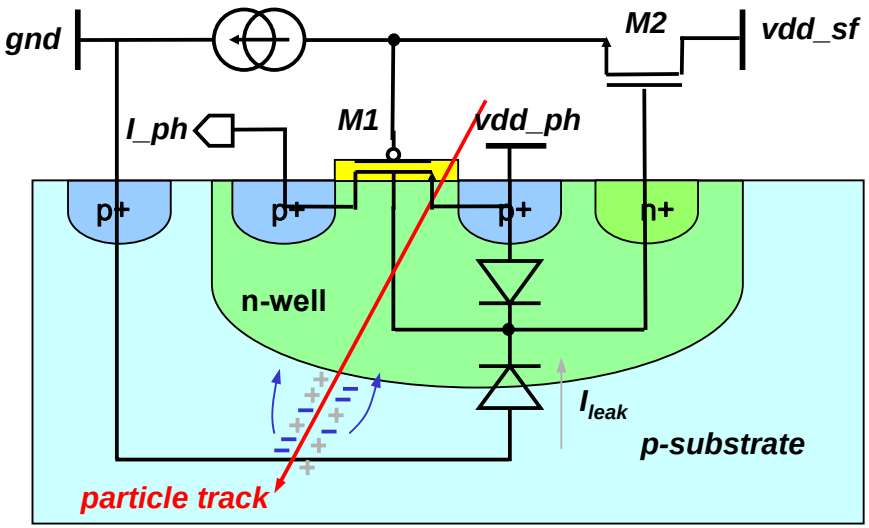
New charge sensing elements: PhotoFET



Charge collected at the N-well affect the threshold voltage of a pMOS transistor and modulates its current: signal amplification

-Charge-to current amplification

-High transconductance = high sensitivity

-Low noise/large collection area

First prototype test results

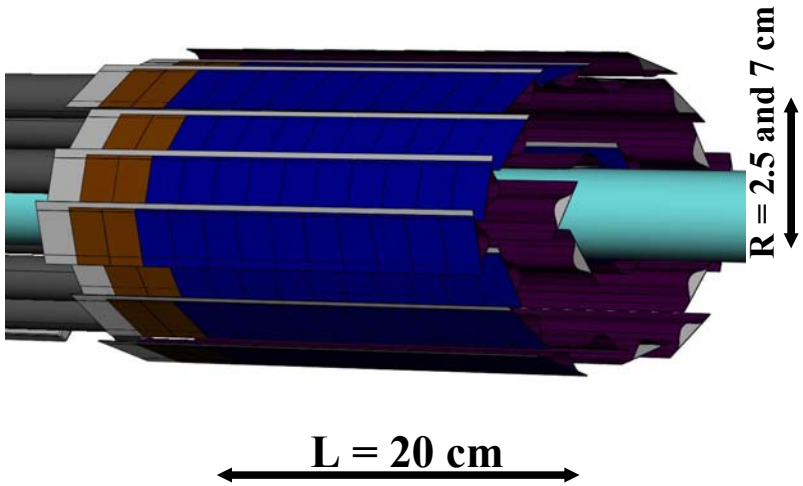
Sensitivity: 330 pA/electron

ENC: ~5 electrons

But serious (and confirmed) performance degradation when assembled in array… Substrate pick-up???

Applications of MAPS in particle physics experiments: slow (serial, analog) readout

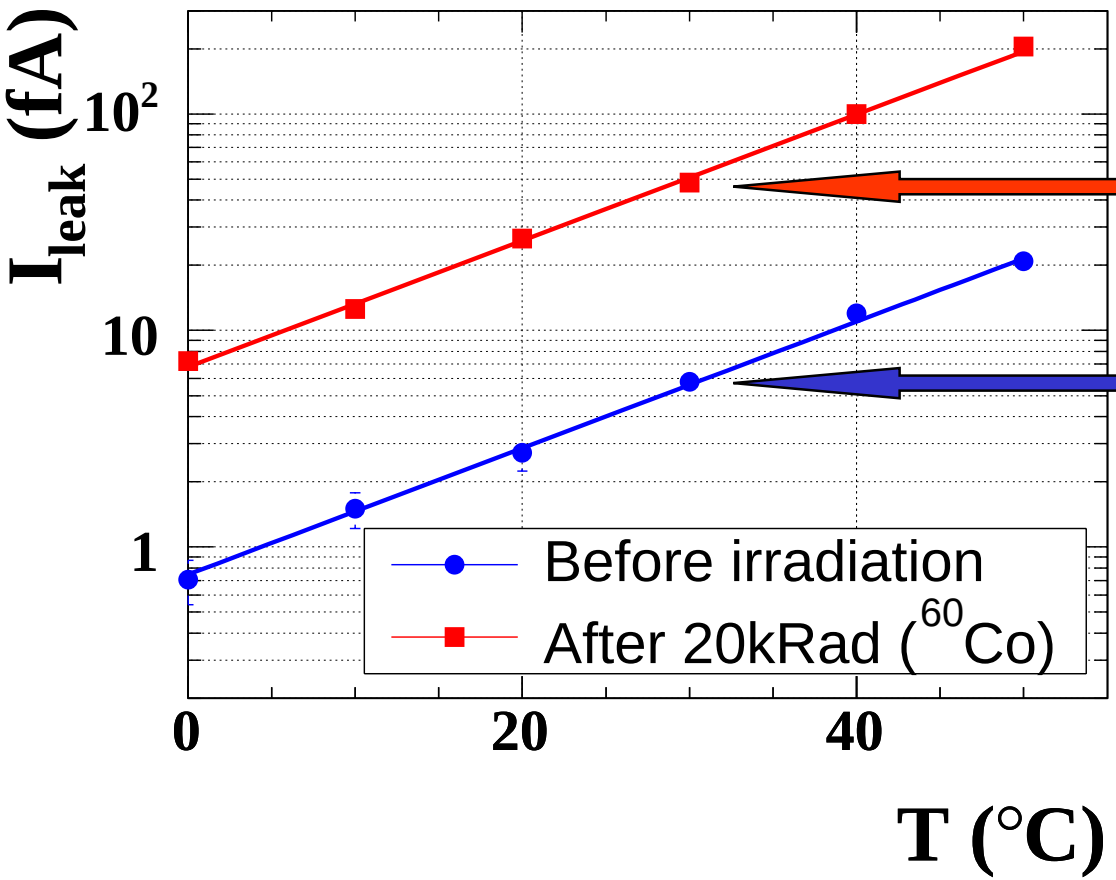
STAR



STAR VxD upgrade 2008: 9+24 ladders

- (analog) readout time = integration time = 2 - 4 ms
- Room temperature operation (chip at ~ ≤40°C)
- Air cooling only
- Ionizing radiation dose:~8 krad/year (3 10^{11} p/cm^2/year)
- The Ultimate Upgrade: luminosity up, dose accordingly higher , integration time ~10x shorter.
- Considered solution is based serial readout for the first upgrade and on column-parallel binary readout for the Ultimate Upgrade

Radiation tolerance for integrated ionizing dose: dark current increase



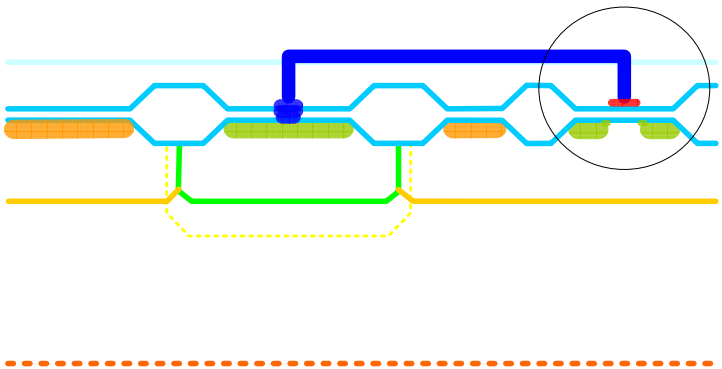
Shot Noise Contribution @ 30°C and @4 ms integration time

ENC_{shot} = 39 electrons

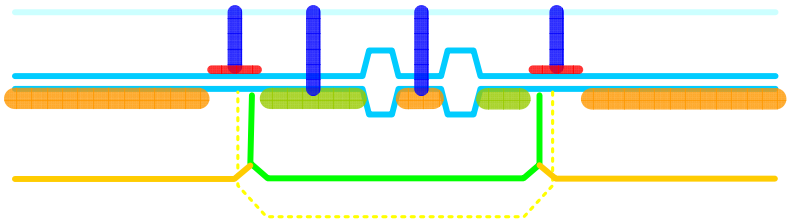
ENC_{shot} = 12 electrons

Standard N-well/p-epi diode dark current increase after irradiation with a ^{60}Co γ source (Mimosa9)

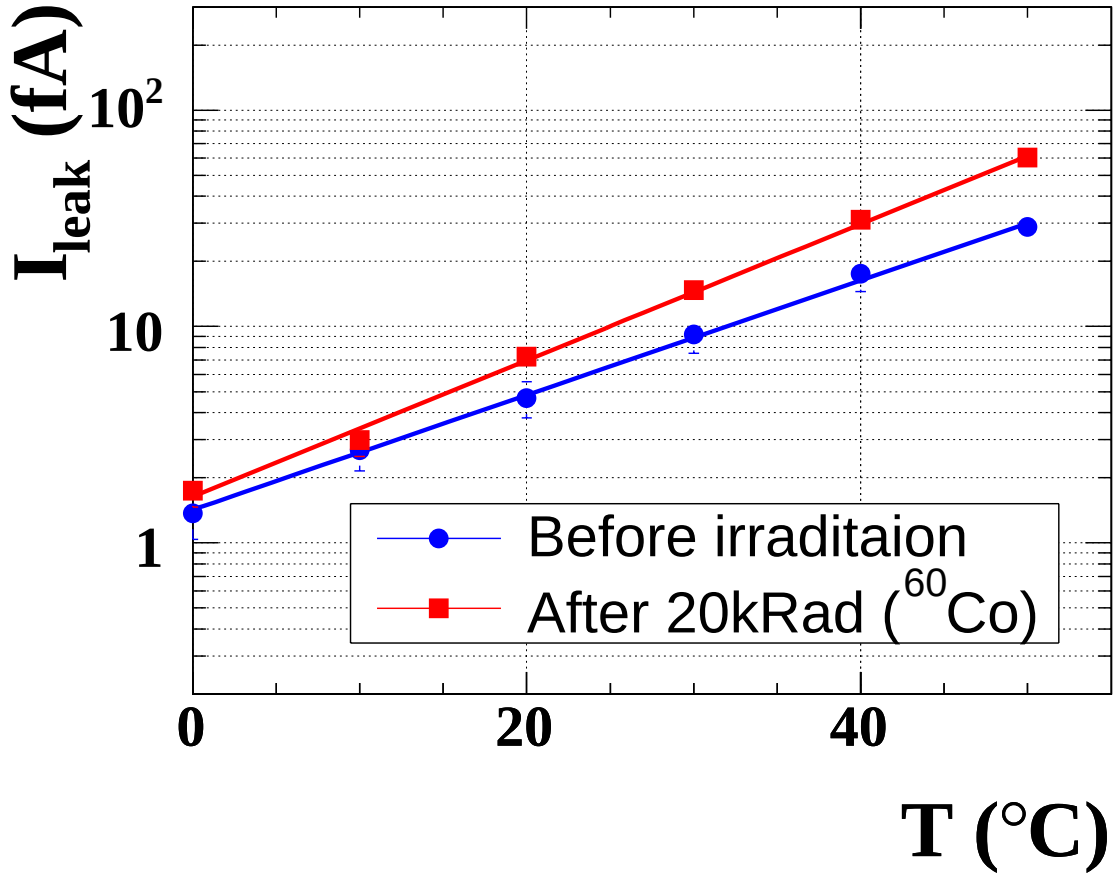
"Thin-oxide" diode dark current increase after irradiation with a ^{60}Co γ source



standard diode layout



thin-oxide diode layout



Recent results (Mimosa15): x10 current increase after 1Mrad

LDFOX

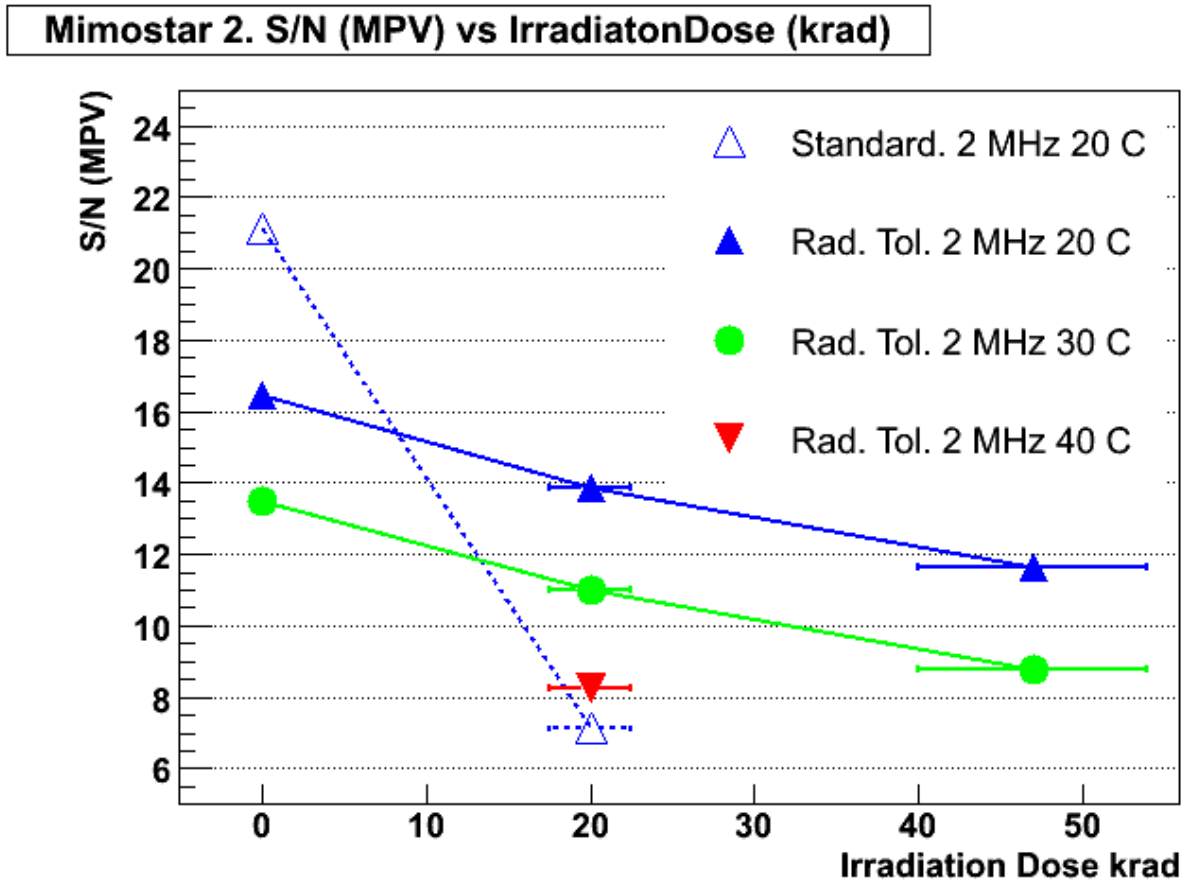
FOX

FOX

FOX

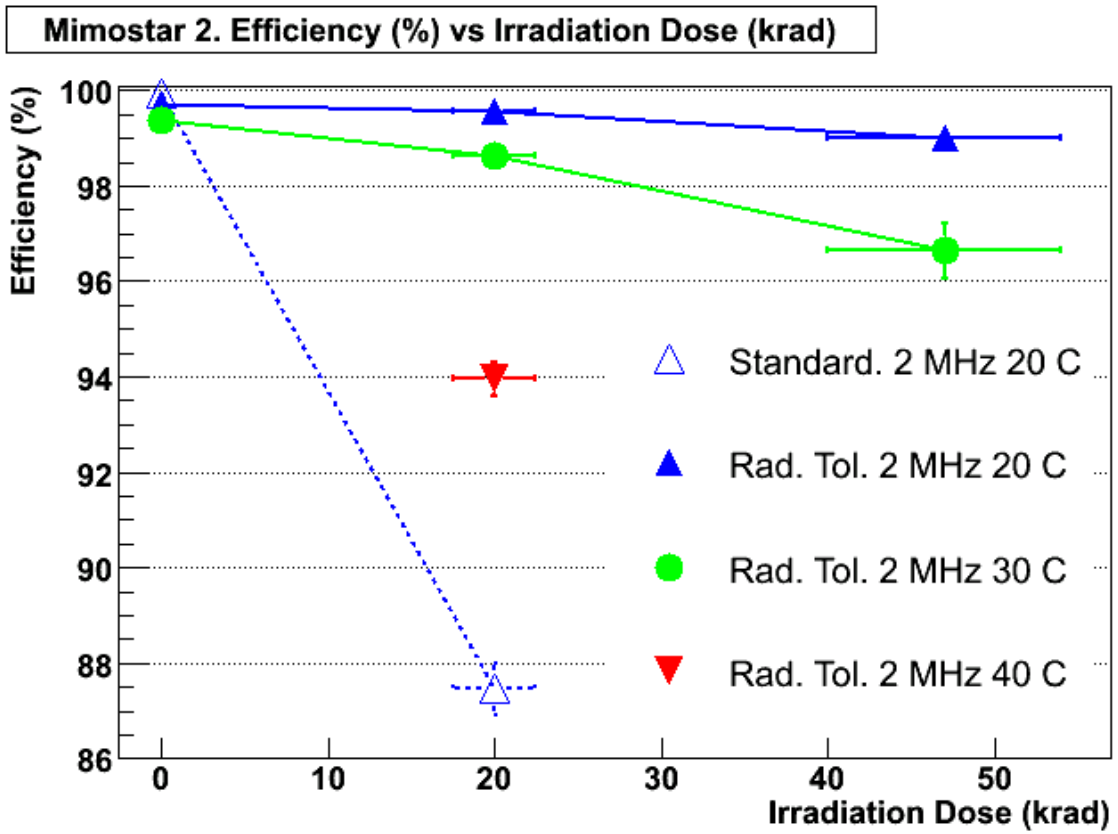
SF

MimoSTAR-2 (30 µm pitch): the demonstrator for STAR experiment microvertex upgrade. Based on radiation tolerant N-well collecting diodes. JTAG based control and bias setting.



S/N vs. dose

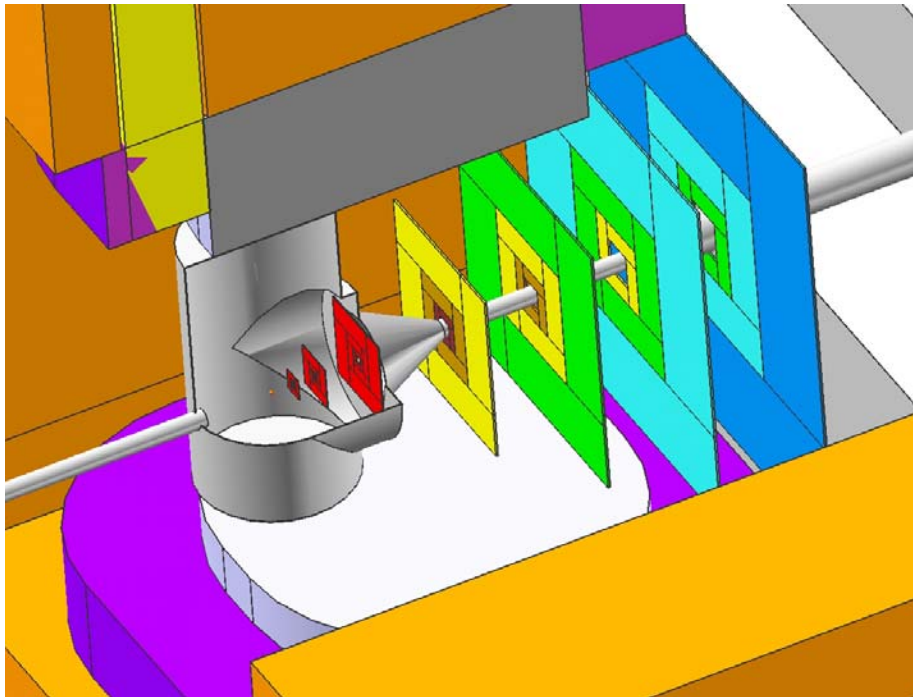
Mimo*2 beam tests: efficiency after irradiation



Efficiency vs. dose, for S/N cuts = 5 (seed) and 2 (crown)

After 47 kRads, efficiency >99 % at room temperature AND long (4ms) integration time, for the fake hits rate $<10^{-4}$

Applications of MAPS in particle physics experiments: fast, column parallel, digital readout



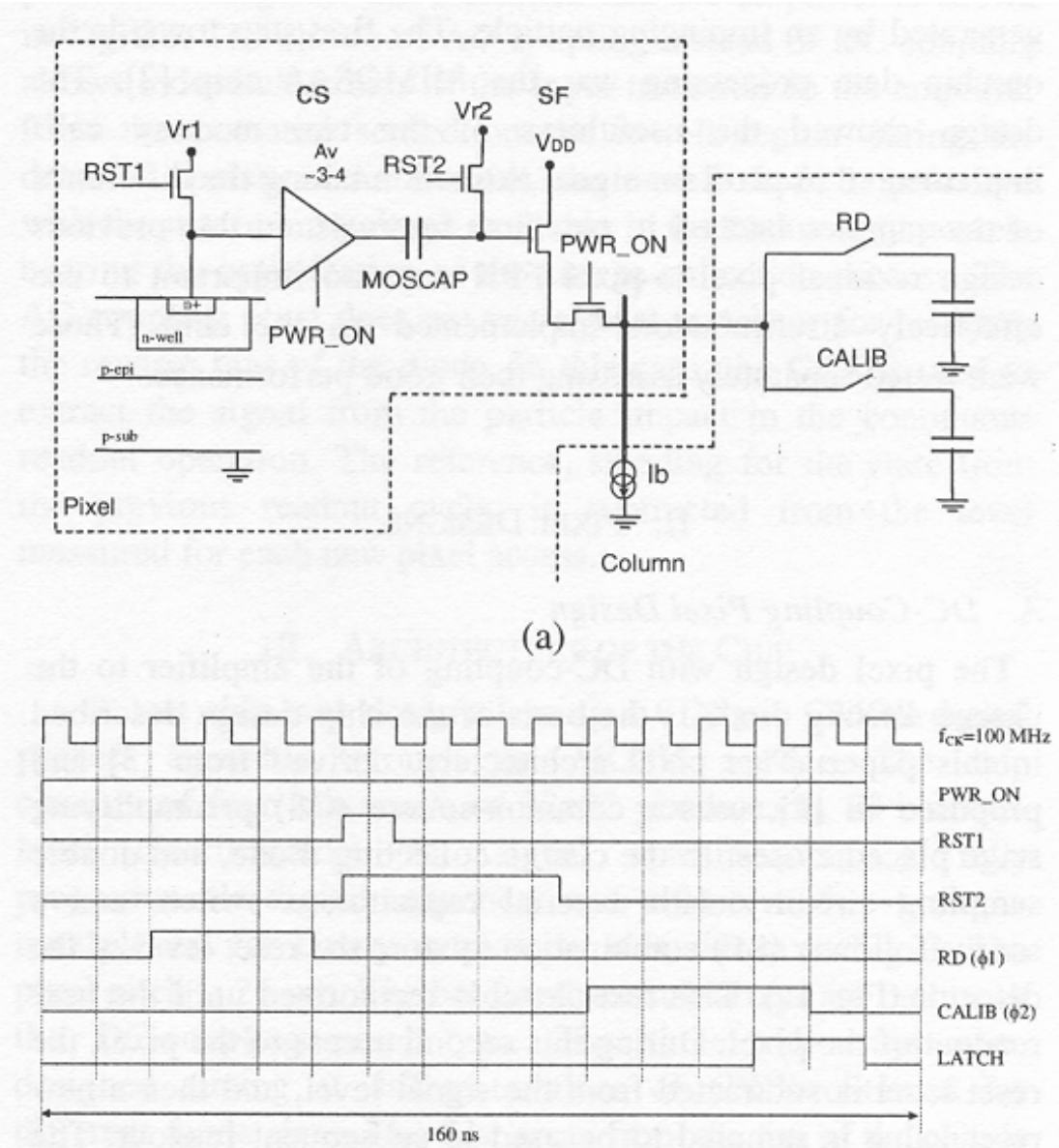
CBM vertex detector (FAIR/GSI)

- Readout time = integration = time resolution: <10 μs
- Binary readout, no zero suppression
- Vacuum operation
- Ionizing radiation dose: >2 MRad
- Neutron fluence (1MeV eq.): $>10^{13}$ n/cm^2
- Total single layer thickness: <150 μm (Si)

Extremely demanding application, but no alterative solution candidates…

Mimosa8 (TSMC-0.25µ, 8 µm epi) – a binary readout demonstrator

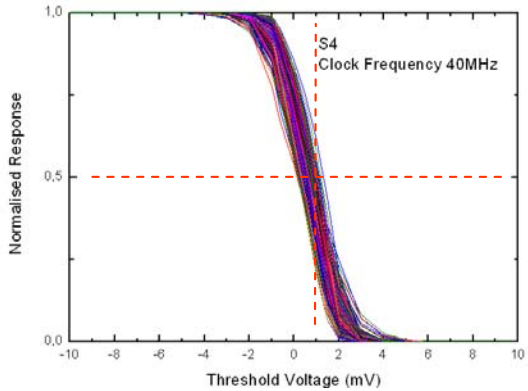
- **CDS in pixel, based on "clamping" circuit solution**
- **On-chip FPN suppression**
- **Offset compensated comparator at the end of each column**
- **Pixel pitch 25 x 25 µm2**



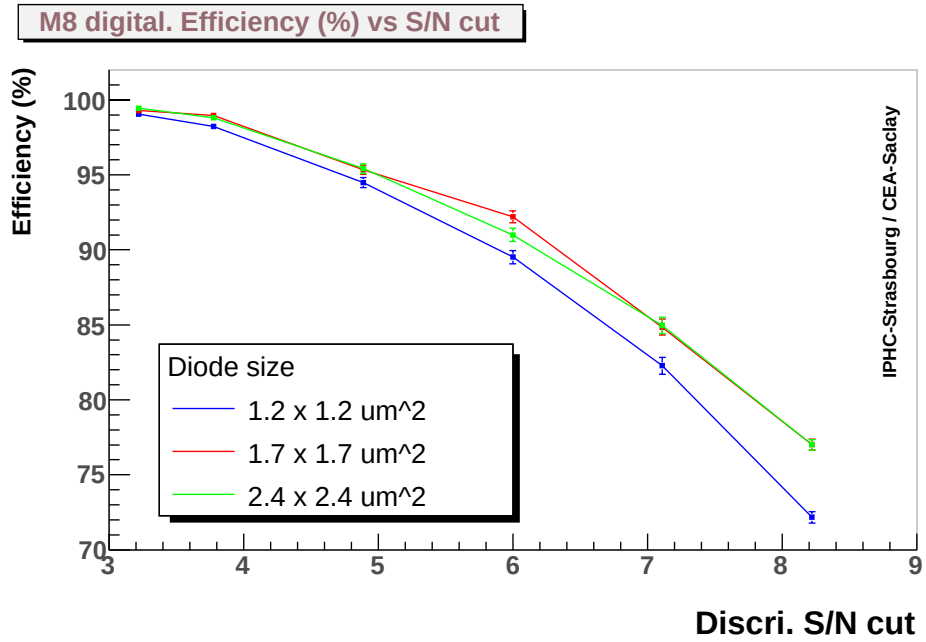
Prototype in collaboration with Dapnia/Saclay
→ Yavuz Degerli (principal author)

Wojciech.Dulinski@ires.in2p3.fr

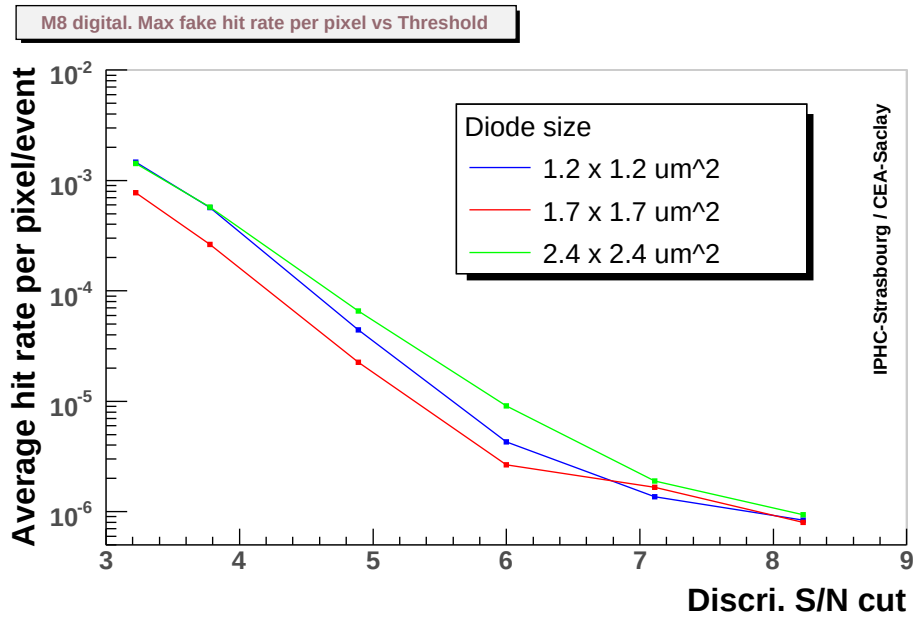
Mimosa8 beam tests results



Comparator voltage scan (all pixels)



- Output noise: 0.9 mV (ENC = 15 electrons)
- Pixel-to-pixel FPN: 0.45 mV (7.5 electrons)
- Spatial resolution: σ_r = ~7 µm



- First demonstration of feasibility of FPN correction using on-chip real time circuitry
- The design goal confirmed by the beam tests results: efficiency > 99 %
-Second version (Mimosa16) in AMS-035 OPTO with 14 and 20 µm epi under test

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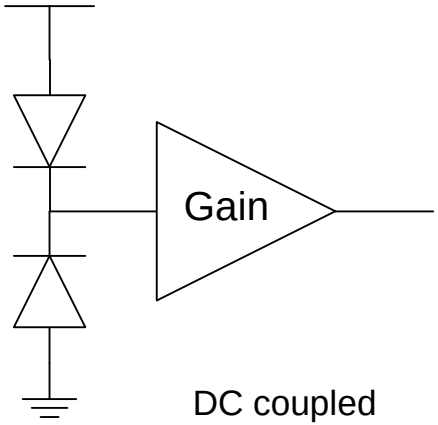
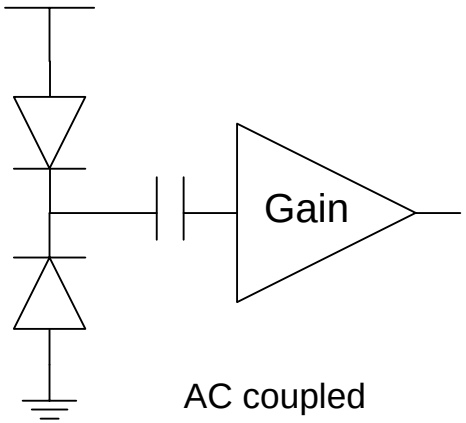
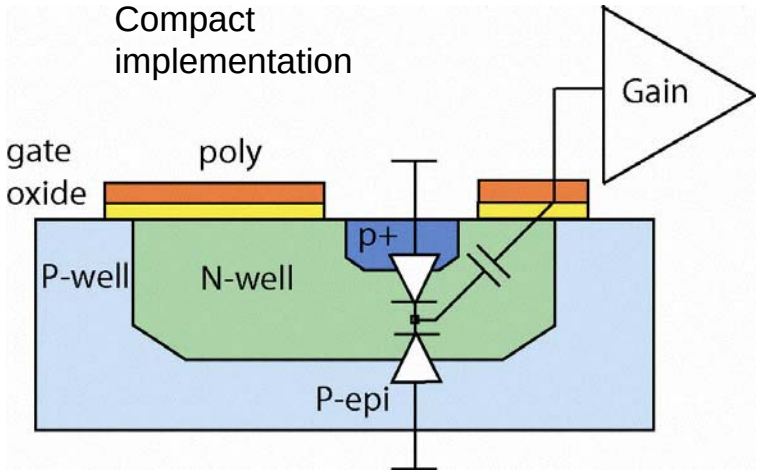
Amplifier optimization: DC coupled and AC coupled on-pixel amplifiers (→ Michal Szelezniak)



AC coupled amp:

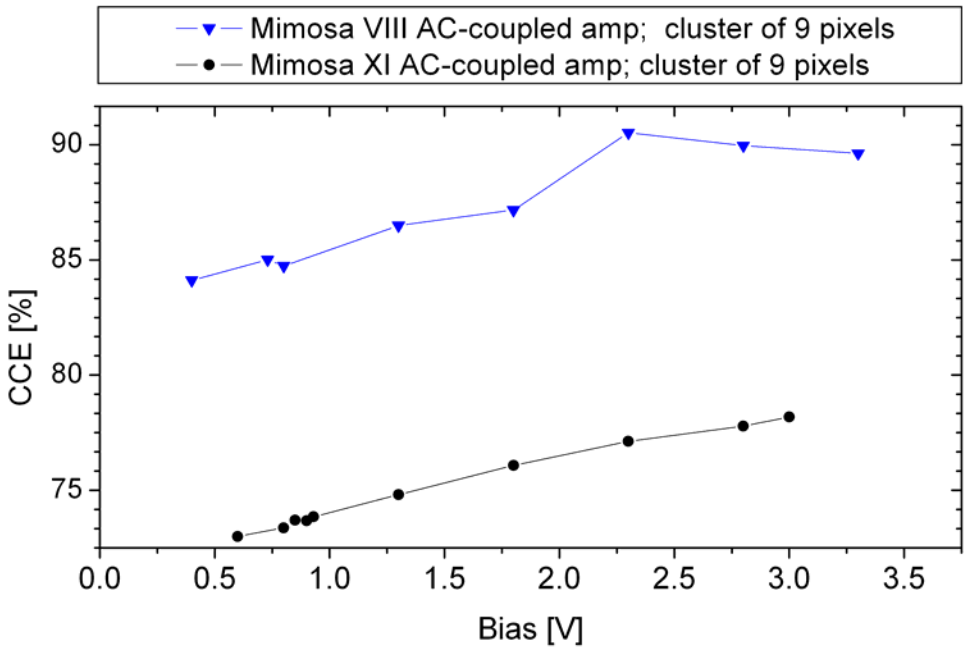
- Separation from power supply of the sensing node
  - Increase of the voltage ⇒ increase of the depleted region ⇒ no change on the operating point
- Separation from influence of the leakage current
  - Increase of the leakage current after irradiation ⇒ change of the bias on the sensing node ⇒ no change on the OP

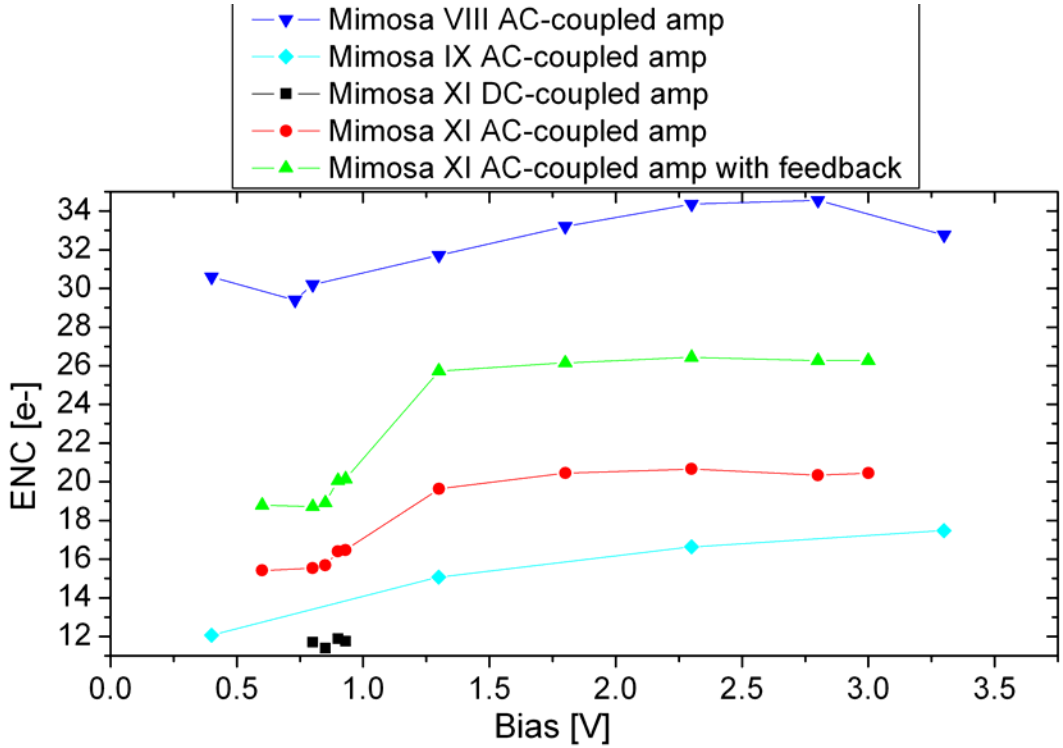




DC versus AC diode coupling

Charge collection efficiency and ENC in function of bias of charge collecting diode

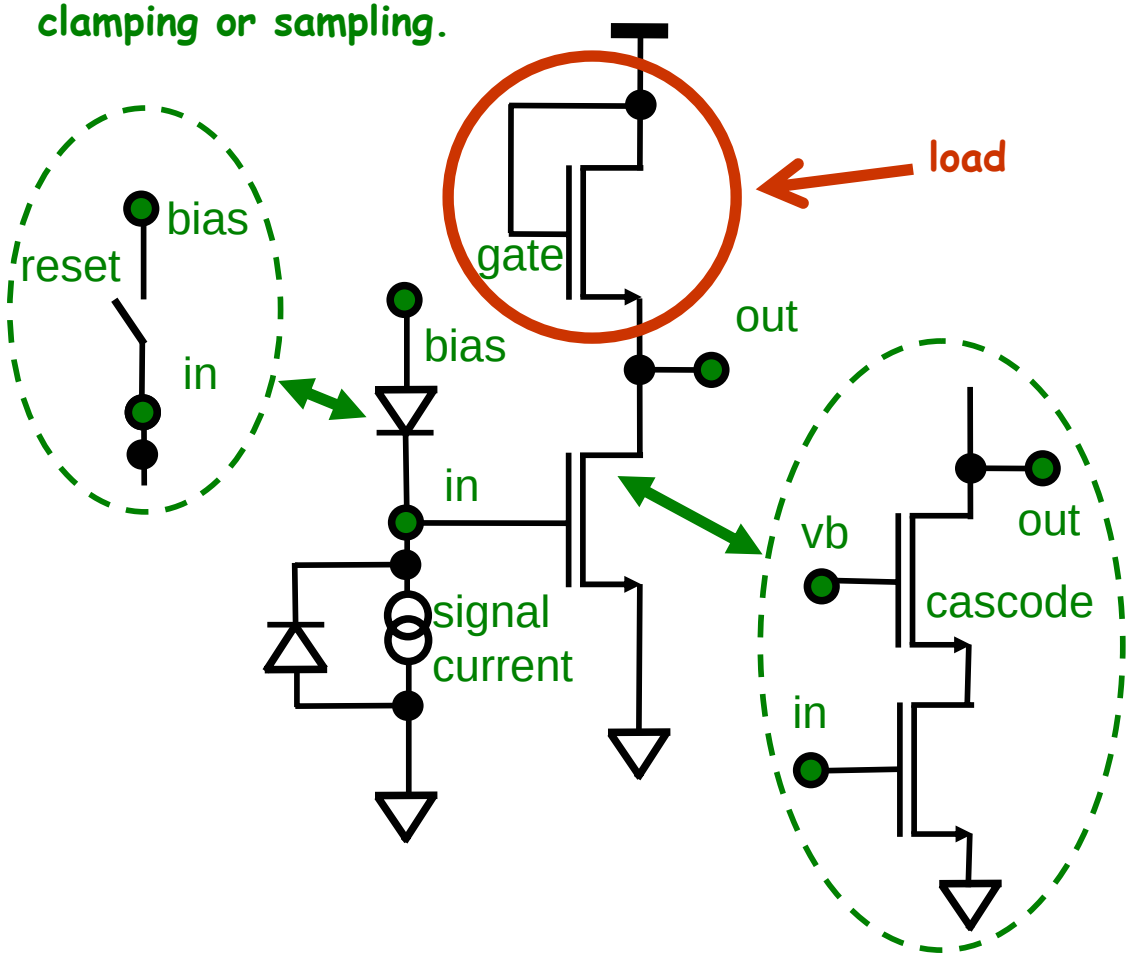




DC seems to win in simplicity and performance…

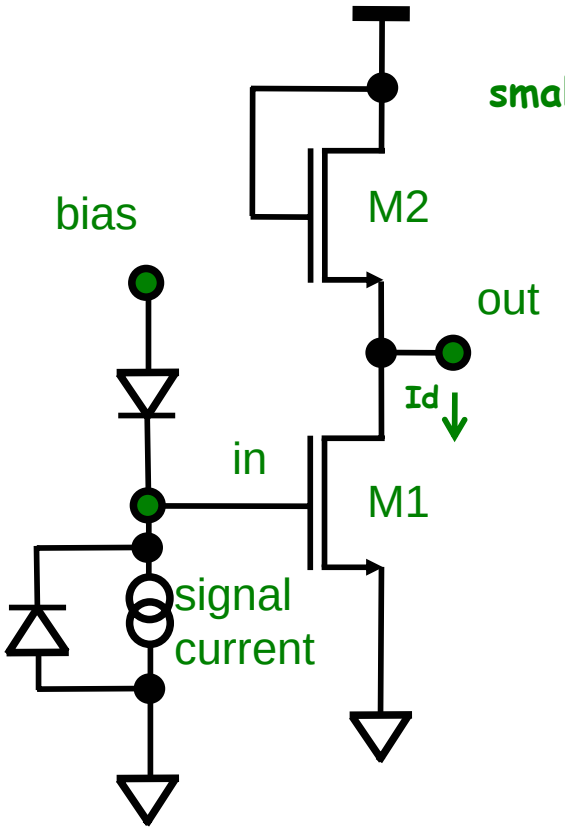
Amplifiers for MAPS (→Andrei DOROKHOV)

Amplification is needed to decrease noise contribution from switching networks, like clamping or sampling.



- PMOS transistors not allowed inside pixel -> signal decrease due to parasitic NWELL
- but using PMOS transistor as a load would be the preferred choice to increase in-pixel amplifier gain…

Amplifiers for MAPS



small signal Gain = $V_{out}/V_{in} = gm_1 /(gm_2 + gmb_2 + gds_1 + gds_2)$

As an example from simulation to be presented later:
gm_1=47 µS gm_2=4 µS gmb_2=0.9 µS gds_1=8 nS gds_2=0.5 µS

- gds_1 and gds_2 << gm_1, gm_2, gmb_2
- so one need to increase gm_1 and decrease gm_2 and gmb_2
- with decreasing gm_2 we decrease DC current, and hence gm_1 so there is a limiting contradiction for the gain/bandwidth of this schematic…

↓

Due to gm_2 there is unwanted dependency of I_d on U_{out} , so can we reduce dependency of I_d on U_{out} without changing gm_2 ?

↓ ?

Improved load for the common source transistor

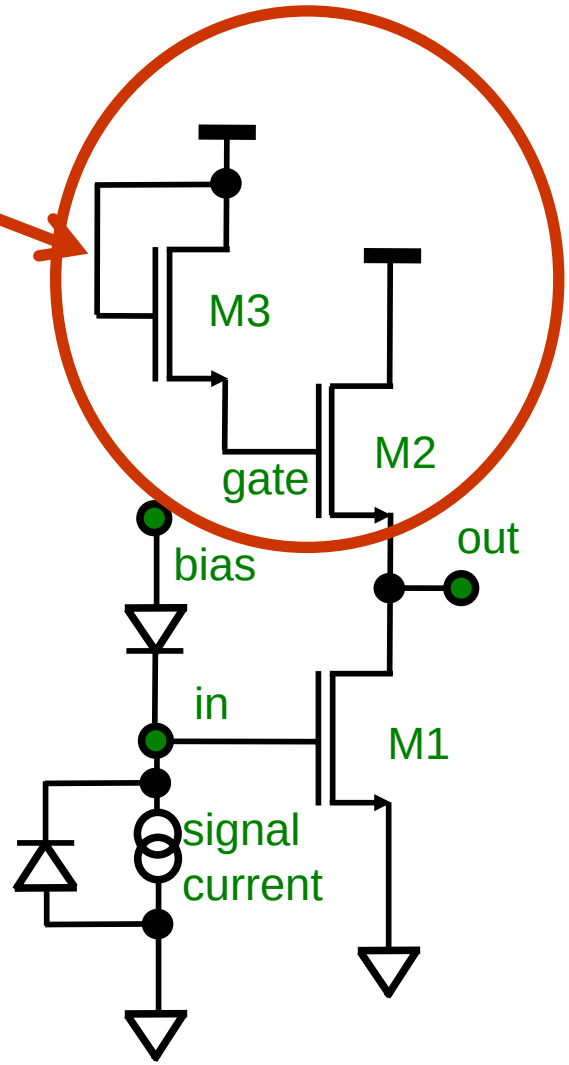
-> decouple the gate of the load transistor from the power supply with one additional NMOS transistor, used as a diode

due to the floating gate and parasitic gate-to-source capacitive coupling the AC voltage at the gate will follow to the output AC voltage ->

- AC current and hence the load for the common source transistor decreases
- load for DC is almost unchanged as DC voltage drop on additional NMOS transistor is small

$$Gain = V_{out}/V_{in} = gm_1 /(\cancel{gm_2} + gmb_2 + gds_1 + gds_2)$$

The AC gain should increase, while the DC operational point should not change!



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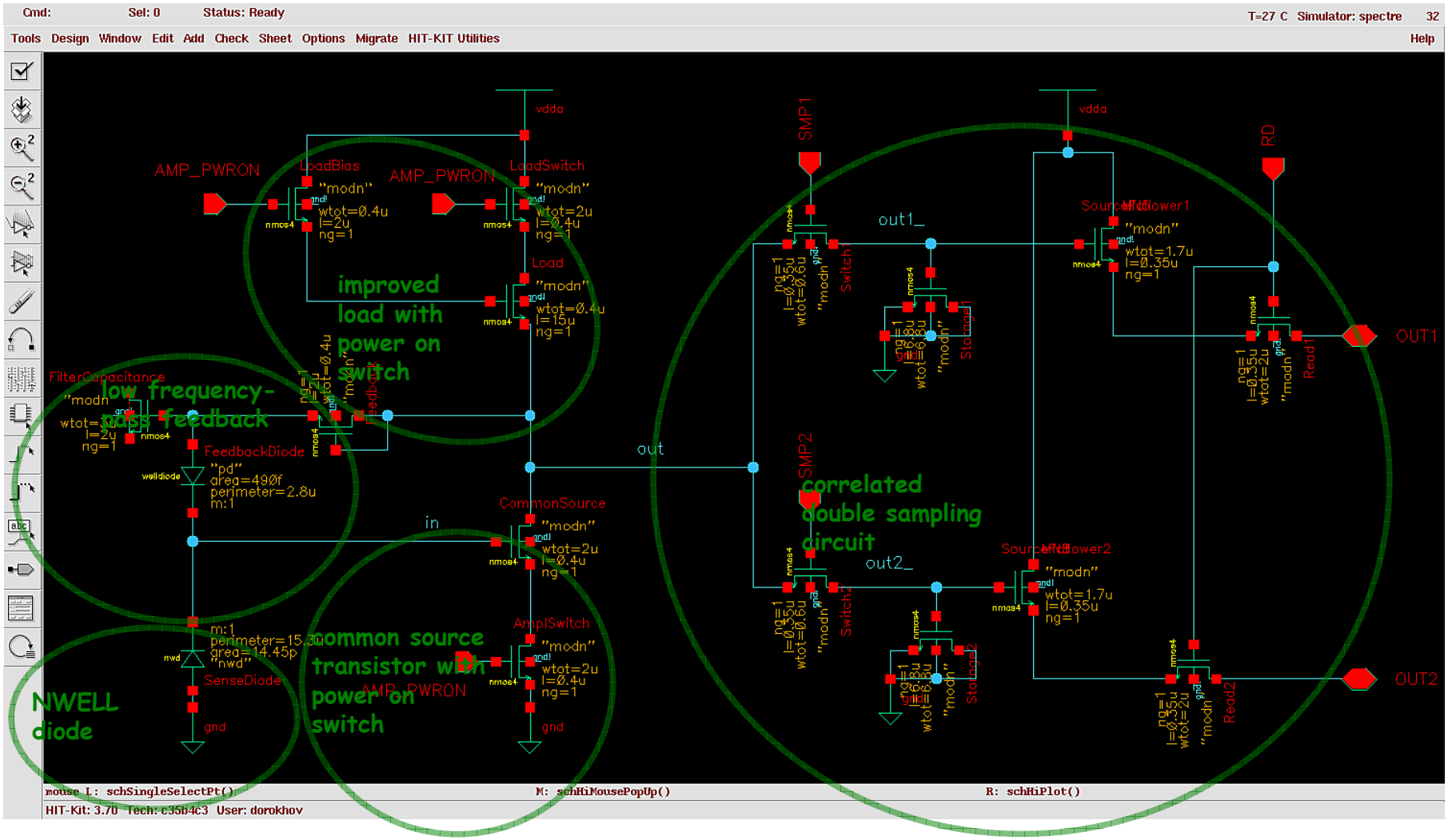
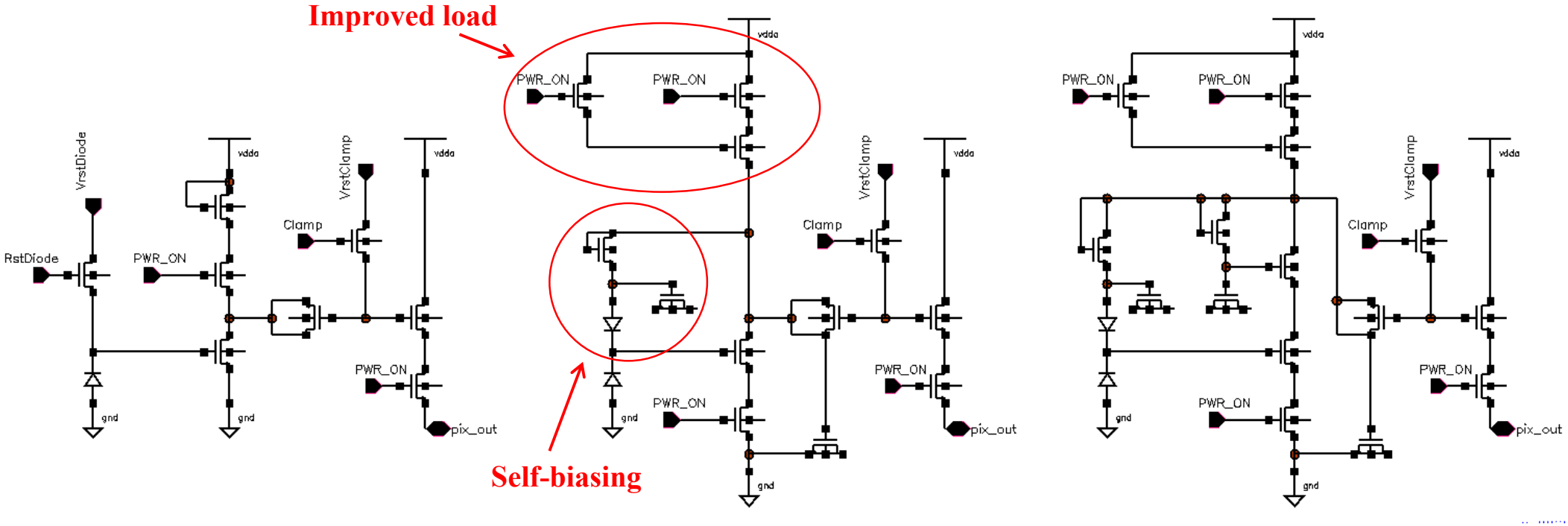
Test structures with new amplifier



- low noise, ~7.5 e (after CDS), and hence higher signal-to-noise ratio
- conversion gain is about 74 mV/e

Pixel optimization: diode size ↑ , charge collection ↑but also parasitic capacity and ENC ↑ !

Examples from measurements using recent AMS-035 OPTO test structures.



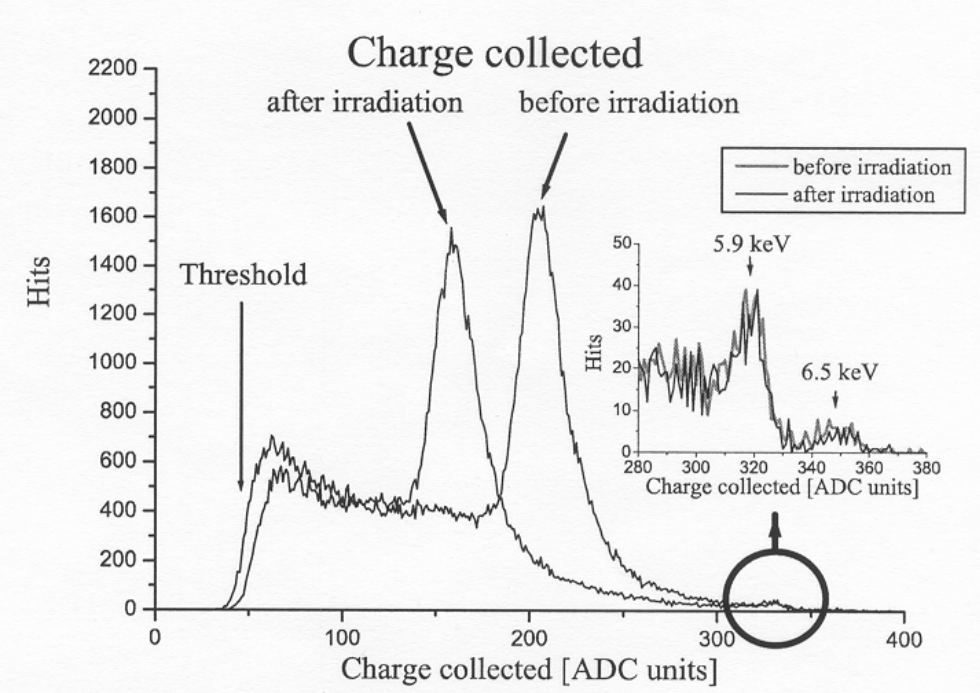
CS, 2.4x2.4 µm diode
ENC = 12 e, G = 65 µV/e
Charge coll. eff. <25%

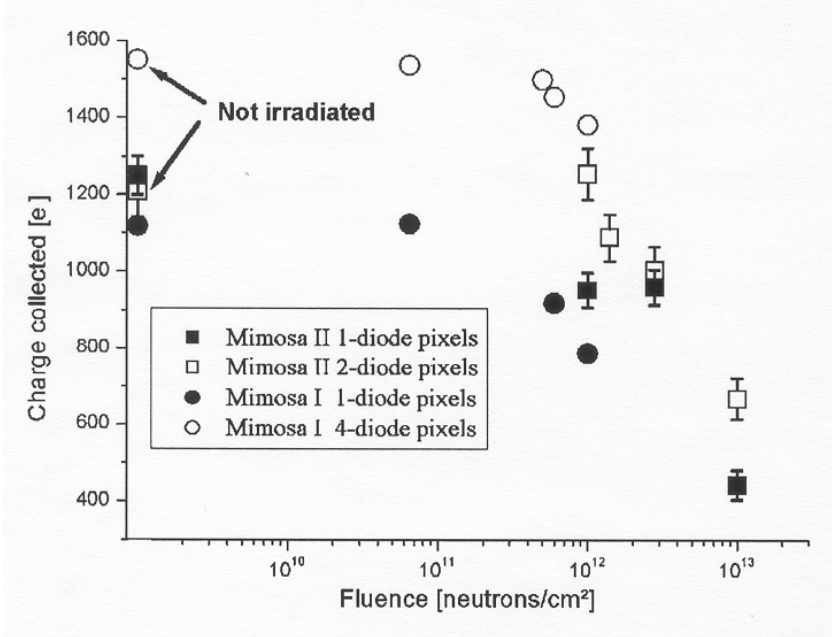
CSFb, 4.5x4.5 µm diode
ENC = 15 e, G = 45 µV/e
Charge coll. eff. >50%

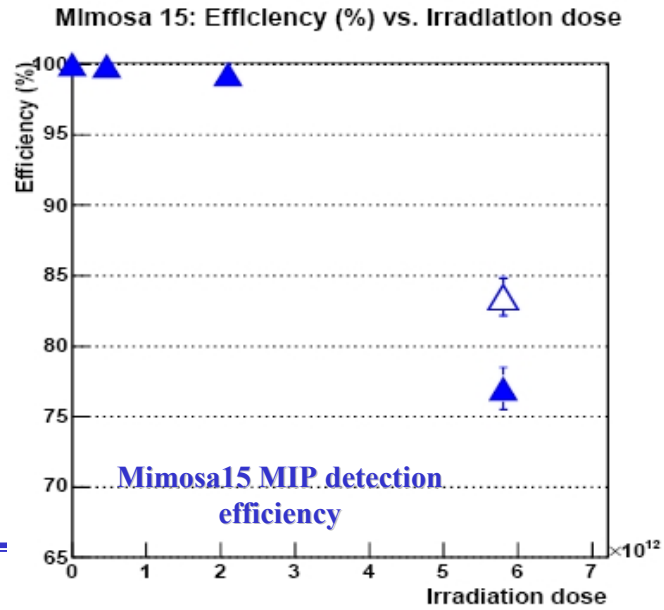
CAFb, 4.5x4.5 µm diode
ENC = 12 e, G = 65 µV/e
Charge coll. eff. >50%

*** Collection efficiency: charge collected in 3x3 cluster, measured on 20 µm thick epi wafer and 25 µm pixel pitch**

Radiation tolerance for the bulk damage: neutron irradiation







Charge loss after ~10^{12} n/cm^2, correlated to the diode/pixel area ratio, seems to be rather basic and process independent

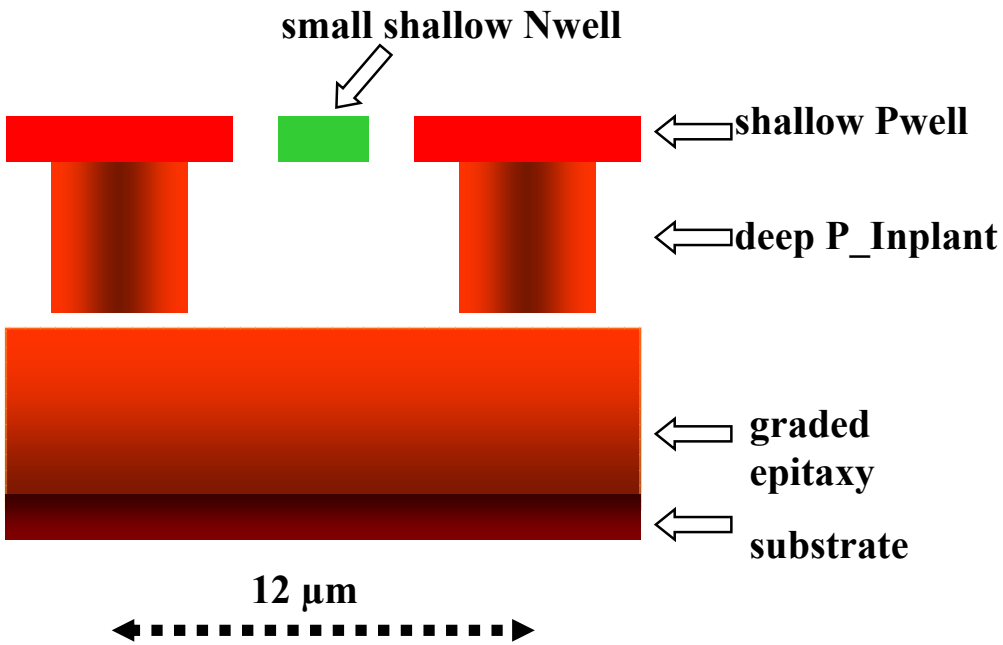
Possible (substantial) improvement

B. Dierickx *"Multiple or graded epitaxial wafers for particle or radiation detection", US Patent 6,683,360 B1, Jan. 2004*

PLUS deep implants available in some BiCMOS processes

Field shaping using doping gradient → faster charge collection → smaller sensitivity to the bulk damage

Field shaping → smaller charge spread → optimum conditions for the binary readout



Example from our simulation of novel MAPS structure (ISE TCAD, realistic doping profiles). In parentheses, typical standard structure.

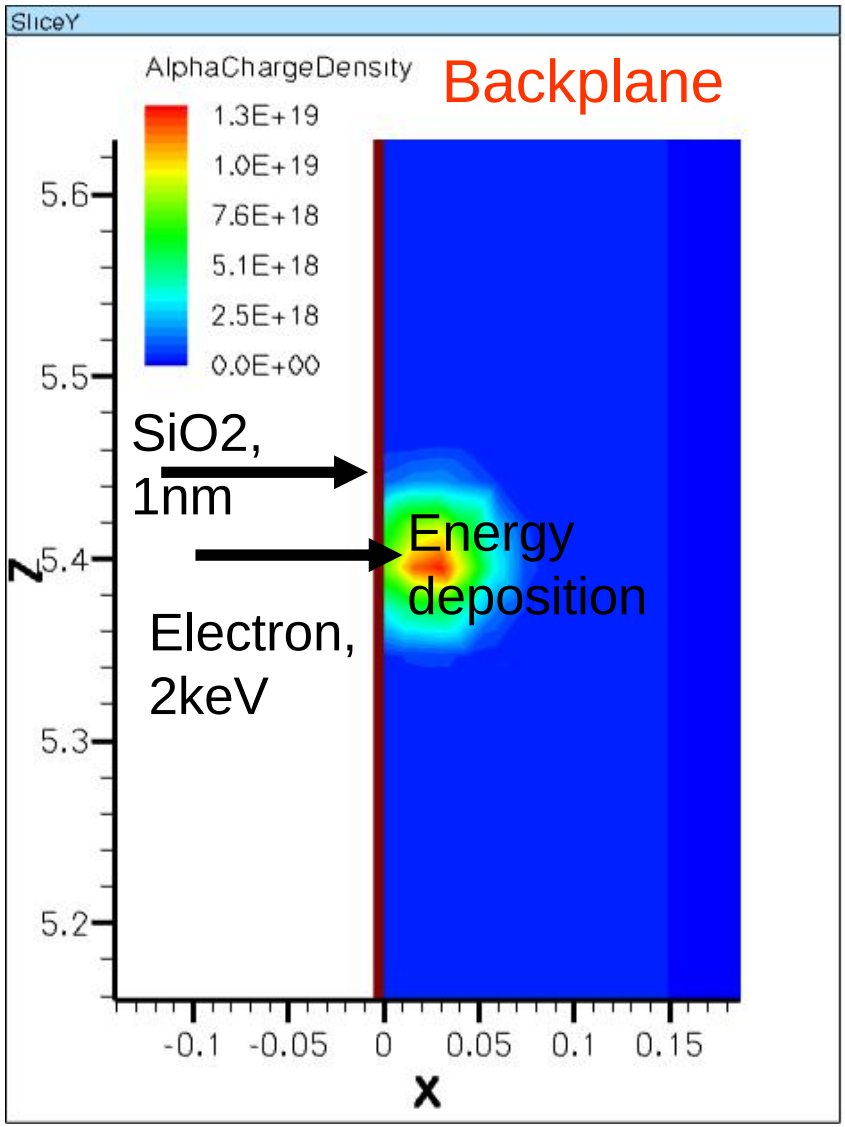
-Charge collection time: < 10 ns (~100ns)

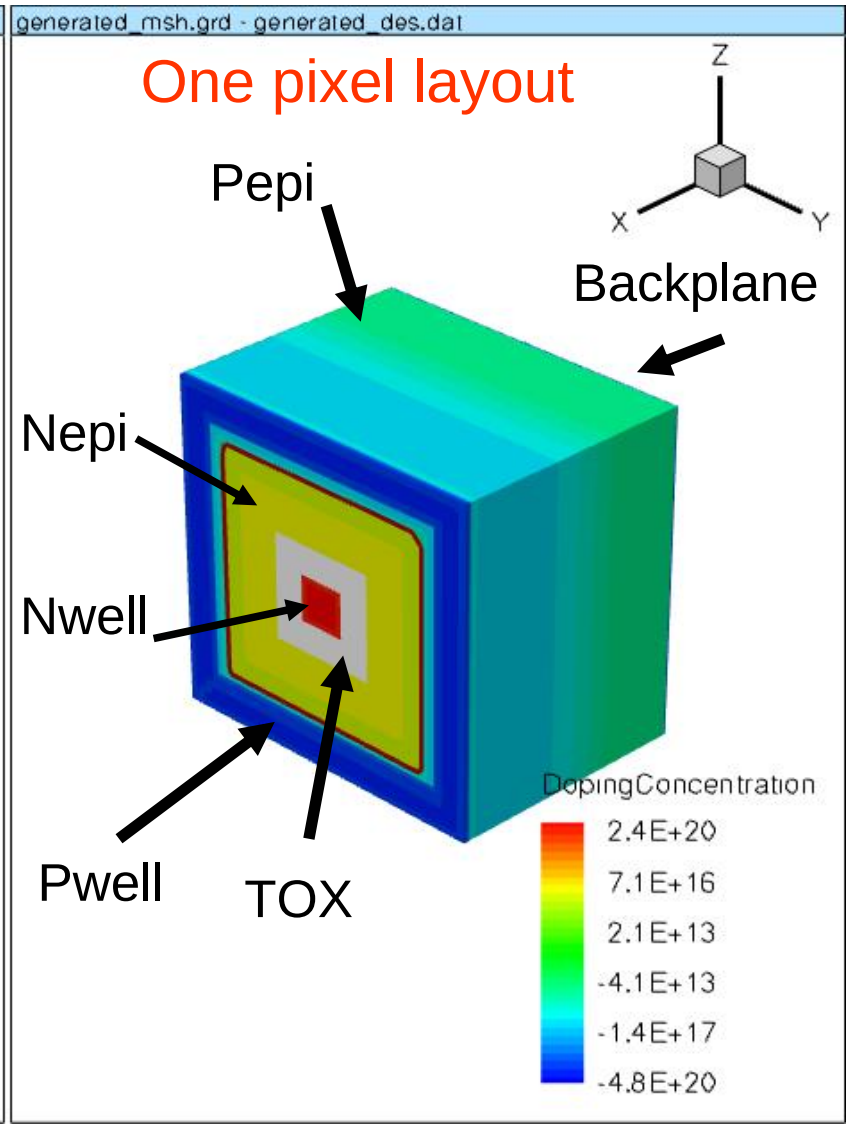
-Charge spread suppression:

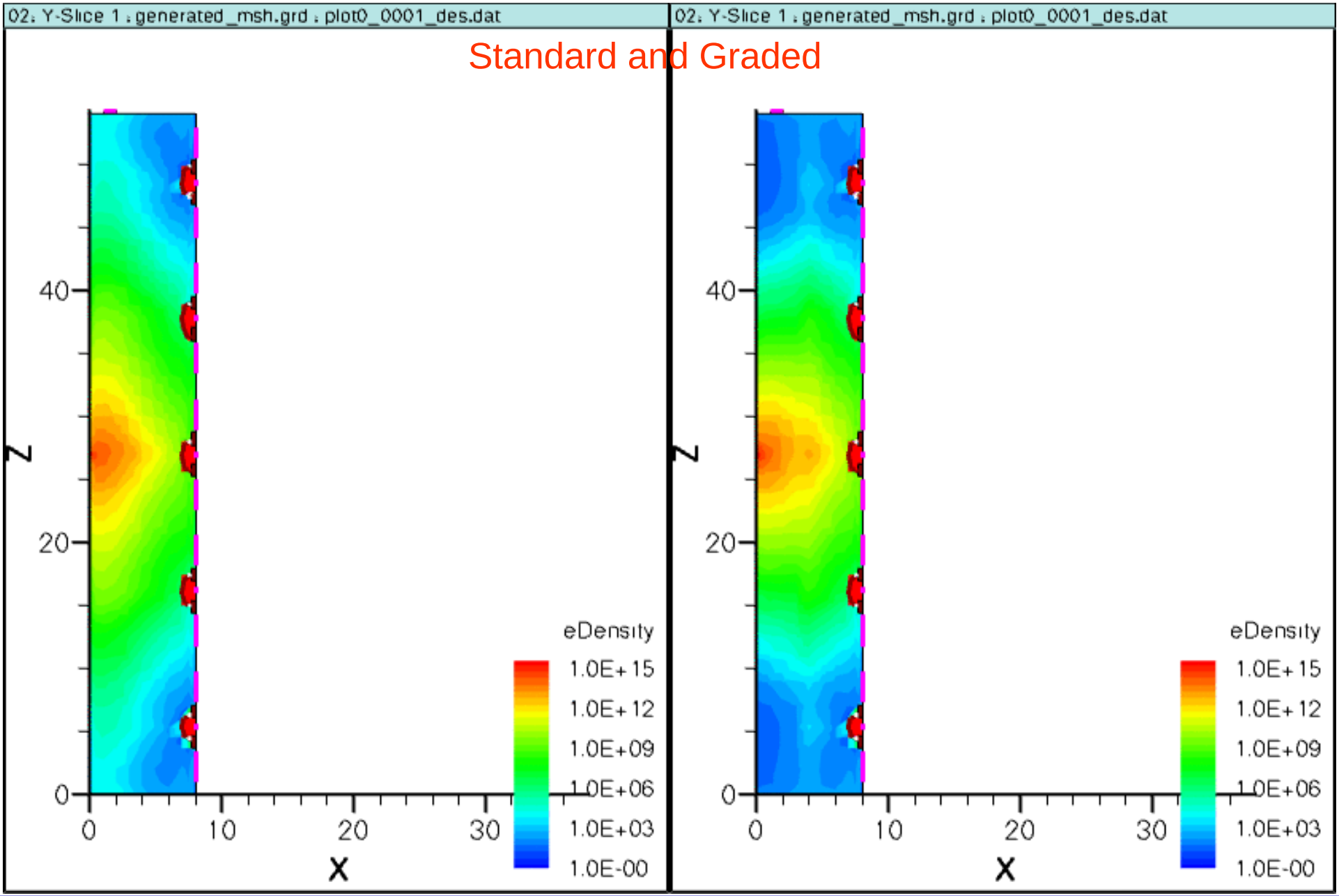
> 60% (<30%) of charge in central pixel, all charge inside < 4 pixels (>9 pixels)

Prototypes in construction!

Particle energy loss distribution and one pixel geometry (Andrei Dorokhov)

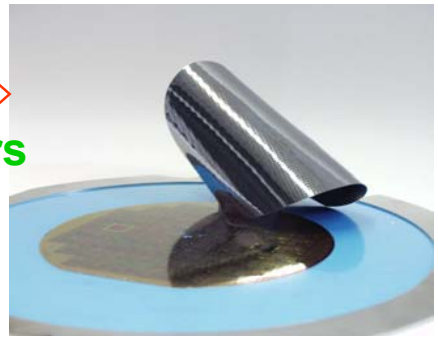


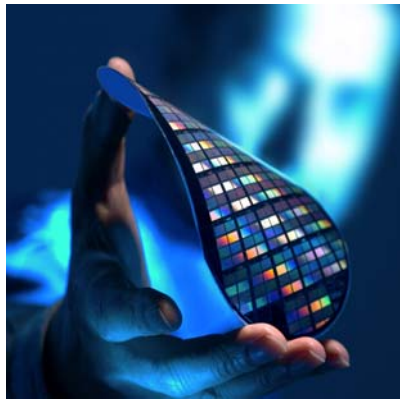




Electrons density (saturated color scale, in the n-well the actual density much larger)

Exploring new possibilities for MAPS performance upgrade, based on Vertical Integration (3D Electronics) industrial process.





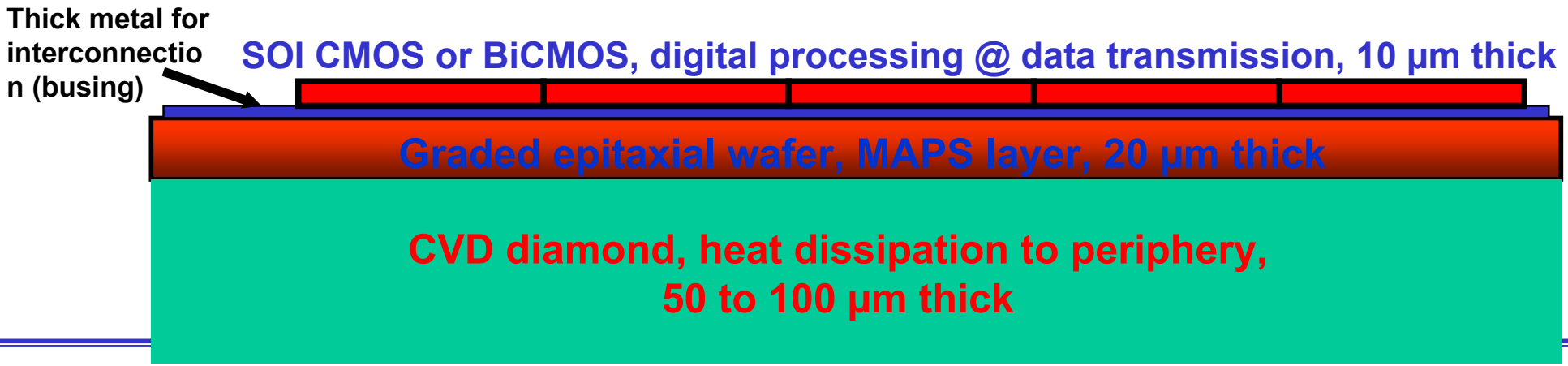
Vertical Integration ingredients:

-Wafers thinning down to 10-20 µm (→ flexible sheet!)
- Precision alignment and molecular bonding of several layers
-Through-wafer vias formation for electrical interconnection

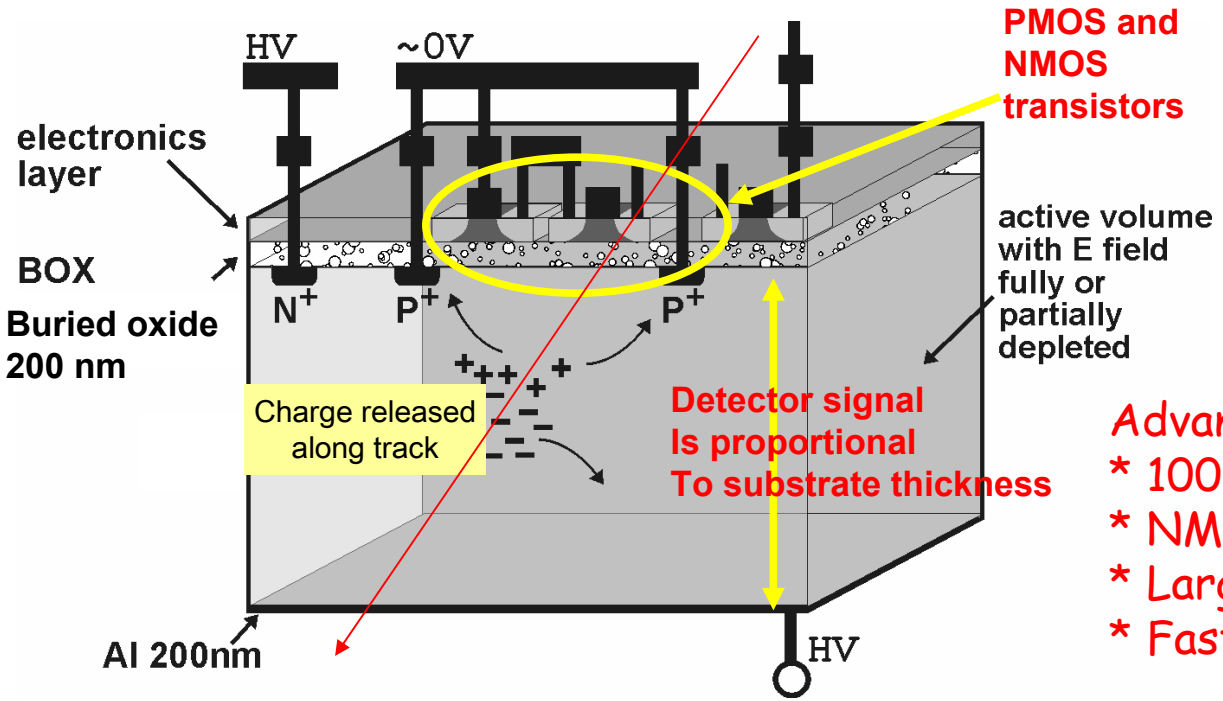
Result: 3D, monolithic circuit (or a sensor system)

Possible applications in tracking systems:

1. Construction of monolithic ladder, integrating two active silicon layers (one full plane, stitched MAPS, plus one signal processing and transmission layer) bonded to heat dissipation, diamond layer. Total thickness < 150µm → proposal for CBM application
2. Increased flexibility for wafer choice: post-processing step. Back-thinning and back-contact re-implementation at low temperature is possible, allowing an optimized use of thick, high-resistivity wafers available in many RF deep-submicron CMOS processes



Active Pixel Sensor in SOI



Advantages:
* 100% fill factor
* NMOS + PMOS transistors
* Large signal
* Faster charge collection

Thin top layer has silicon islands in which PMOS and NMOS transistors are built.
A buried oxide layer (BOX) separates the top layer from the substrate.
The high resistivity substrate forms the detector volume.
The diode implants are formed beneath the BOX and connected by vias.
The raw SOI wafers are procured from commercial vendors such as SOITEC in France.

©Ray Yarema

Fermilab SOI Detector Activities

SOI detector development is being pursued by Fermilab at two different foundries :OKI in Japan, and American Semiconductor Inc. (ASI) in US . The two processes have different characteristics as seen below

Process	**0.15μm Fully-Depleted SOI CMOS process, 1 Poly, 5 Metal layers (OKI Electric Industry Co. Ltd.).**
SOI wafer	**Wafer Diameter: 150 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、>1k Ω-cm (*No type assignment)*, 650 μm thick (SOITEC)**
Backside	**Thinned to 350 μm, no contact processing, plated with Al (200 nm).**

OKI Process
(available for HEP community through KEK)

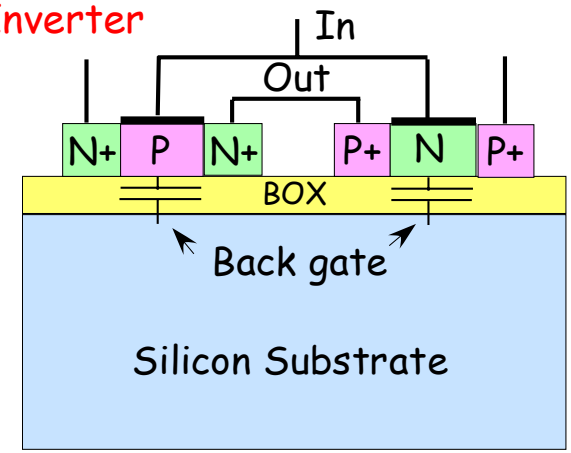
Process	**0.18μm partially-Depleted dual gate SOI CMOS process, Dual gate transistor (Flexfet), No poly, 5 metal (American Semicondutor / Cypress Semiconductor.)**
SOI wafer	**Wafer Diameter: 200 mmϕ, Handle wafer: FZ>1k Ω-cm (*n type)***
Backside	**Thinned to 50-100 μm, polished, laser annealed and plated with Al.**

ASI Process

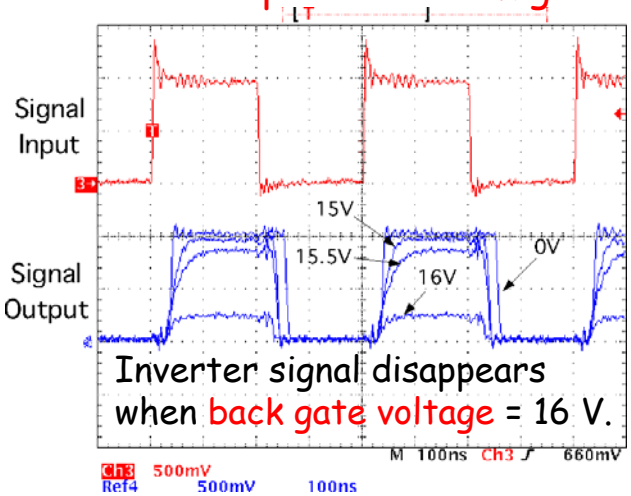
Wojciech.Dulinski@ires.in2p3.fr

Back gate Effect in OKI Process

Inverter

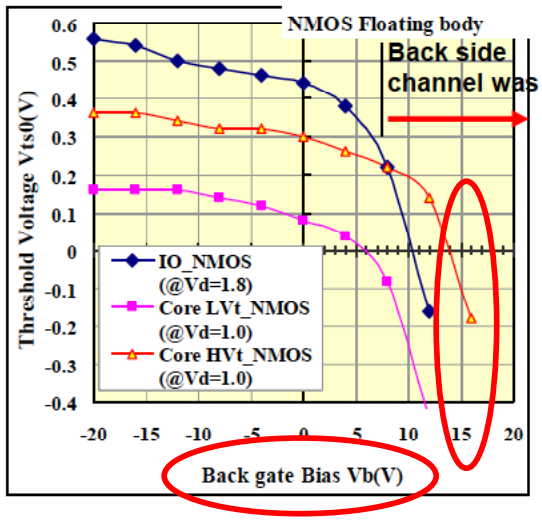


Inverter response to back gate

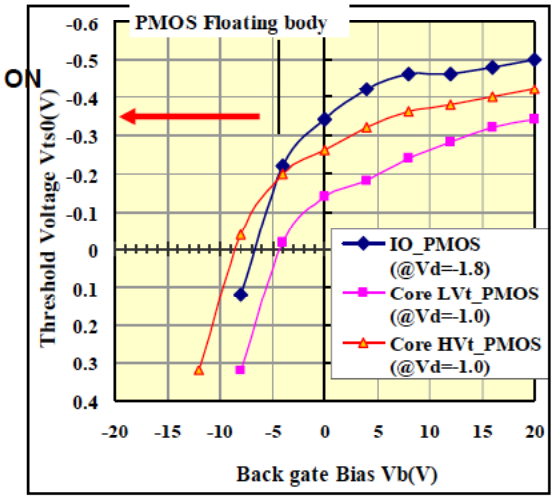


Substrate voltage acts as a back gate bias and changes transistor threshold

NMOS transistor



PMOS transistor



The threshold shift problem exists for SOI transistors in processes like OKI which have a floating body. The ASI process has a discrete back gate which shields the transistor from the substrate and thus eliminates the problem.

Results from KEK previous SOI-OKI submission: 2006.9.12 yasuo.arai@kek.jp(STD6)

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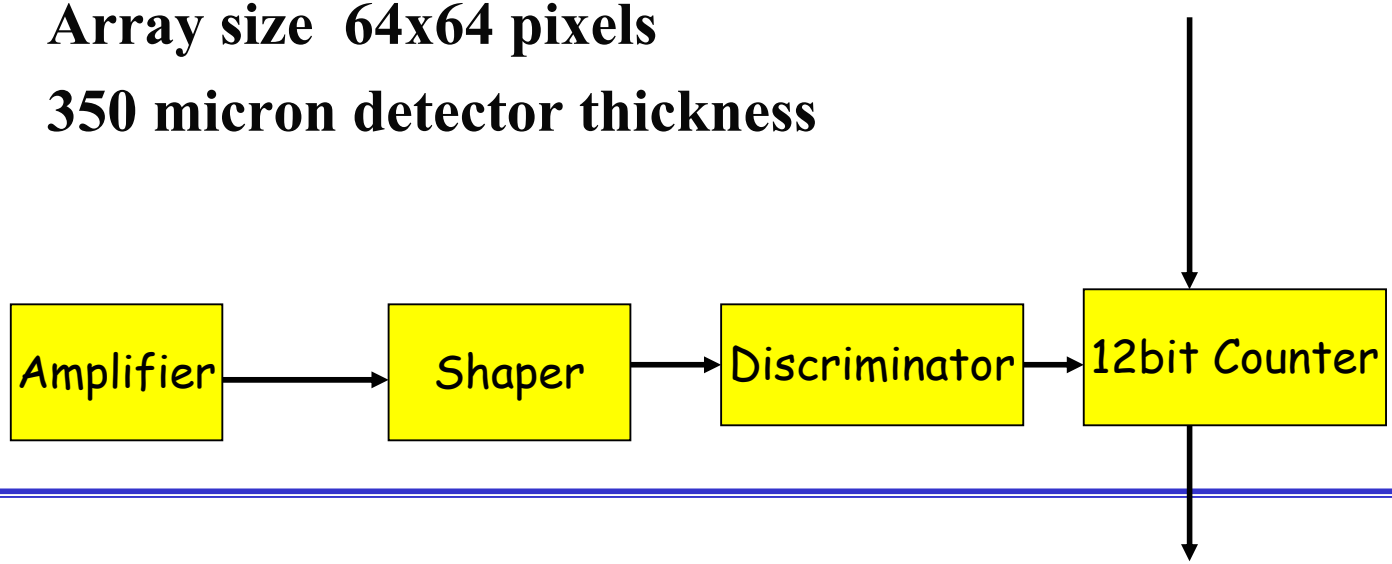
Fermilab MPW Pixel Design for OKI (→ Grzegorz Deptuch)

- Counting pixel detector plus readout circuit
  - Maximum counting rate ~ 1 MHz/pixel.
- Simplified architecture due to design time constraint
  - Reconfigurable counter/shift register
    - 12 bit dynamic range
  - Limited peripheral circuitry
    - Drivers and bias generator
- Array size 64x64 pixels
- 350 micron detector thickness

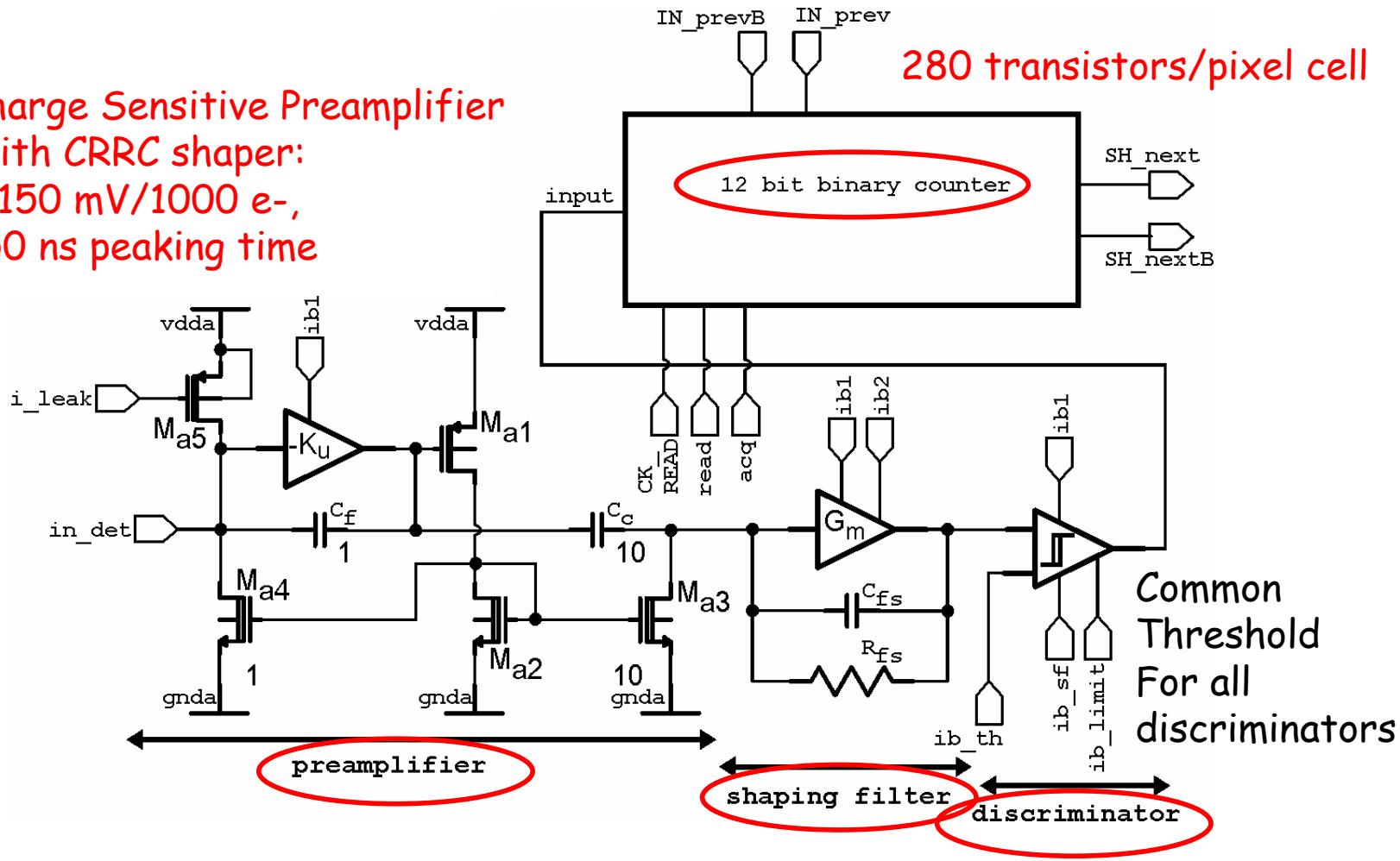


Wojciech.Dulinski@ires.in2p3.fr

Pixel Design in OKI Process

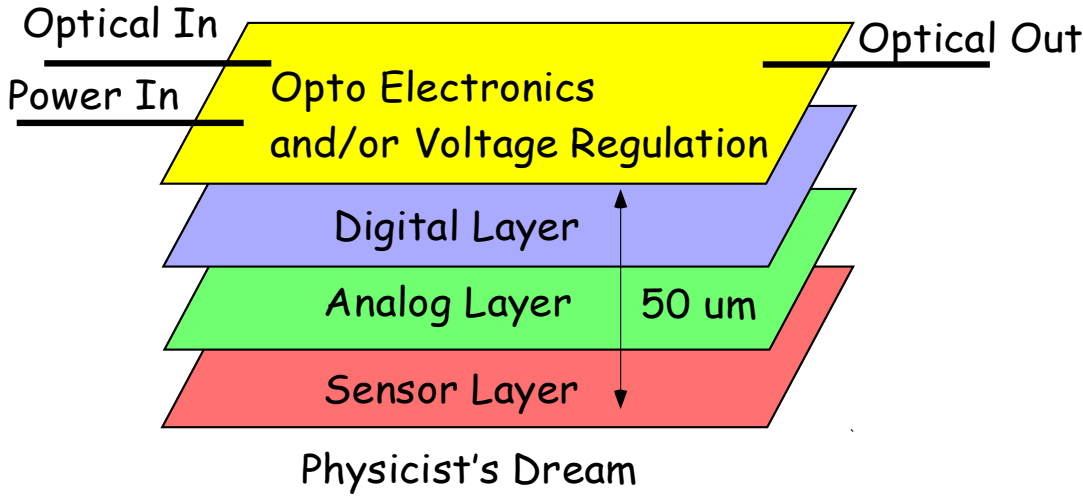
Charge Sensitive Preamplifier
with CRRC shaper:
~ 150 mV/1000 e-,
150 ns peaking time

280 transistors/pixel cell



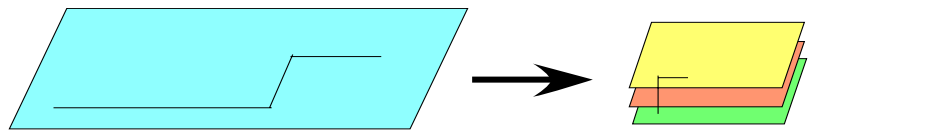
Vertical Scale Integration (3D): credit to Ray Yarema from FNAL!

- SOI detector technology offers several advantages over MAPS.
- 3D offers advantages over SOI detectors
  - Increased circuit density due to multiple tiers of electronics
  - Independent control of substrate materials for each of the tiers.
  - Ability to mate various technologies in a monolithic assembly
    - DEPFET + CMOS or SOI
    - CCD + CMOS or SOI
    - MAPS + CMOS or SOI



3D Integrated Circuits

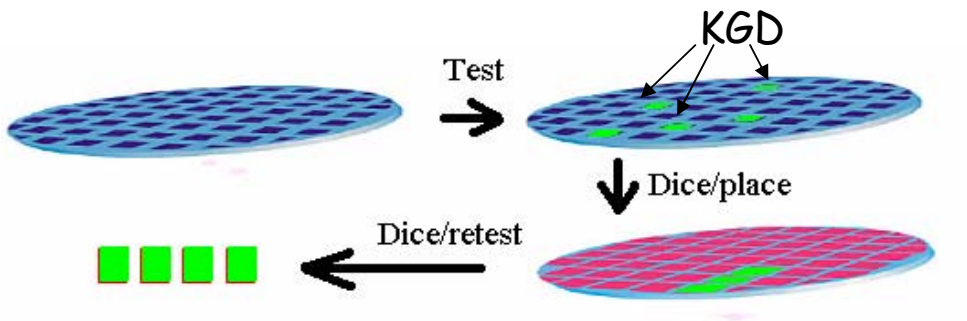
- A 3D chip is generally referred to as a chip comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded, and interconnected to form a "monolithic" circuit.
- Often the layers (sometimes called tiers) are fabricated in different processes.
- Industry is moving toward 3D to improve circuit performance. (Performance limited by interconnect)
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power and crosstalk



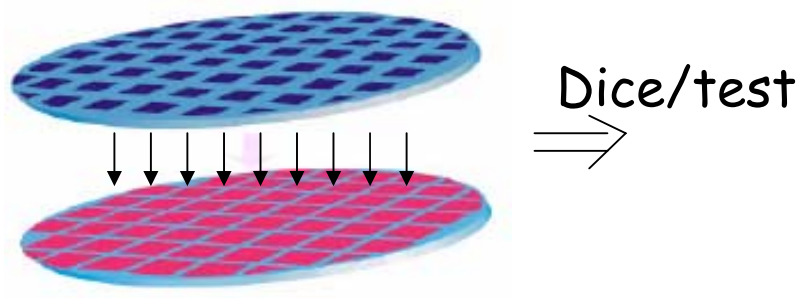
- HEP should watch industry and take advantage of the technology when applicable.
- Numerous examples of industry produced devices.[5,6,7] (See backup slides)

Two Different 3D Approaches for HEP

- Die to Wafer bonding
  - Permits use of different size wafers
  - Lends itself to using KGD (Known Good Die) for higher yields
- Wafer to Wafer bonding
  - Must have same size wafers
  - Less material handling but lower overall yield



Die to wafer bonding



Wafer to wafer bonding

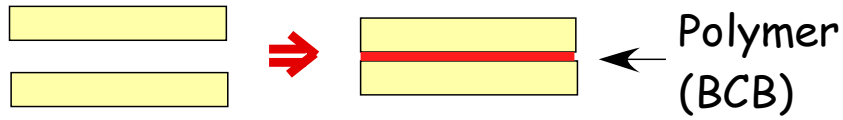
Key Technologies for 3D

- There are 4 key technologies
  - Bonding between layers
  - Wafer thinning
  - Through wafer via formation and metalization
  - High precision alignment
- Many of these technologies are also used in the development of SOI detectors

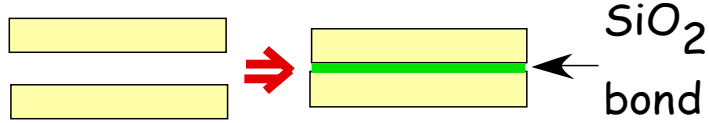
Key Technologies

1) Bonding between Die/Wafers

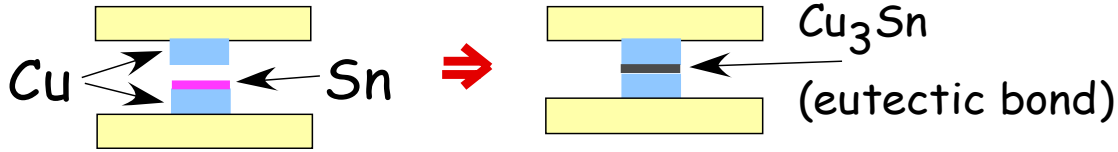
a) Adhesive bond



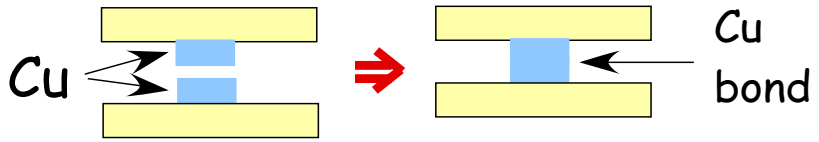
b) Oxide bond (SiO2 to SiO2)



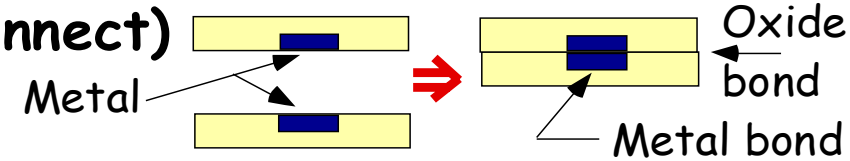
c) CuSn Eutectic



d) Cu thermocompression



e) DBI (Direct Bond Interconnect)



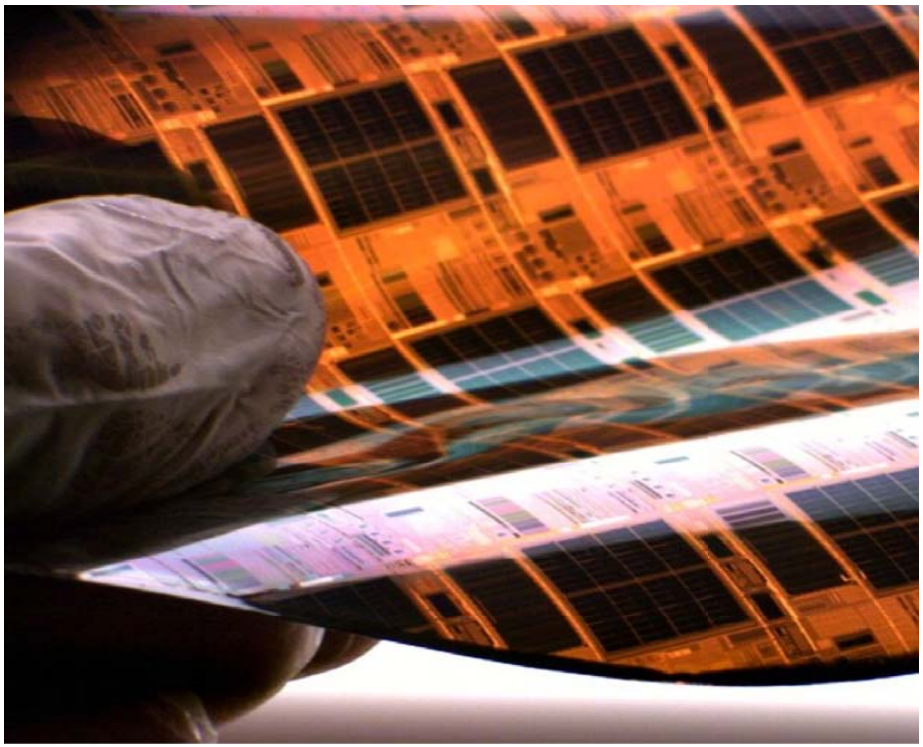
For (a) and (b), electrical connections between layers are formed after bonding. For (c), (d), and (e), the electrical and mechanical bonds are formed at the same time.

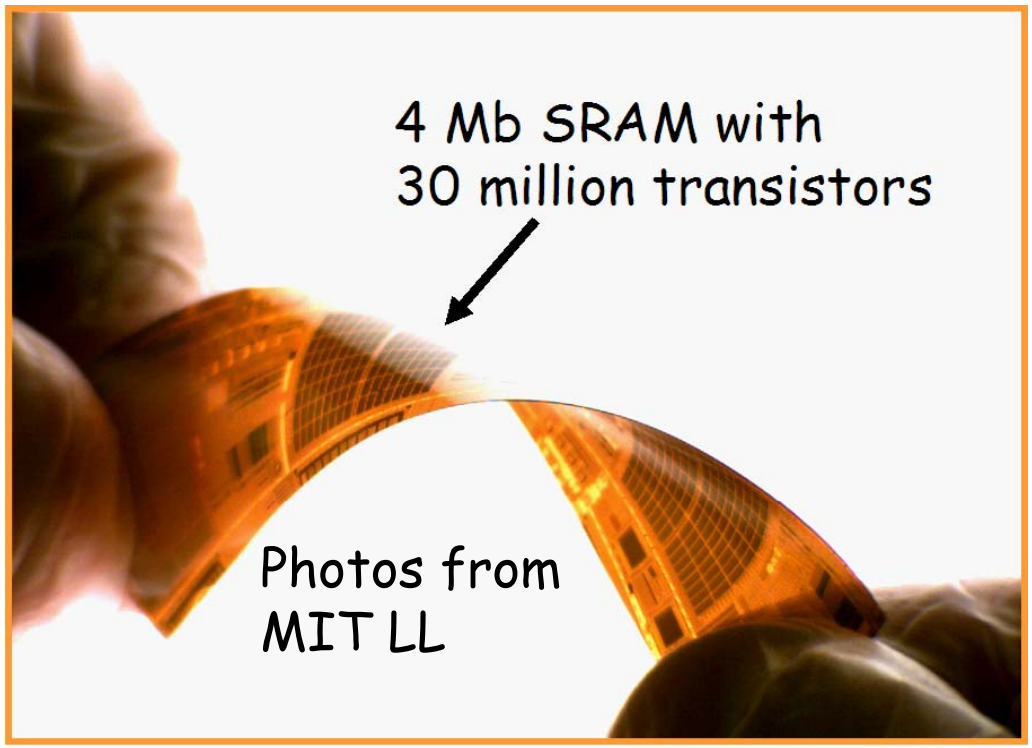
©Ray Yarema

Key Technologies

2) Wafer thinning

Through wafer vias typically have an 8 to 1 aspect ratio. In order to keep the area associated with the via as small as possible, the wafers should be thinned as much as possible. Thinning is typically done by a combination of grinding, lapping, and chemical or plasma etching.





Six inch wafer thinned to 6 microns and mounted to 3 mil kapton.

Key Technologies

3) Via formation and metalization

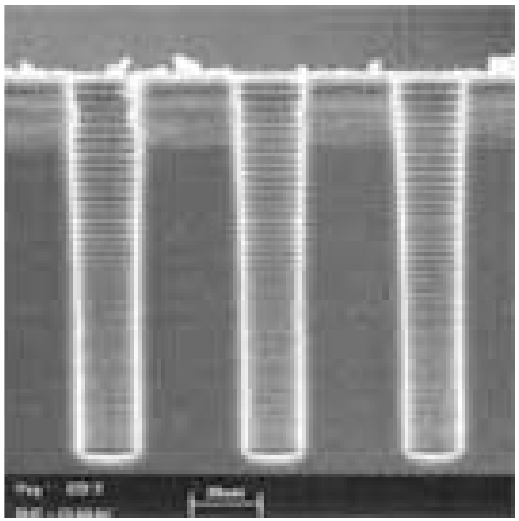
Two different proceedures are generally used:

Via First - vias holes and via metalization take place on a wafer before wafer bonding.

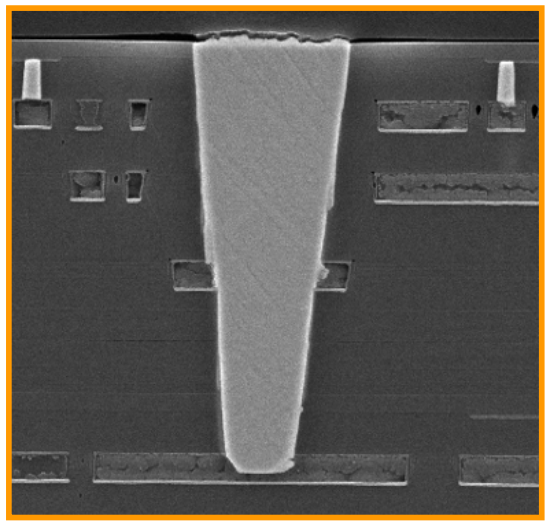
Via Last - vias holes and via metalization take place on a wafer after wafer bonding.

Vias in CMOS are formed using the Bosch process and must be passivated before filling with metal while Vias in SOI are formed using an oxide etch are filled without passivation.

SEM of 3 vias using Bosch process[8]



Via using oxide etch process (Lincoln Labs)



Typical diameters are 1-2 microns

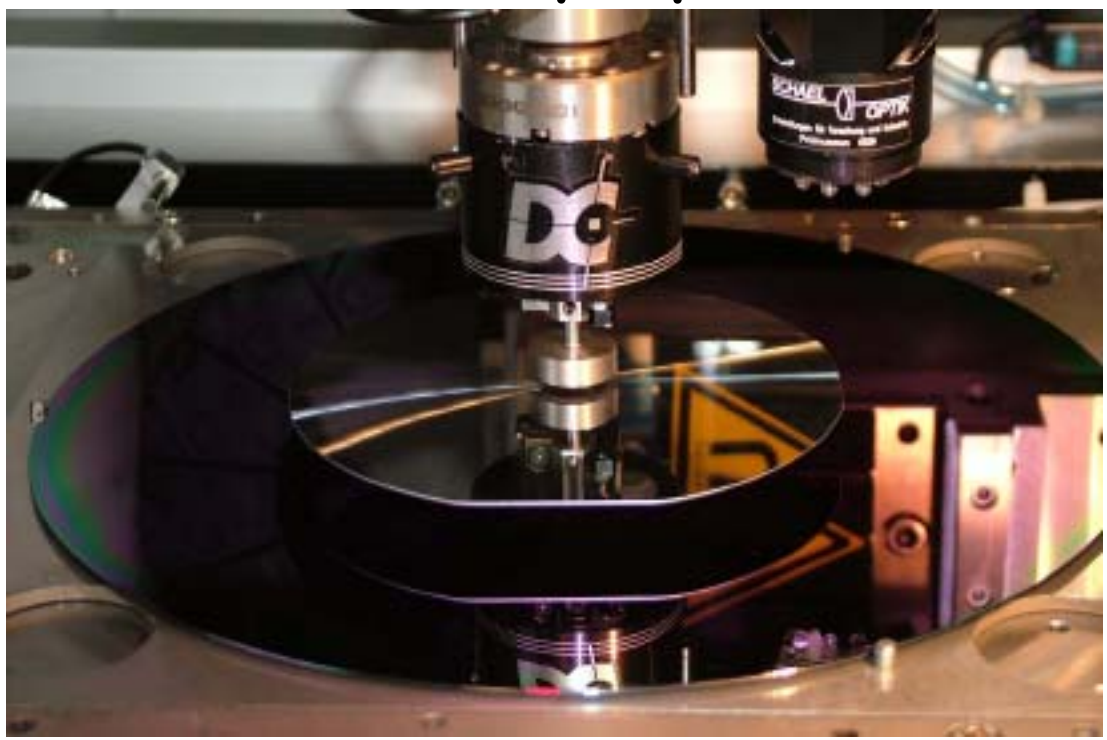
©Ray Yarema

Key Technologies

4) High Precision Alignment

Alignment for both die to wafer and wafer to wafer bonding is typically better than one micron. (Photos by Ziptronix.)

Die to Wafer alignment and placement

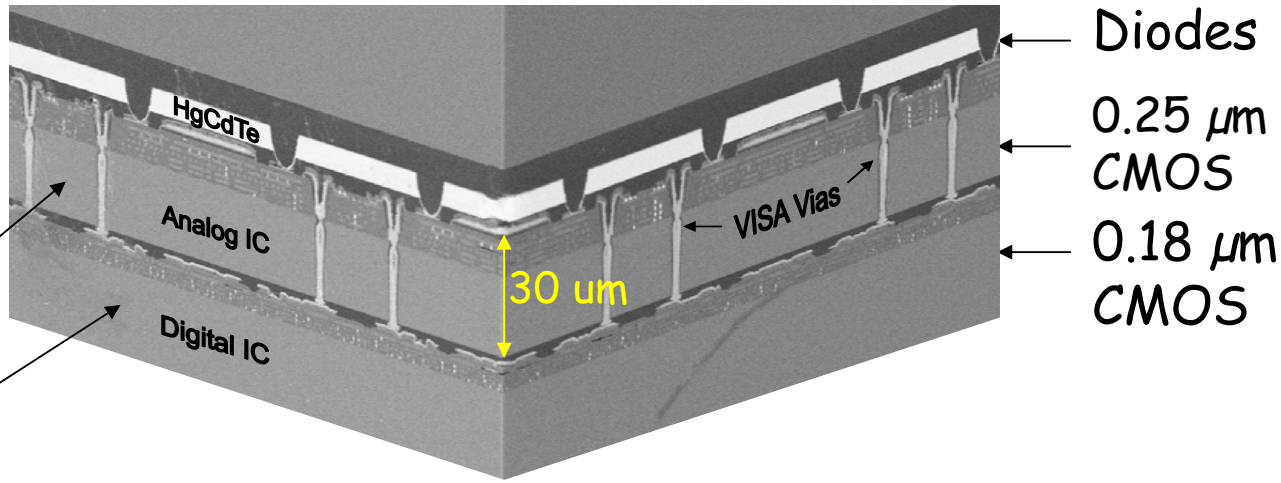


Wafer to Wafer alignment and placement

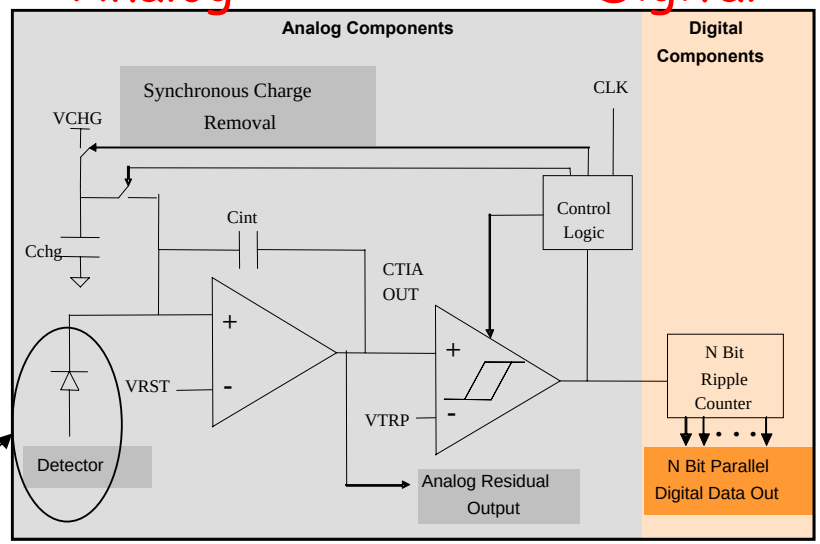
©Ray Yarema

Example1: RTI 3D Infrared Focal Plane Array

- 256 x 256 array with 30 µm pixels
- 3 Tiers
  - HgCdTe (sensor)
  - 0.25 µm CMOS (analog)
  - 0.18 µm CMOS (digital)
- Die to wafer stacking
- Polymer adhesive bonding
- Bosch process vias (4 µm) with insulated side walls
- 99.98% good pixels
- High diode fill factor



Array cross section

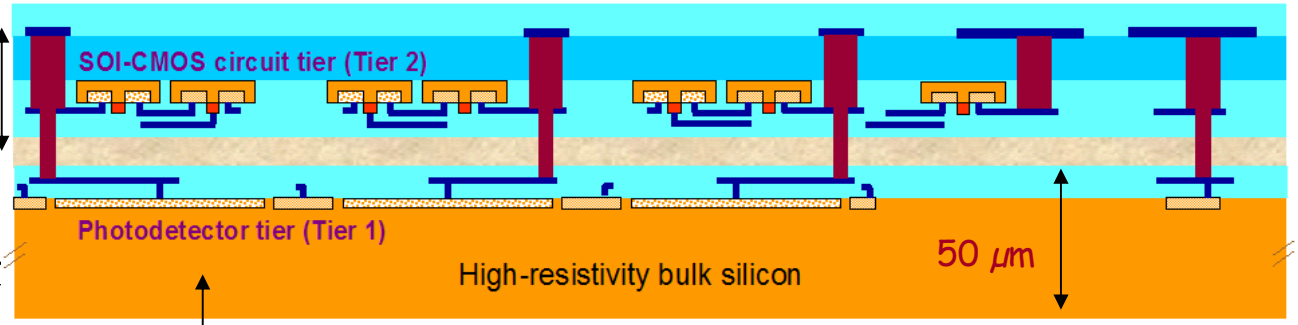


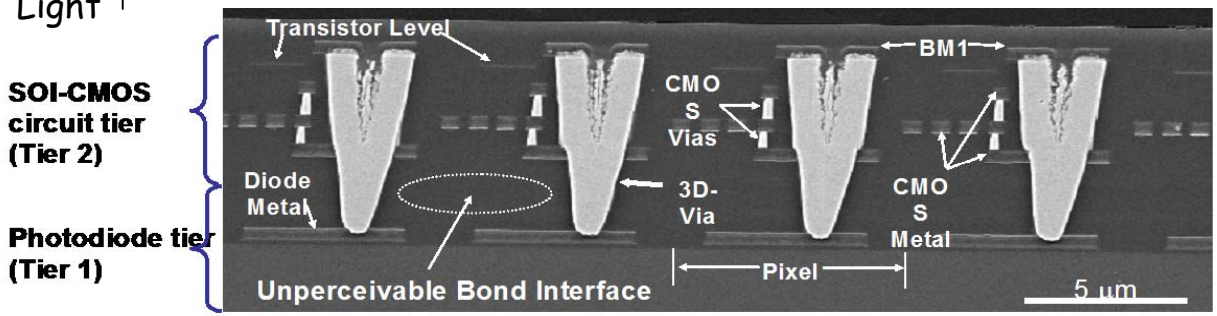
3 Tier circuit diagram

Infrared image

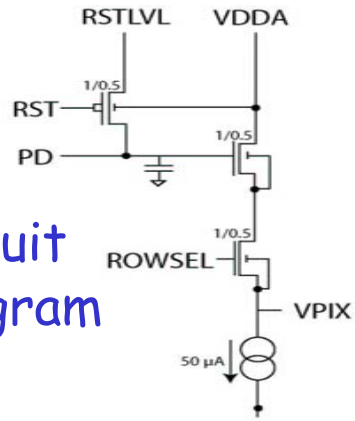
Example2: MIT LL3D Megapixel CMOS Image Sensor

- 1024 x 1024, 8 µm pixels
- 2 tiers
- Wafer to wafer stacking (150 mm to 150 mm)
- 100% diode fill factor
- Tier 1 - p+n diodes in >3000 ohm-cm, n-type sub, 50 µm thick
- Tier 2 – 0.35 um SOI CMOS, 7 µm thick
- 2 µm square vias, dry etch, Ti/TiN liner with W plugs
- Oxide-oxide bonding
- 1 million 3D vias
- Pixel operability >99.999%
- 4 side abuttable array





Drawing and SEM Cross section



Circuit Diagram

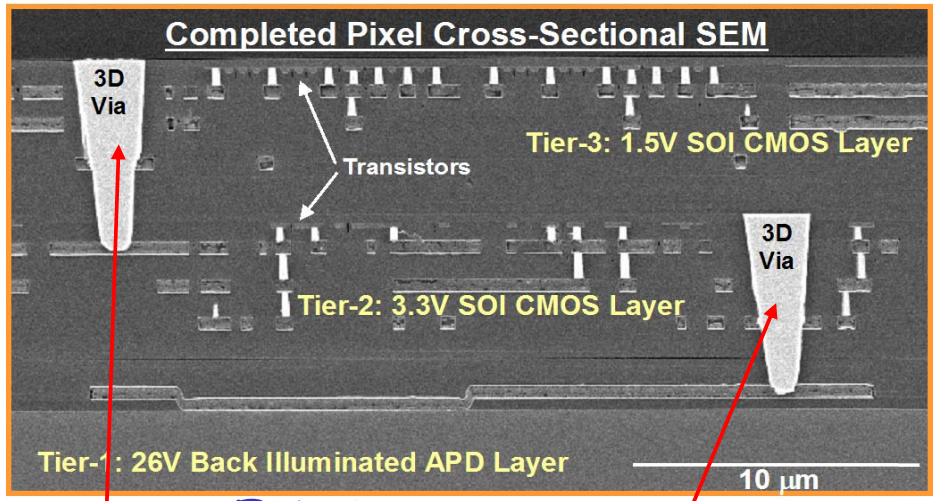
Image

©Ray Yarema

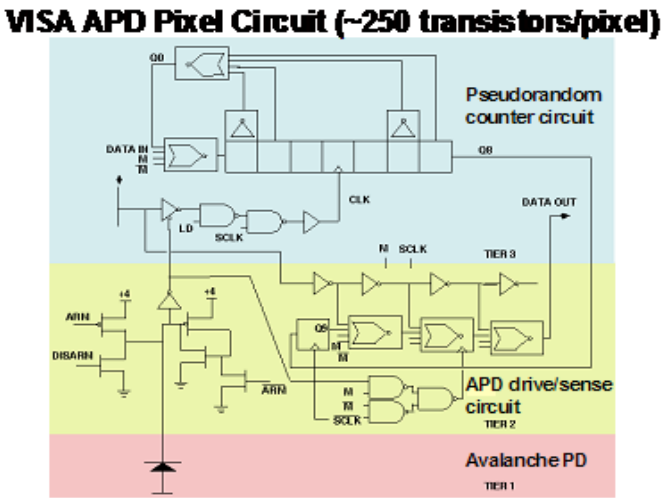
Example3: MIT LL 3D Laser Radar Imager

64 x 64 array, 30 μm pixels
3 tiers
- 0.18μm SOI
- 0.35 μm SOI
- High resistivity substrate diodes

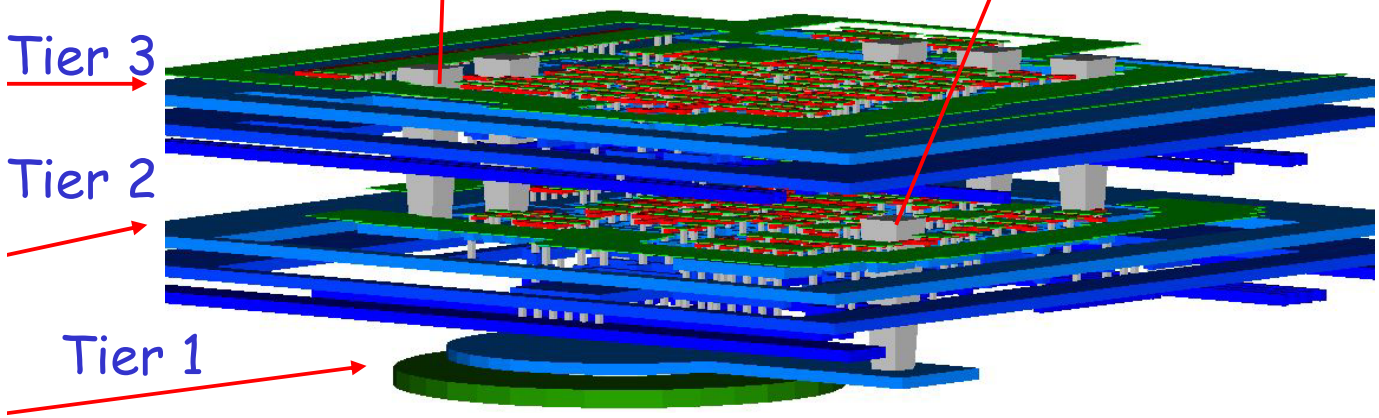
Oxide to oxide wafer bonding
1.5 μm vias, dry etch
Six 3D vias per pixel



SEM Cross section



Schematic



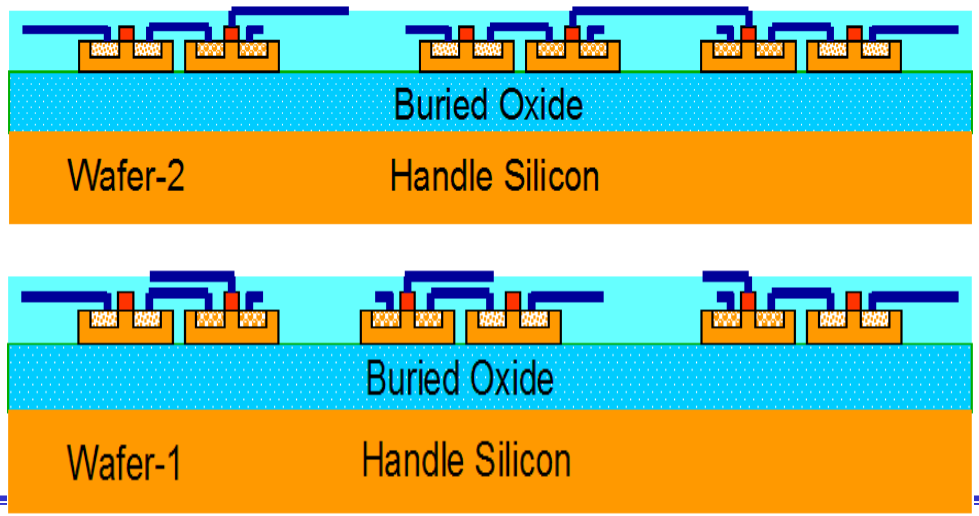
CAD Drawing

Wojciech.Dulinski@ires.in2p3.fr

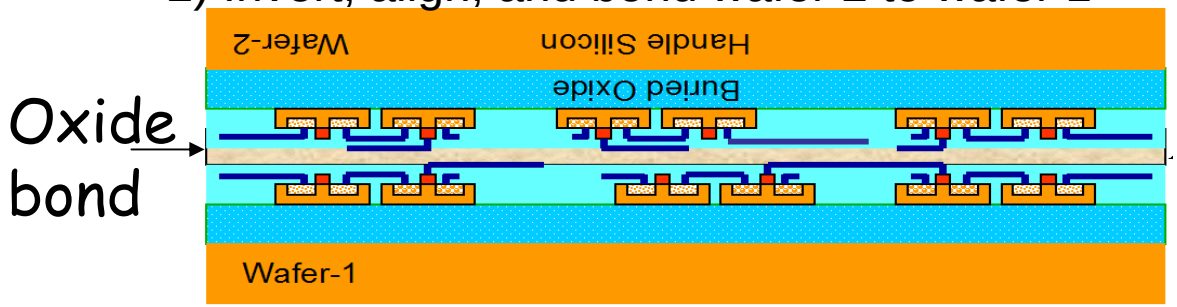
Process Flow for MIT LL 3D Chip

- 3 tier chip (tier 1 may be CMOS)
  - 0.18 um (all layers)
  - SOI simplifies via formation
- Single vendor processing

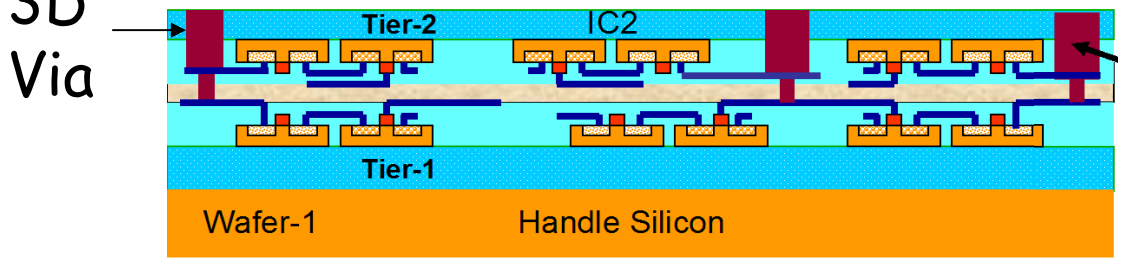
1) Fabricate individual tiers



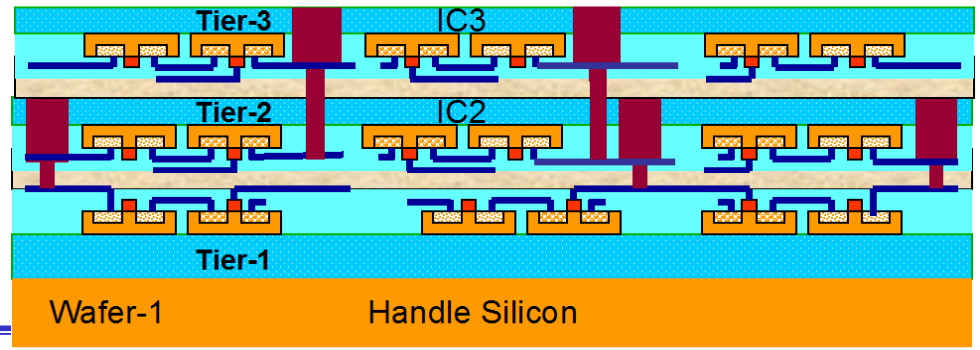
2) Invert, align, and bond wafer 2 to wafer 1



3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



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Who is Working on 3D ICs?

USA:
Albany Nanocenter
U. Of Kansas,
U of Arkansas
Lincoln Labs, AT&T
MIT,RPI, RTI, TI
IBM, Intel, Irvine Sensors
Micron, Sandia Labs
Tessera, Tezzaron,
Vertical Circuits, Ziptronix

Asia:
ASET, NEC, University of Tokyo,
Tohoku University, CREST,
Fujitsu, ZyCube, Sanyo,
Toshiba, Denso, Mitsubishi, Sharp,
Hitachi, Matsushita, Samsung

Europe: Fraunhofer IZM, IMEC Delft,
Infineon, Phillips, Thales, Alcatel Espace,
NMRC, CEA-LETI, EPFL, TU Berlin

Conclusions

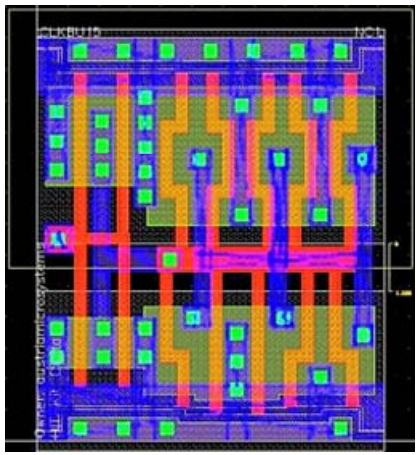
ILC is still not approved, but in order to satisfy all requirements for the Vertex Detector there, we must:

- **Continue to study and use newly available VLSI fabrication processes, but follow industry "mainstreams"**
- **Start to use new "packaging" technologies**
- **Increase flexibility using "post-processing" or "pre-processing" steps**
- **Limit the power dissipation!**
- **Have a new CAD tools for simulation!**
-
- **There is a physical limit coming from the data flow, even if front-end circuitry can be replaced by power efficient elements (for example based on avalanche diodes, like SiPMs ???)**

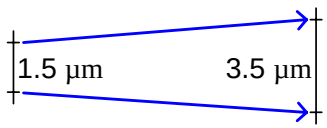
Appendix
How to modify standard library cells (AMS-0.35) in order to decrease ionization induced Single Event Latch up (SEL), using minimum effort approach

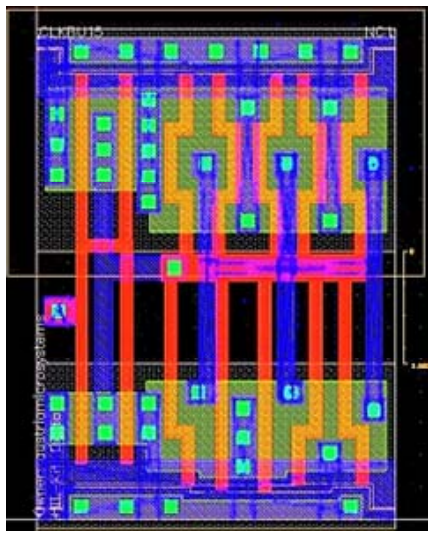
Differences between registers

- STD & 3B – AMS standard cells
- 2µ & 5µ stretched registers – distance between complementary transistors was increased:



Standard cell





2u Stretched cell

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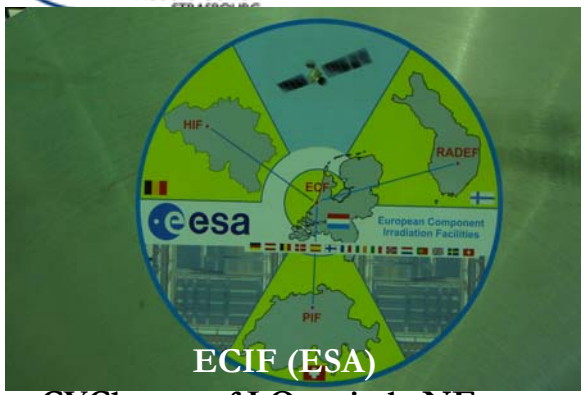
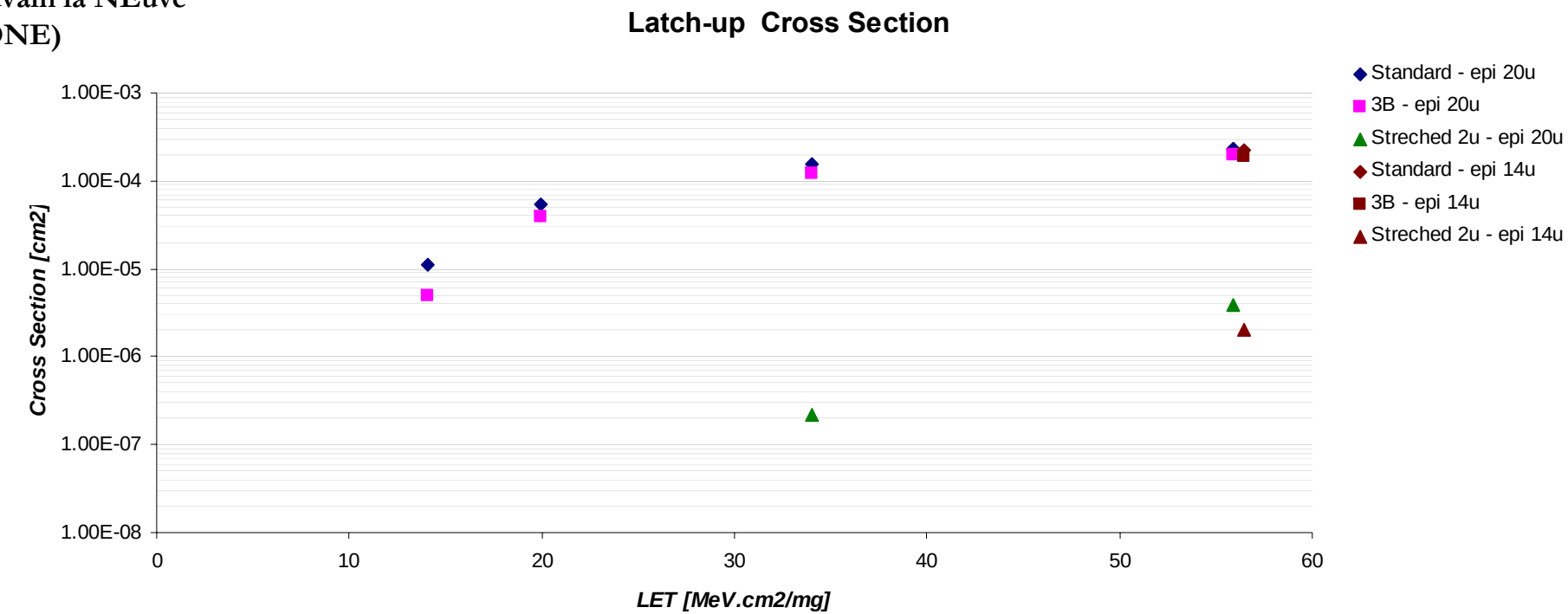
SEL tests results of modified cells (D flip-flops, buffers, I/O pads)



ECIF (ESA)
CYClotron of LOuvain la NEuve (CYCLONE)



- for 2u stretched cells latch-up hardness is 2 orders of magnitude better
- for 5u we didn't observe any events