Latches SEU en techno IBM 130nm pour SLHC/ATLAS

CPPM, Université de la méditerranée, CNRS/IN2P3, Marseille, France

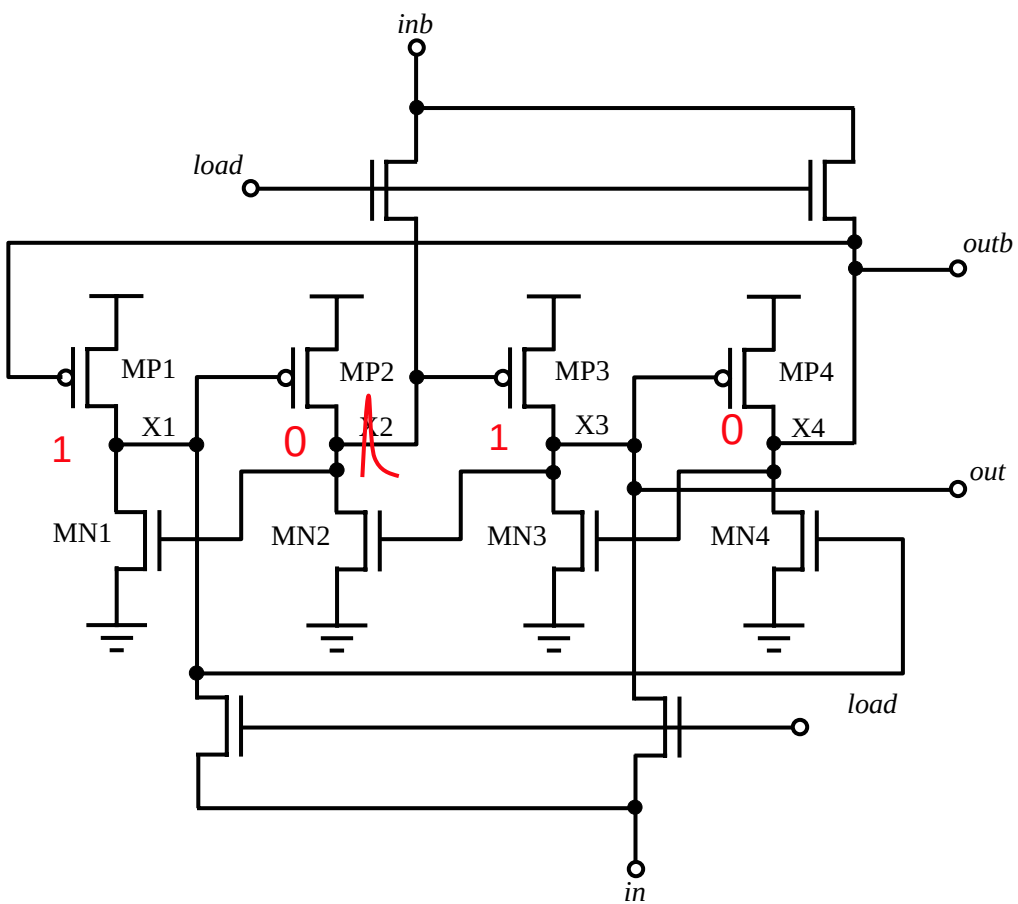
Outline

- Introduction
- Description of the DICE latch
- Different implemented layouts for the DICE latch
  - Measurement and comparison of implemented latches
- Proposed implementation for the pixel configuration block
- Conclusion

Introduction

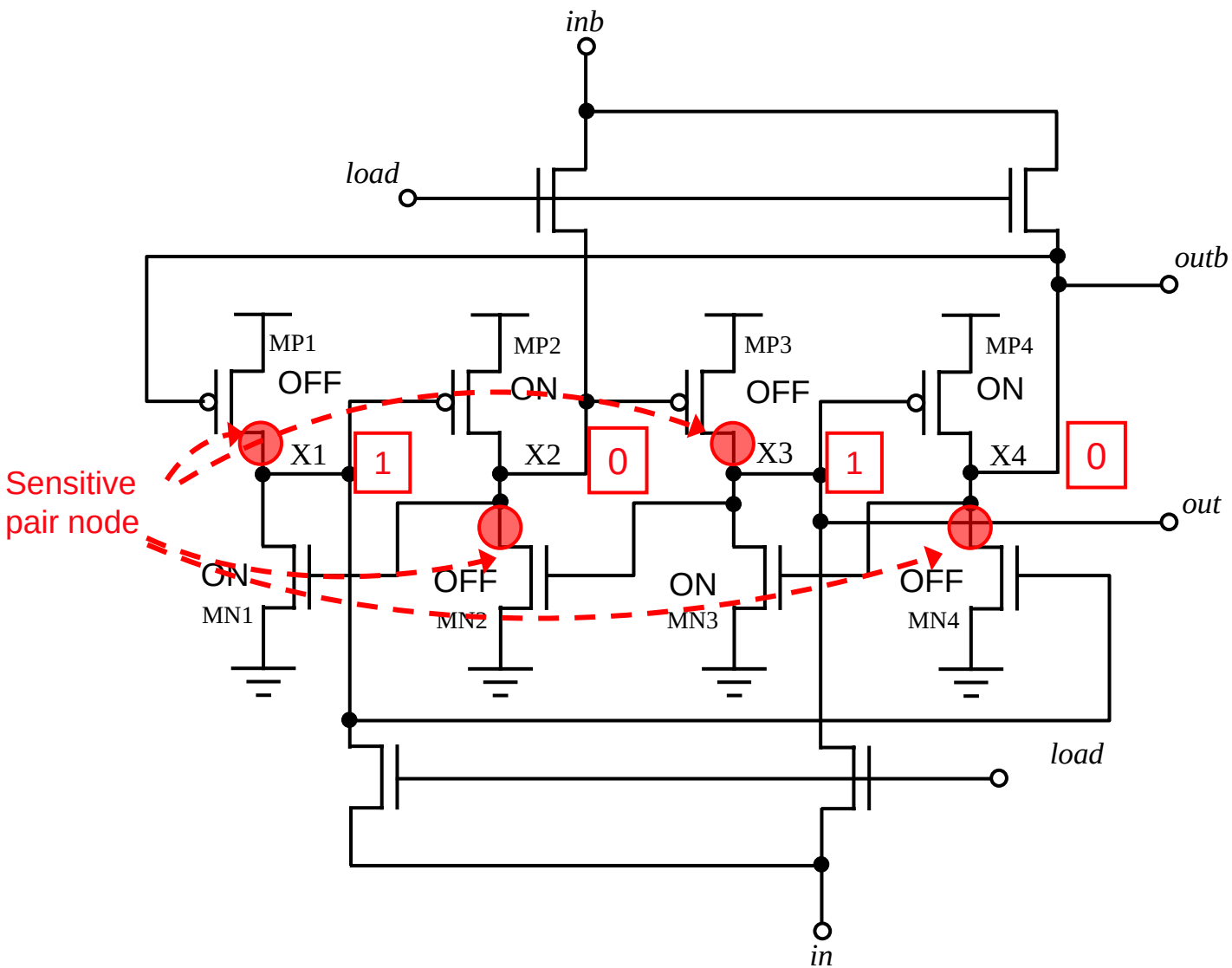
- hardened by design (HBD) approaches are used to reduce the effect of single bit upsets.
- Dual Interlocked Cell (DICE) latches have redundant storage nodes “dual node” and theoretically restores the original state when an upset occurs in one node.
- The upset may appear if the charge collected in two nodes exceed the critical value
- test circuits using the130 nm CMOS process designed in order to study the effect of layout techniques on the tolerance of the DICE latch to single event upsets.
- Irradiation tests were carried out using IRRAD3 beam line of the Proton Synchrotron (PS) facility at CERN. The test beam provides a beam of 24 GeV protons
- Proposed structure for :
  - Pixel configuration block
  - Global configuration block

Dice Latch description



- The DICE latch is based on the conventional cross coupled inverter latch structure
- If we assume a positive upset pulse on the node X2
  - MP3 is blocked (ON -> OFF) avoiding the propagation of this perturbation to the node X3
    - For a single node, the critical charge is very high (~1 pC)
  - If 2 sensitive nodes of the cell storing the same logic state (X1-X3) or (X2-X4) are corrupted due to the effect of a single particle impact, the immunity is lost and the Dice latch is upset.
    - The critical charge becomes low (~40 fC) when a charge from upset is collected by a sensitive node pair

Sensitive areas



- For out =1
  - X1=X3=1 and X2=X4=0
  - Sensitive area corresponds to the OFF transistor drain area
- Sensitive area has to be minimized
- Spatial separation for the drain of MN1-MN3, MN2-MN4
- Contacted guard ring and nwell separation for pmos MP1-MP3, MP2-MP4

Test Set up

Control room

irradiation area

LabWindows software

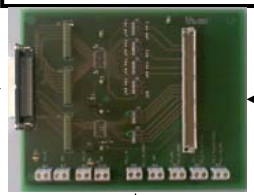
PCIMCIA
acquisition board

Serial link

A

Current supply control

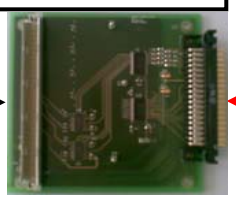
TTL -LVDS

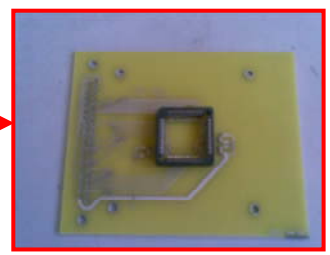


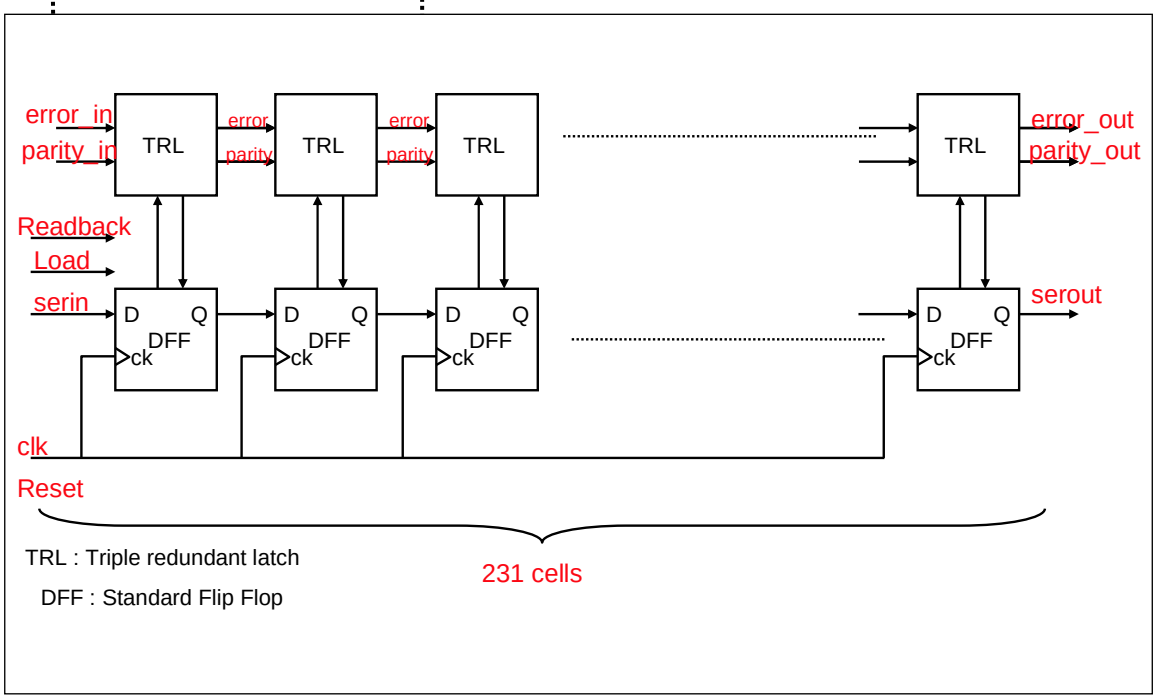
LVDS signals

~20 meters

LVDS-TTL

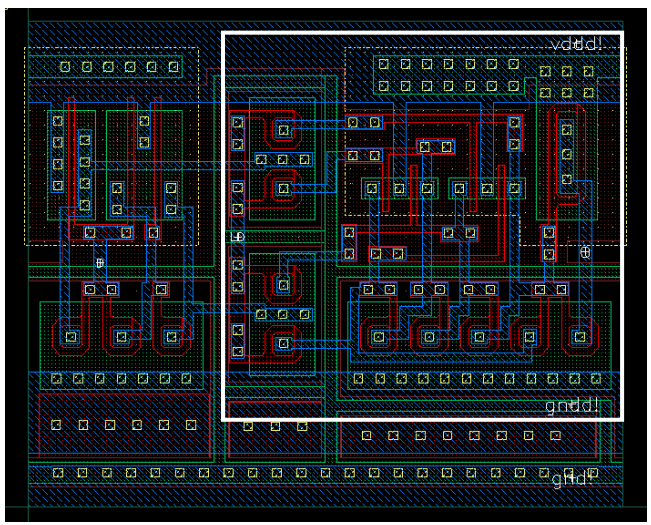






Layouts implemented in the chip SEU1

FEI3_DICE latch (latch 1)

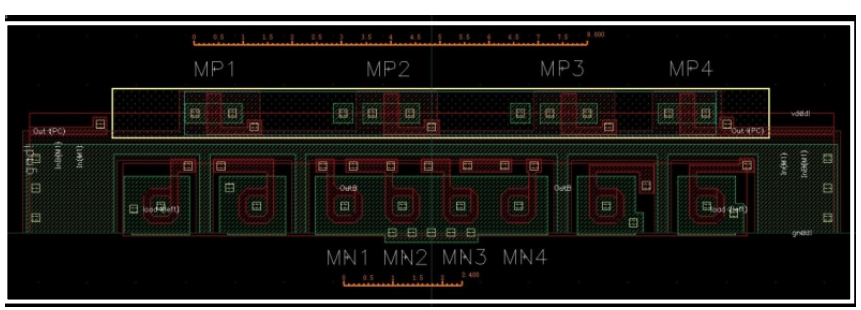


Latch Area = 54 µm²

Latch type	area	1->0 Cross section (cm²/bit)
Latch 1	54 µm²	$3.2\ 10^{-15}$
Latch 5	48 µm²	$0.96\ 10^{-16}$

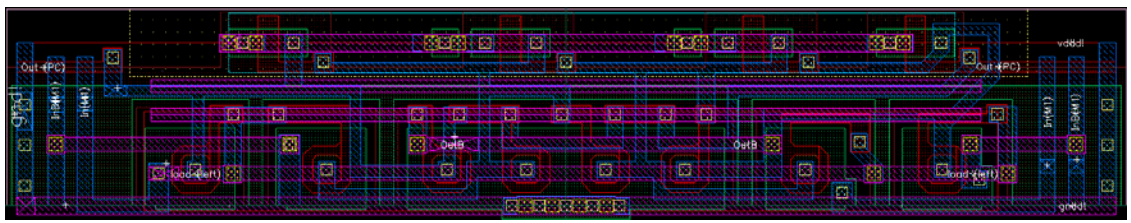
Measurements made in 2007 for the chip SEU1

Improved DICE latch (latch 5)



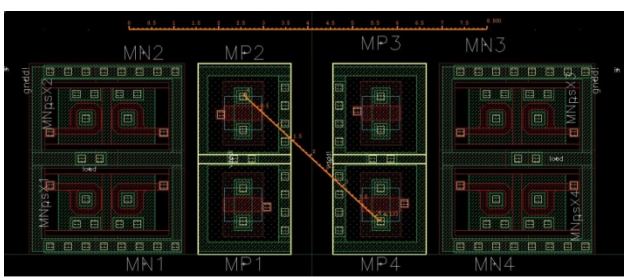
Latch Area = 48 µm²

Layouts implemented in the chip SEU2



- Different layout versions were implemented in the SEU2 chip
  - Same schematic but different layout

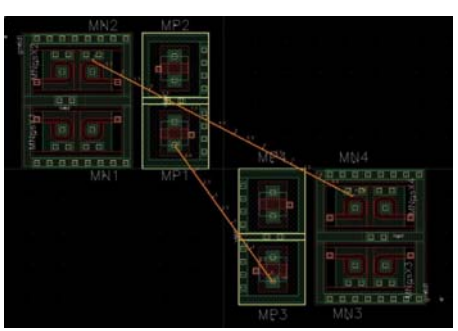
Latch 5: pmos in same nwell, enclosed and separated nmos with guard ring (pmos separation: 8µm, nmos separation: 2.4µm)



Latch 5.2: pmos in isolated nwell, enclosed nmos with guard ring (pmos separation: 4µm, nmos separation: 8µm)

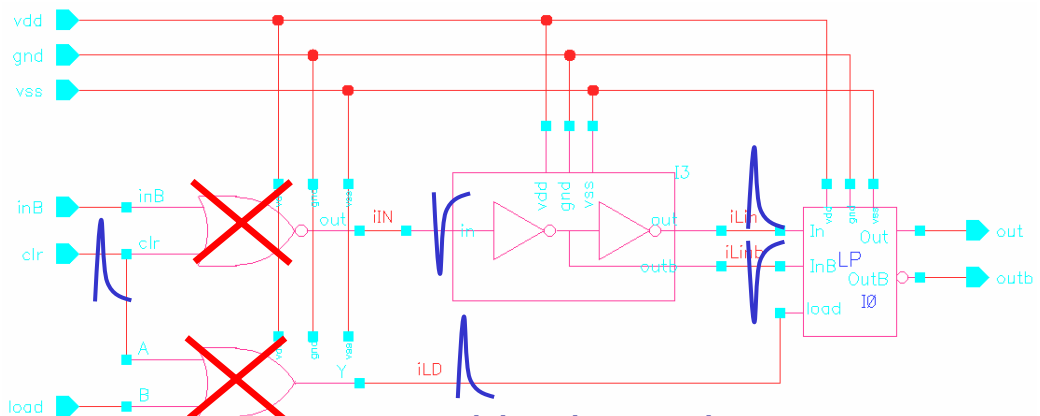
Latch type	area	Cross section cm²/bit		
		1->0	0->1	1->0 and 0->1
Latch 5	48 µm²	$(1.5 \pm 0.1).10^{-15}$	$(2.2 \pm 0.3).10^{-16}$	$(5.9 \pm 0.5).10^{-16}$
Latch 5.2	48 µm²	$(3.4 \pm 0.6).10^{-16}$	$(4.2 \pm 0.4).10^{-16}$	$(3.6 \pm 0.5).10^{-16}$
Latch 5.3	48 µm²	$(3.0 \pm 0.6).10^{-16}$	$(3.3 \pm 0.3)10^{-16}$	$(2.4 \pm 0.5).10^{-16}$

Measurements made in 2008 for the chip SEU2

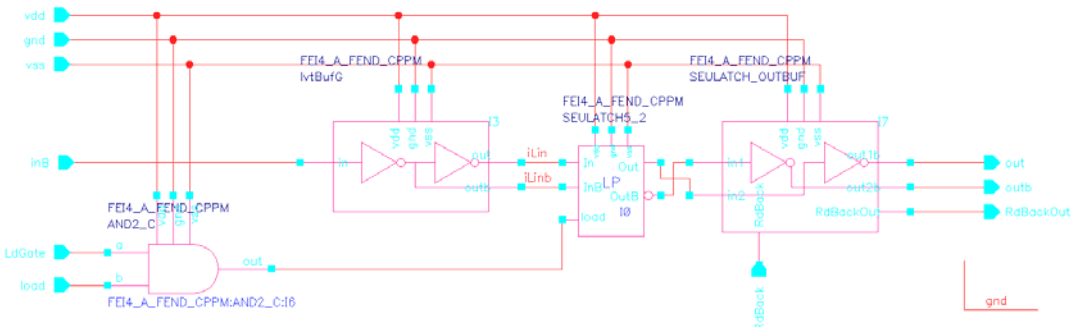


Latch 5.3: same structure like latch 5.2 with interleaved layout
Pmos separation: 5.4µm, nmos separation: 9µm)

« SEULATCH_wGate » schematic

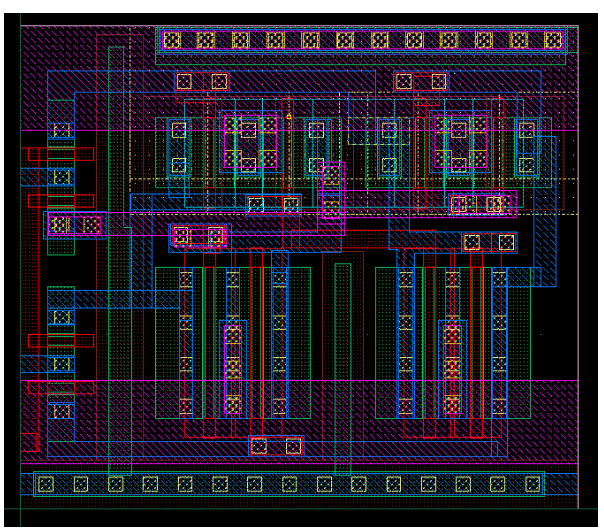


Old schematic



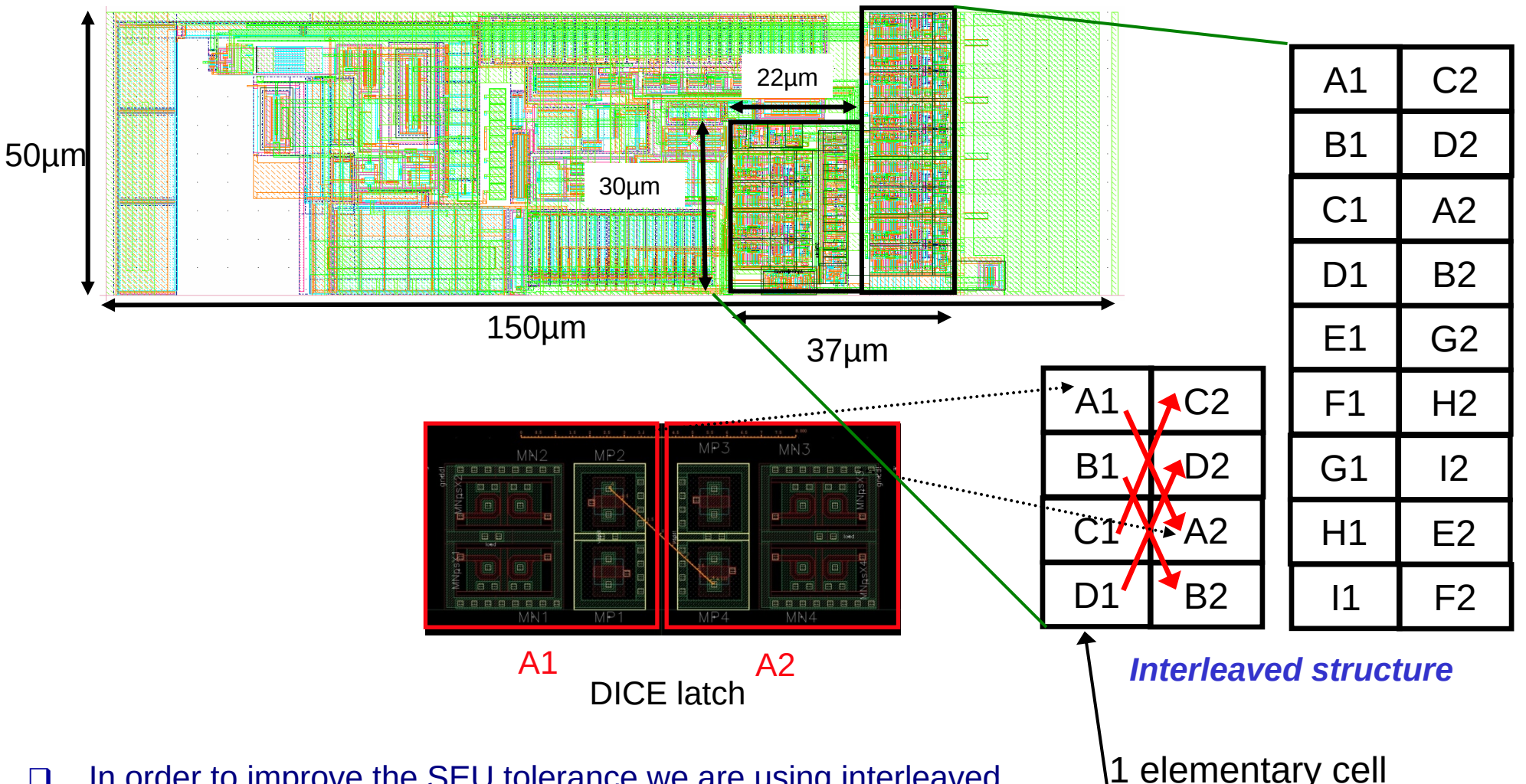
New schematic

- A modified schematic is proposed :
  - Remove the « latchclear » signal
  - We add a readback option for all latches to improve tests
- The latch clear operation can be done by loading 00…00 pattern



FEI4-Proto DICE latch 36µm²

proposed layout “Configbloc_wGate”



- In order to improve the SEU tolerance we are using interleaved layout for each latch in the pixel configuration block

Future

- Finalize proposal layout in FEI4-P2 for several columns
  - Fit SEU tolerant latch in the pixel dedicated area
    - Finalize interconnections to realize an interleaved structure
  - Fit SEU tolerant latch for global configuration block
    - Using triple redundant latch
- Prepare future radiations tests:
  - work with a higher frequency (40MHz)