Design of High Dynamic Range DAC

Outline

- Choice of the DAC architecture.
- Design and test results of a 12 bit DAC. **(MEMS)**
- Design and test results of a 14 bit DAC. **(ILC Si-W Ecal)**
- Summary of the DACs main features.

DAC architecture

Switched Capacitors Array & Dynamic Element Matching

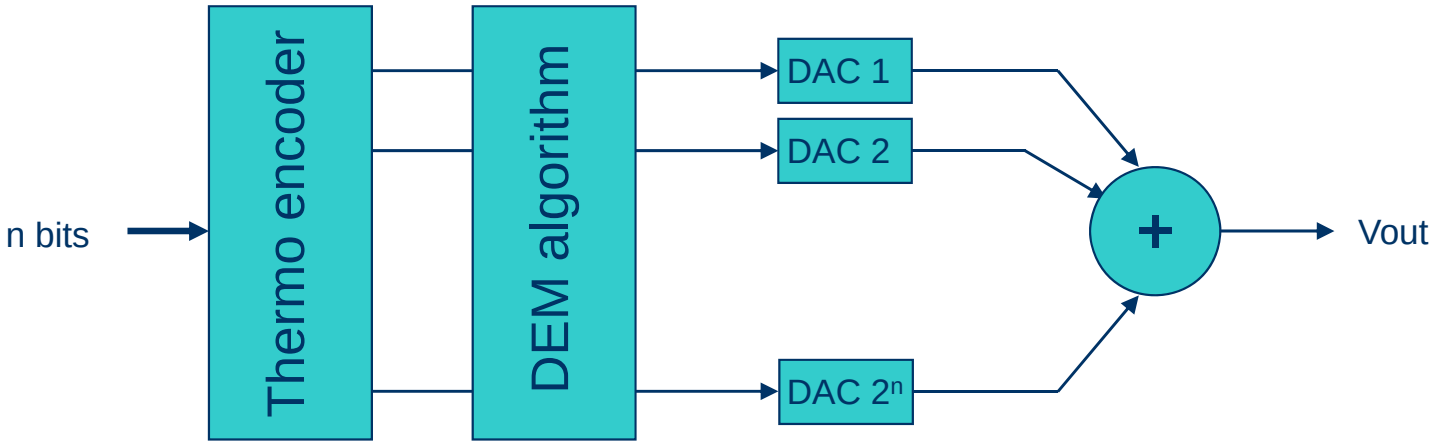
- Power consumption constraint => **switched capacitors** architecture.
- The linearity will be limited by the **matching errors** of the capacitors.
- => Linearization methods have to be used.
- The **Dynamic Element Matching** (DEM) is commonly used in **high resolution multi bit Sigma-Delta converters.**
- The DEM **turns harmonic distortion into noise**, this noise is then reduced by the converter's low pass filter.

DAC architecture

Dynamic Element Matching : block diagram

The DEM algorithm has to be coupled to a **Thermometer DAC**.

Such n bit DAC uses 2^n equally weighted converters.



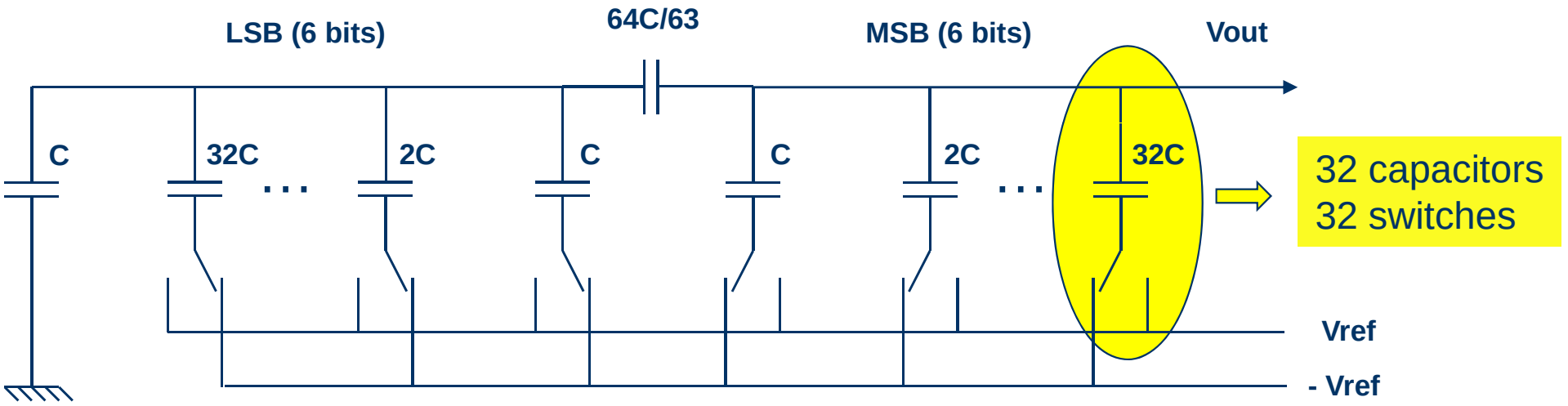
Without DEM : Input code = 3 => Vout = DAC1 + DAC2 + DAC3

With DEM : the selected 3 DACs are different for each conversion (scrambling)

The effects of the matching errors are spread over the whole dynamic range.

Design of a 12 bit, 5 Msps Digital to Analog Converter

Segmented array of switched capacitors



32 capacitors
32 switches

$$Vout = \frac{1}{64}\left(\frac{2l-63}{64} + 2m - 63\right)Vref$$

l = 6 bit LSB

m = 6 bit MSB

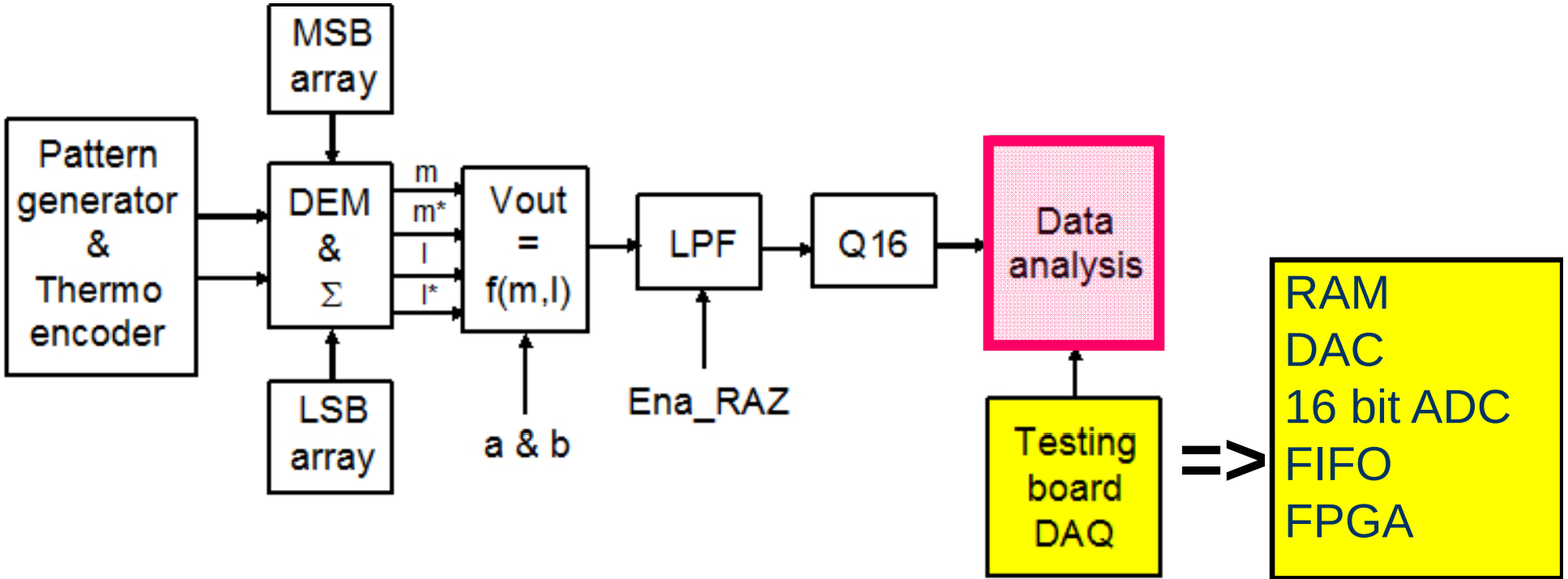
The DEM efficiency has to be evaluated for such a network

=> **high level simulation : fast and exhaustive evaluation.**

Design of a 12 bit, 5 Msps Digital to Analog Converter

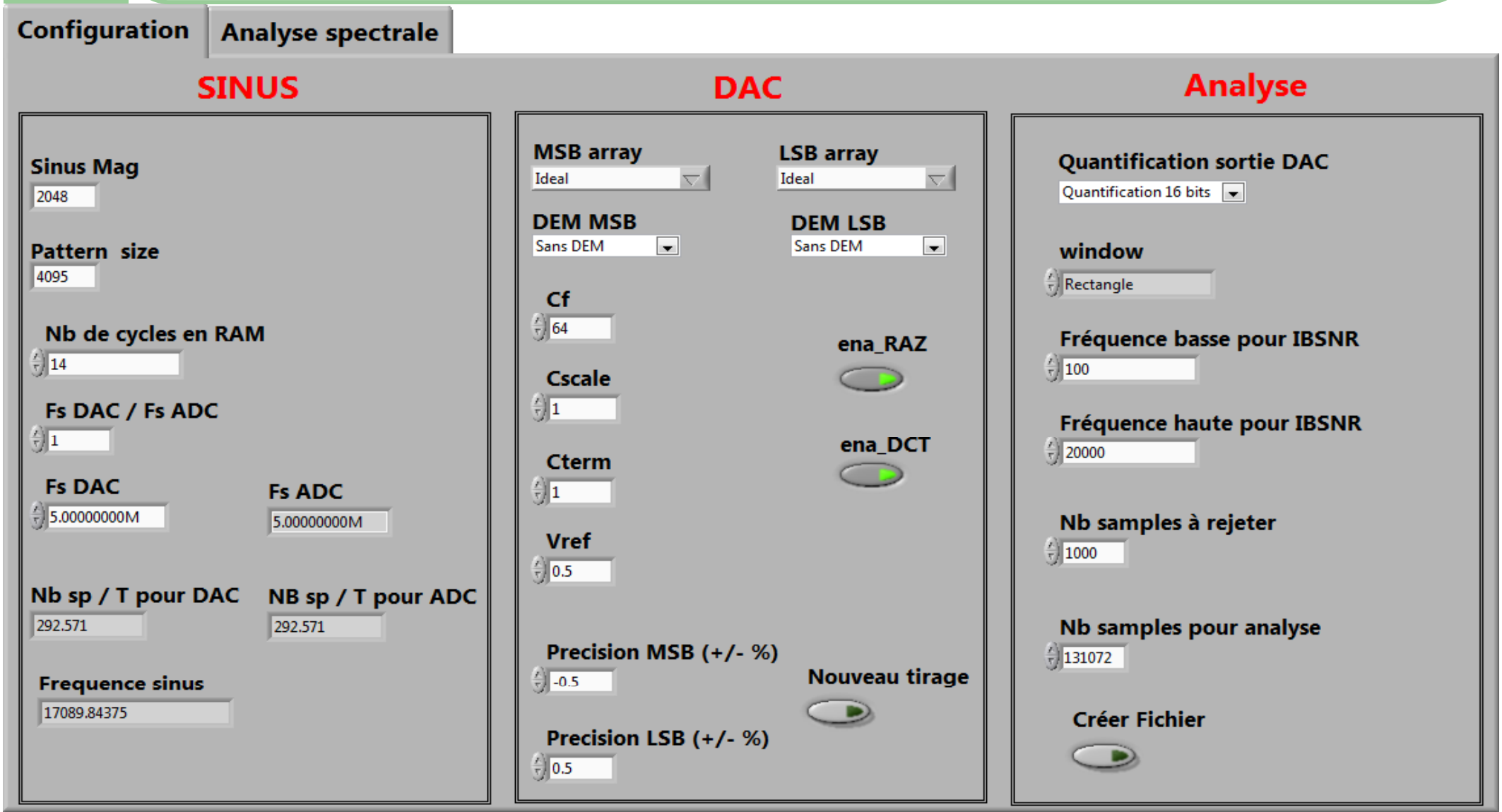
Simulation software

- **Labview** was used for the simulation and for the test bench control.
- Simulated and measured data are processed in the same way by the block labelled *Data Analysis*. This block computes the INL, DNL,THD, SNR, ...
  It also extracts the capacitors matching errors.



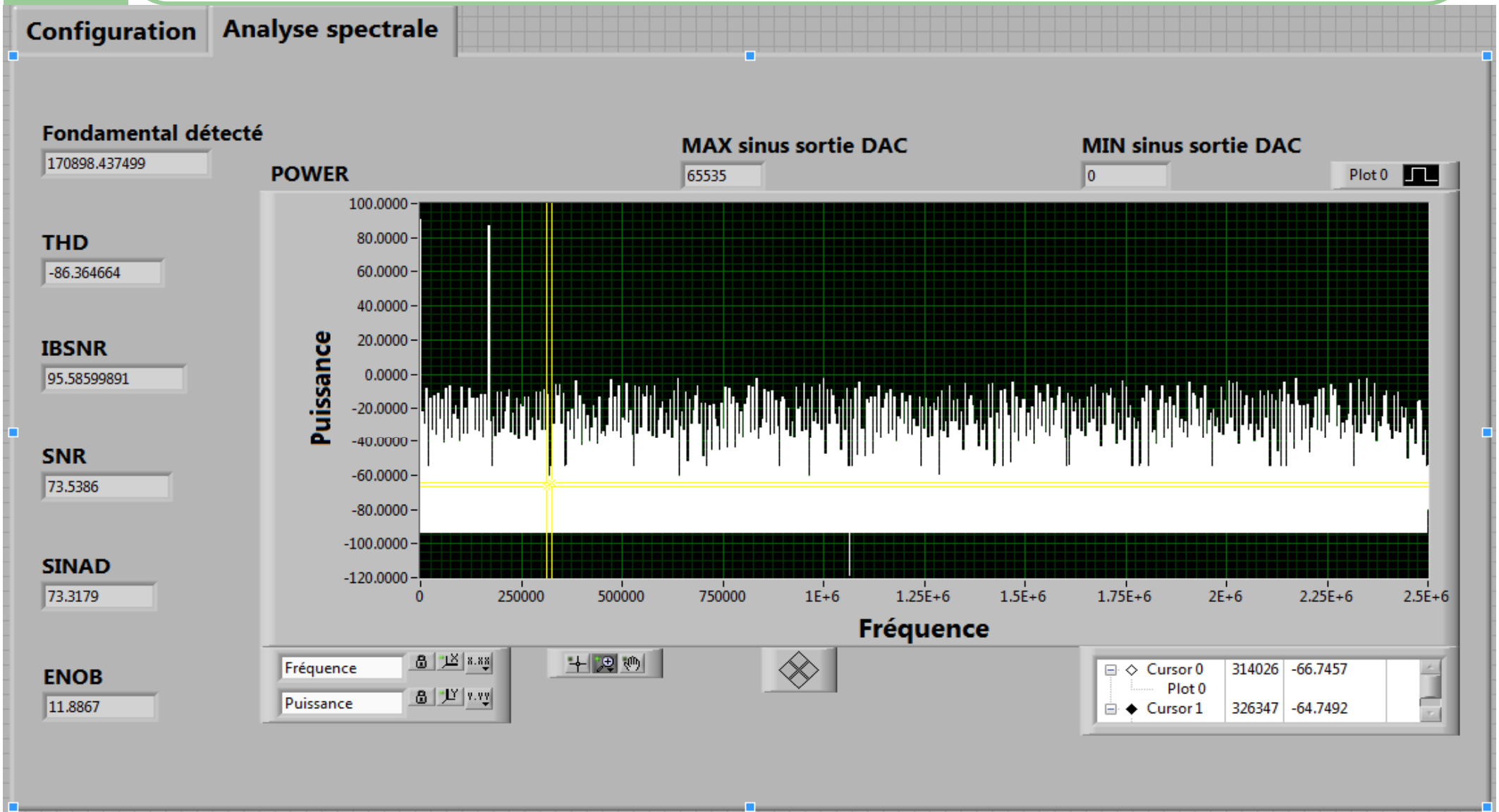
Design of a 12 bit, 5 Msps Digital to Analog Converter

Simulation software : spectral analysis



Design of a 12 bit, 5 Msps Digital to Analog Converter

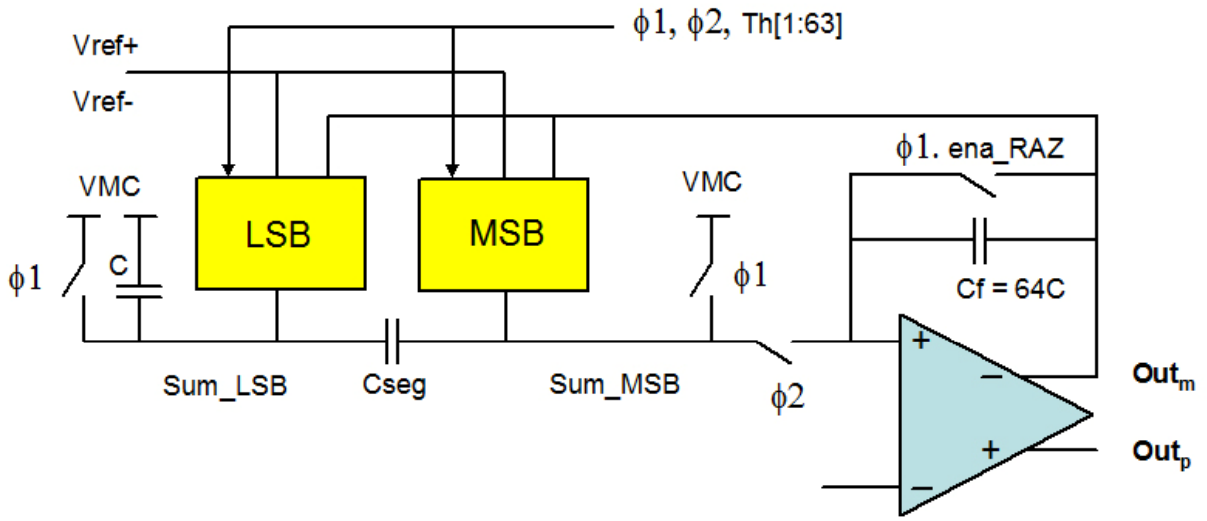
Simulation software : spectral analysis



Design of a 12 bit, 5 Msps Digital to Analog Converter

Differential implementation

- Inherits the OTA designed at LPSC for a pipeline ADC (Dzahini, Rarbi).
- Low sensitivity to parasitic capacitors (substrate coupling):
  - Sum_LSB : very low sensitivity on LSB side.
  - Sum_MSB : OTA 90dB open loop gain => $\Delta V=0$.
  - Parasitic capacitors in parallel with each C_i => matching errors : processed by the DEM algorithm.
- Sensitive component : **Cseg, must match the MSB array mean value**.



Design of a 12 bit, 5 Msps Digital to Analog Converter

Power consumption - Layout

Vdd = 3.3 V

DEM => 0.3 mW @ 5MHz

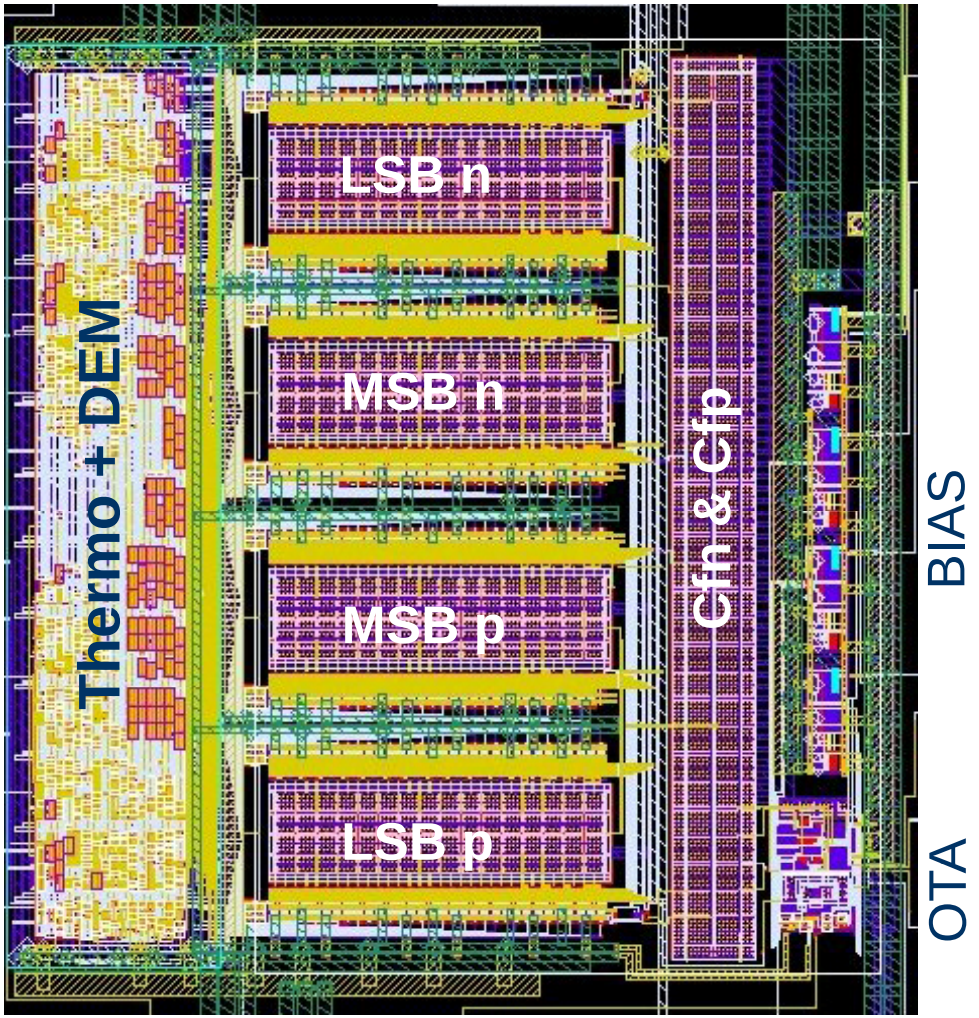
OTA => 2.2 mW

BIAS => 2.5 mW

DAC12 => 5 mW

Idle mode : < 1 µW

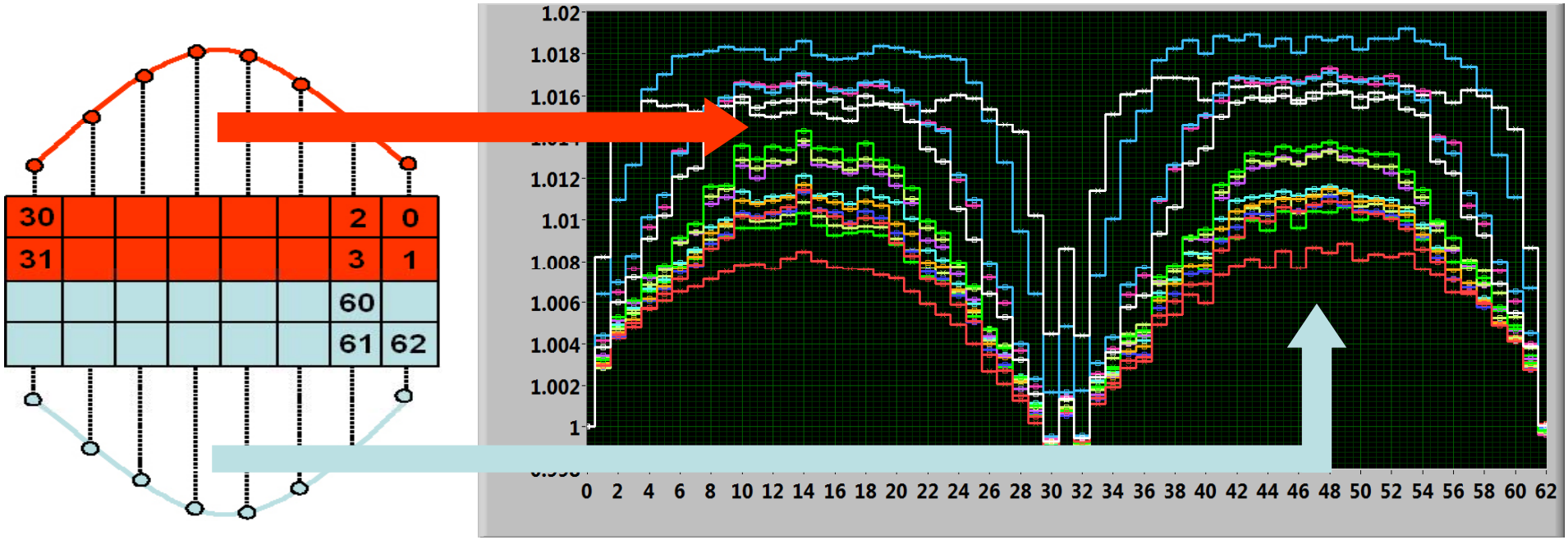
1300x1200 μm^2 = 1.6 mm^2



Design of a 12 bit, 5 Msps Digital to Analog Converter

Test results – Matching errors in a 63 capacitor array

- 15 chips tested
- **Systematic matching error : from 0.8% up to 1.8%**
- Gradient not constant over the array => effect not cancelled by a Common Centroid layout.

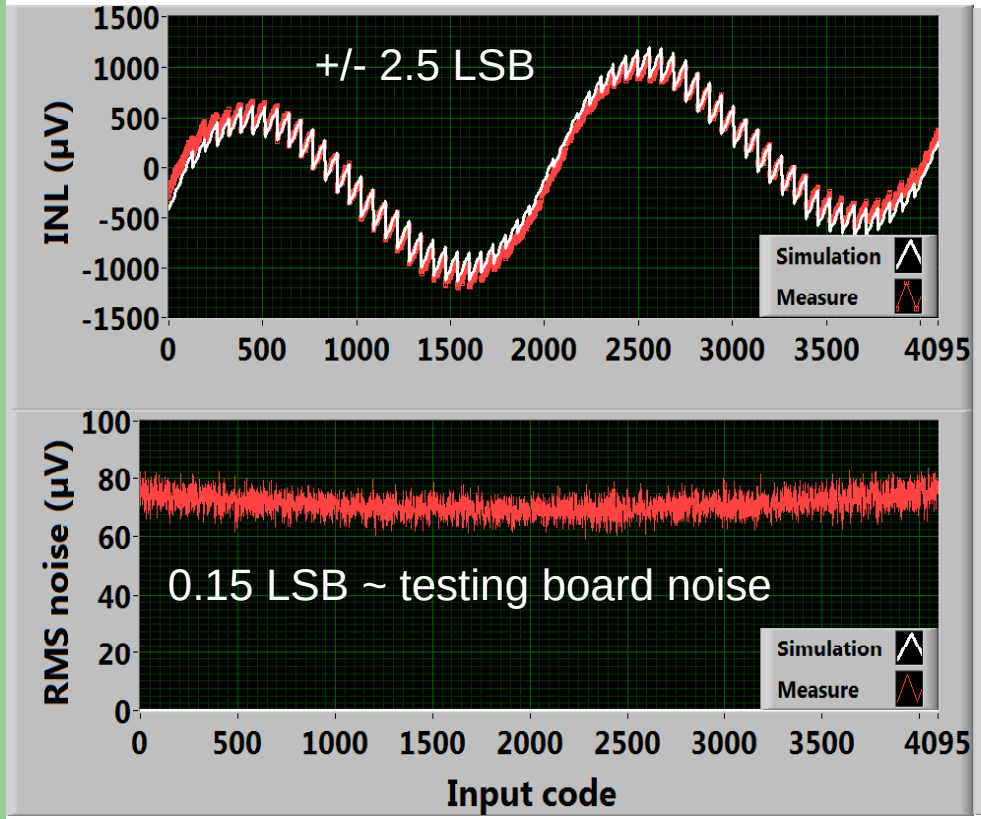


Design of a 12 bit, 5 Msps Digital to Analog Converter

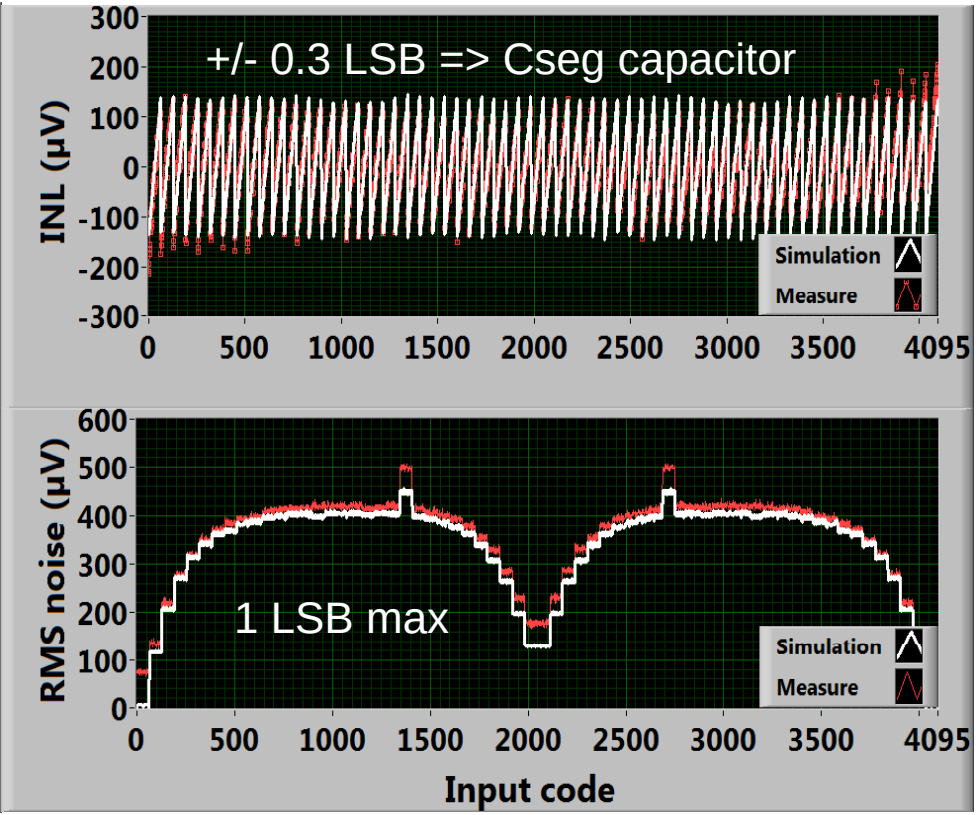
High level simulation versus test results - INL and RMS noise

The DEM improves the INL by a factor of 8 => 3 bits

Without DEM



With DEM



Design of a 12 bit, 5 Msps Digital to Analog Converter

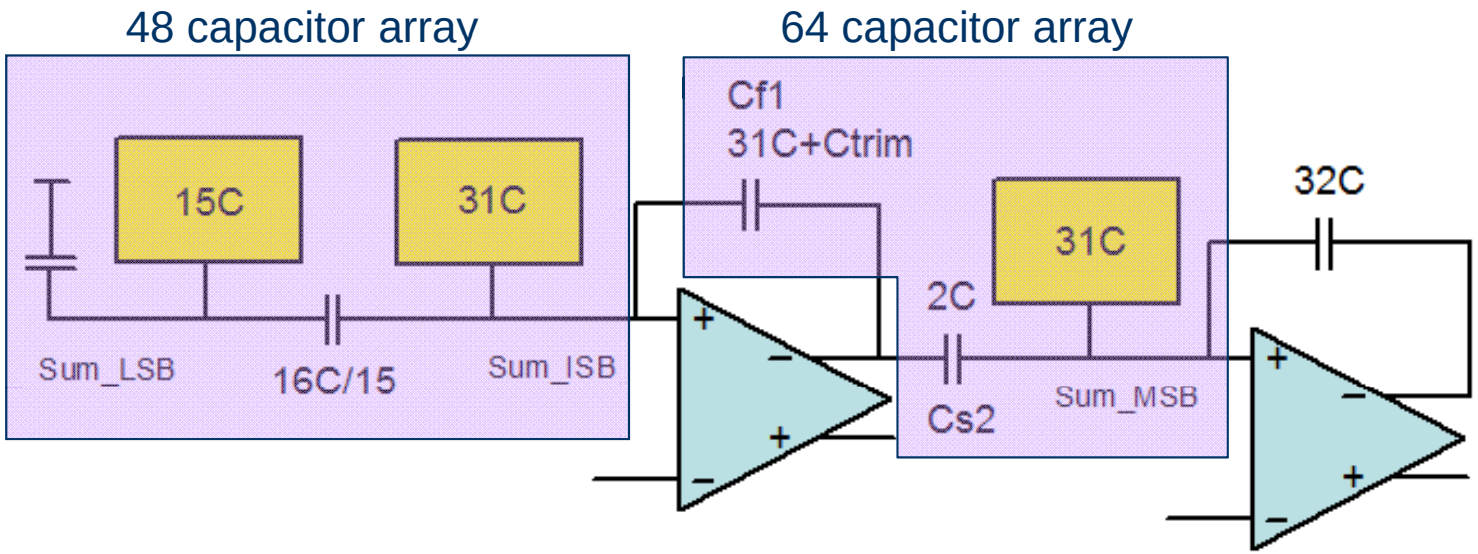
Conclusion for the 12 bit DAC

- The DAC **satisfies the constraints** of the MEMS sensor project. (Power consumption, Sampling rate, INL,THD, IBSNR).
- **The capacitors matching errors are larger than expected in a CMOS 0.35µ process.**
- **The DEM improves the INL by a factor of 8 (3 bits) and induces a 1 LSB RMS noise.** (**without external filter**)
- **Our high level simulation is a fast and reliable tool.**

Design of a 14 bit, 5 Msps Digital to Analog Converter

Block diagram

- Number of capacitors reduced compared to the 12 bit DAC (144/191).
- Very low sensitivity to parasitic capacitors (substrate coupling).
- Cf_1, Cs_2, MSB array mean value : matching has to be better than 0.3%.
- Cf_1 : trimming capability for this first 14 bit prototype (0.1C step).



Design of a 14 bit, 5 Msps Digital to Analog Converter

Power consumption - Layout

Vdd = 3.3 V

DEM => 0.2 mW @ 5MHz

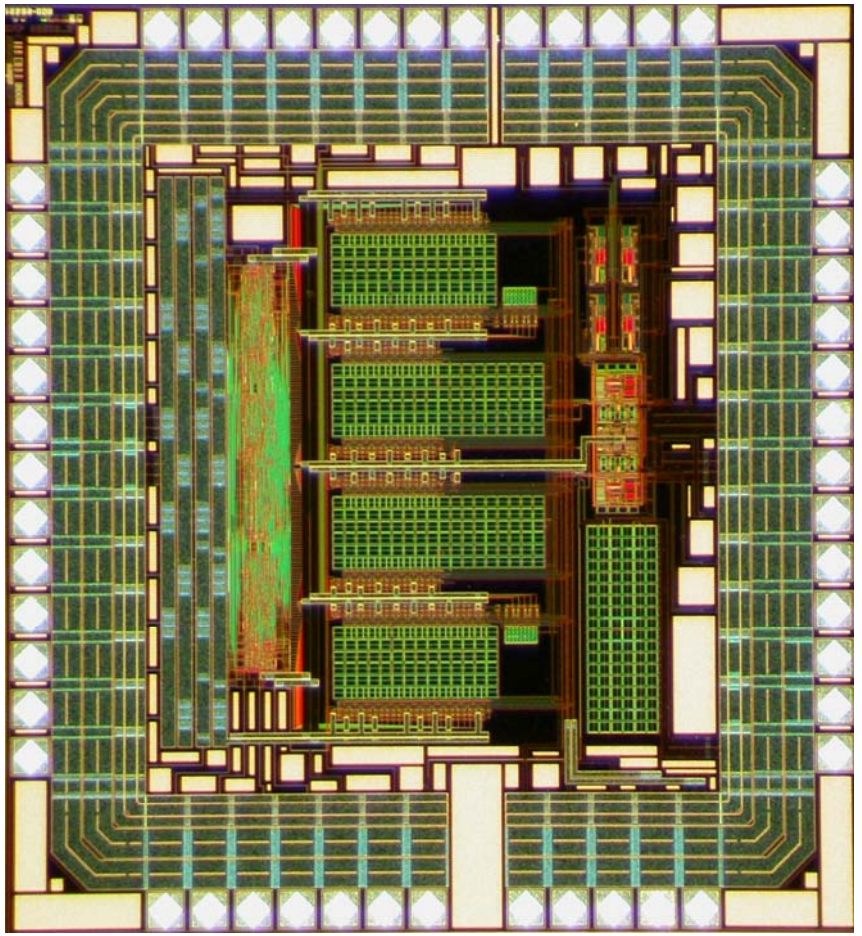
OTA => 2 x 2.2 mW

BIAS => 2.5 mW

DAC14 => 7.1 mW

Idle mode : < 1µW

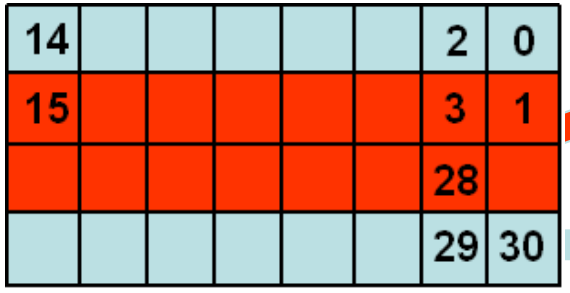
1300x1100 μm^2 = 1.4 mm^2

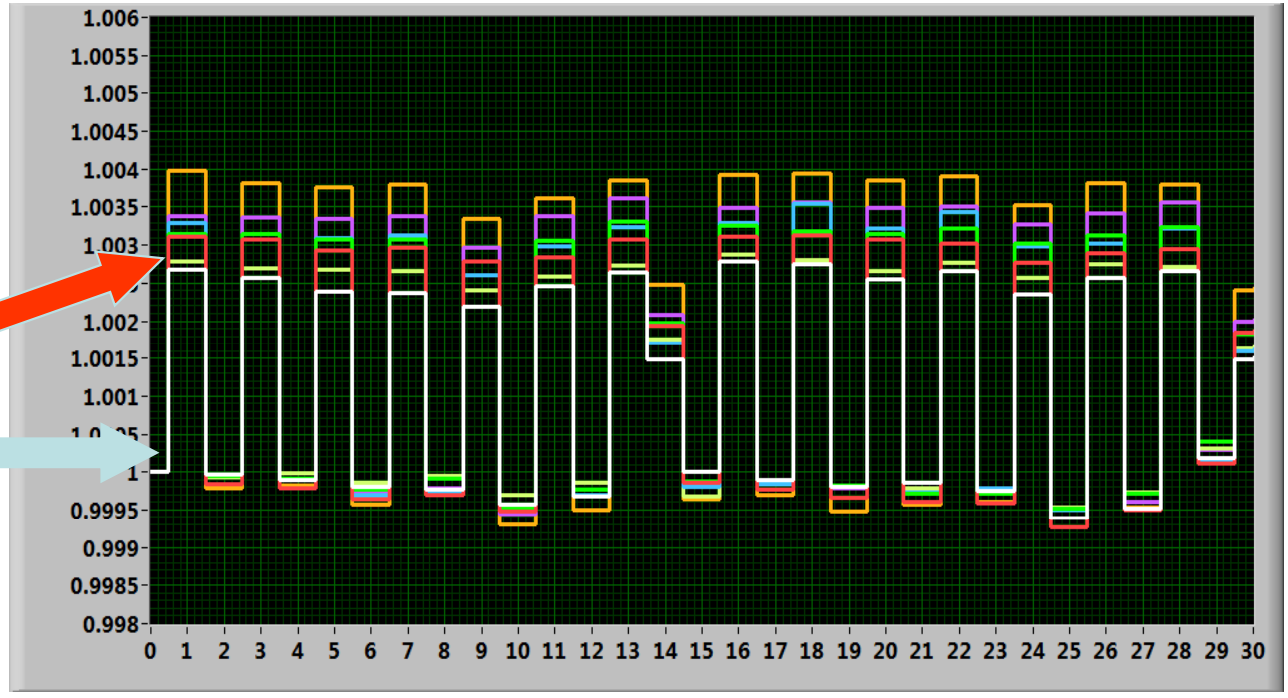


Design of a 14 bit, 5 Msps Digital to Analog Converter

Test results – Matching errors in a 31 capacitor array

- 9 chips successfully tested.
- Systematic matching error : from 0.25% to 0.4%
- Mismatch due to interconnections : < 0.1% (AV_extracted view).



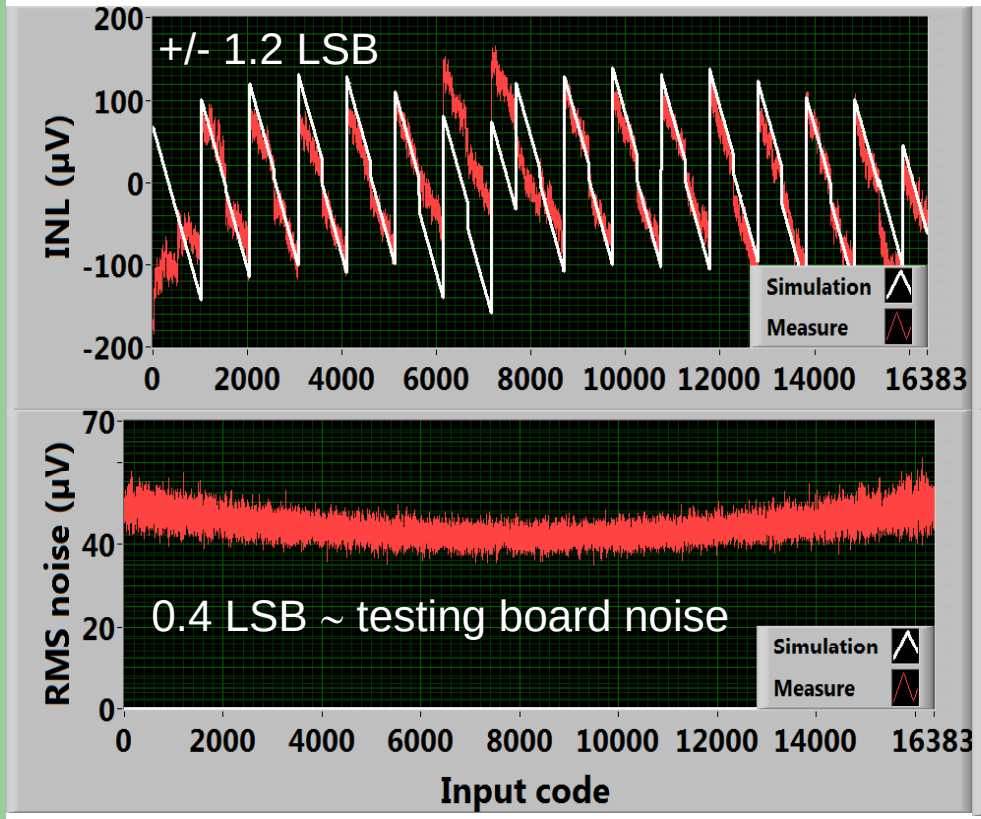


Design of a 14 bit, 5 Msps Digital to Analog Converter

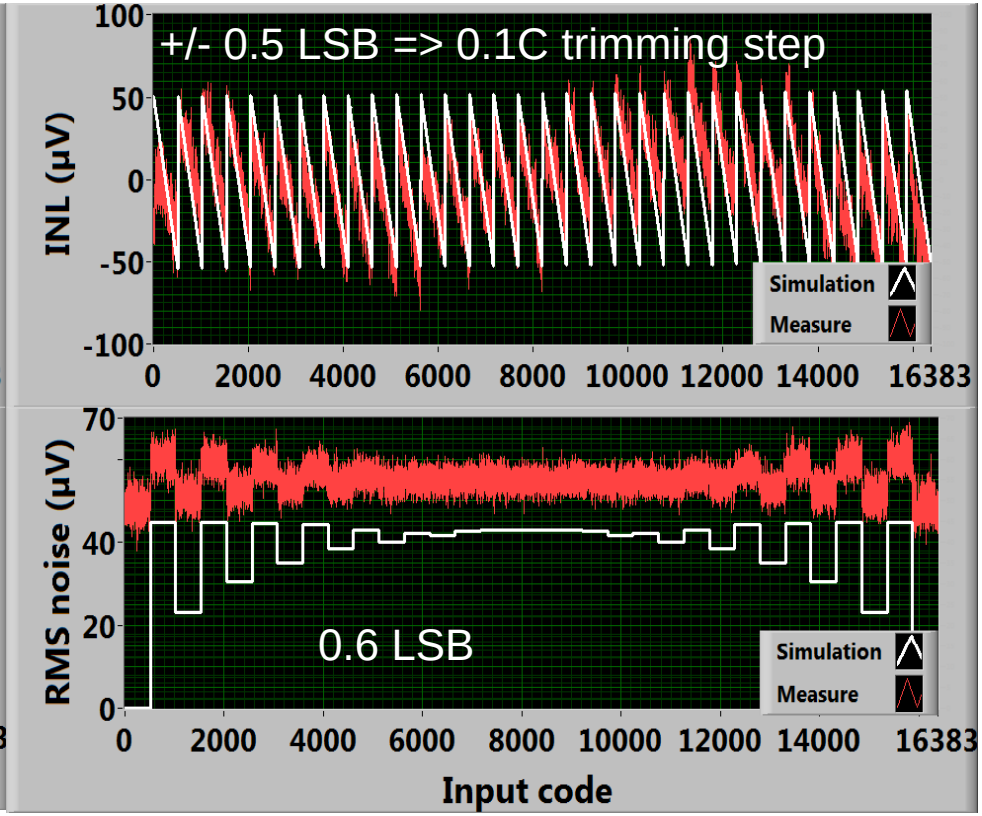
Test results – INL and RMS noise

The DEM improves the INL by a factor of 2

Without DEM

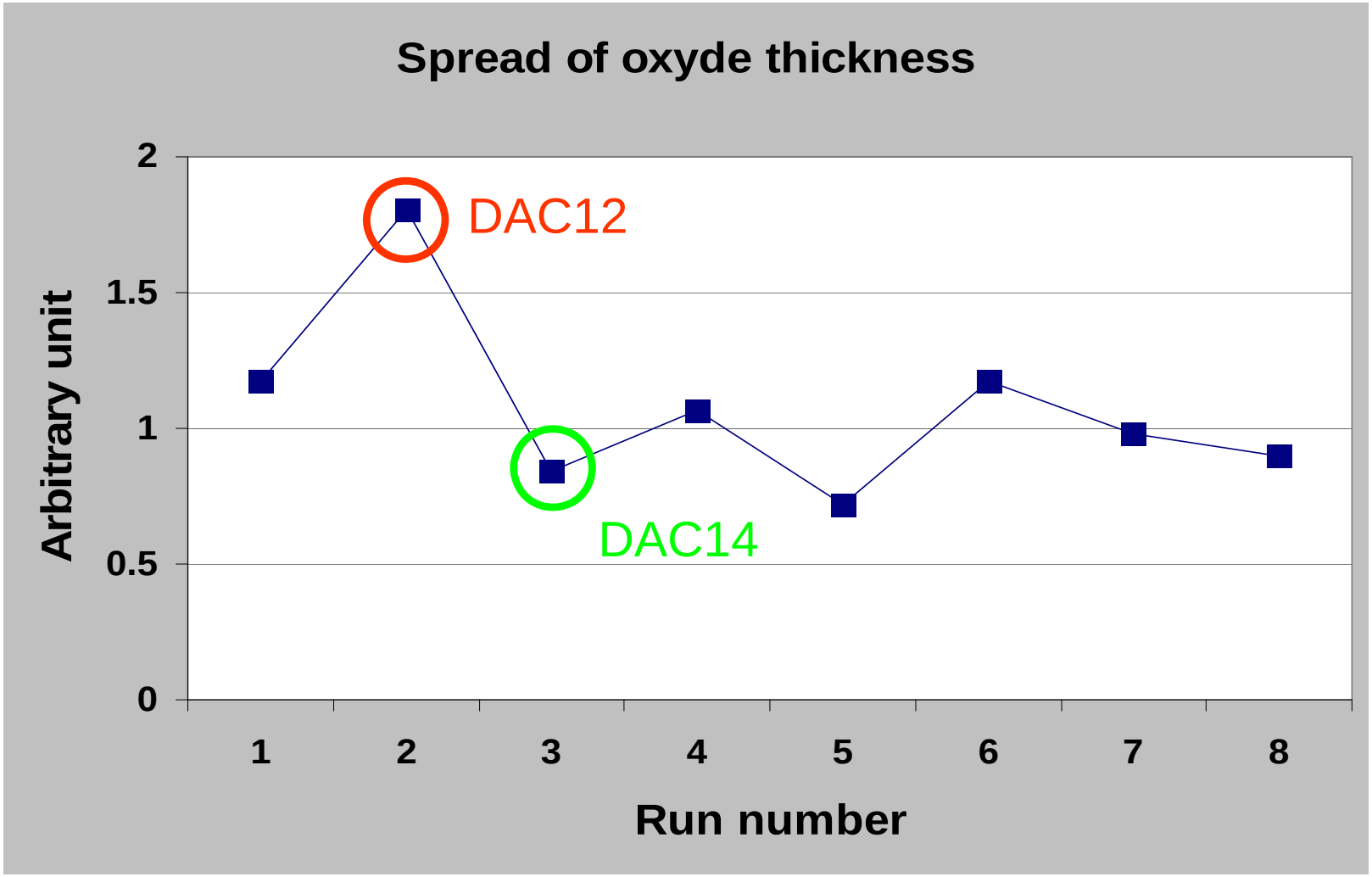


With DEM



Process reliability

Spread of oxyde thickness for 8 runs in 2008 & 2009



Main features of the 2 DACs

Static and dynamic parameters (**without external filter**)

	12 bit DAC		14 bit DAC	
	DEM on	DEM off	DEM on	DEM off
Area (mm^2)	1.6		1.4	
Power (mW)	5		7	
Frequency (MHz)	5		5	
INL (LSB / µV)	0.3 / 150	2.5 / 1200	0.5 / 60	1.2 / 150
RMS noise (LSB / µV)	1 / 500 **	0.15 / 70	0.6 / 70 *	0.5 / 60 *
THD (dB)	-87	-67	-96	-89
SNR (dB)	66 **	77	81 *	82 *
SFDR (dB)	86	68	96	92
ENOB	10.7 **	10.8	13.2 *	13.2 *

** **limited by the DEM noise**

* **limited by the testing board noise**

Design of a 14 bit, 5 Msps Digital to Analog Converter

Conclusion : Process reliability – Trimming issue

- The **matching errors** are **much smaller in the 14 bit DAC** compared to the 12 bit DAC, whereas the capacitor arrays are similar (larger dummies in the 14 bit DAC).
- The **spread of the oxide thickness** for the **12 bit DAC** run is **twice the spread** for the **14 bit DAC** run (it was the worst among the chips submitted by LPSC in 2008/2009).
- The optimal trimming value is the same for the 9 tested DAC. **The same value is also found with high level simulation.**
- For **this run,** the **DAC satisfies the constraints of a 14 bit design without trimming.** (since the optimal value can be predicted).
- **A self trimmed 14 (or 15 ?) bit DAC will be submitted in 2010.**