Post Processing & Packaging

Manuel FENDLER

Plan

1- Identification des systèmes d'assemblage
2- Caractéristiques des systèmes d'assemblage (SOC, MCM, SIP, SOP)
3- Filières d'intégration 3D (chip / package) stacking
4- Technologies non TSV (câblage filaire, flip chip)
5- Technologies TSV (Through Silicon Via)
6- Wafer Level Packaging (WLP)

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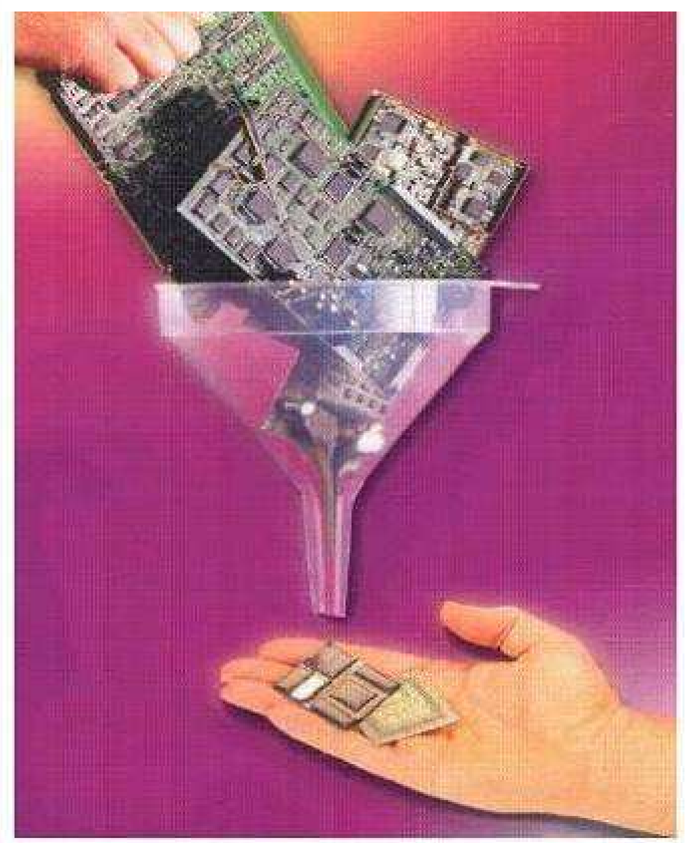
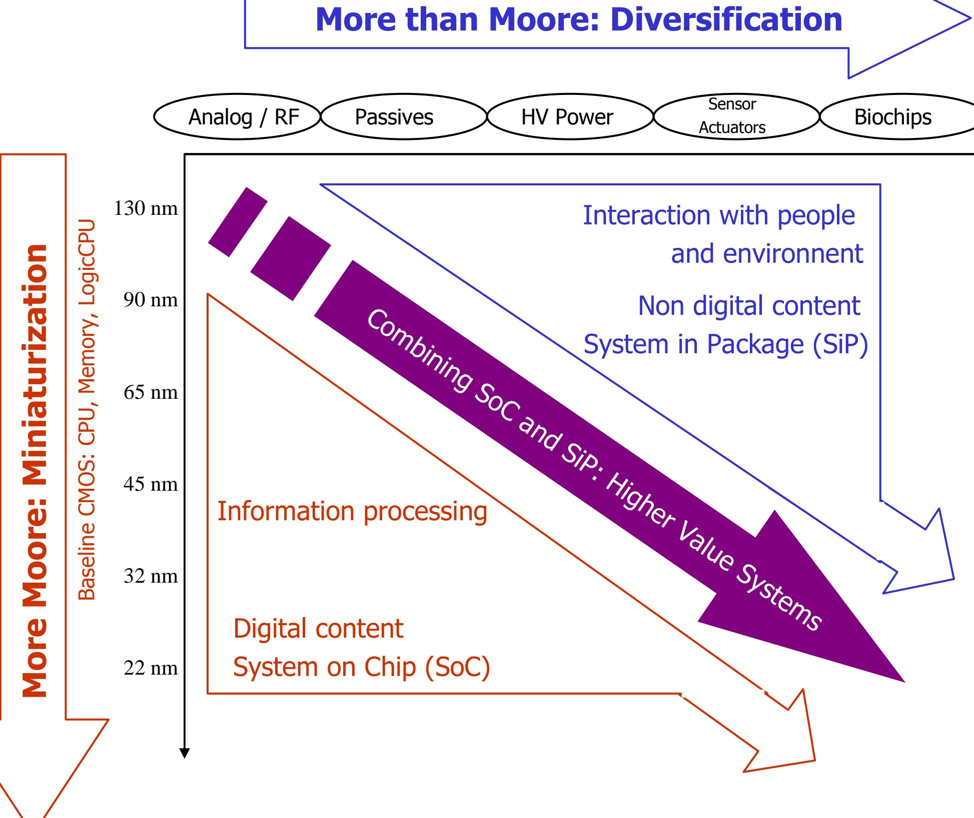
Miniaturisation des systèmes





Source ITRS'07

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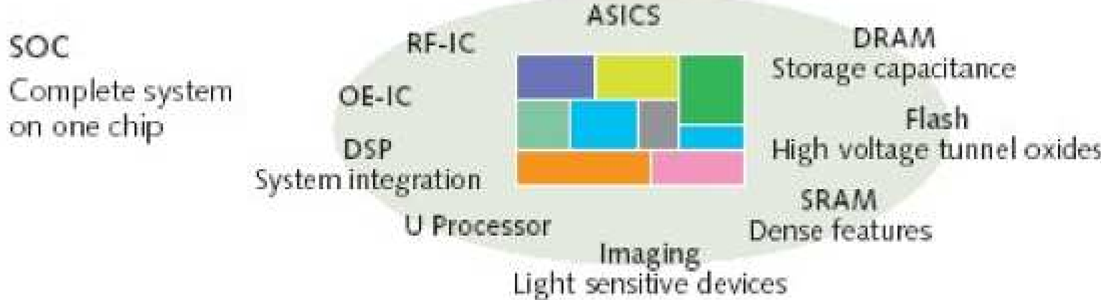
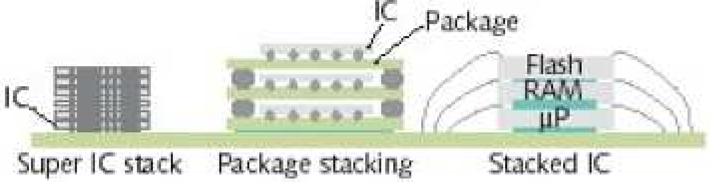
Technologie des systèmes

SOC
Complete system on one chip



MCM
Interconnected components

SIP
Stacked chip/package



SOP
- Optimizes functions between ICs andpackage
- Miniaturizes systems

Best of Both IC & Package

Source Georgia Tech

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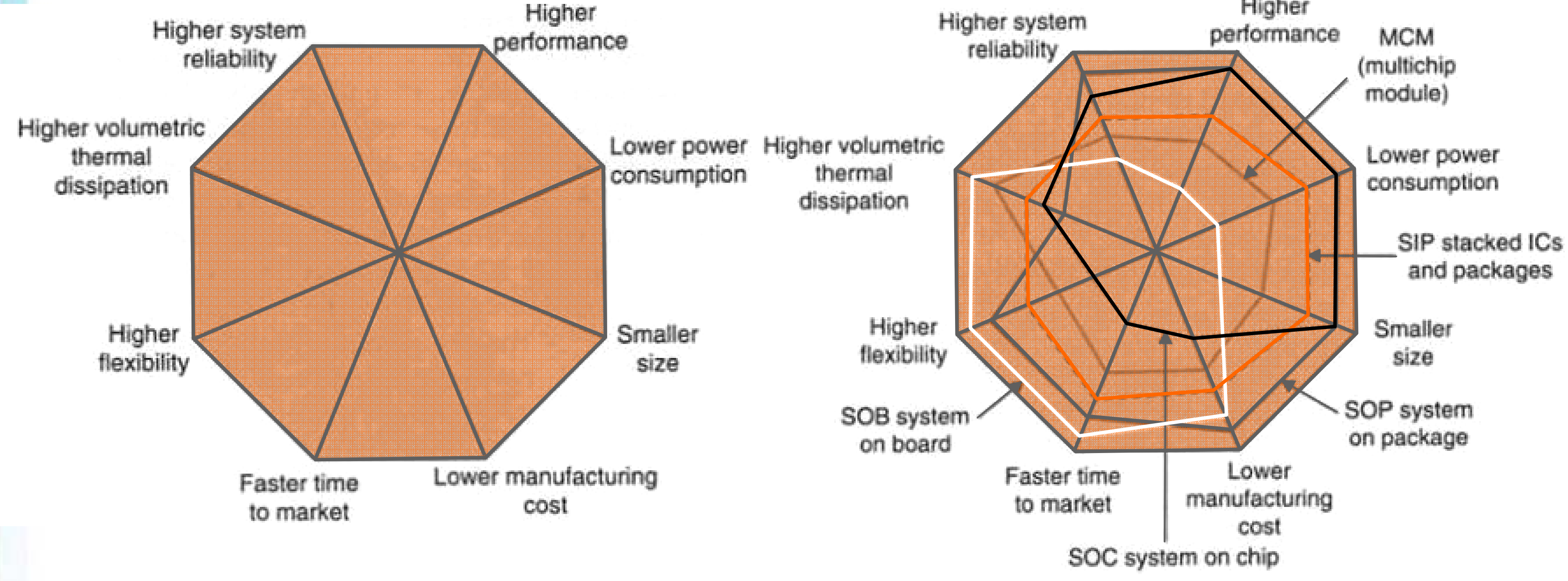
Comparaison des technologies



R.Tummala [1]

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Comparaison des technologies

System on Chip

Bio-Interface

Power supply

MEMS

SiP and 3D Packaging

Cost / function

Time to market

System complexity

ITRS'05

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Comparaison des technologies

Item	SiP	SOC
Technology Limiters	• KGD : Wafer (level) burn-in • Interconnect Process • PCB technology • Pad redistribution	• Analog + Digital Process • Different Voltage • Low Wafer Yield • High pad count interconnection
Delivery	• Shorter term delivery • Fast market driven	• Longer term delivery • Volume market driven
Performance (Power Consumption, EMI, Max frequency)	• Inferior to SOC in general • In the case of super-connect, superior to SOC	• Superior to SIP in general • In case of parallel layout, inferior to SIP
Cost	• Lower Fab (mask) cost • Lower revision cost • Lower EDS load	• Higher Fab (mask) cost • Higher revision cost • Higher EDS load

Samsung / JISSO'05

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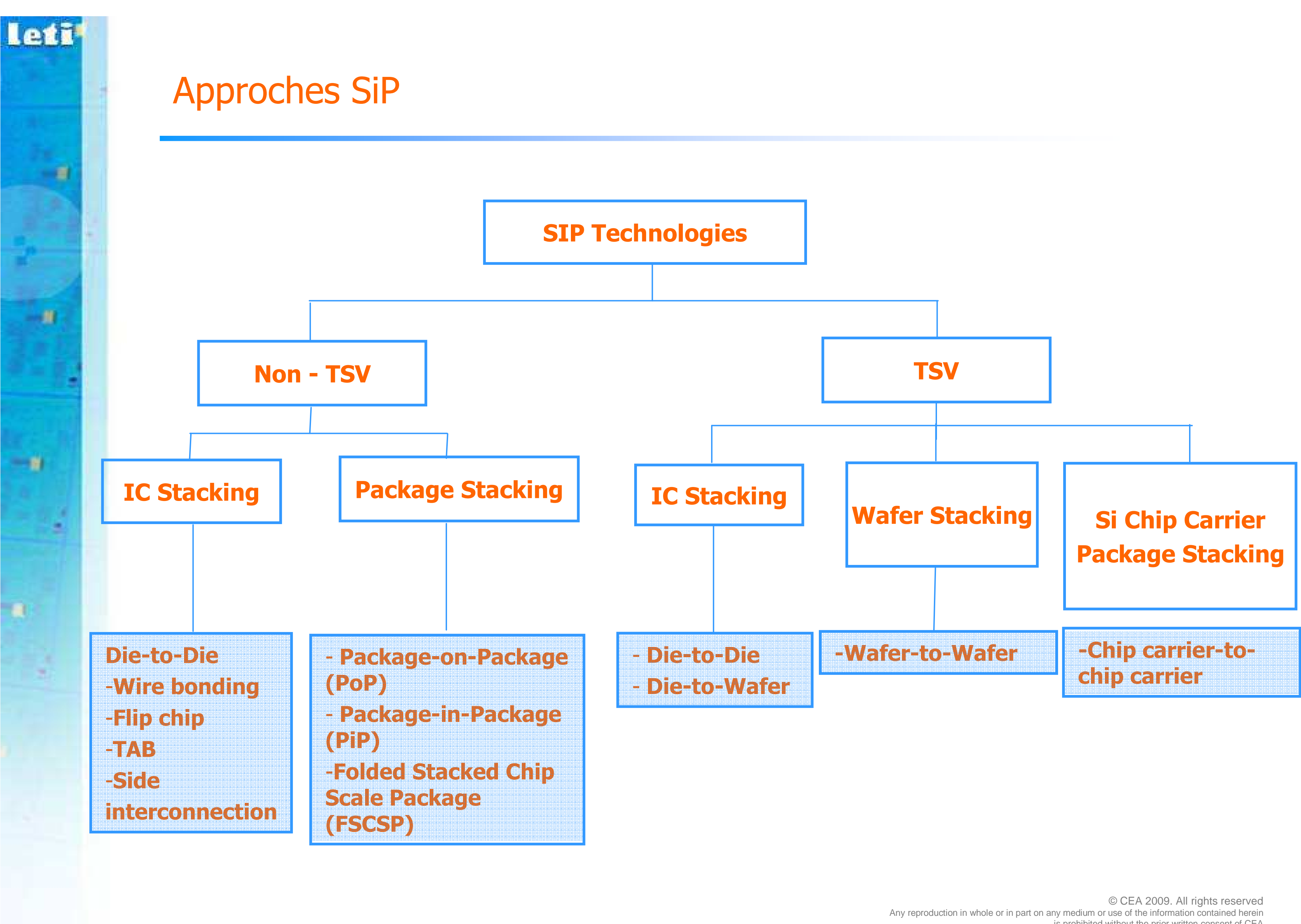
Approches SiP



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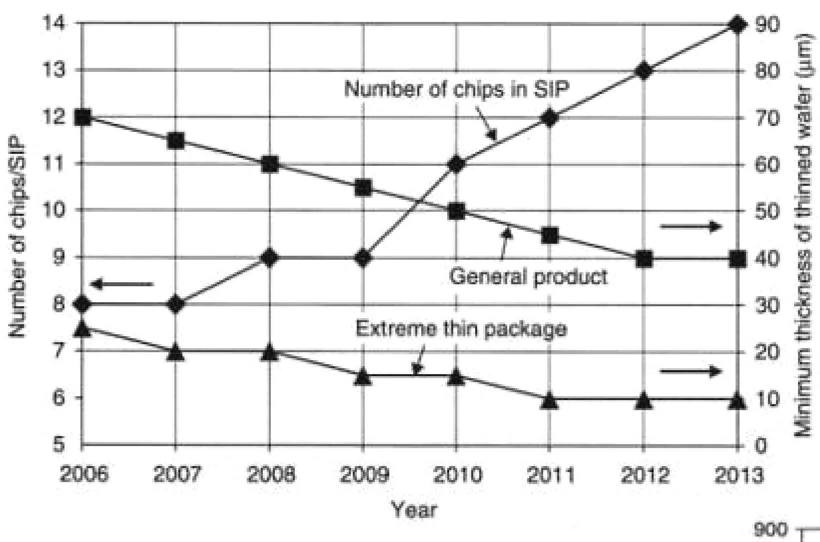
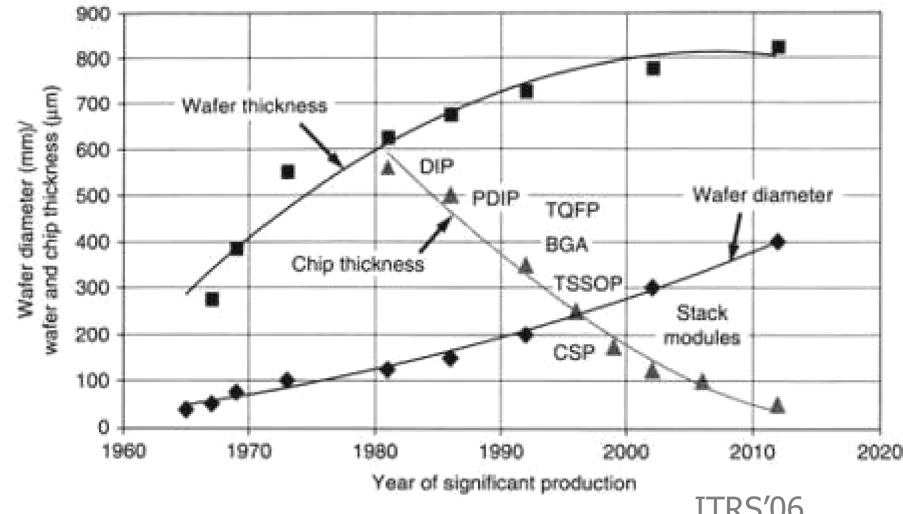
Empiler pour être plus fin



S.Savastiouk [2]



ITRS'06

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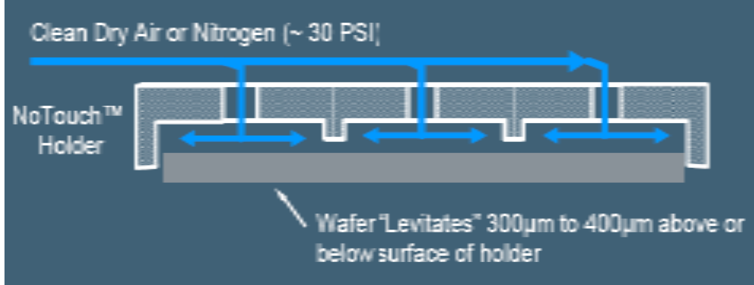
Comportement du silicium aminci



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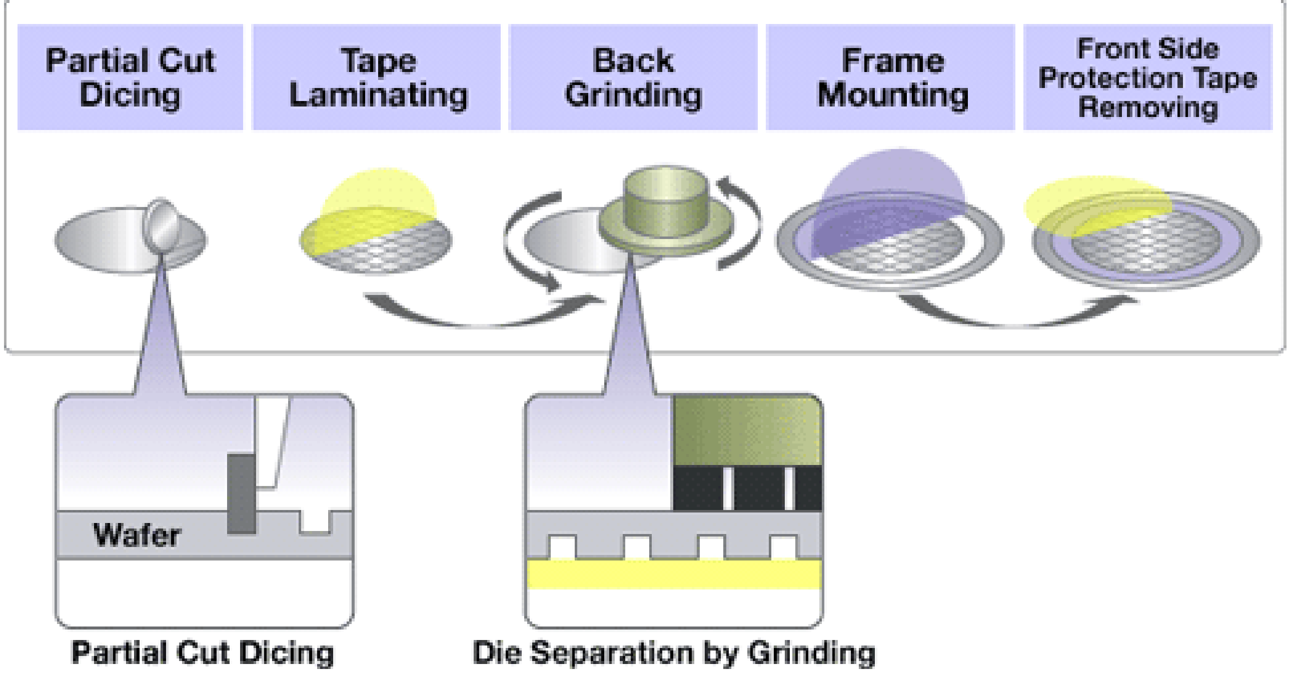
Procédé DBG: Dicing Before Grinding



Source Disco HiTec

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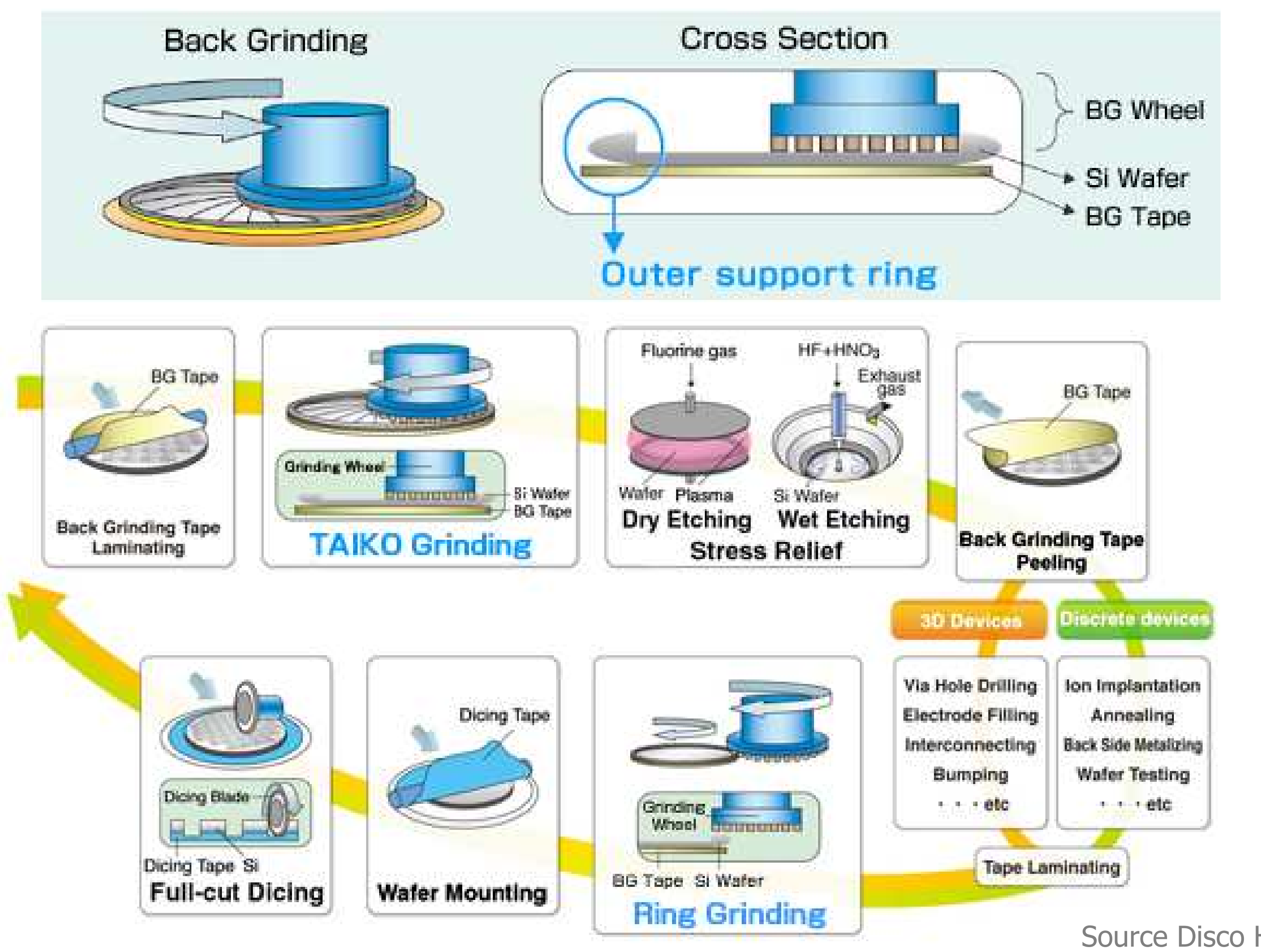
Procédé Taiko



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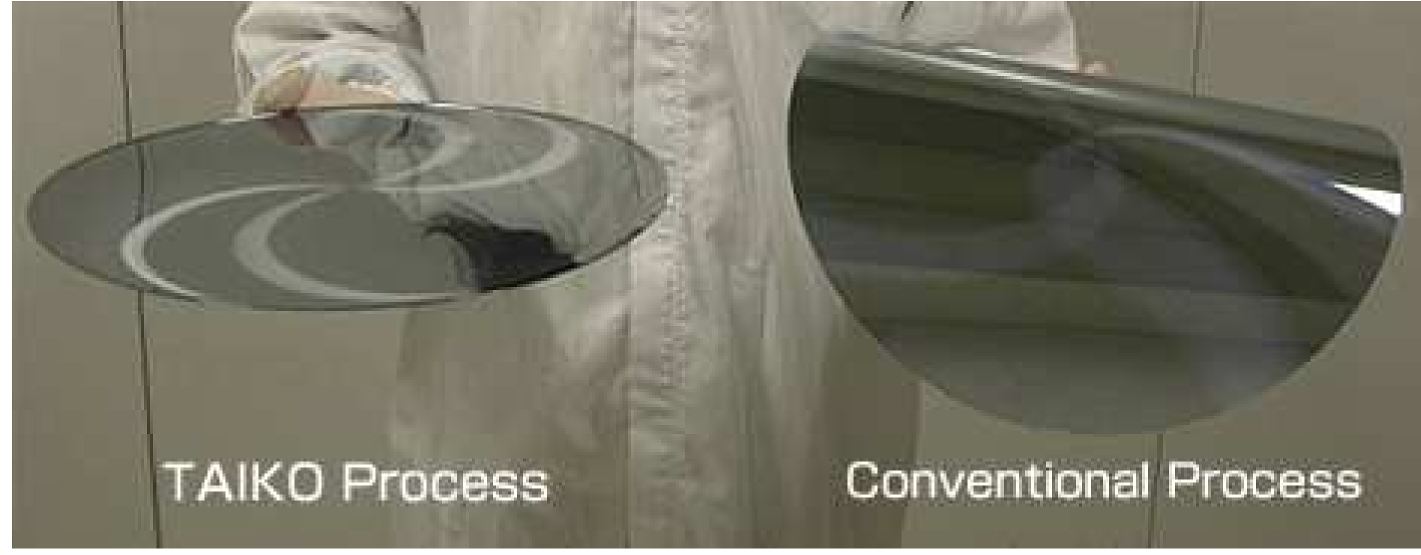

Source Disco HiTec

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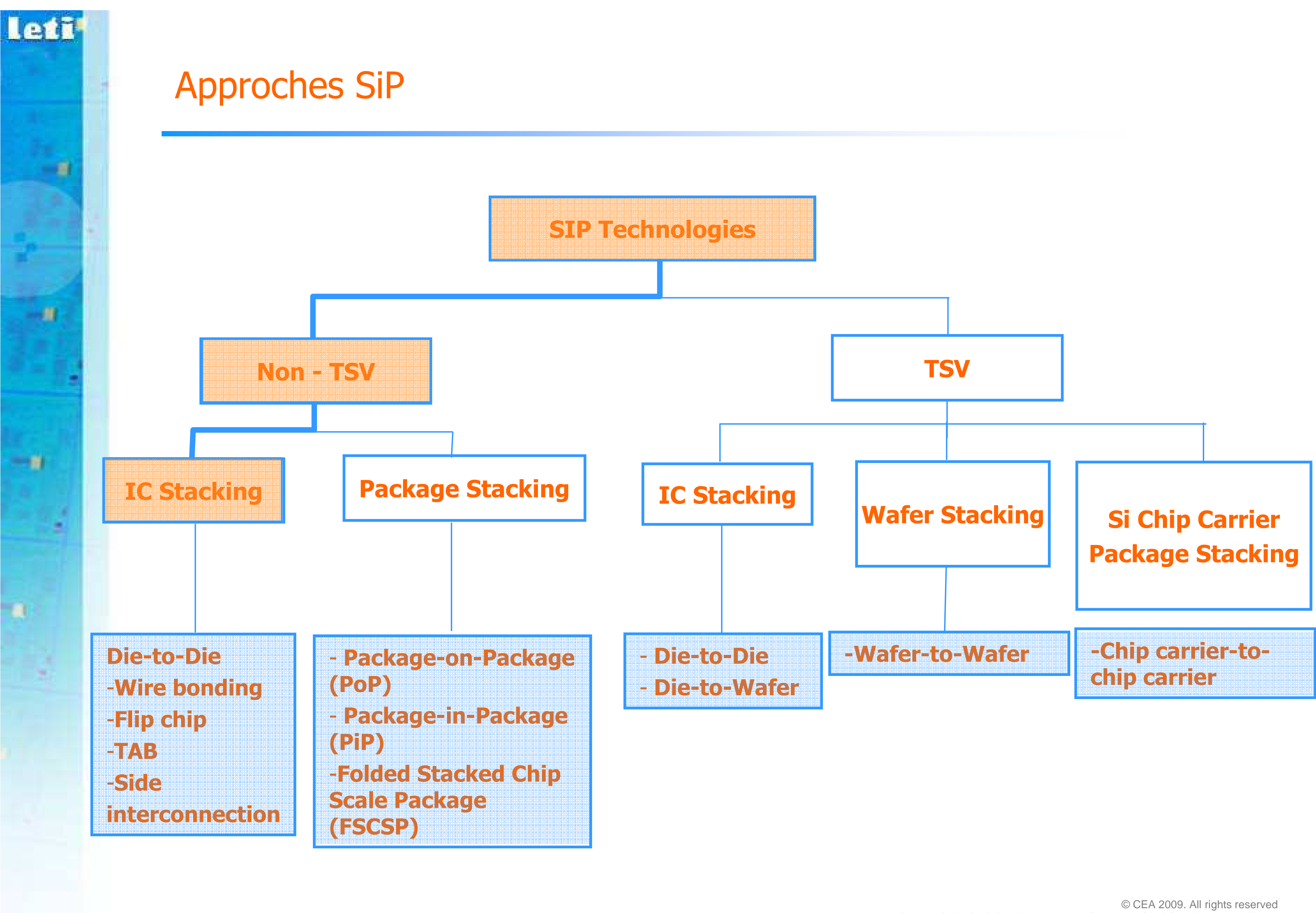

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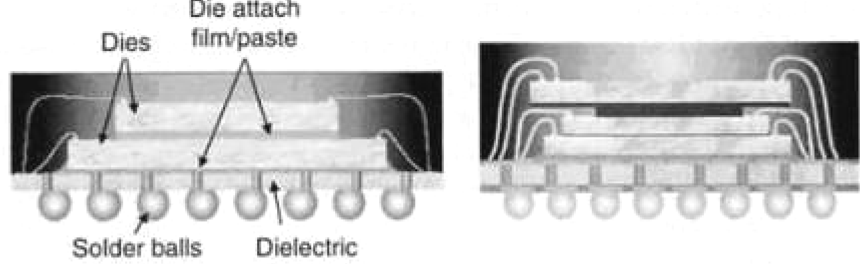
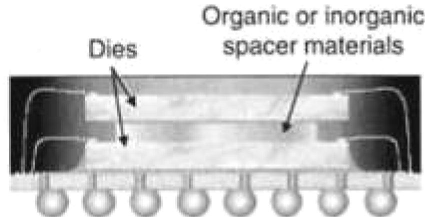
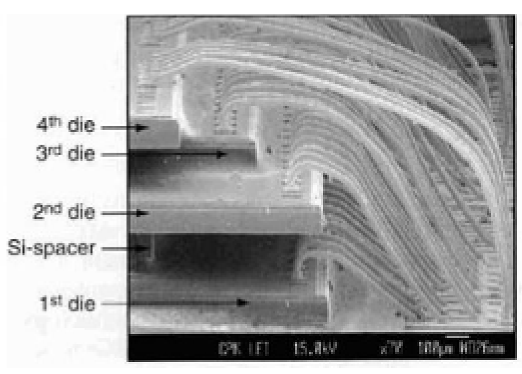
Configurations câblées

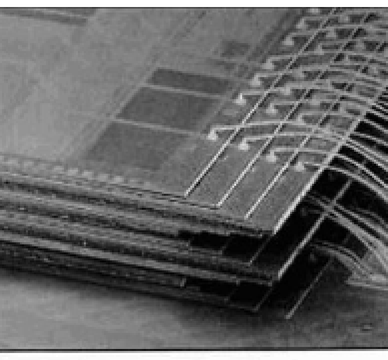


Pyramid and overhang stacking (Amkor [3])

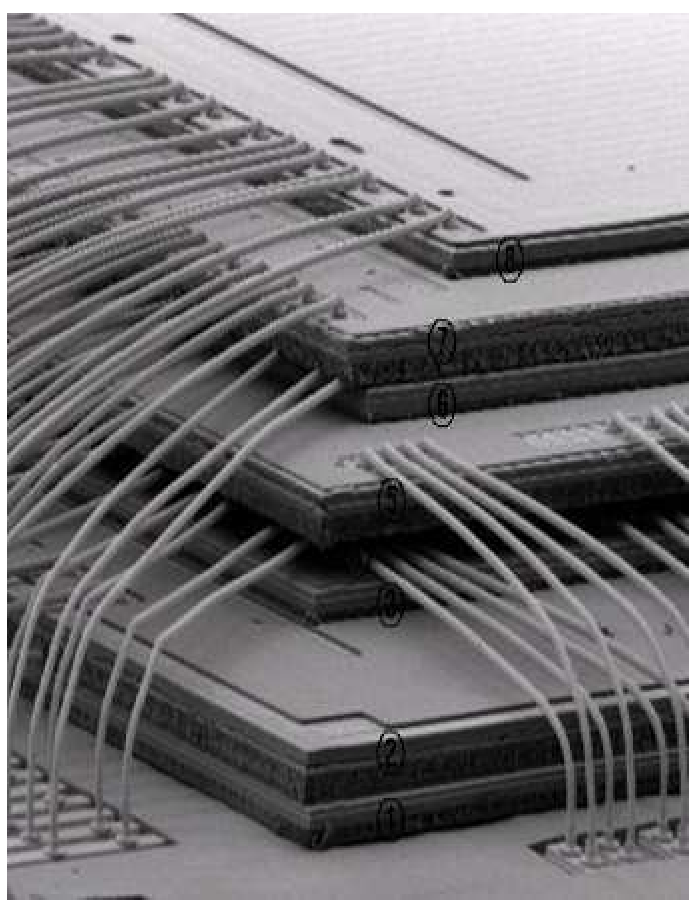




ChiPac (4+1)



20 x 25 µm thick (Hynix)



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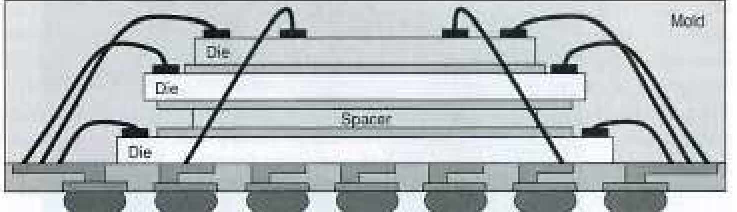
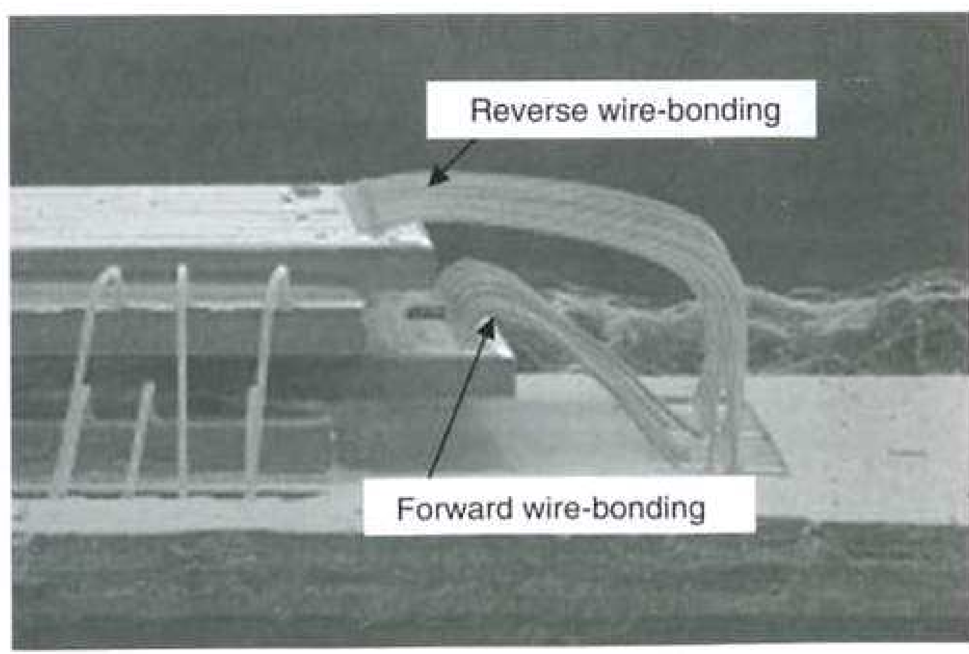
Configurations câblées





Top logic die + 2 memory dies (Intel [4])

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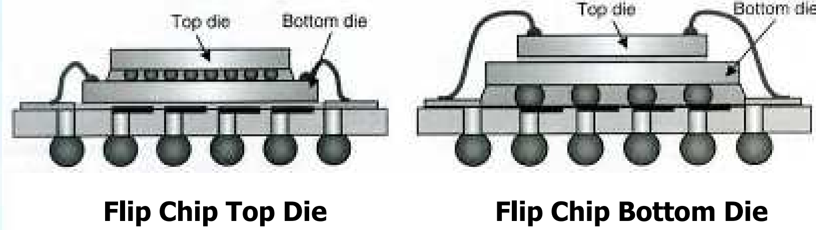
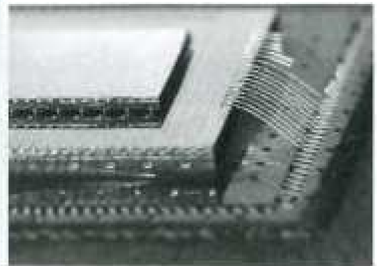
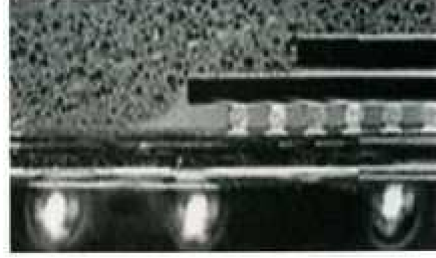
Configurations flip chip

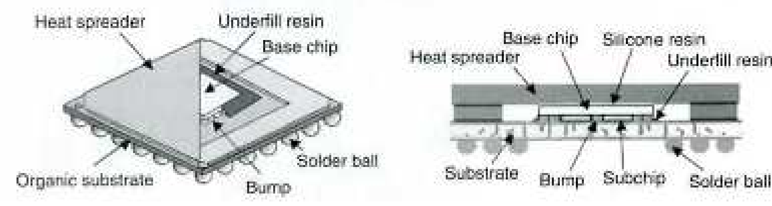


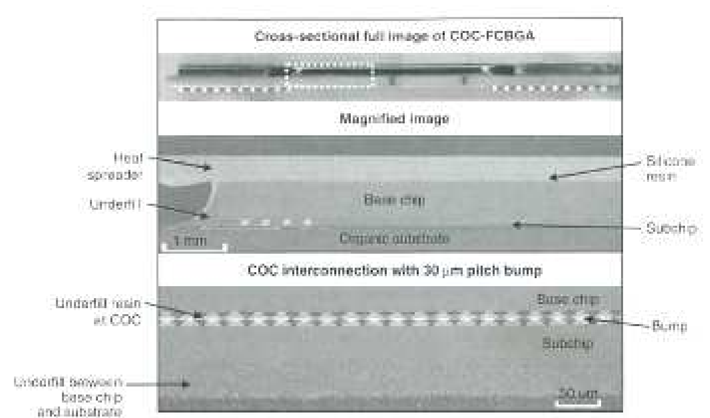
Flip Chip Top Die **Flip Chip Bottom Die**





Flip Chip [30] & Wire bonding stacking [5]





COC chip on chip (30 µm pitch) [6]

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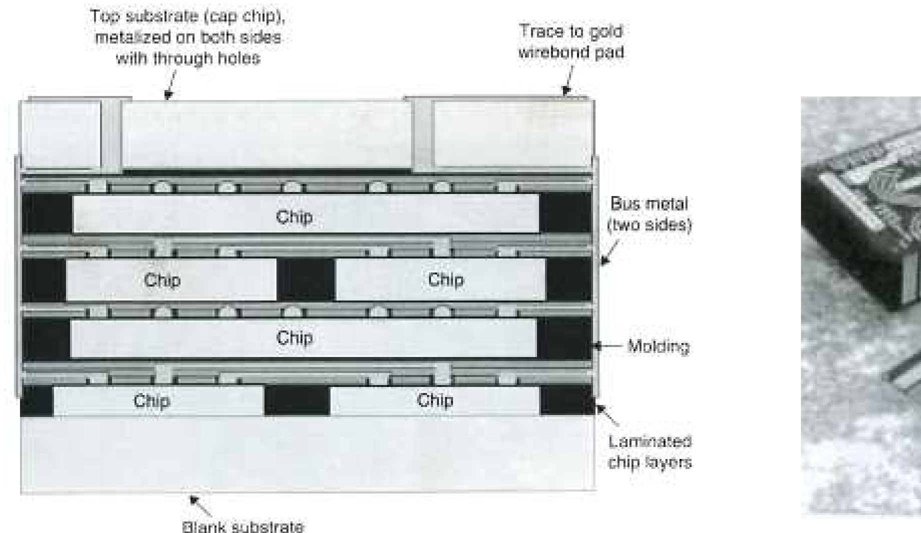
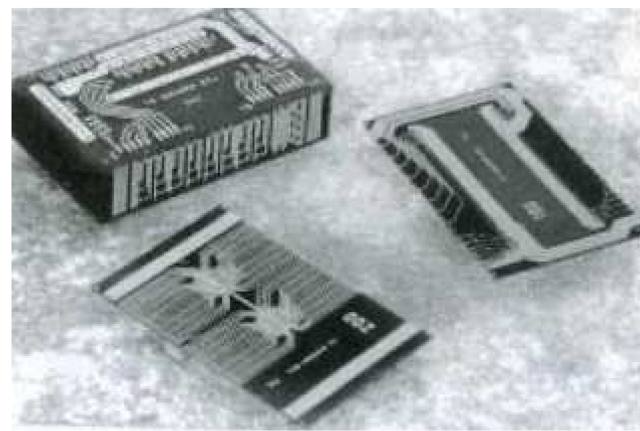
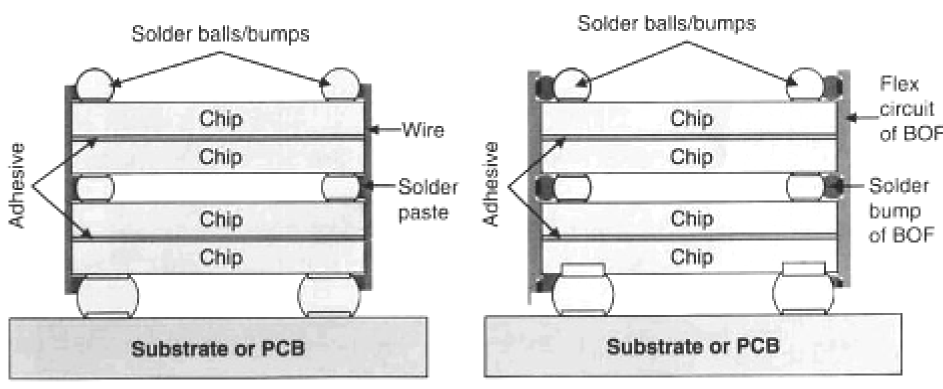
Interconnexions latérales

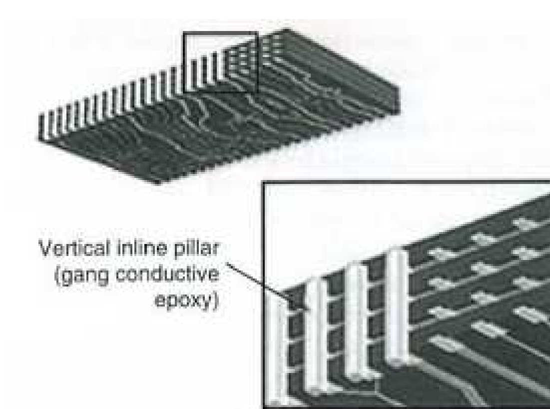




Flash Memory Chip stacking by side metallization [7-8]



Wire On Bumps (WOB) **Bumps On Flex (BOF)**
Side terminations [9]



Chip stacking with conductive polymer Side terminations [10]

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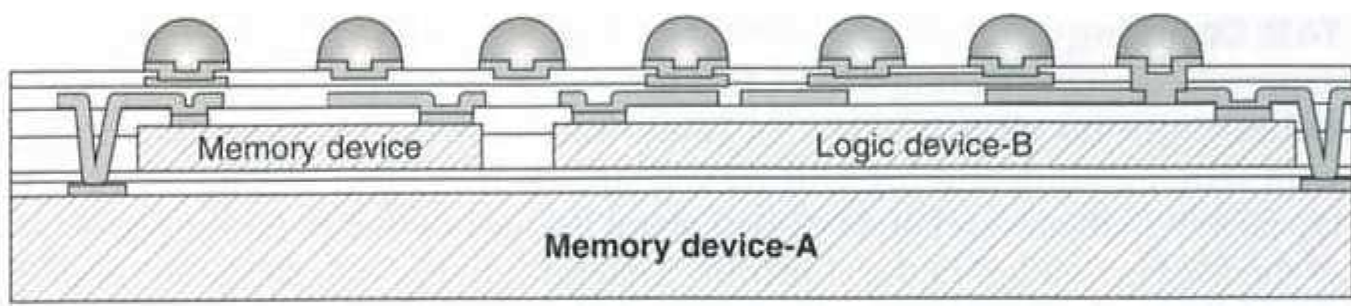
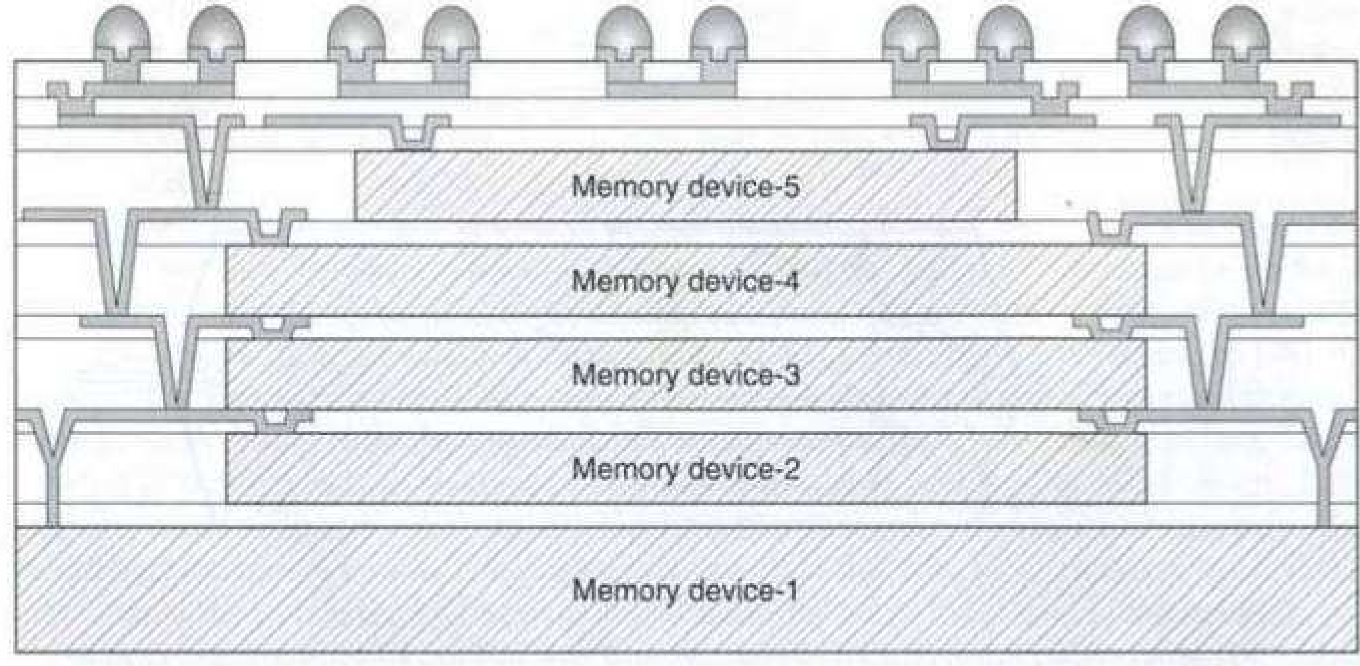
Composants enterrés (embedded)





High capacity memory applications [11]

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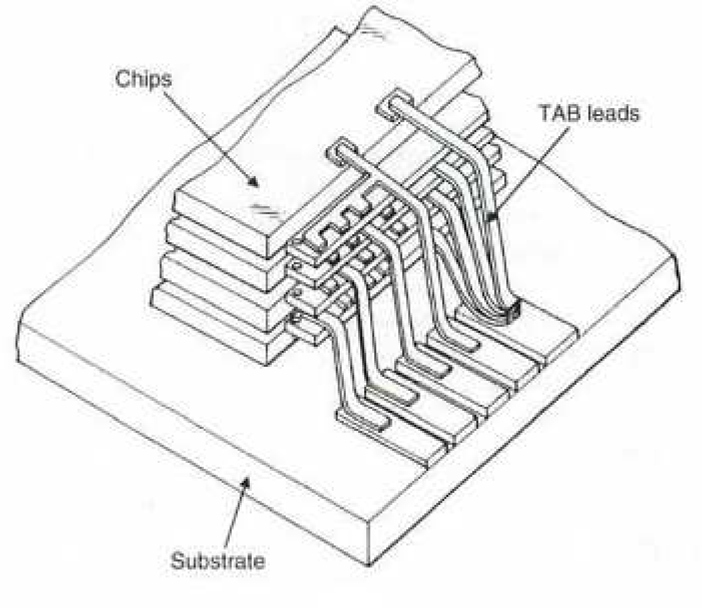
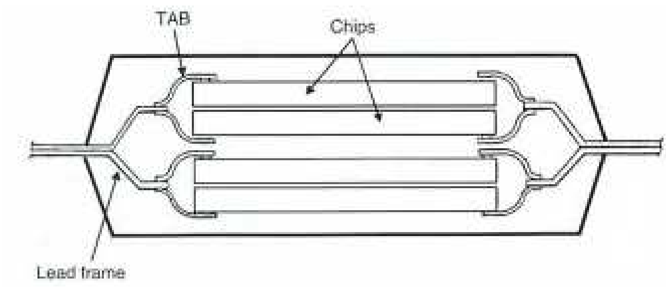
Composants empillés (TAB)



Stacked TAB on PCB



Stacked TAB on Lead Frame

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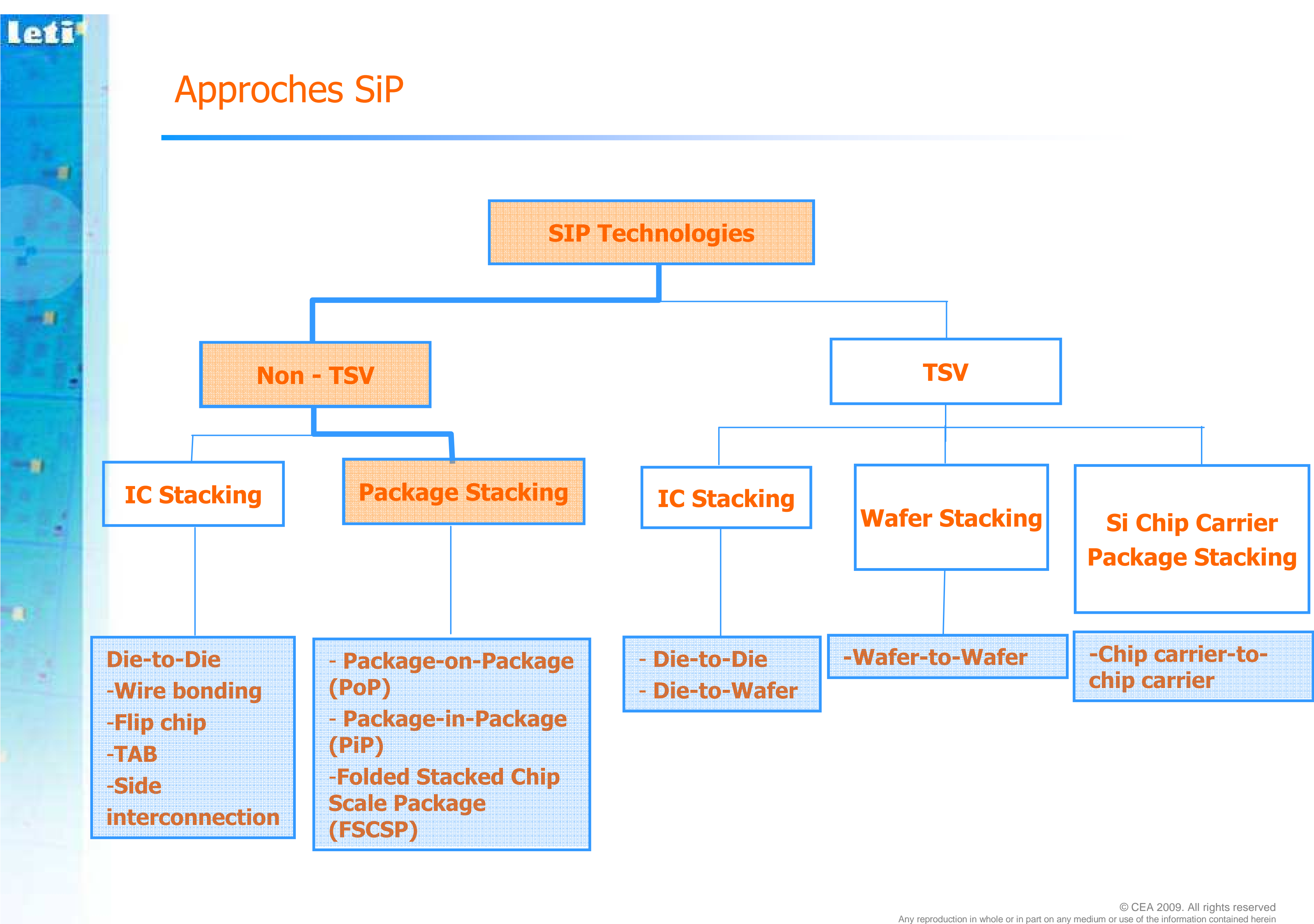
Approches SiP



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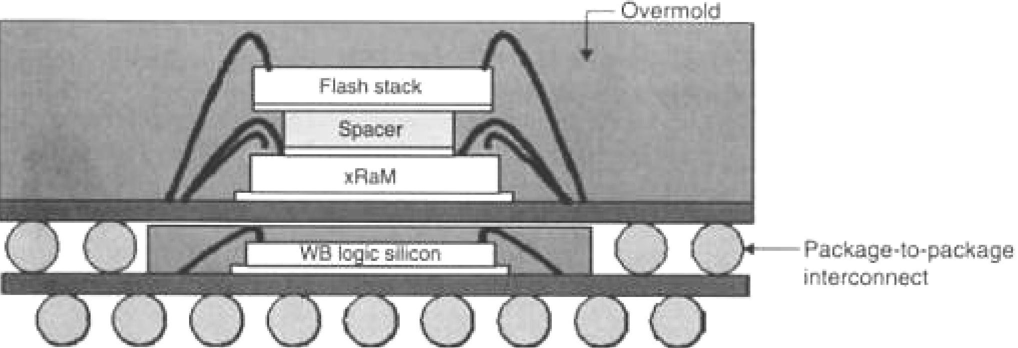
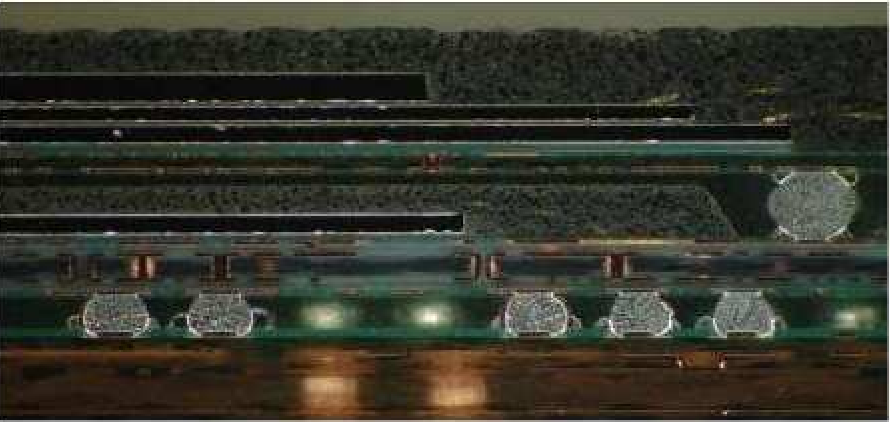
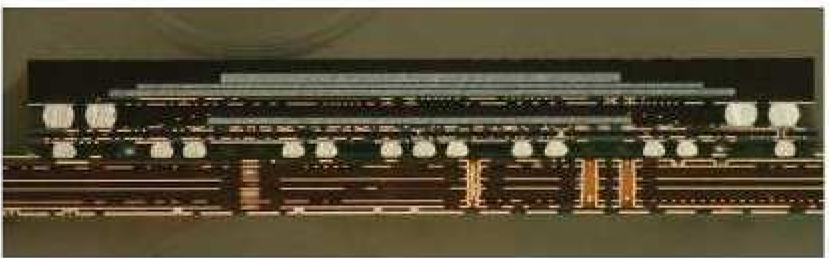
Package On Package PoP - SiP







Four chip PoP on a mobile handset [12]

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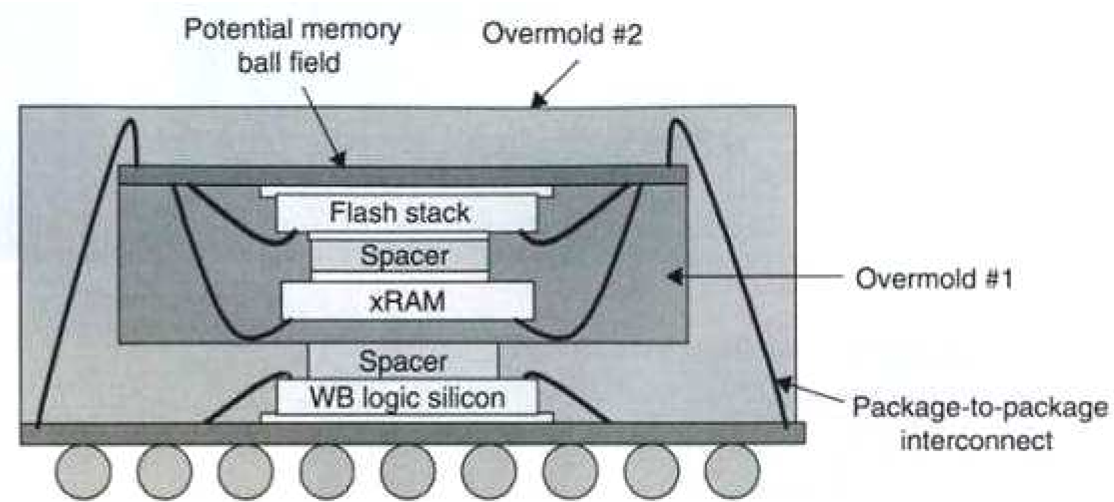
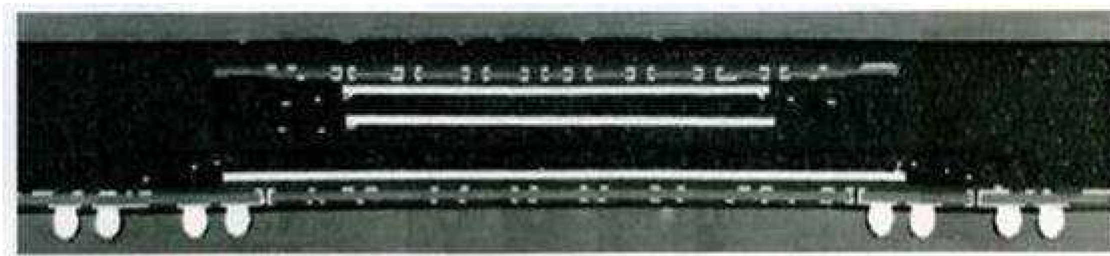
Package In Package PiP - SiP





Stacked memory package (top) and ASIC package (bottom) [13]

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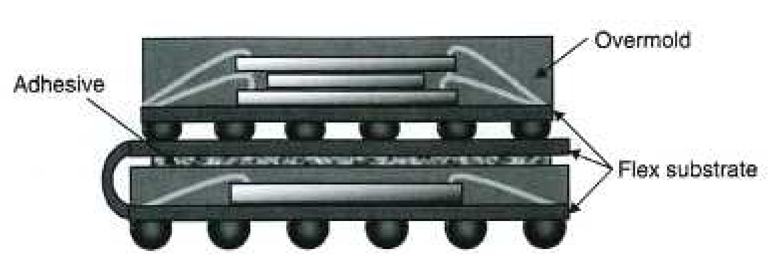
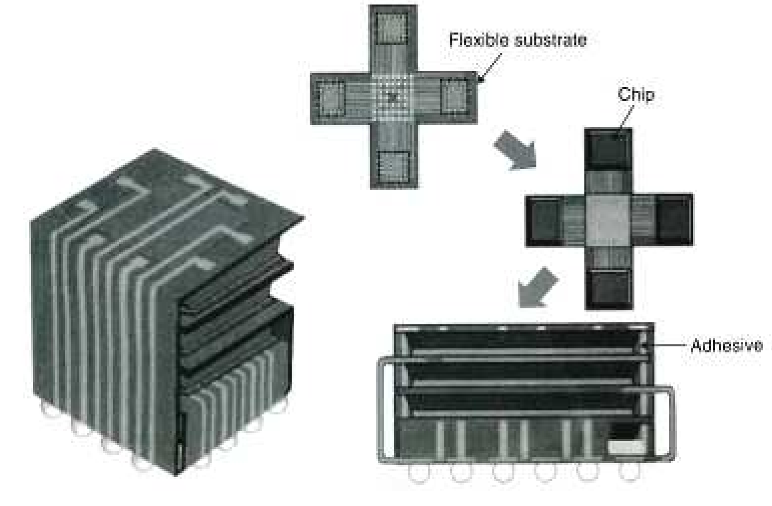
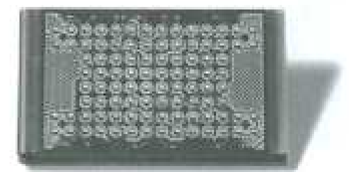
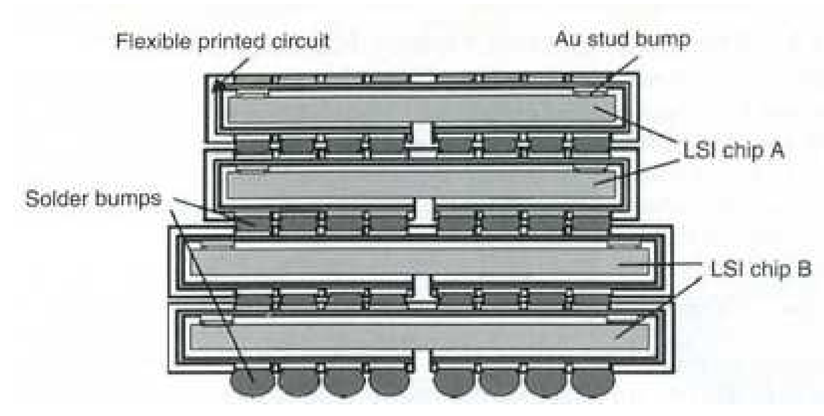
Folded Sheet Chip Scale Package (FSCSP)







Tessera [14]



NEC [15]

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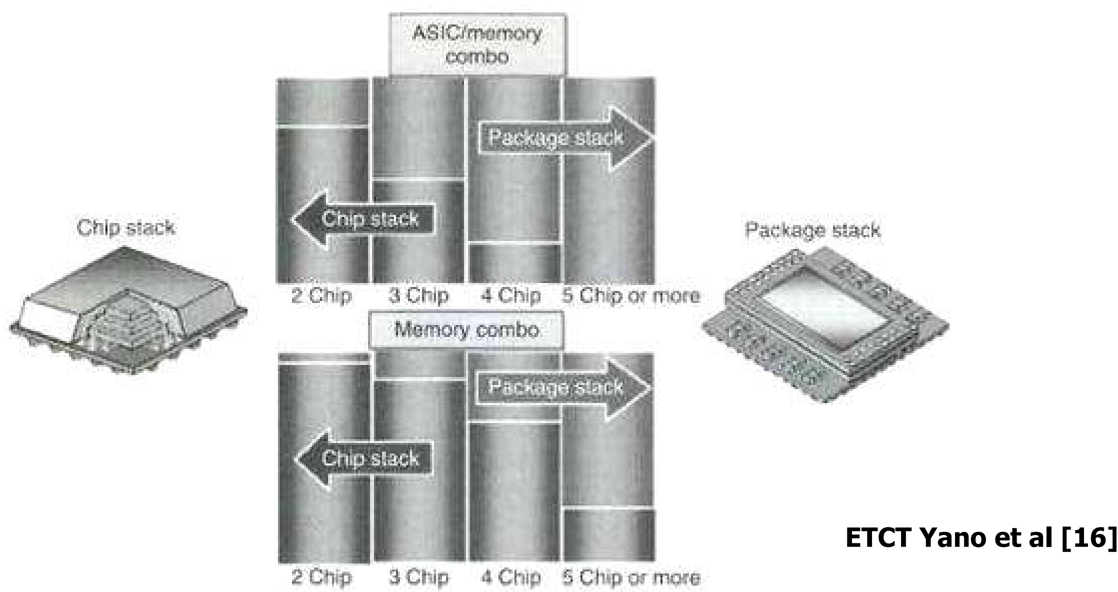
SiP Non-TSV Comparaison



ETCT Yano et al [16]

	Chip stacking	Package stacking
Pros	• Low package profile available with advanced wafer thinning technology. • Existing SMT line infrastructure available • Cost reduction by minimum substrate consumption	• Testability at individual package level for KGD • Greatly increased package stacking yield • Flexible selection of chips to be stacked
Cons	• KGD required for high product yield • Single sources product • New development needed to change stacked device	• Higher package profile • Lack in infrastructures for package stacking

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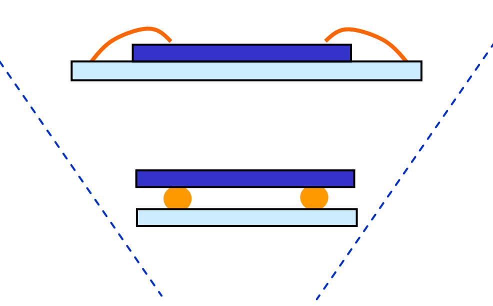
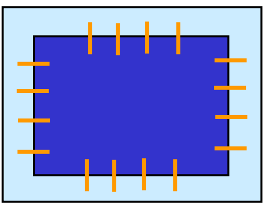
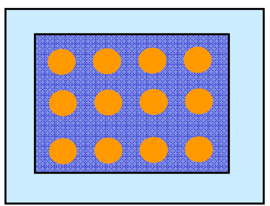
SiP Non-TSV : du fil et des billes…

Size Reduction



Number of I/O's





Smaller pitch

Flip Chip

- Size reduced
- Higher integration
- Shorter connection length
- Smaller pitch
- Self alignment
- Collective process
- Efficient heat dissipation

Wire Bonding

– Industrially proven
– Moderate cost
– Reliability
– Compatibility (housings, connectors)
– Standard metallurgy (no post process)

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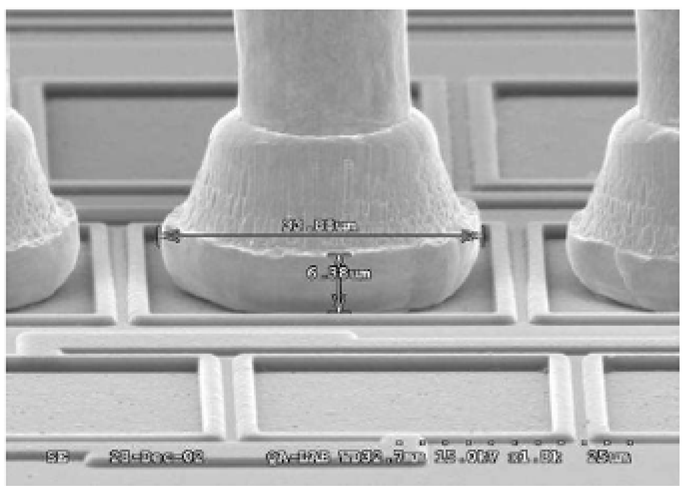
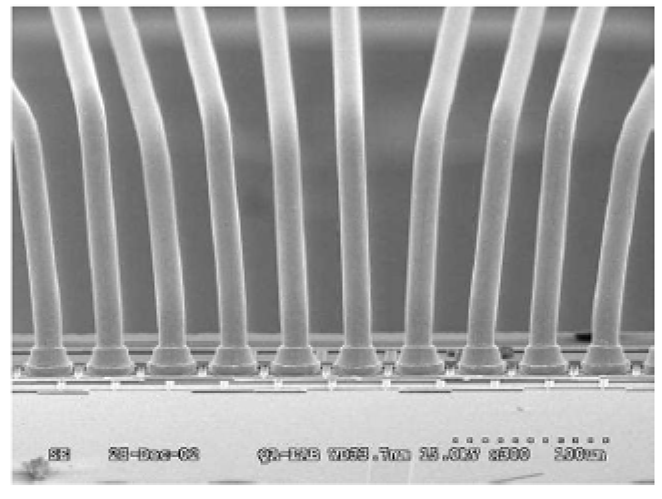
leti

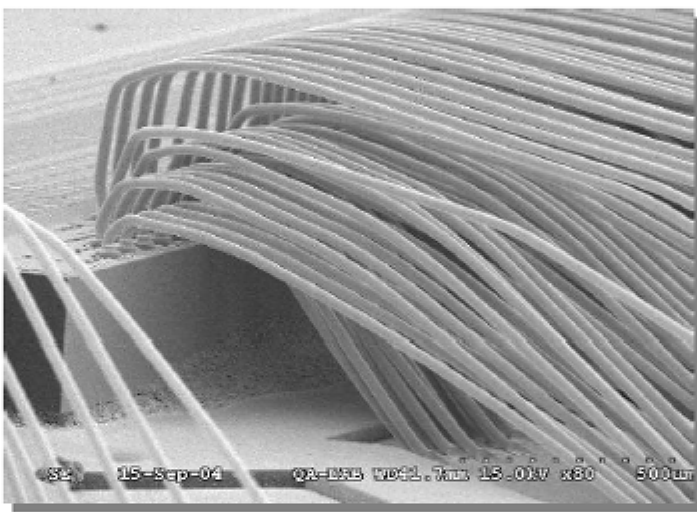
SiP Non-TSV : câblage filaire…



Fine pitch



Fine pitch



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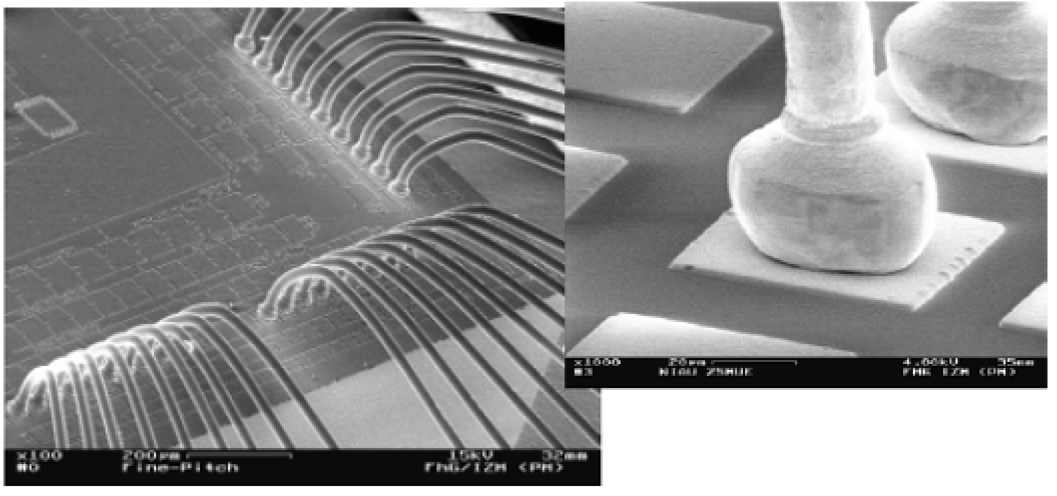
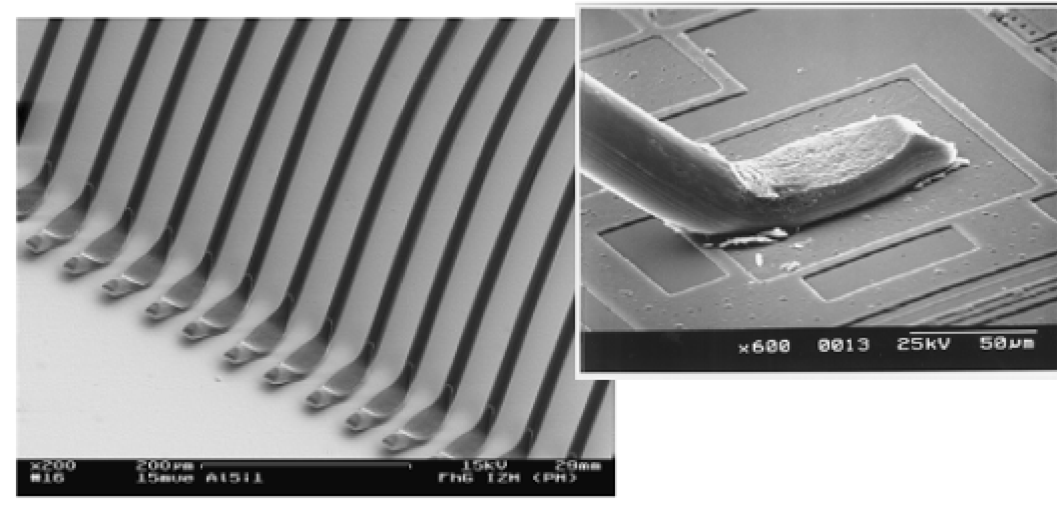
SiP Non-TSV : câblage filaire…

- **Bonding type**
- Ball - Wedge
- Wedge – Wedge

- **Energy application**
- Thermocompression (T, p)
- Ultrasonic (p, US)
- Thermosonic (T, p, US)

- **Wire processing**
- Heavy wire bonding
- Thin wire bonding
- Ribbon bonding





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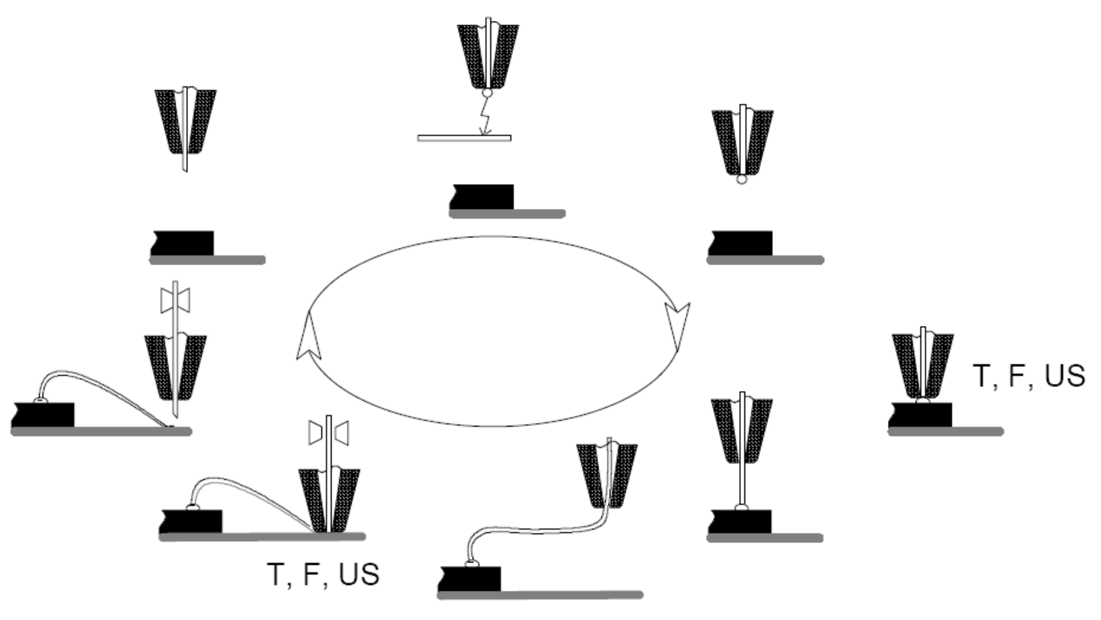
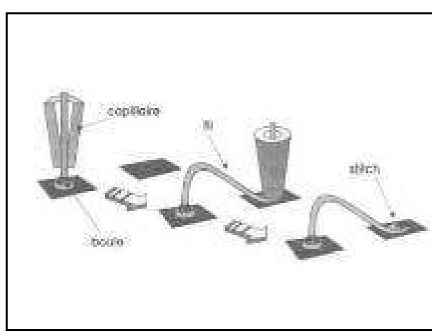
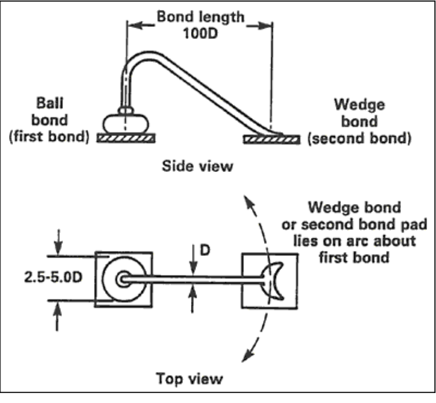
SiP Non-TSV : câblage filaire…ball-wedge bonding

Au wire

Typical metallization: thin Al (<1 µm) or thick Au (>0.5 µm)







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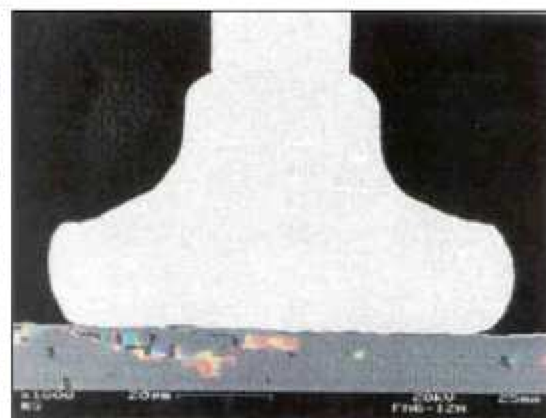
SiP Non-TSV : câblage filaire…ball-wedge bonding



Ball **Wedge** **Cross section**

Typical process parameters for thermo sonic (gold wire with 25µm diameter):

- Bond temperature: 80 - 250 °C
- Bond force: 30 - 90 cN
- Ultrasonic power: 100 - 500 mW (at 60 kHz - 120 kHz)
- Bond time: 20 - 100 ms

Higher bonding temperature (280 – 350°C) with thermo compression bonding only.

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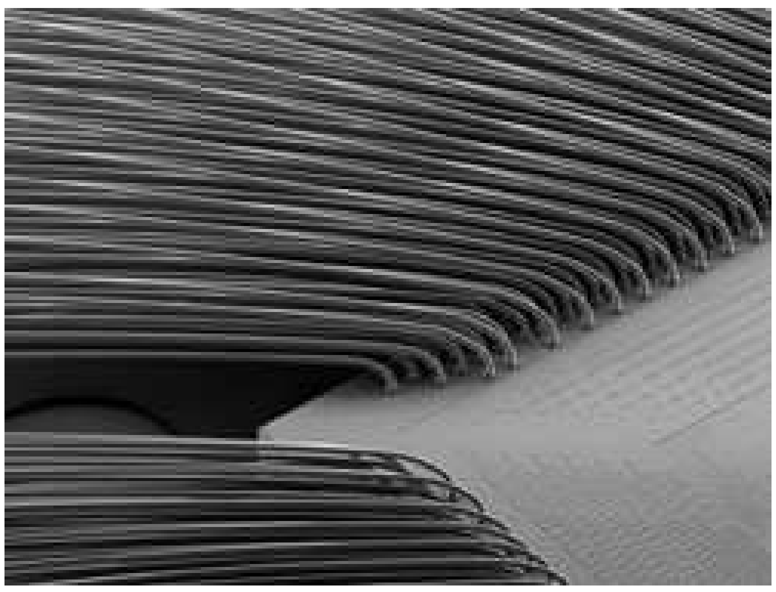
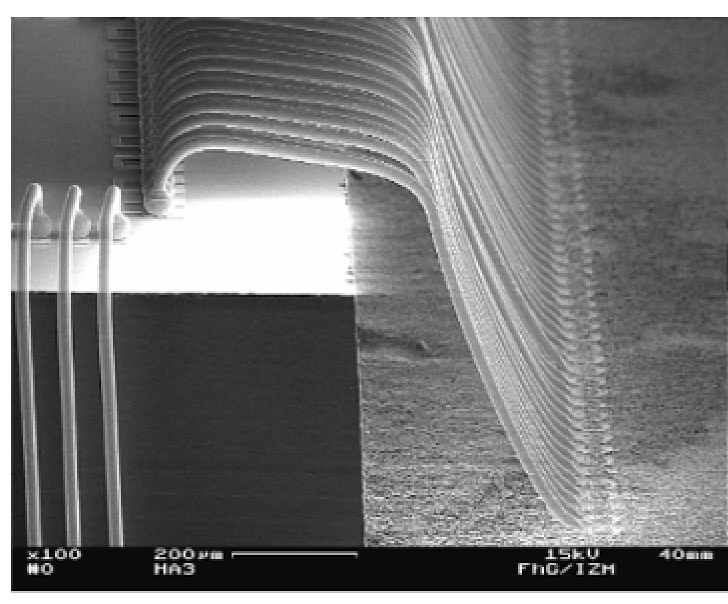
SiP Non-TSV : câblage filaire…ball-wedge bonding



Long loops



Short loops

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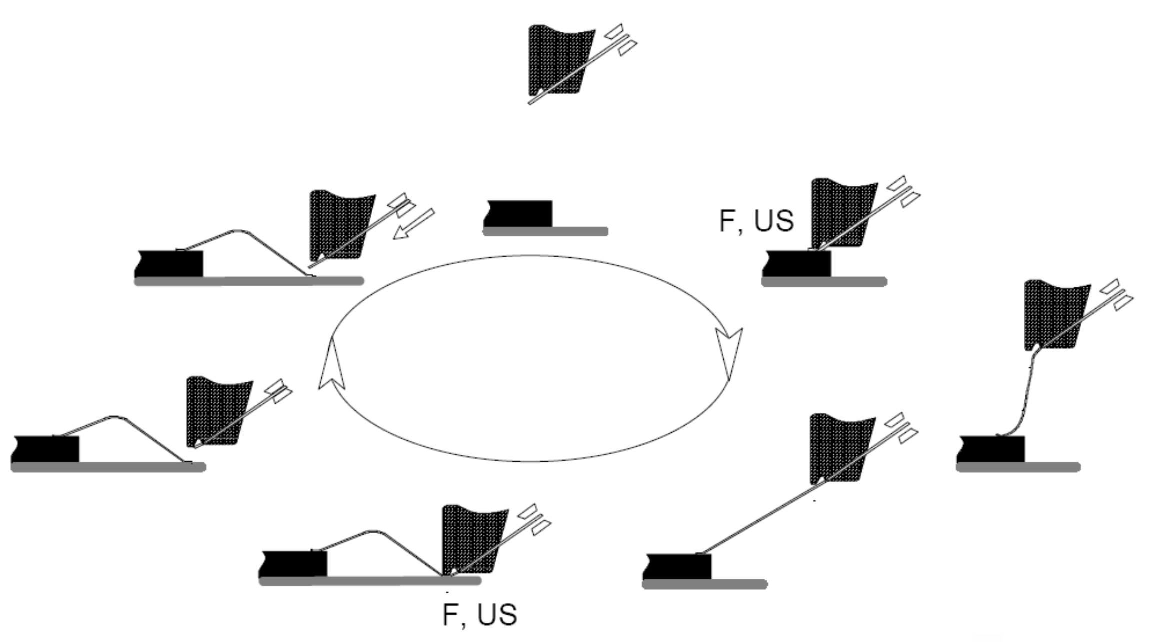
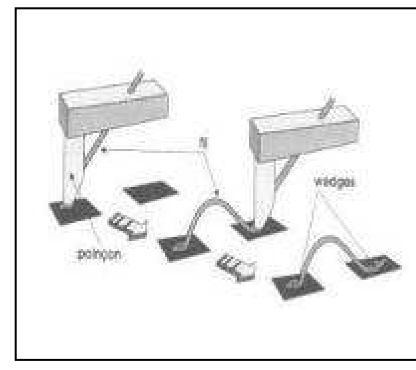
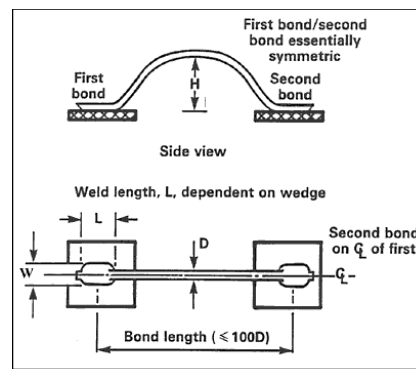
SiP Non-TSV : câblage filaire…wedge-wedge bonding

Wedge-Wedge Bonding: Al wire (Au is also possible)
Typical metallization: thin Al (<1 µm) or thin Au (<0.1 µm)
e.g. Ni/Au







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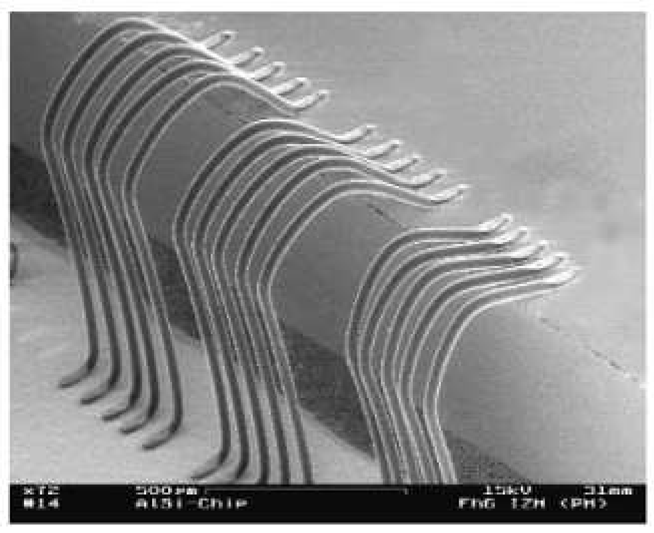
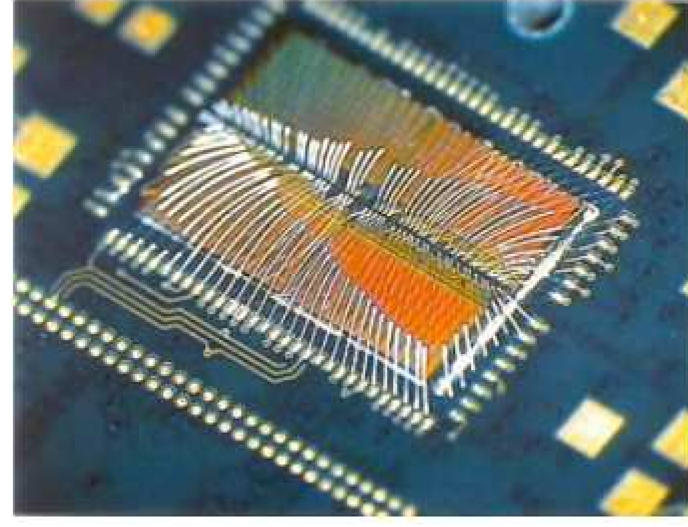
SiP Non-TSV : câblage filaire…wedge-wedge bonding

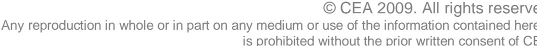




Short loops < 0,5 mm **Long loops < 8 mm**

Process parameters US bonding (AlSi1 wire with 25 µm diameter)

- Bonding temperature: room temperature
- Bonding force: 25 - 40 cN
- Ultrasonic power: 100 - 500 mW (at 60 kHz - 120 kHz)
- Bonding time: 30 - 90 ms



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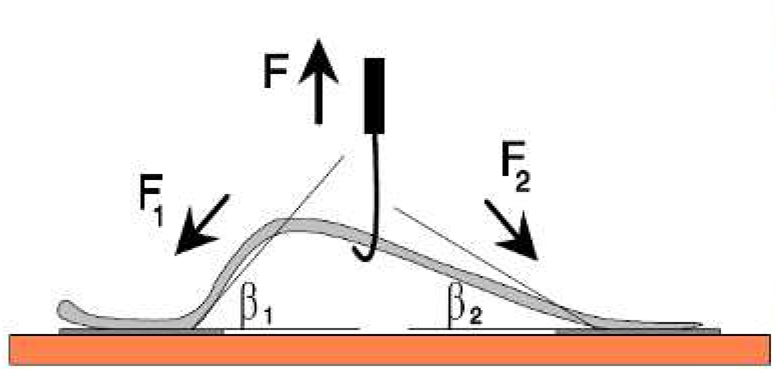
SiP Non-TSV : câblage filaire…bonding pull test



$\beta_1 = \beta_2 = 30°$

Short loops < 0,5 mm **Long loops < 8 mm**

Pull Test typical values

1.5 g < < 8 g

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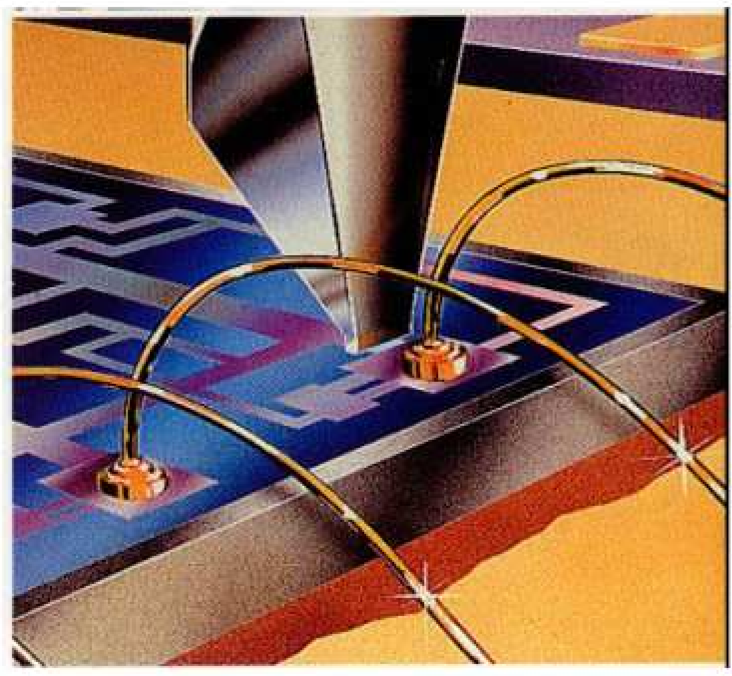
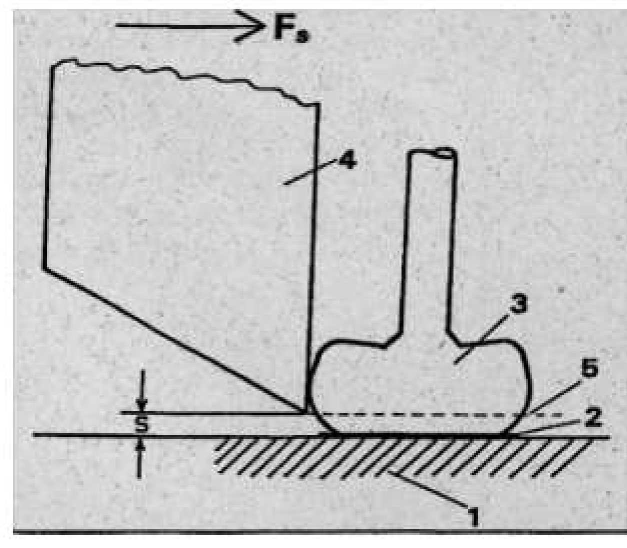
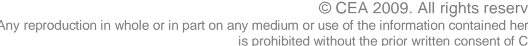
SiP Non-TSV : câblage filaire…bonding shear test



Source: Dage Firmenschrift and DVS-Merkblatt Drahtbonden



1 Substrate / Pad (pad lift)
2 Interface Ball / Substrate (ball lift)
3 Au-Ball (ball shear)
4 shear tool
5 Shear level
S shear height
F_S shear force



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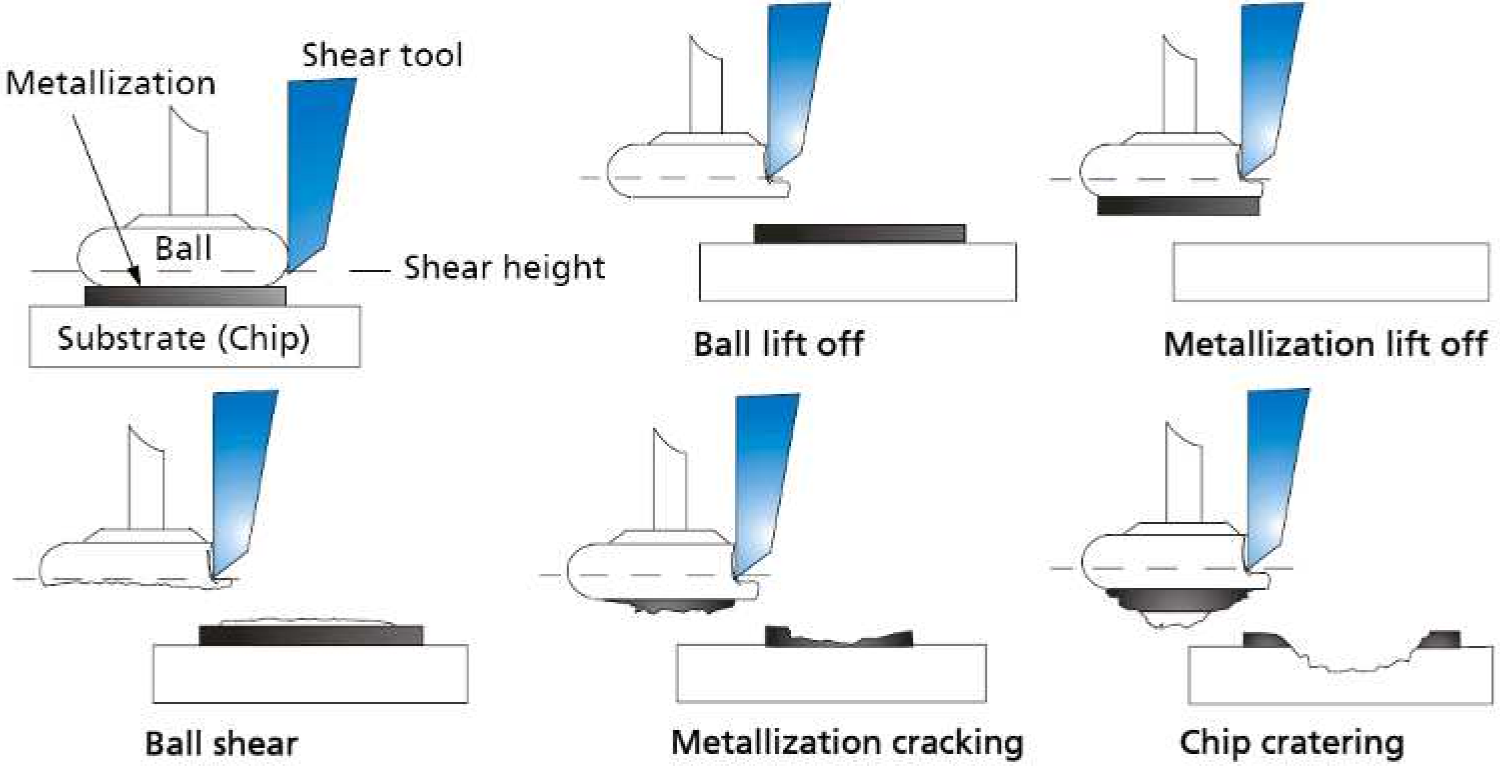
SiP Non-TSV : câblage filaire…bonding shear test



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SiP Non-TSV : câblage filaire…modes de défaillances

Wire Bond Related Failures in COB

Fracture

Electrical Overstress

Metallurgy

Corrosion

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SiP Non-TSV : câblage filaire…équipements de production

35 µm pitch

±2.5 µm accuracy

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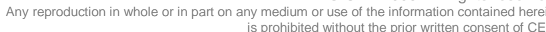
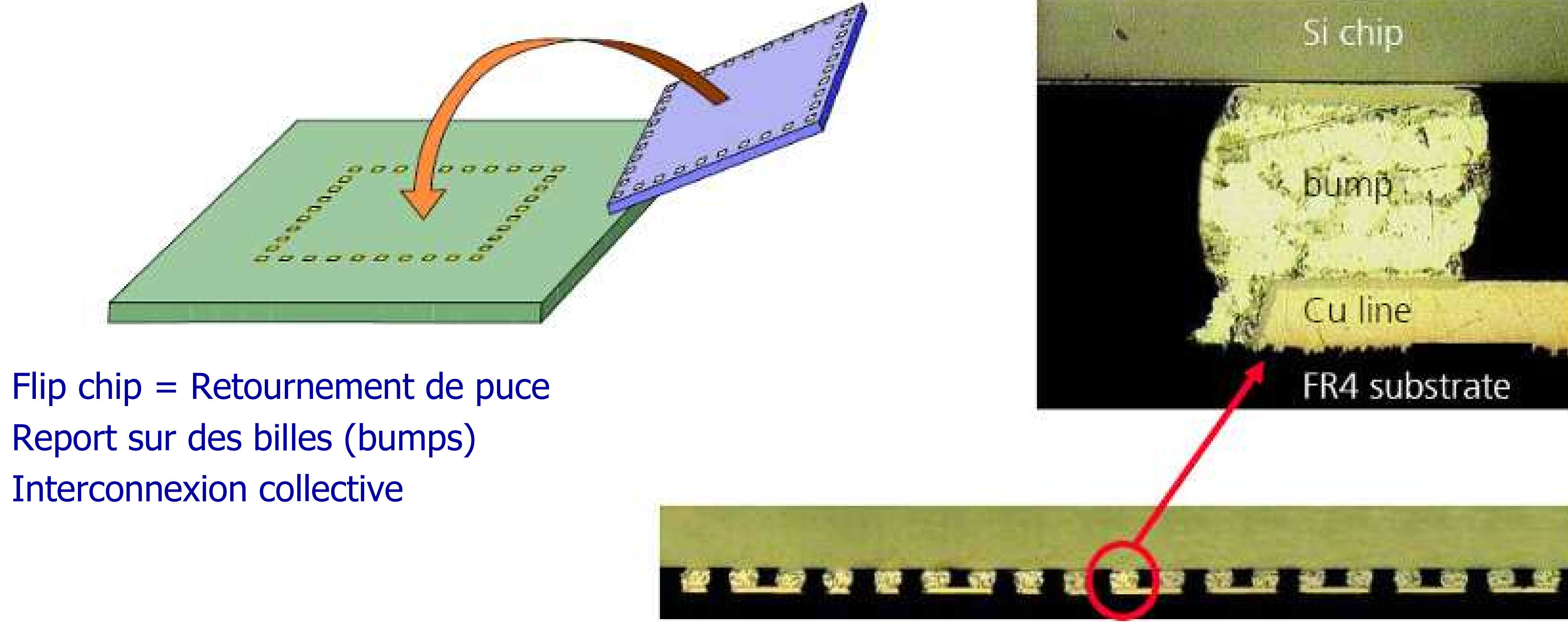


SiP Non-TSV : flip chip bonding



Flip chip = Retournement de puce
Report sur des billes (bumps)
Interconnexion collective

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SiP Non-TSV : flip chip bonding

Flip Chip Technologies

- Welding
  - Thermo Sonic — Au, In
  - Thermo Compression — Au
- Adhesive Joining
  - ICA Isotropic Conduct. — Ni/Au, Au + ICA paste
  - ACA Anisotropic Conduct. — Ni/Au, Au + ACA film paste
  - ACA Anisotropic Conduct. — Au studs +NCA film, paste
- Soldering
  - Thermode Soldering — PbSn
    - Pull Compression — Au+Cu/Sn
  - Reflow Soldering — PbSn, SnAg, AuSn

Underfill required for mechanical stability

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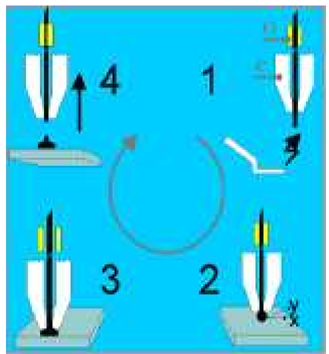
SiP Non-TSV : flip chip bonding…soudage

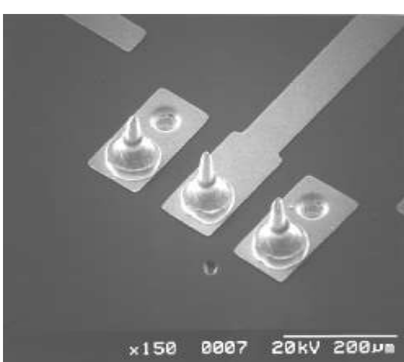
Principle:
- Plastic deformation of the Au surfaces (force)
- Diffusion between the surfaces (temperature) or ultrasonic (soft substrates)

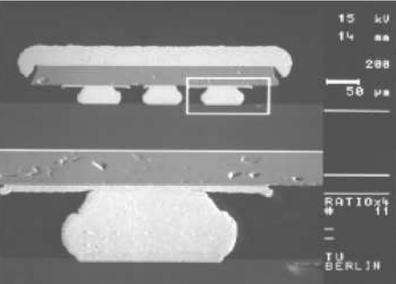
Advantages:
- Maskless process
- Wire bonder
- Very flexible
- Suitable for single chip and Substrates
- Fluxless

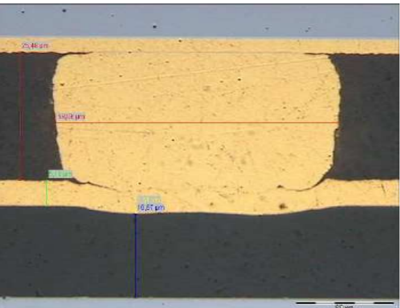
Thermo-compression Bonding
- 60 µm minimal pitch
- Thermal treatment : 250°C or Thermal-sonic

Limitations:
- No self alignment
- Interfacial temperature higher than 200°C
- High pressure on thermal compression can damage sensitive materials (CdZnTe)









Source: FhG - IZM

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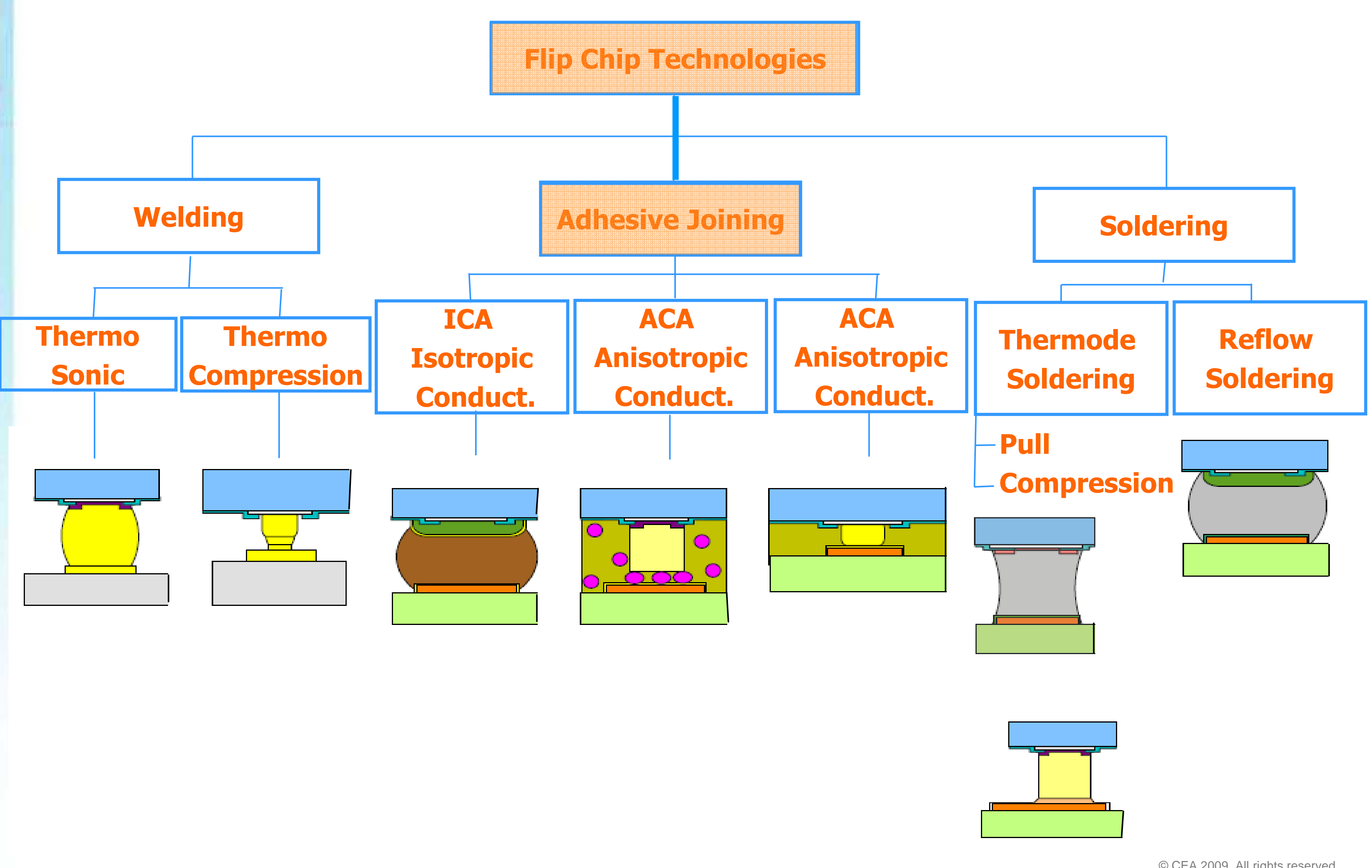
SiP Non-TSV : flip chip bonding



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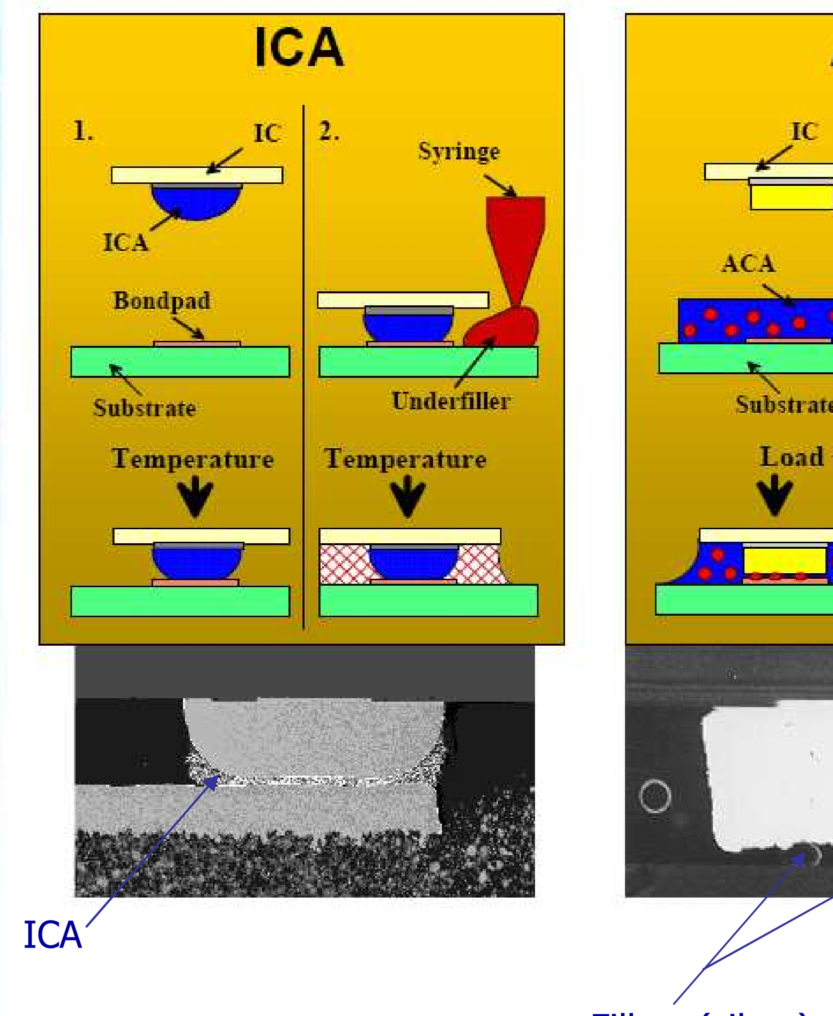
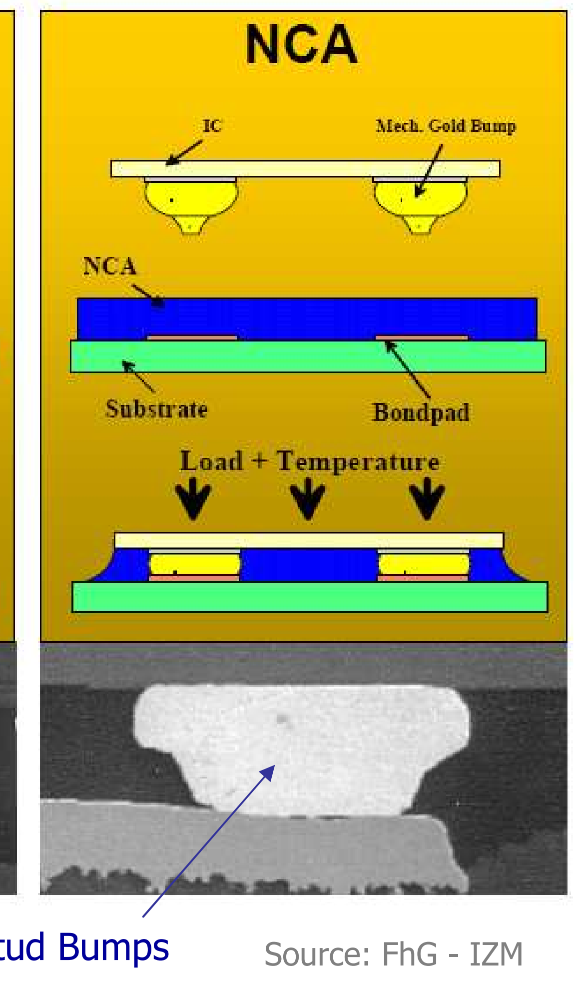
SiP Non-TSV : flip chip bonding…collage





ICA

Fillers (silver)

Stud Bumps

Source: FhG - IZM

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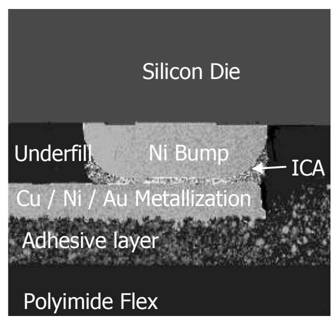
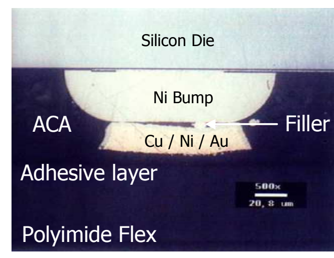
SiP Non-TSV : flip chip bonding…collage



Limitations:
- Substrate: Polyimide, Polyester, FR4
- Pitch: 150µm (flex), 200µm (FR4)
- Metallization: Cu/Ni/Au
- Bumps: Ni/Au, Au

Components: FC, SMD
Curing: down to 5min @ 150°C
Contact resistance: 25 mOhm



Limitations:
- Substrate: Polyimide, FR4, glass
- Pitch: 150µm (flex), 65µm (glass)
- Metallization: Cu/Ni/Au, Mo, ITO/Au
- Bumps: Ni/Au, Au

Components: Flip Chip
Curing: down to 5sec @ 200°C
Contact resistance: 10...15mOhm (flex), 0.2 ...1 Ohm (glass)

Limitations:
- Substrate: Polyimide, FR4
- Pitch: 100µm
- Metallization: Cu/Ni/Au
- Bumps: Au stud

Curing: down to 5sec @ 200°C
Contact resistance: 5...7 mOhm

Source: FhG - IZM

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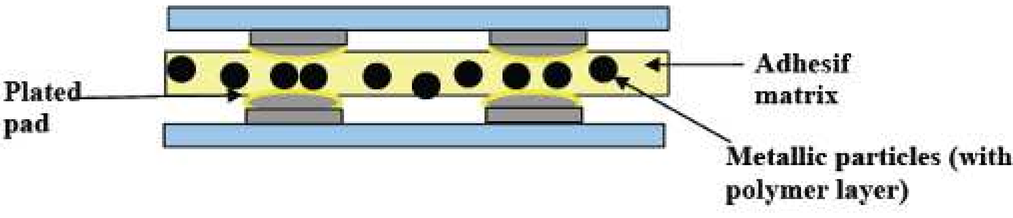
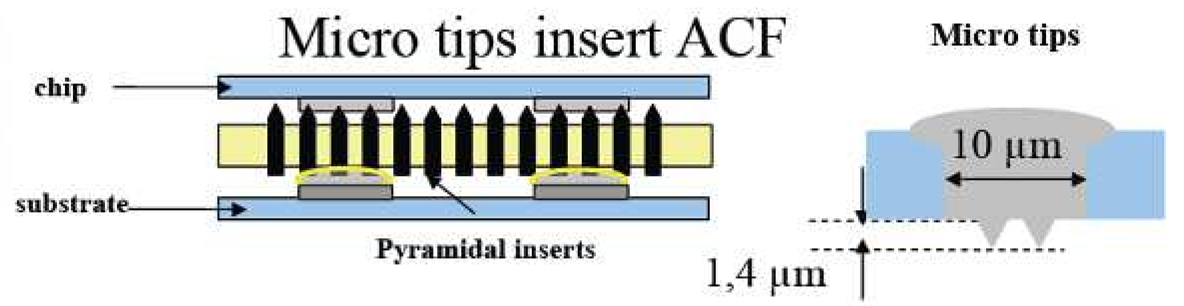
SiP Non-TSV : flip chip bonding…collage

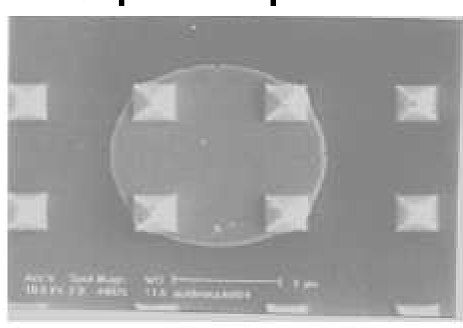
ACF(A) Structurés

5552 R Film 3M



Microtips developed at LETI





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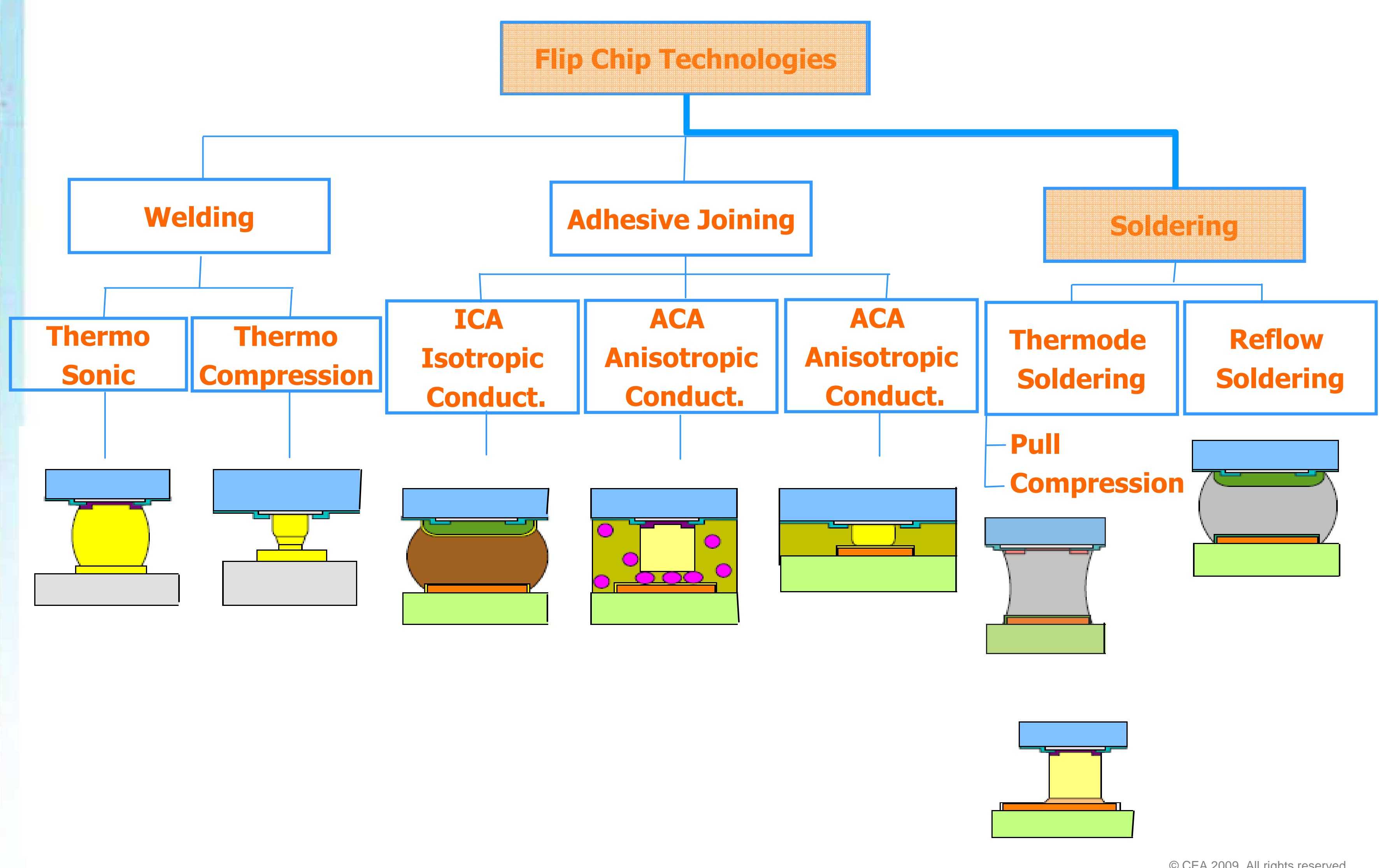
SiP Non-TSV : flip chip bonding



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SiP Non-TSV : flip chip bonding…brasage

Flip Chip BGA Constructions
Numerous Material & Process Options

Adhesion Layer: Ti, TiW, Al, Cr,...

Pad/Thin Film Wiring:
Al/Al, Al/Cu, Cu/Cu,...

Barrier Layer: Ni, Ni(V), CrCu,...

Wetting Layer: Cu, Cu/Au,...

~0.01 cm

Passivation, Repassivation
or Redistribution:
Nitride, Oxide,
Polyimide, BCB,...

Wafer Material: Si, GaAS, SiGe, InP,...

Dielectric:
Oxide,
Silk, Low-k,...

Eutectic, 97/3 PbSn,
95/5 PbSn, 90/10 PbSn,
Au, Sn/Ag, Sn/AgCu,...

Solder

~0.008 cm

Underfill:
Sumitomo,
Hysol,...

Wetting Layer: Au, OSP,...

Solder Mask:
Photosensitive
Polymers,...

Barrier Layer: Ni,...

Solder
Ball

Eutectic
Pb-Free,...

Substrate:
Organic: FR4, BT, FR5, GETEC, Build-Up,...
Ceramic: Alumina, LTCC, Glass Ceramic,...
Semiconductor: Si, GaAs,...
Metal: Cu, Cu/Cr/Mo/Cr/Cu, Cu/Invar/Cu,...

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SiP Non-TSV : flip chip bonding…brasage

Process Steps:

1. ASIC / Chip post process: Under Bump Metallurgy (UBM)
2. Bumping
3. Solder Reflow
4. Flip Chip Bonding
5. Underfilling

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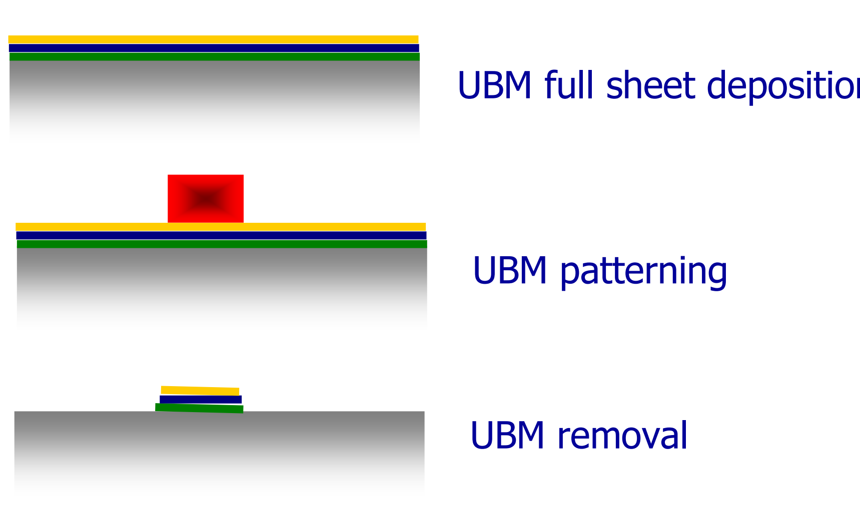
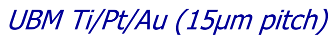
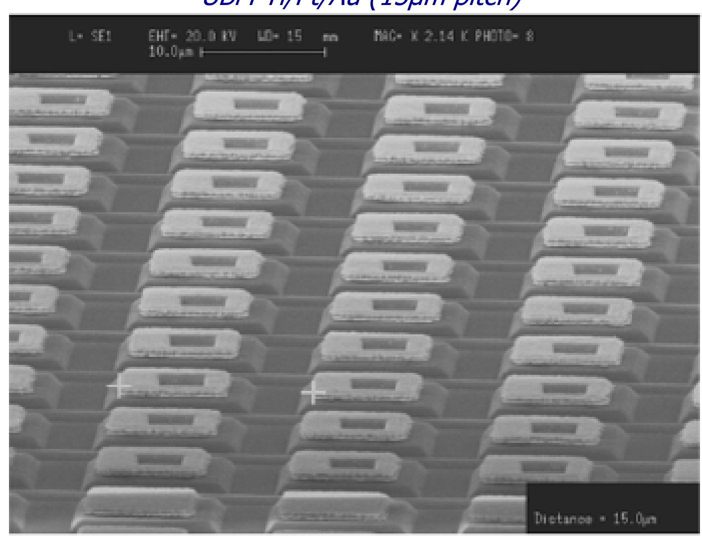
SiP Non-TSV : flip chip bonding…brasage

Under Bump Metallurgy (UBM): PVD







Source: LETI

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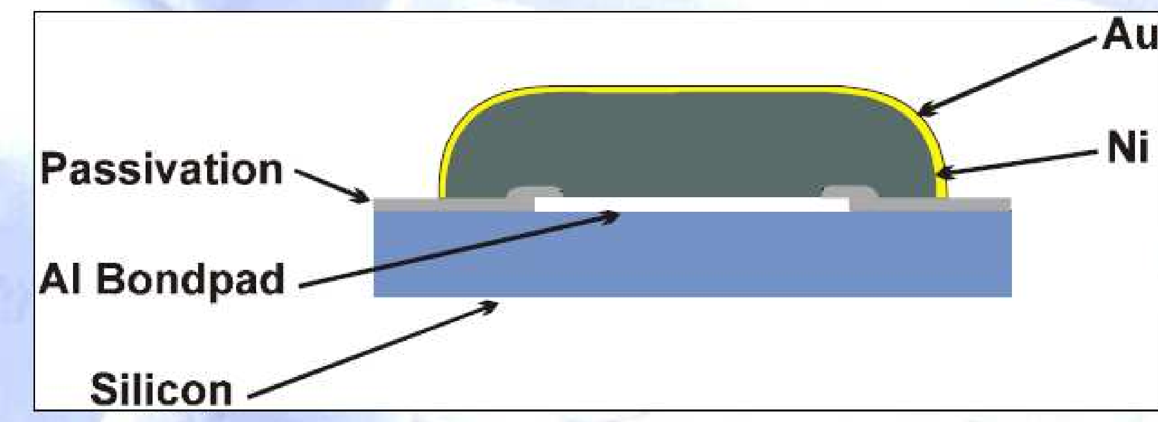
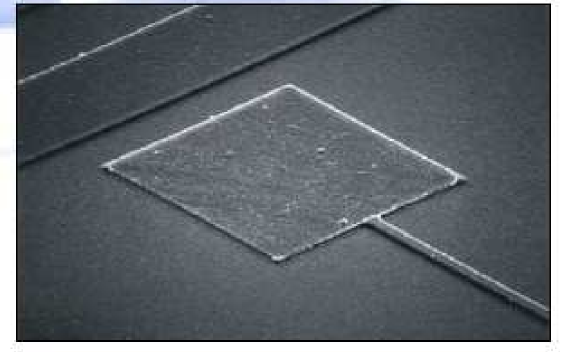
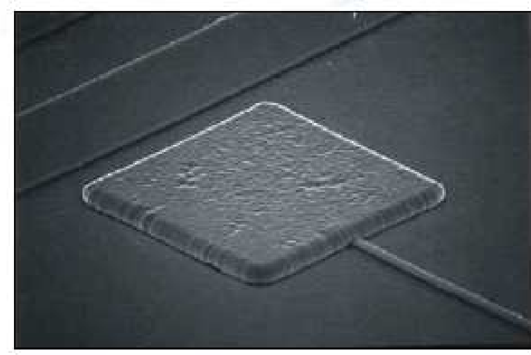
SiP Non-TSV : flip chip bonding…brasage

Under Bump Metallurgy (UBM): Electroless

- Backside Coating
- Pad Cleaning
- Pad Activation
- Electroless Nickel
- Flash Gold
- Coating Removal







1 µm < Ni < 30 µm
Au 0.05 µm

Source PacTech

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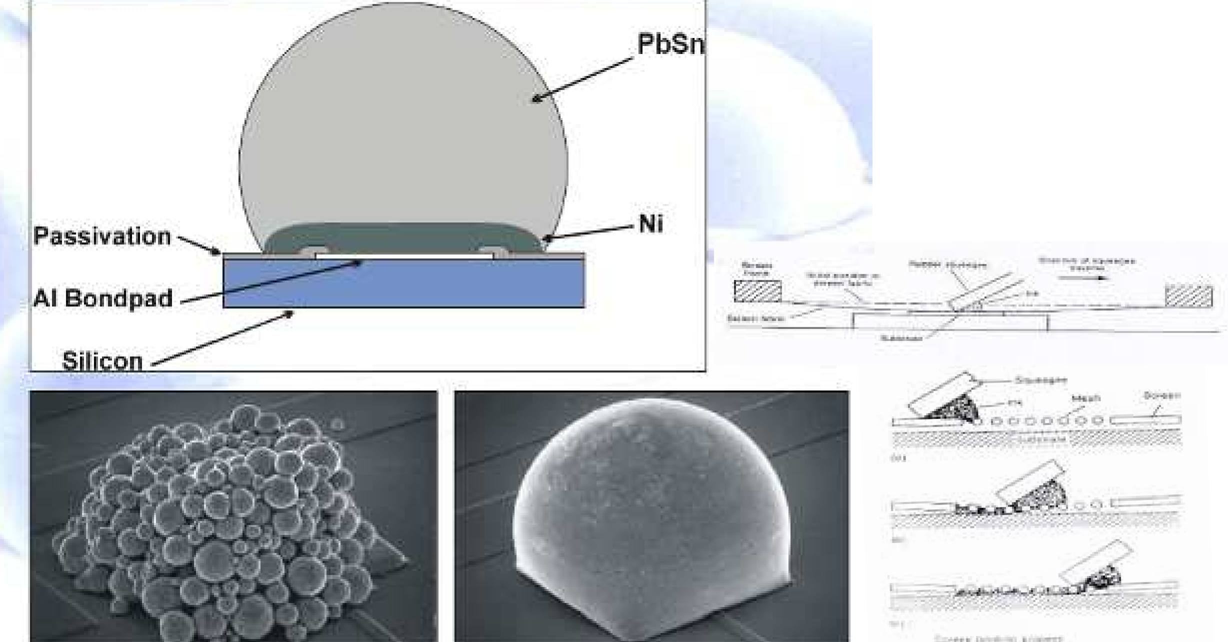
SiP Non-TSV : flip chip bonding…brasage

Bumping & Reflow: Stencil Printing



Source PacTech

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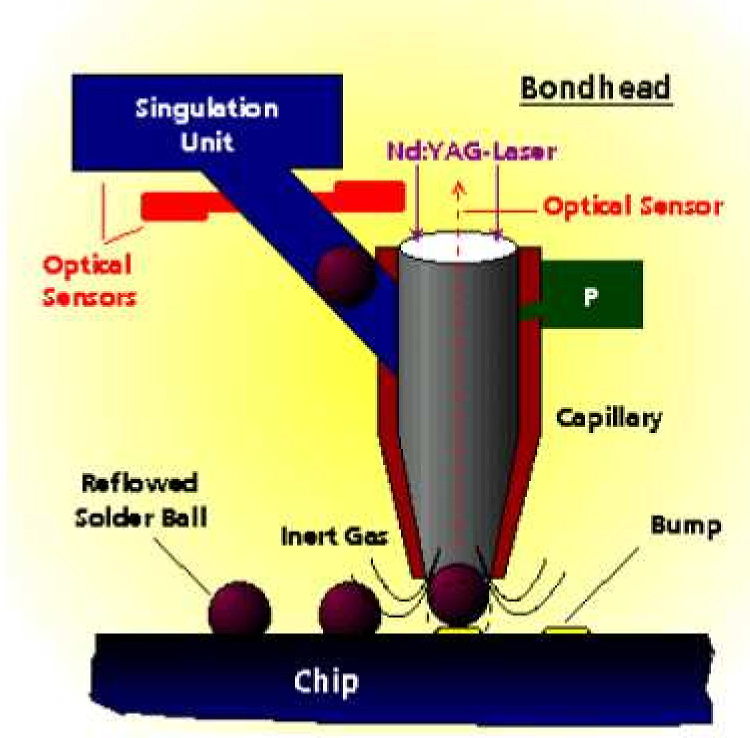
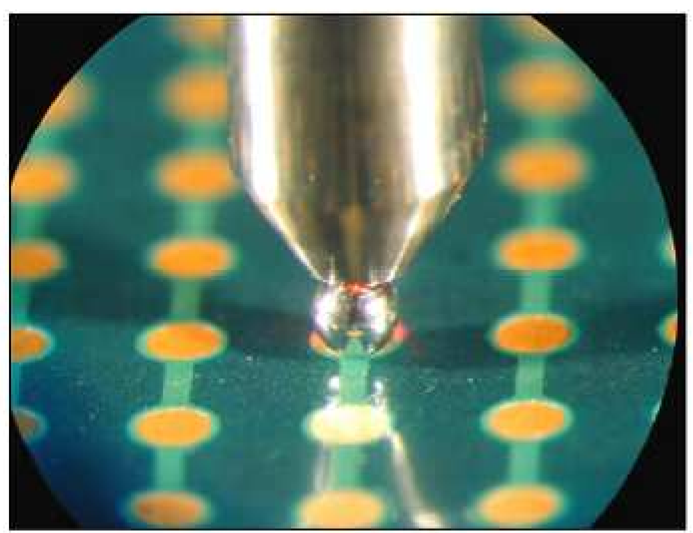
SiP Non-TSV : flip chip bonding…brasage

Bumping & Reflow: Jet Printing



Placement & Reflow of Solder Balls



Source PacTech

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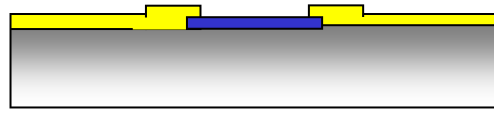
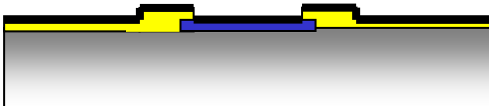
SiP Non-TSV : flip chip bonding…brasage

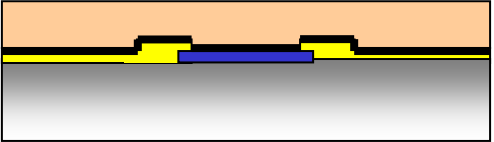
Bumping & Reflow: Electroplating



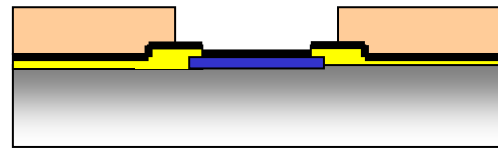
Step 1 :
Via Opening



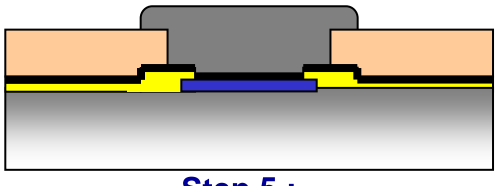
Step 2 :
UBM deposition (PVD)



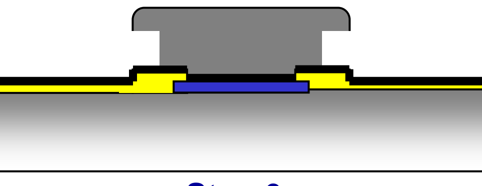
Step 3 :
Photoresist spin coating



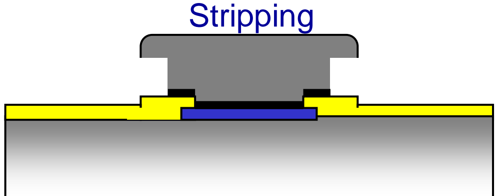
Step 4 :
Patterning



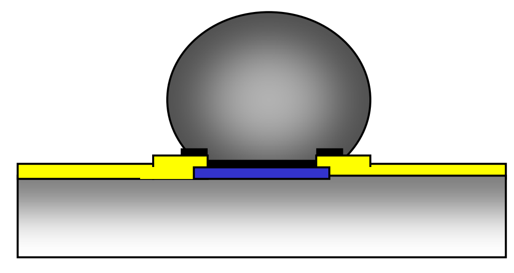
Step 5 :
Solder electroplating



Step 6 :
Stripping



Step 7 :
UBM removal



Step 8 :
Solder reflow

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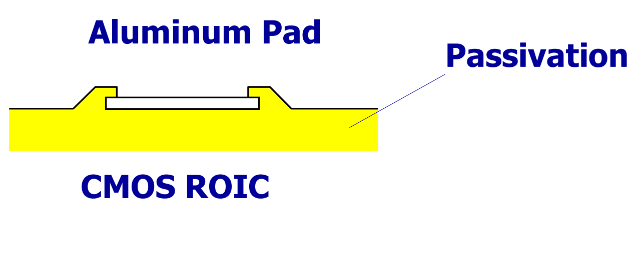
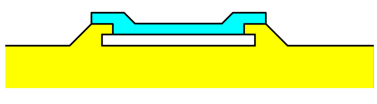
SiP Non-TSV : flip chip bonding…brasage

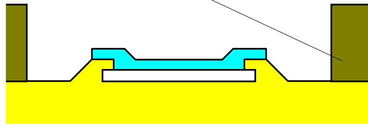
Bumping & Reflow: Lift Off



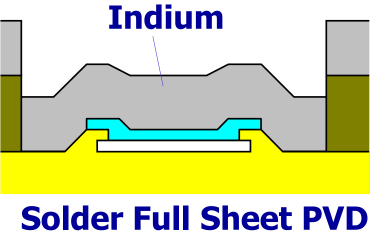


UBM (PVD Patterning)

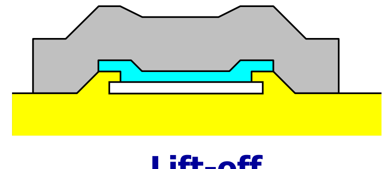
Photoresist



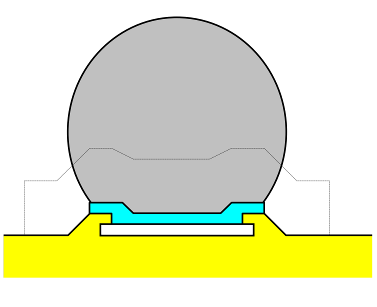
Patterning



Solder Full Sheet PVD



Lift-off



Reflow

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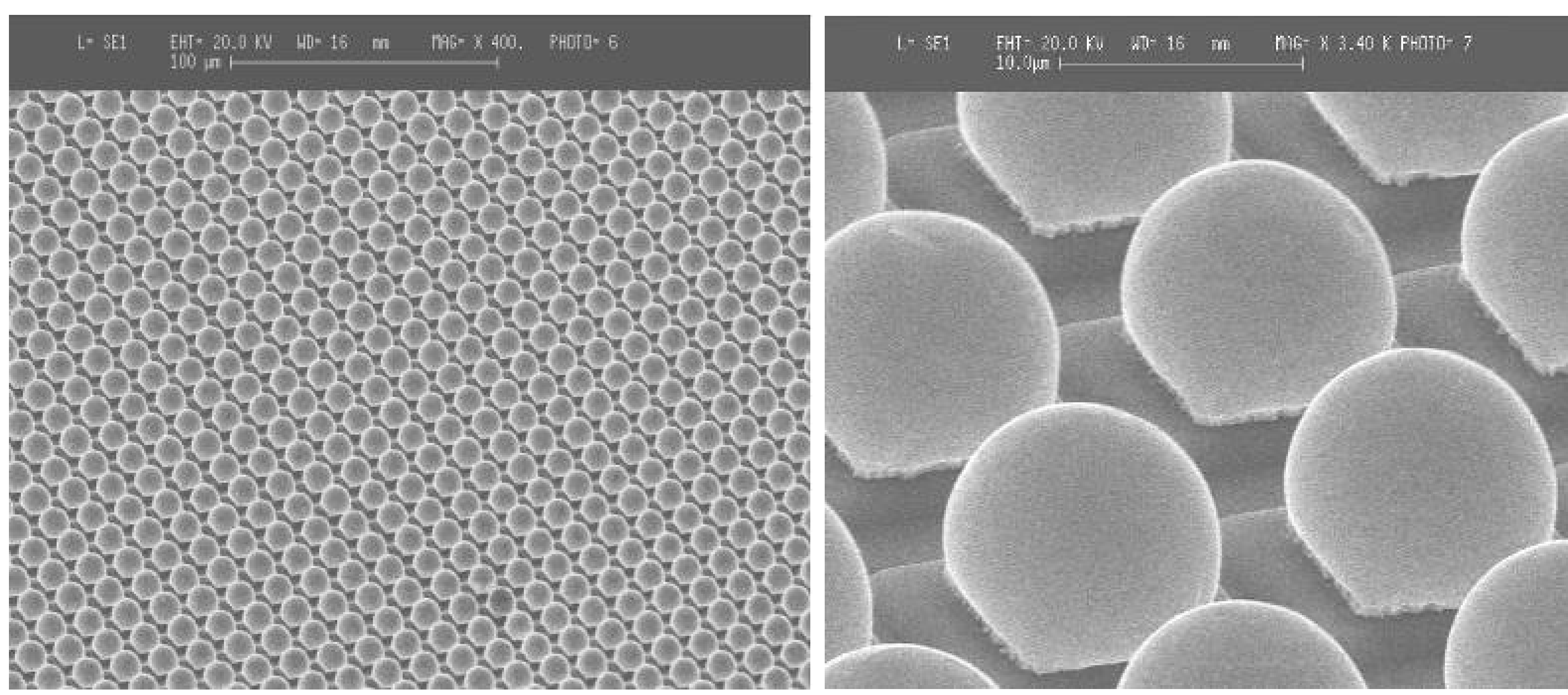
SiP Non-TSV : flip chip bonding…brasage

Bumping & Reflow: Lift Off

Fine pitch 15 µm indium micro-bumping (Leti)



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SiP Non-TSV : flip chip bonding…brasage

Bumping & Reflow: Process

	Pros	Cons	Size
Evaporation	Thin film process Uniformity Flexibility	Cost Time	10 – 100 µm
Electroplating	Low cost Fine pitch	Flexibility	10 – 200 µm
Stencil Printing	Cost Simplicity Production	Pitch limitation	150 – 1000 µm
Jet Printing	Limited number of bumps No mask	Pitch limitation	> 150 µm

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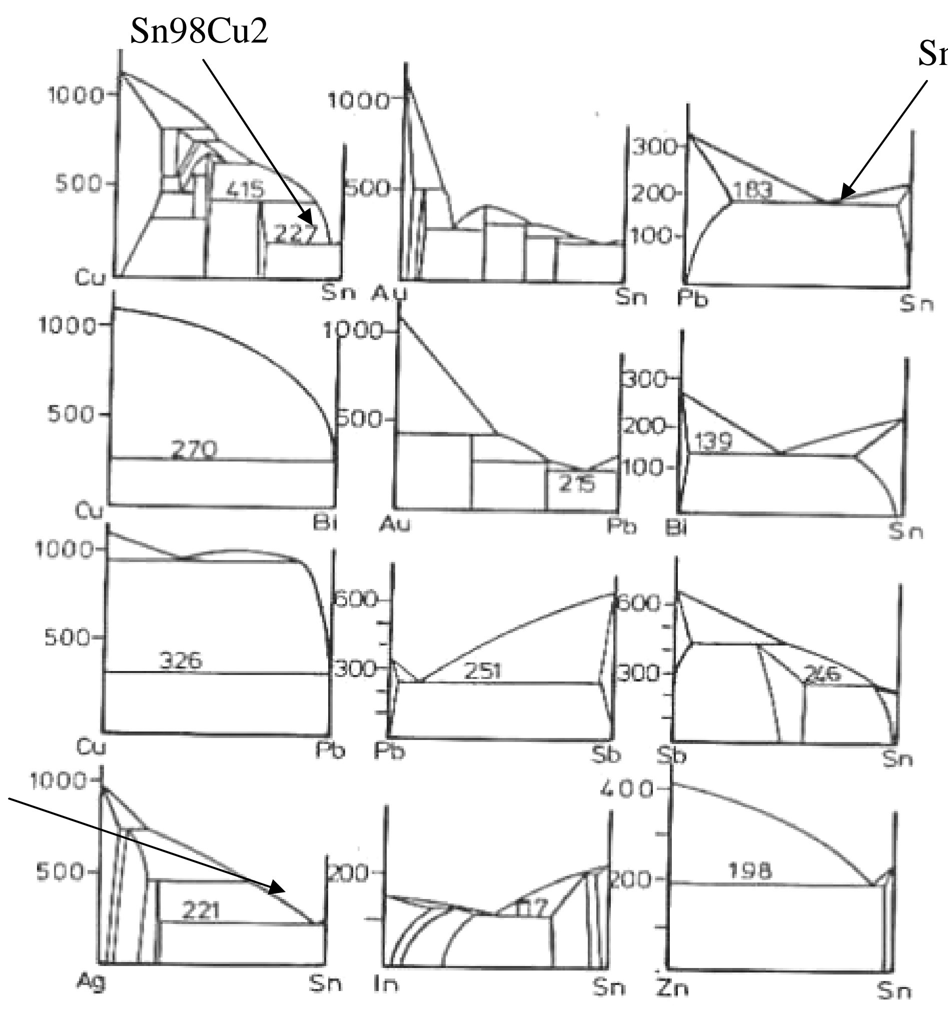
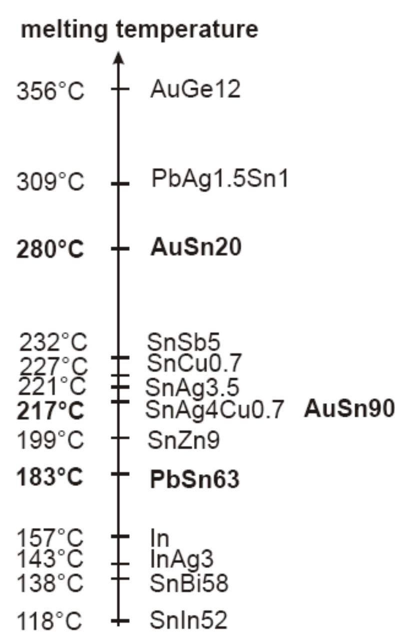
SiP Non-TSV : flip chip bonding…brasage

Bumping & Reflow: Alloys





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SiP Non-TSV : flip chip bonding…brasage

Bumping & Reflow: Lead Free Requirements

Pure Sn : « whiskers », electromigration

Alternatives :

Sn-based alloys with Ag, Cu, Bi, Zn

Ag, Zn lower melting point, good mechanical properties
Cu lower dissolution of UBM
Bi wettability

Requirements :

Melting point close to SnPb (183°C)
Good wetting properties with conventional UBM (Cu, Ni/Al, Sn,…)
Controlled growing of intermetallic compounds (IMC) with good mechanical

Properties:

Good thermo-mechanical properties

Sn preferred (low cost, good knowledge, stable IMC)

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SiP Non-TSV : flip chip bonding…brasage

Bumping & Reflow

Alloys	Melting Point (°C)	Cost versus Sn63/Pb37	
		Volume	Weight
96.3Sn/3.2Ag/0.5Cu	217 – 218	1.9	2.3
96.5Sn/3.5Ag	221	2.0	2.3
98Sn/2Ag	221 – 226	1.6	2.0
99.3Sn/0.7Cu	227	1.2	1.5
95Sn/5Sb	232 – 240	1.2	1.4
98Sn/1Cu/1Sb	env. 240	1.2	1.4

Source R.Tummala [1]

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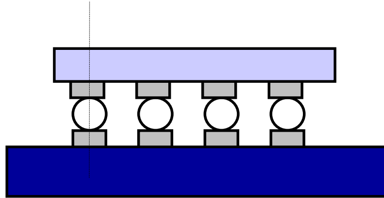
SiP Non-TSV : flip chip bonding…brasage

Flip Chip Bonding

FC150 SET equipment issued by Leti

X
Y
Alignment microscope



Step 1:
Alignment

Step 2:
Positioning

Step 3:
Self alignment - Sodering

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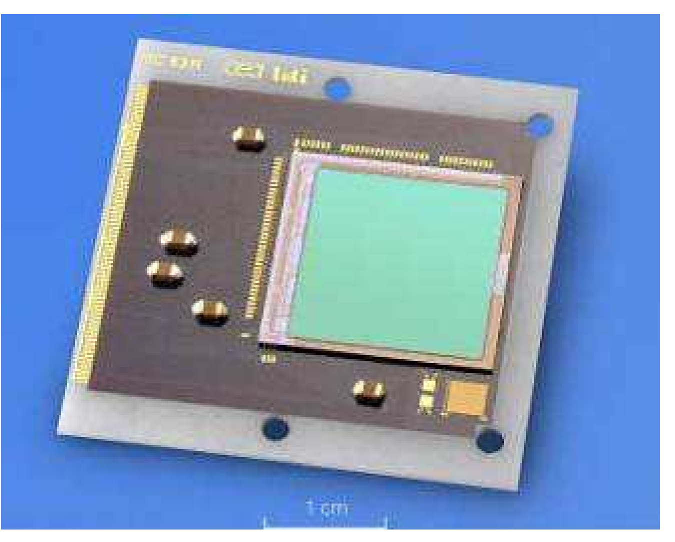
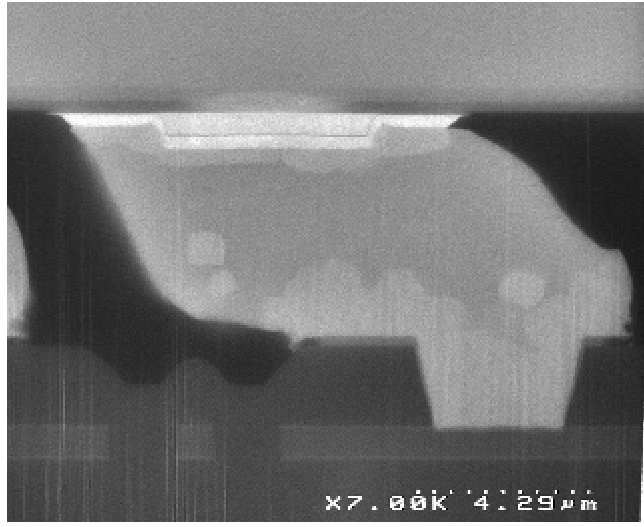
SiP Non-TSV : flip chip bonding…brasage

Flip Chip Bonding





Megapixel 1024 x 1024 15 µm pitch Infrared Detector Array
Indium Bump Cross Sectional View (LETI)

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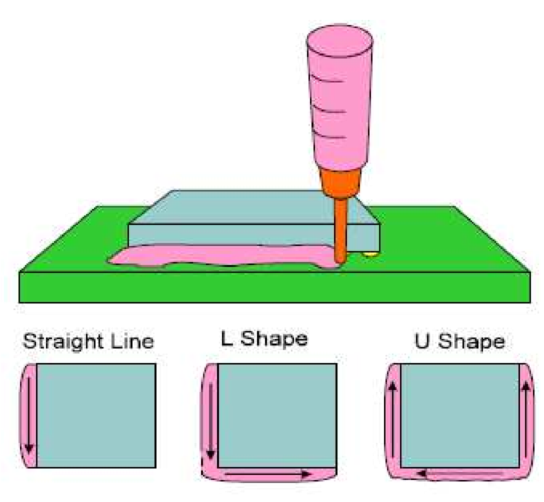
SiP Non-TSV : flip chip bonding…brasage

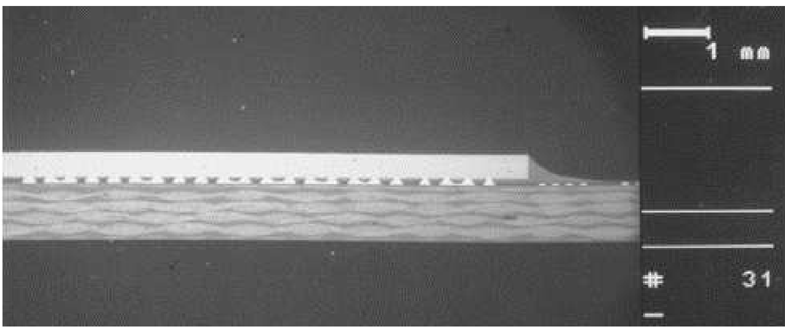
Underfilling

Encapsulation Provides Improved Properties by

- Mechanical Protection of the Die and Interconnections
- Protection Against Ingress of Humidity and Corrosive Media
- Compensation for Thermal Mismatch Between Chip and Substrate



Underfill application



Source FhG IZM

Chip Cross Sectional View

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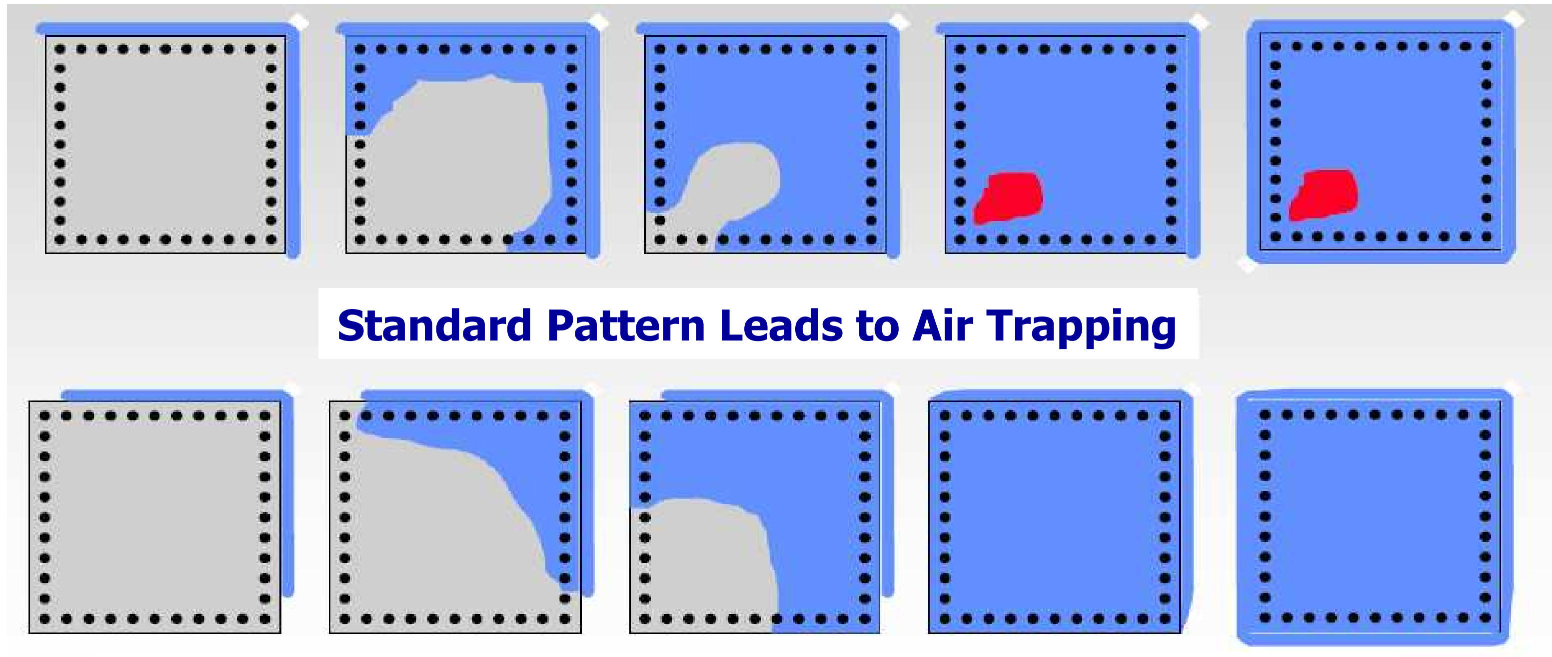
SiP Non-TSV : flip chip bonding…brasage

Underfilling



Optimized pattern results in a Reliable Underfilling Process

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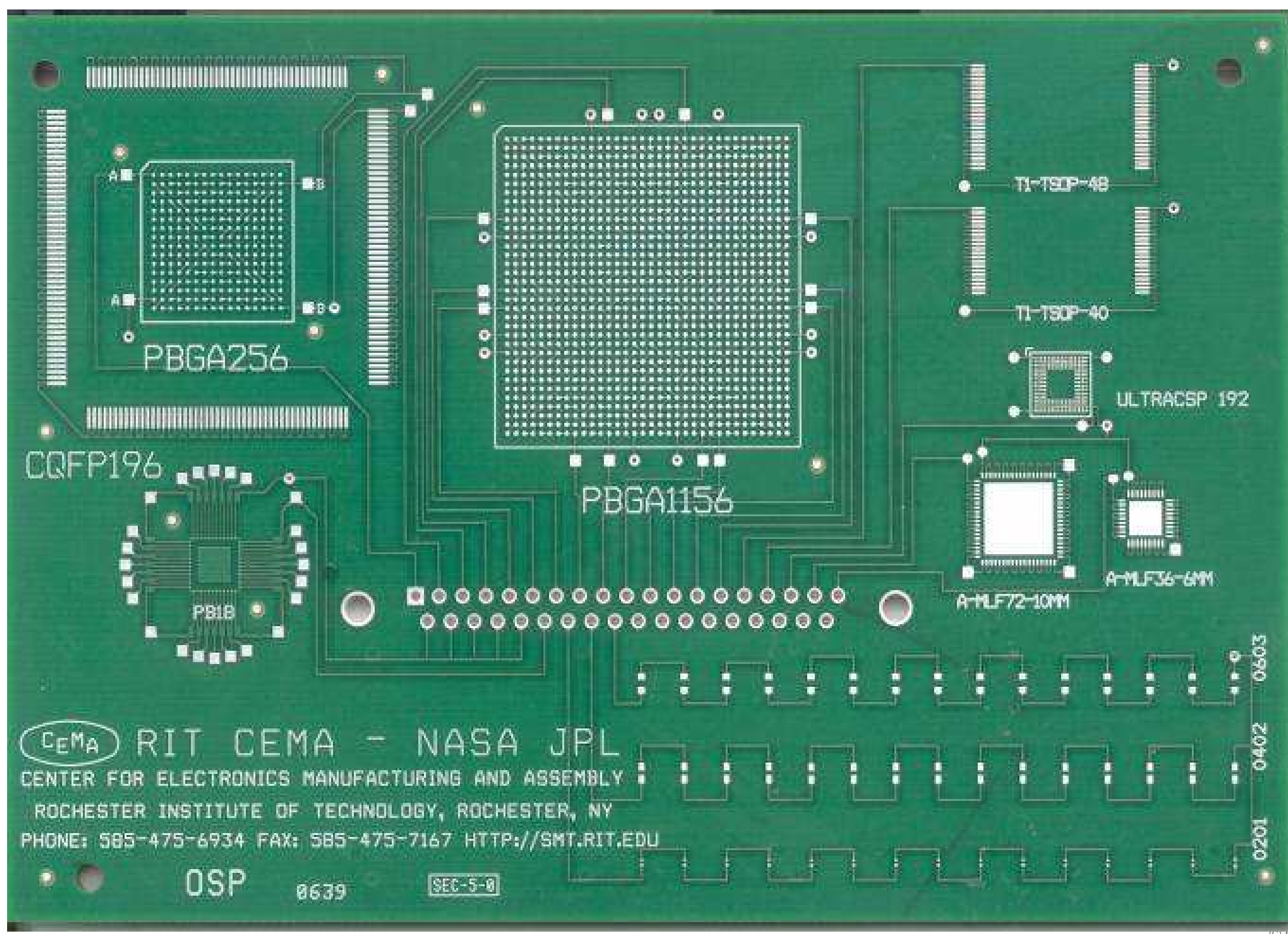
SiP Non-TSV : flip chip bonding…les verrous

Low pitch / High Ios / RoHS



Source NASA JPL

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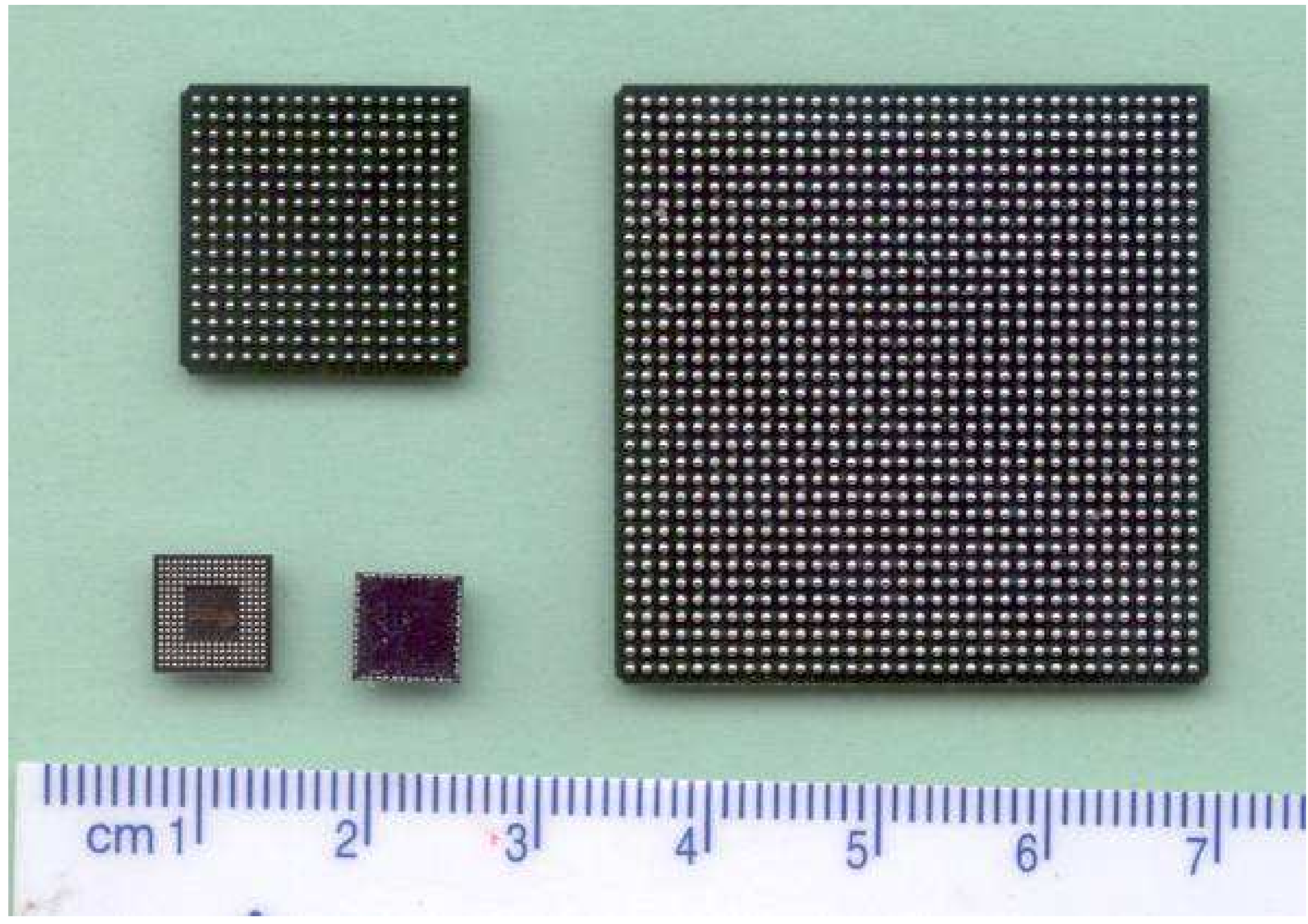
SiP Non-TSV : flip chip bonding…les verrous

Low pitch / High Ios / RoHS



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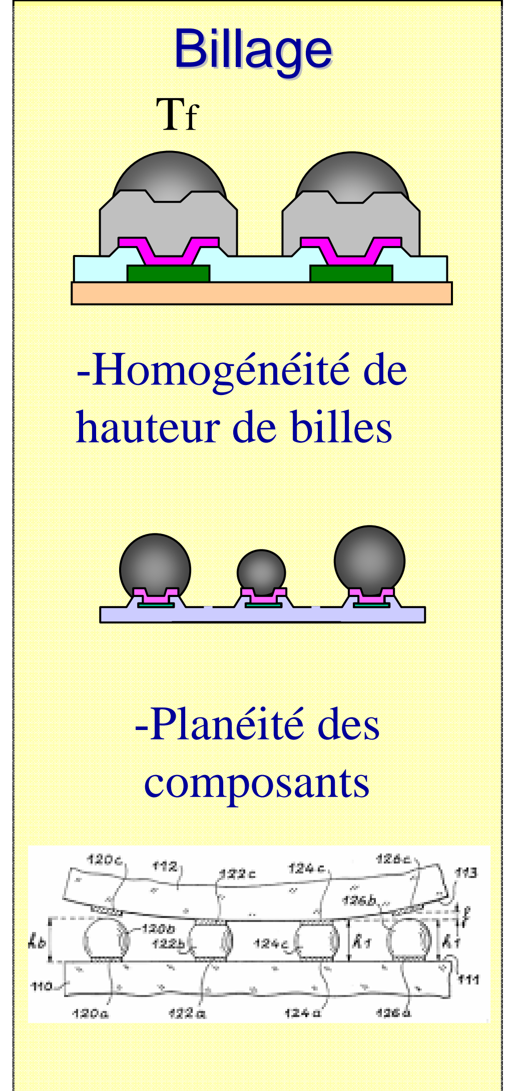
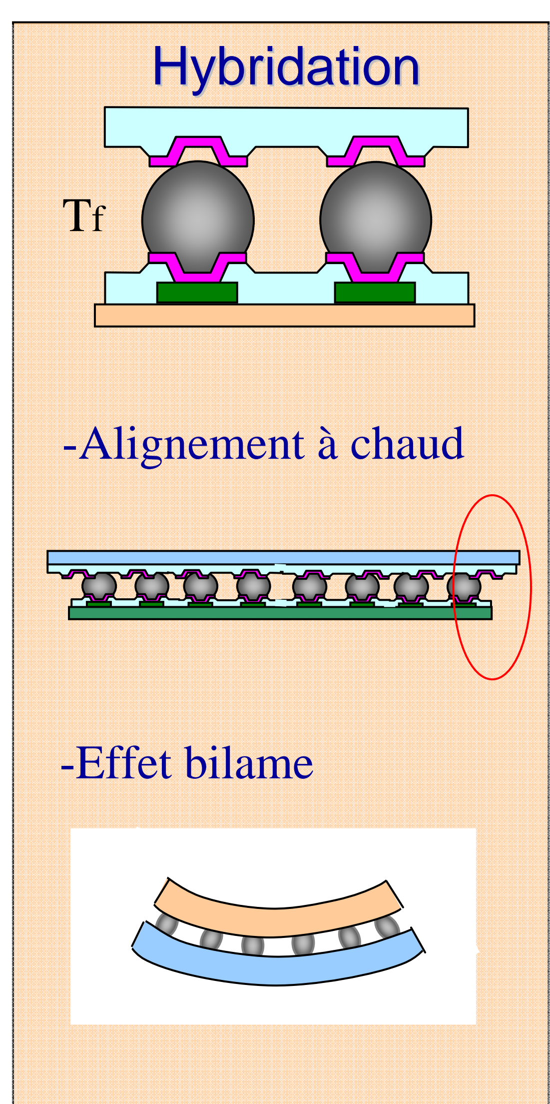
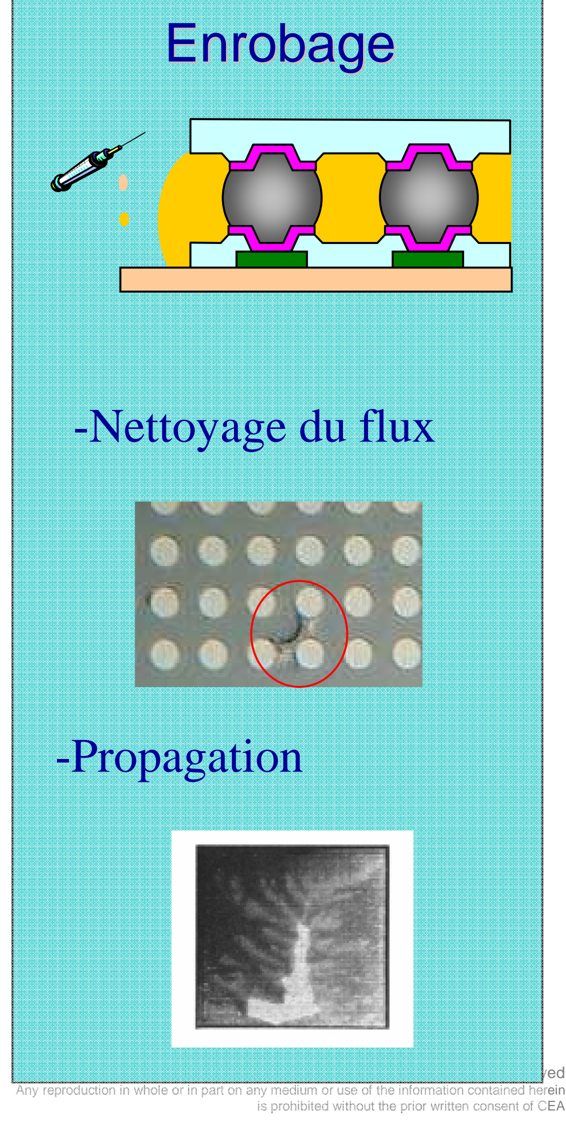
SiP Non-TSV : flip chip bonding…les verrous







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SiP Non-TSV : flip chip bonding…comparaison technique

	Dispense and Process	Pitch	Contact Resistance	Assembly and Temperature	Reliability	Cost
Solder FC	Stencil Printing, Electroplating, Vapour deposition, Jetting, Post Process required	150 µm, 15µm and below	1.2 mΩ	Depends on solder Reliable low temperature solder: In Self Alignment Cleaning required	Reliable with under filling Reworking	Depends on solder Expensive In
Stud Bump FC	Standard wire bonding equipment, No Post Process	60 µm	5 – 10 mΩ	Over 200ºC Pressure applied (50 – 100 g/bump) No self alignment No cleaning	Reliable No Reworking	40$ / wafer with 250000 bumps / wafer (flipchips.com)
Polymer FC	Stencil Printing dispensing, Post Process required	125 µm	50 mΩ (with 10 particles / pads)	Below 100ºC No self alignment No cleaning	Limited reliability for dense connection No Reworking	Low Cost
ACF	Commercially available films, Post Process required	50 µm		100 ºC Pressure applied (15 – 30 kg/cm²) No self alignment No cleaning	Limited reliability for dense connection No Reworking	Low Cost

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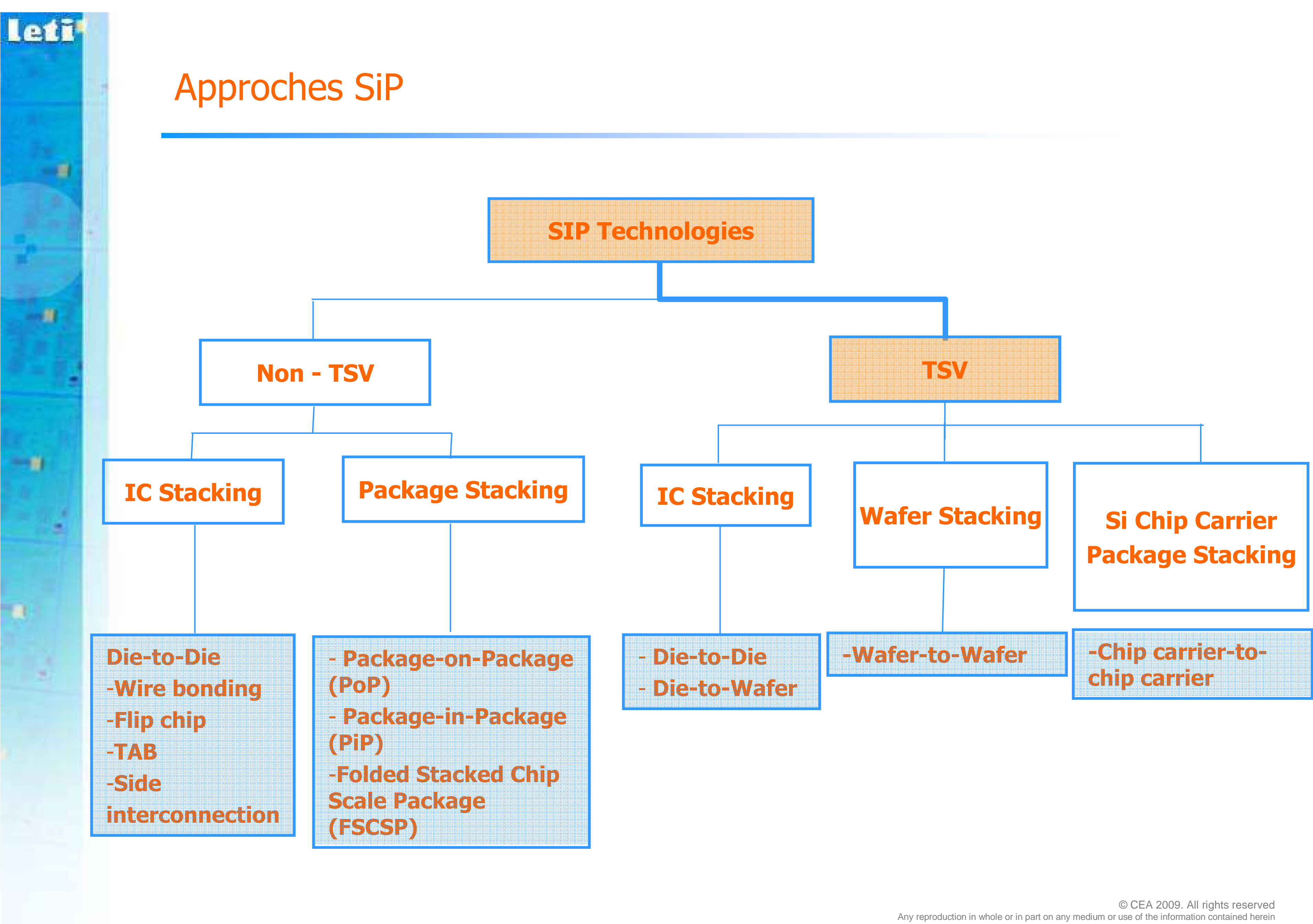
Approches SiP



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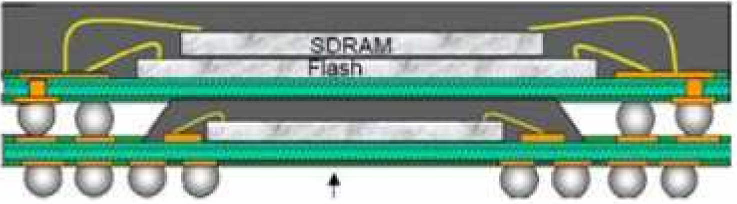
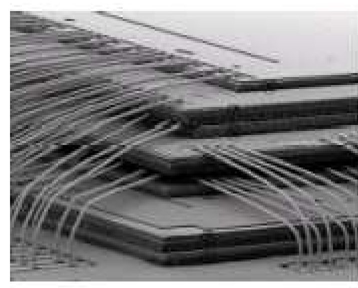
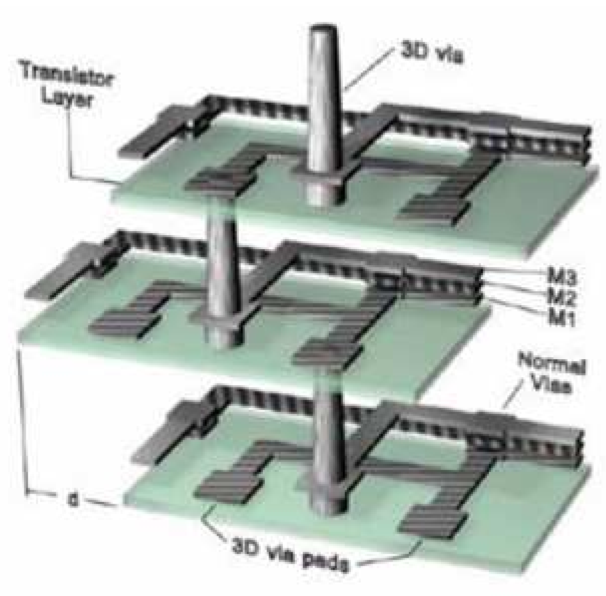
Approche SiP via TSV







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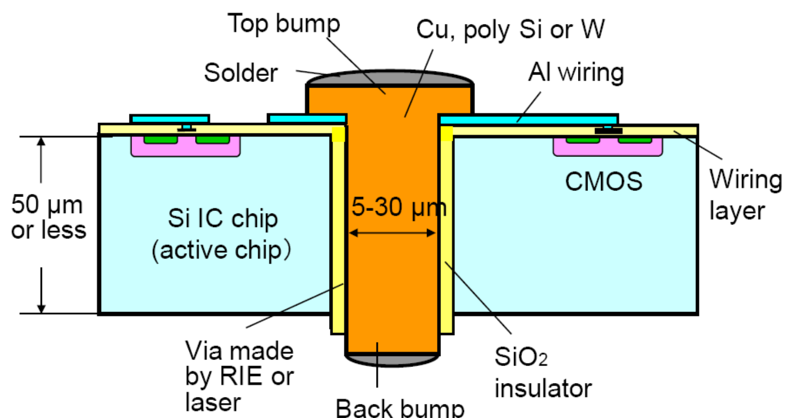
Procédés TSV

Perçage Vias	Remplissage Vias	Assemblage Chip / Wafer		Amincissement
		Puce / Puce	Puce / Wafer	
Technologies				
• Perçage laser • Gravure sèche DRIE • Gravure humide	• Electrolyse • Dépôt CVD • Photolithographie	• Adhérence moléculaire • Scellement métal-métal • Alignement de puces	• Adhérence moléculaire • Scellement métal-métal • Alignement de wafers	• Rodage • Amincissement mécano-chimique • Gravure humide • Gravure sèche



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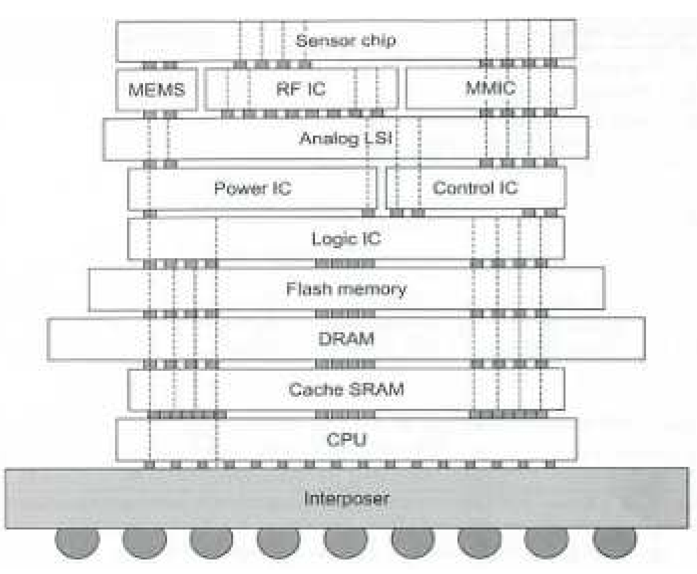
Technologie TSV vs Wirebonding

Heterogeneous integration by 3D TSV technology (Zycube)



Characteristics	TSV	Wire bonding
Interconnection arrangement	Interconnections can be array or peripheral	Only peripheral interconnect
Interconnection length	Shorter interconnections	Much longer interconnect length
Electrical parasitics	Much lower electrical parasitics	Higher parasitics
I/O density	Potentially high density achievable	Lower I/O density
Reliability	Higher reliability	Less reliable
Processing	IC fabrication process	Packaging process

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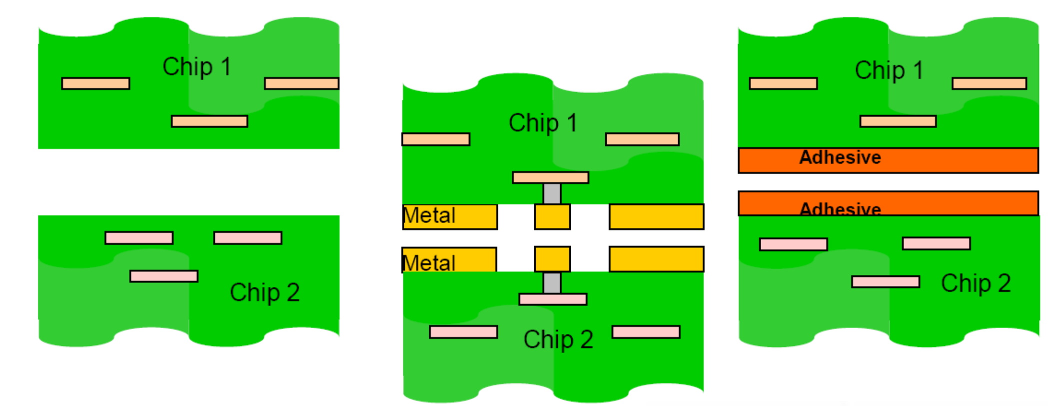
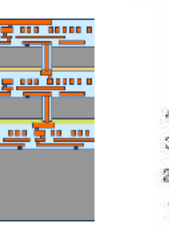
Procédés d'assemblage

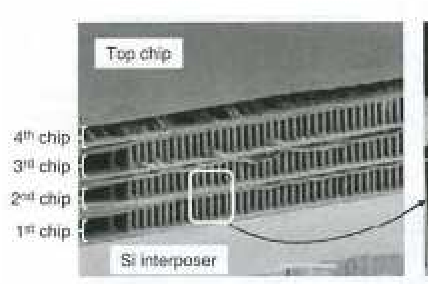


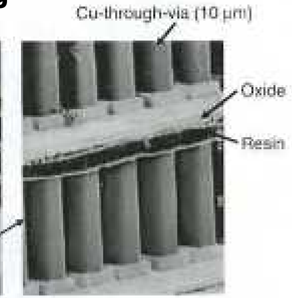
Oxide Fusion Bonding / Metal Metal Bonding / Polymer Adhesive Bonding

Via drilling/filling *Thinning* *Bonding*

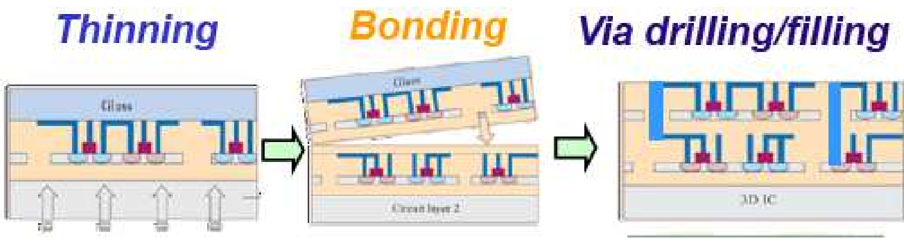


IMEC via first 3D integration

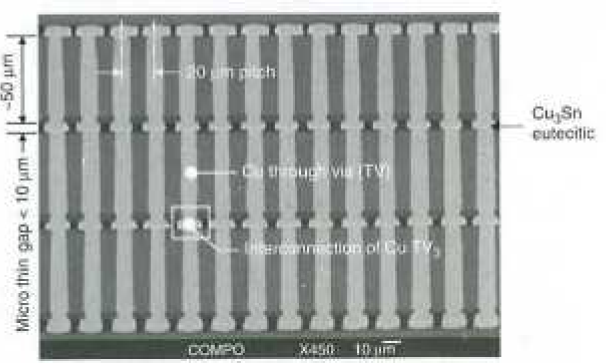




Thinning *Bonding* *Via drilling/filling*

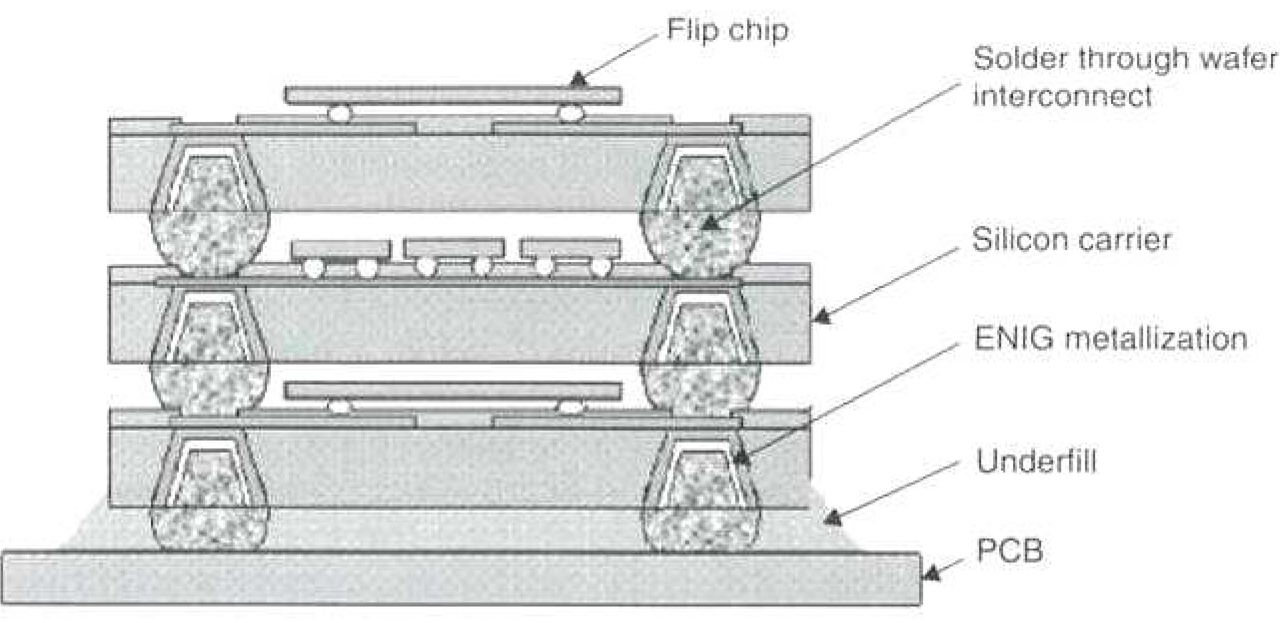


IBM's via last 3D integration



Copper Interchip TSV (ASET)

Configuration avec interposeur



3D stacked Si chip carrier module
(ENIG= Electro less Nickel Immersion Gold)

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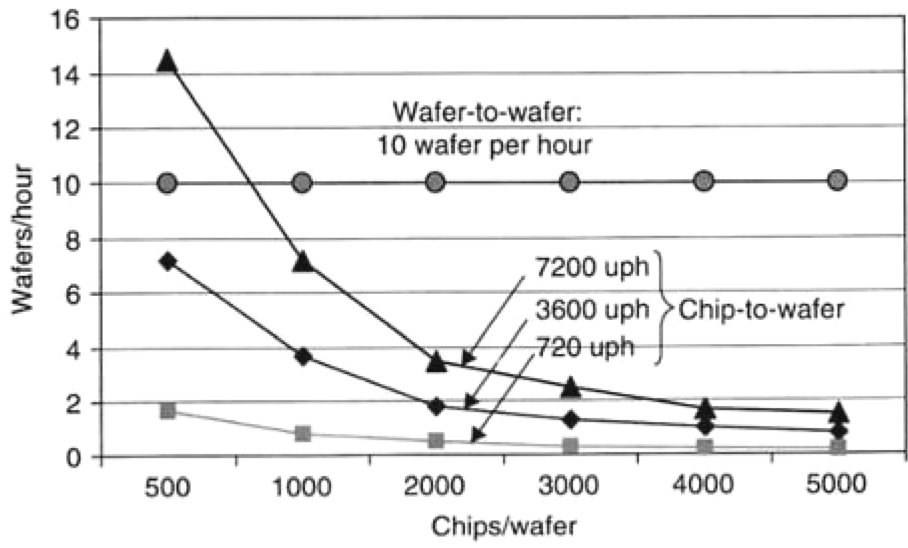
Stratégies d'empilement



A throughput comparison between chip to wafer and wafer to wafer stacking T.Matthias [17]

Die to die stacking	Wafer to wafer stacking
• Different sized dies can be stacked	• Individual die sizes must match
• Alignment is easier	• Alignment is more difficult
• It uses known good die (KGD) for stacking; hence, there is a much higher yield	• There is a lower yield because of KGD issues
• Throughput is lower	• Throughput is higher

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Verrous technologiques du SiP

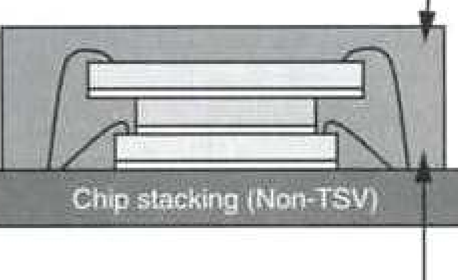
Matériaux et Procédés

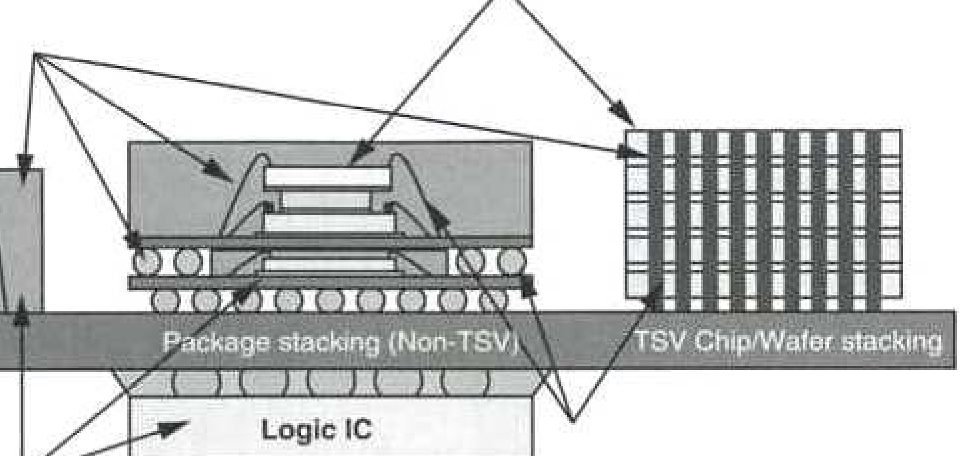
Propriétés électriques
- Constante diélectrique
- Isolation
- Conductibilité électrique

Propriétés mécaniques
- Coefficients de dilatation thermique
- Module d'Young
- Fluage

Propriétés thermiques
- Conductivité thermique

Mécanique
- Puces ultra fines
- Stress lié à l'assemblage
- Surplomb
- Accords de dilatations thermiques
- Ecart au point neutre





Thermique
- Points chauds
- Peu d'espace pour la dissipation thermique
- Faible transfert thermique de puce à puce (colles)
- Resistances thermiques importantes (interconnections)
- Positionnement échangeur thermique
- Design thermique

Electrique
- Intégrité du signal
- Inductances parasites
- Interférences électromagnétiques (EMI)
- Compatibilité électromagnétique (EMC)
- Répartition des fonctions

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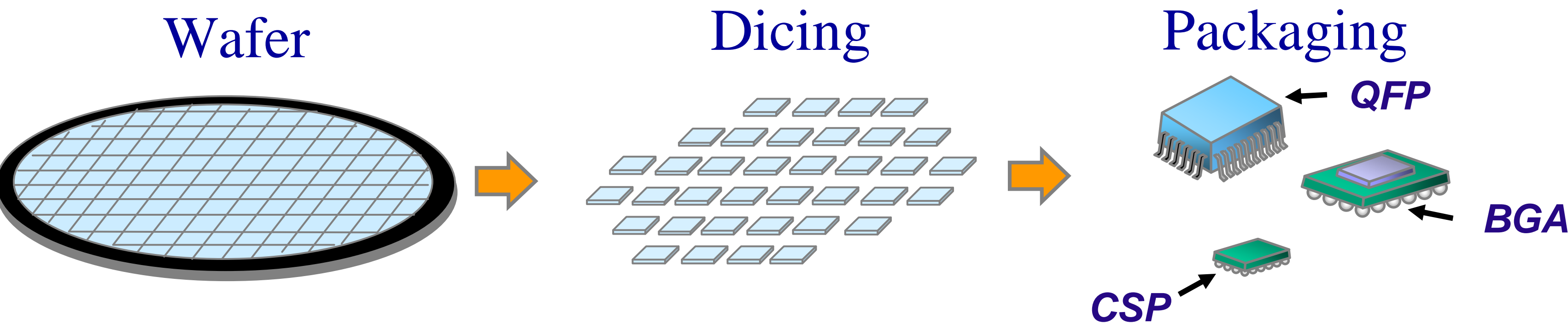
Wafer Level Packaging



Source Fujikura

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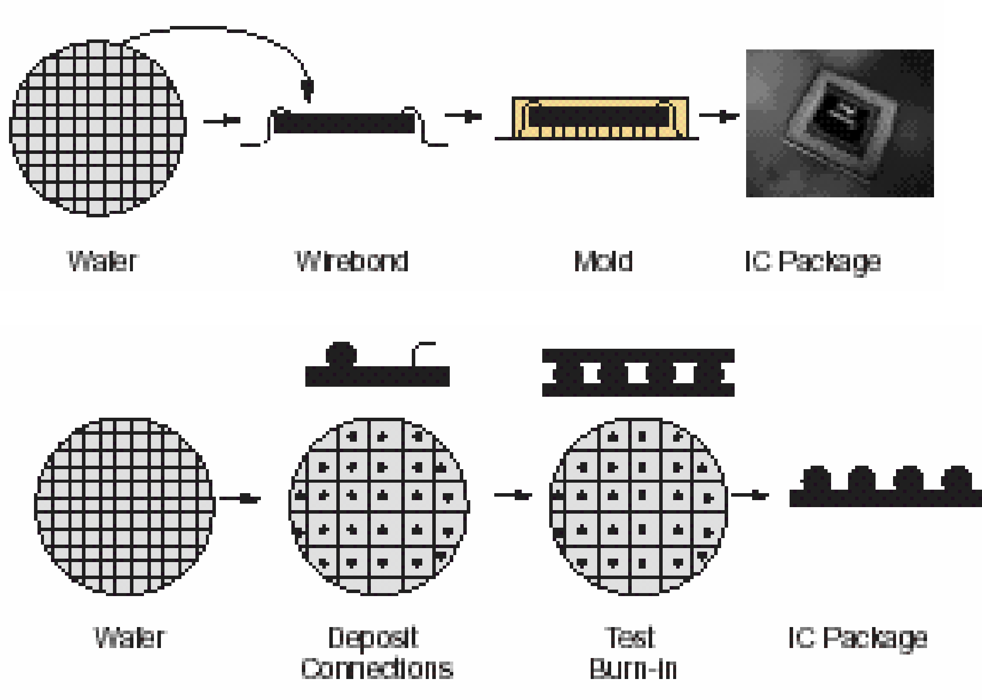
Wafer Level Packaging



WLP is made of technology consisting in device interconnection and protection at the wafer level before dicing

To be defined as WLP, the device must have:
- RDL for electrical redistribution
- Interconnect between chip & board
- Environmental / mechanical protection

WLP Potential:
- 10-50 x size reduction
- 10x cost reduction
- Better electrical performance
- Acceptable mechanical performance

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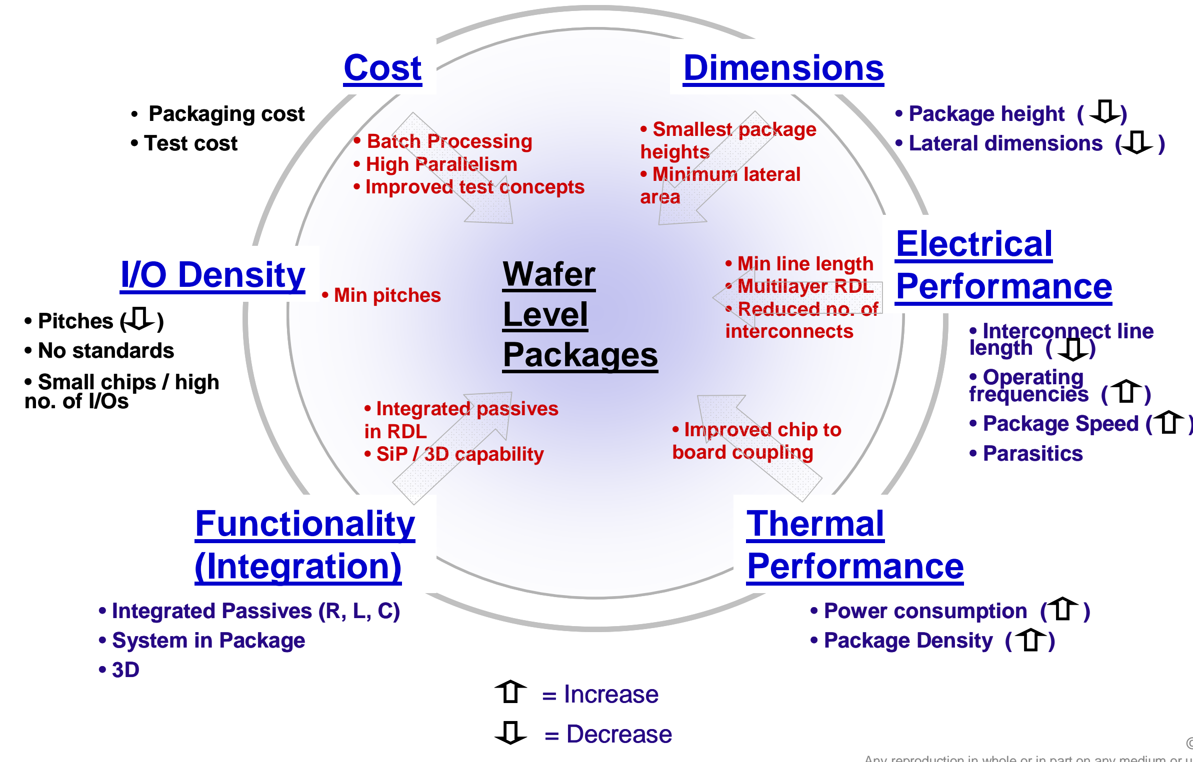
Wafer Level Packaging

WLP is mainly constrained to low IOs (Analog, Passives, RF, Power, Discretes),
→ but trend is to integrate WLP to higher IOs (SRAM/DRAM, ASICS, µP)

Year	2007	2009	2010	2015	2020
Wire bond	30	25	25	20	20
Area array flip chip	120	100	90	80	70
Peripheral flip chip	30	25	20	20	20

ITRS'07 Roadmap for interconnect pitch (µm)



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Epanouissement WLP / Adaptation des pas

Embedded Thin Film Components in the RDL

Processing steps of wafer level redistribution ultra CSP

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leti

Les verrous du WLP

WLP challenges

- Design
  - Minimals interconnection parasitics RLC
  - Small form factor (height)
  - Low stress
  - Minimal current crowding
- Material
  - High electrical counductivity
  - Strength and fatigue resistance
  - Barriers/UBM with designed interfaces
  - Low stiffness for stress relief
- Processes
  - Scalability to submicron pitch (planarity, uniformity, tolerance)
  - Plating controlled compositions
  - Minimal and low cost steps
  - Temperature compatibility
- Assembly and reliability
  - Assembly tools for <1–10 micron pitch
  - Electromigration
  - Thermomigration
  - Thermomechanical reliability

Wafer level interconnect trend

>100 µm pitch — Lead-fee with underfill; Compliant interconnection

50–100 µm pitch — Copper pillar; Bonding layer

1–20 µm pitch — Cu-Cu Bonding

<1 µm pitch — Nano interconnection

Source R.Tummala [1]

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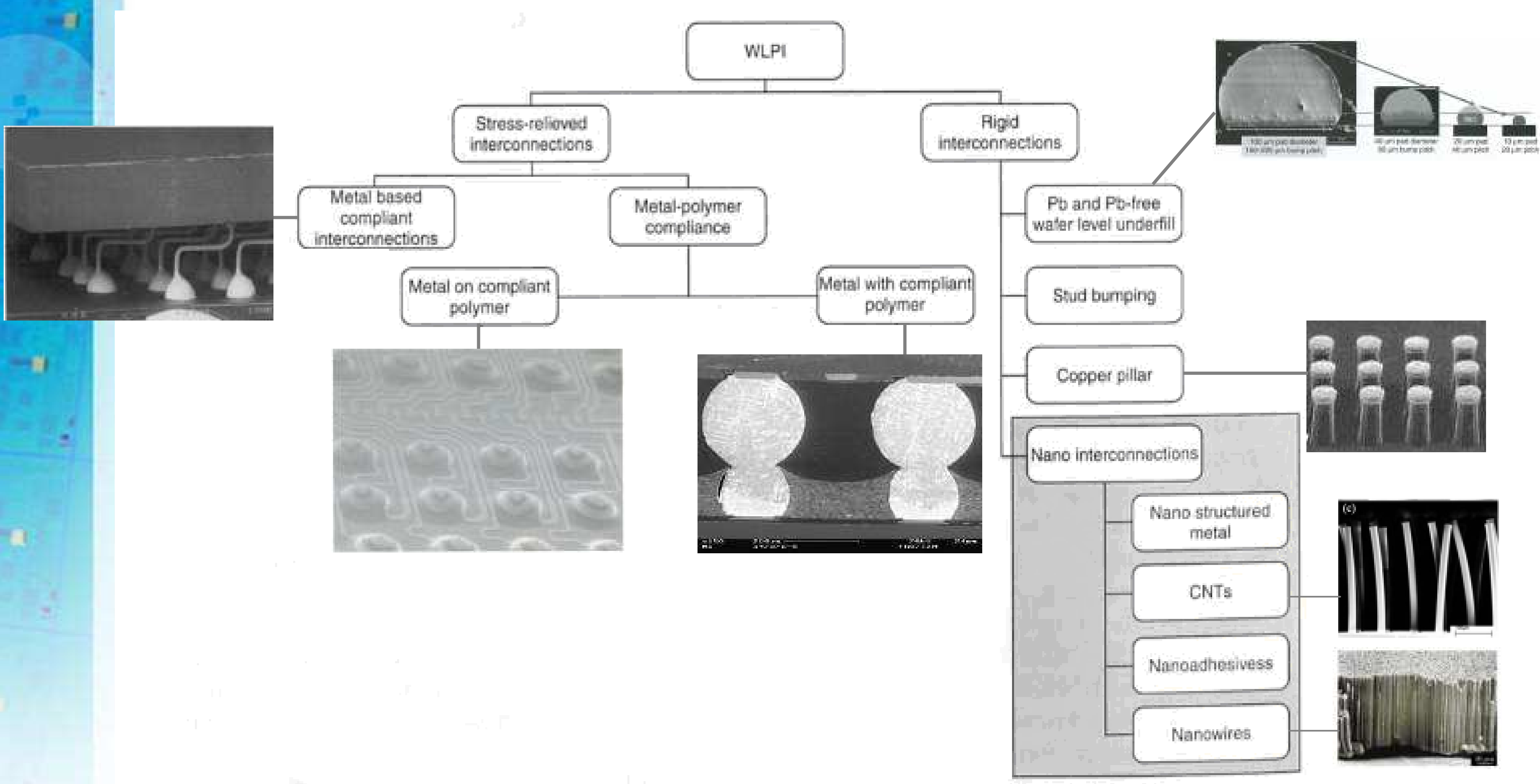
Les verrous du WLP



Source R.Tummala [1]

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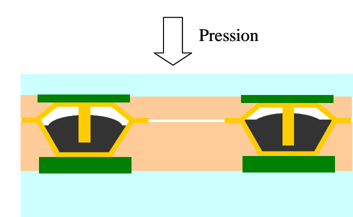
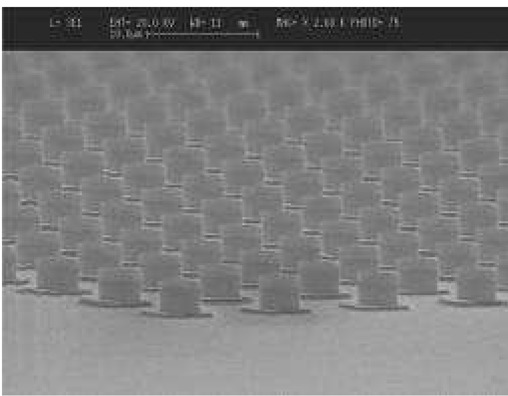
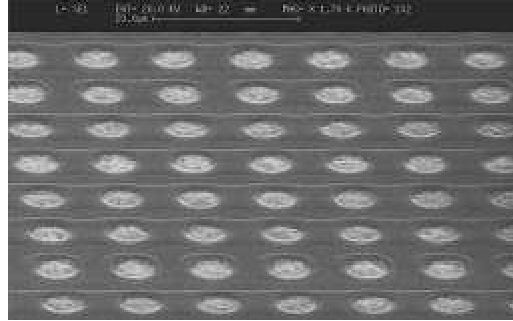
Les verrous du WLP : interconnexion très faible pas







FC300 SET equipment issued by Leti

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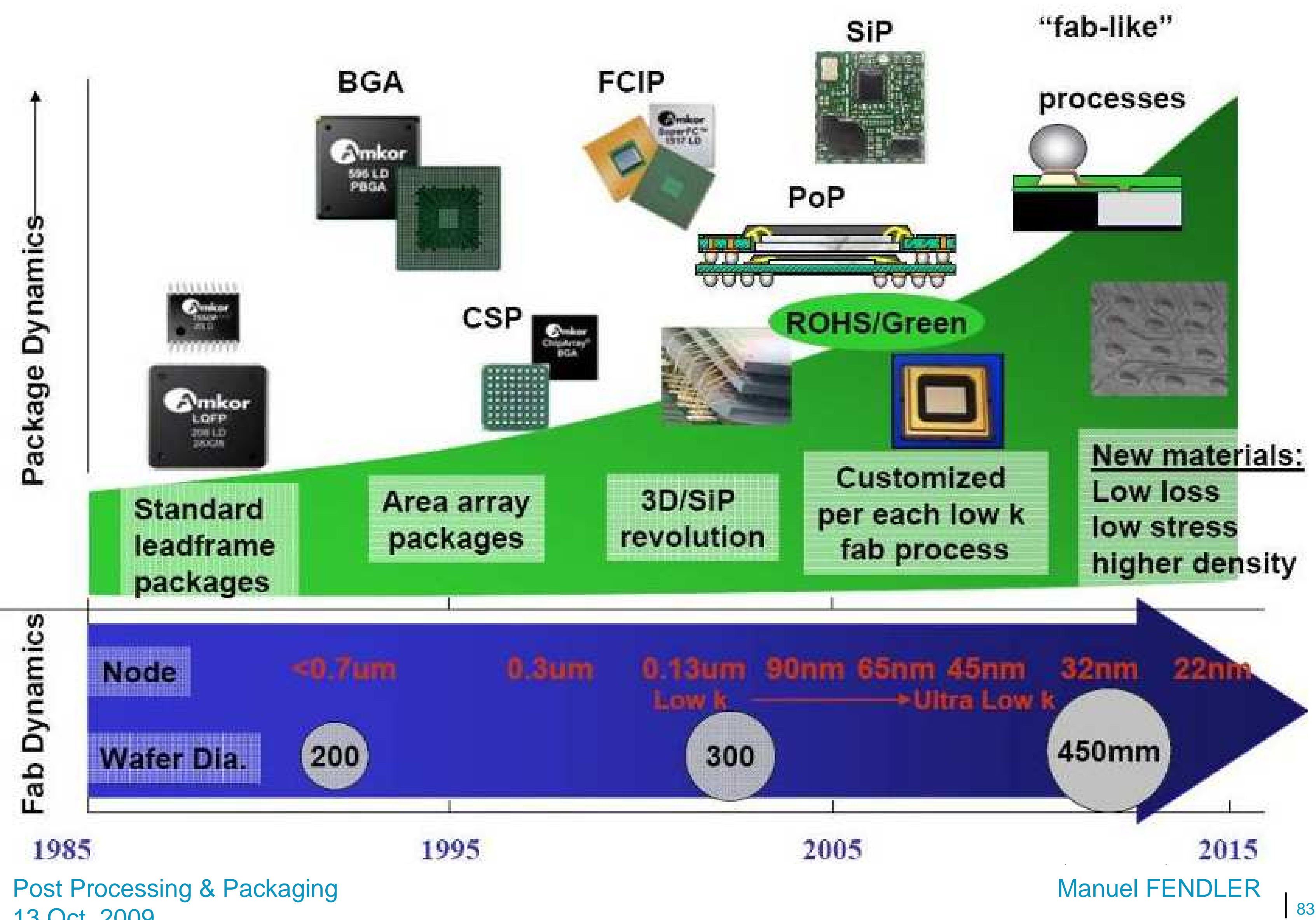
Conclusion: Evolutions croisées Composants / Packaging



Conclusion: Révolution 3D SiP

2009

- 65nm

Horizontal Placement: Wire Bonding Type, Flip Chip Type

Stacked Structure:
- Interposer Type: Wire Bonding Type, Wire Bonding + Flip Chip Type, Flip Chip Type
- Interposer-less Type: Terminal Through Via Type

Embedded Structure: Chip(WLP) Embedded + Chip on Surface Type, 3D Chip Embedded Type, WLP Embedded + Chip on Surface Type

Figure AP15 Categories of SiP

2015

< 32nm

- 3D, Through Silicon Via
- Wafer Level Packaging
- System in Package
- <100 micron pitch FC
- Smaller, thinner die
- Lead-Free + Underfills

Table 101 System-in-a-Package Requirements

Year of Production	2015	2016	2017	2018	2019	2020	2021	2022
Low cost handheld / #die / stack*	14	15	15	16	16	17	17	18
high performance / #die / stack	5	6	6	6	7	7	7	8
Low cost handheld / #die / SiP	14	15	15	16	16	17	17	18
high performance / #die / SiP	8	9	9	9	10	10	10	11

Sources ITRS'07

Limited by thermal density

Conclusion: Fab-Like Process

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