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Serial Powering

L’école de Microélectronique,

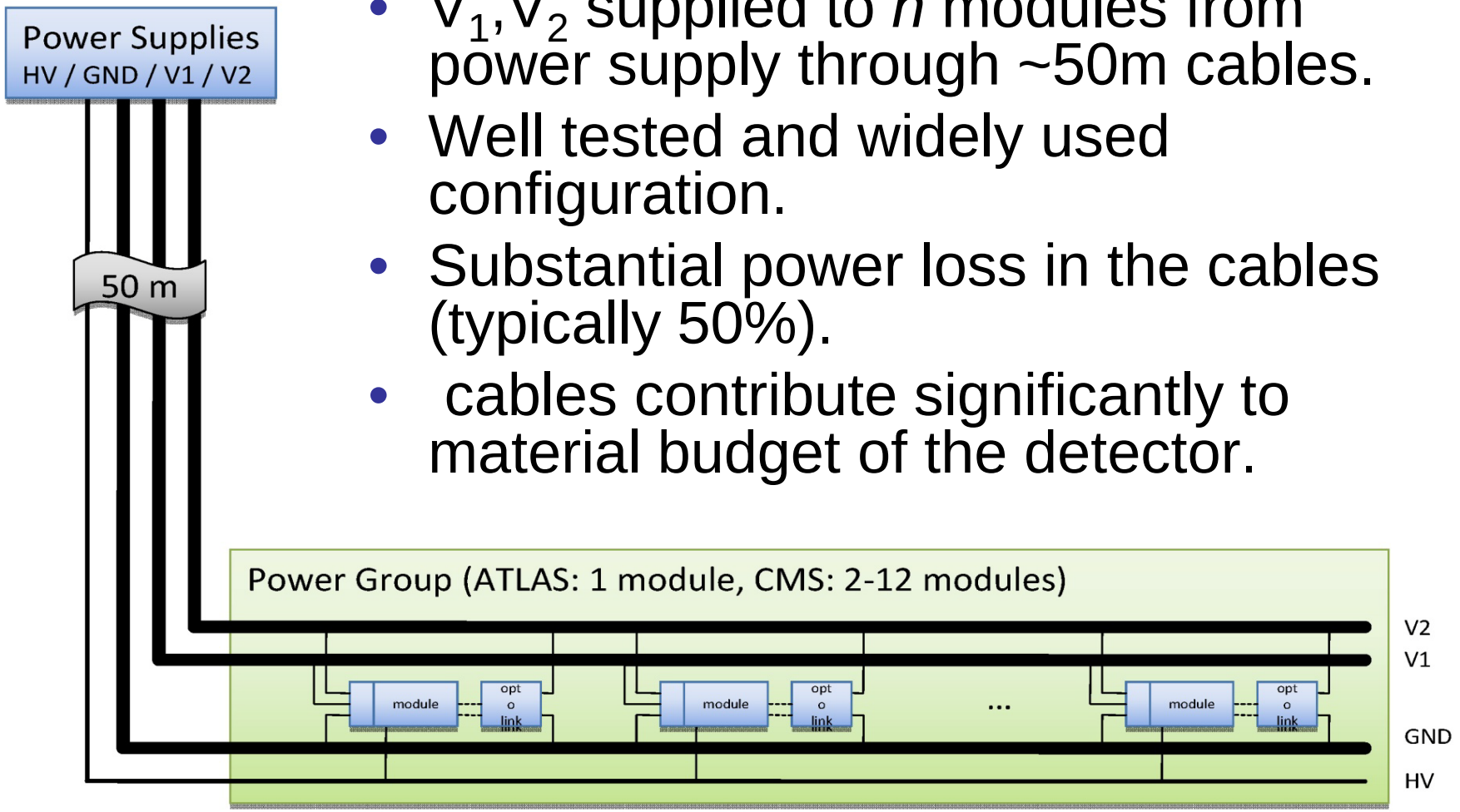
La Londe les Maures, 15-10-2009

Content

- The problem: How to bring the power (low voltages, high currents) to the tracking detectors inside the huge LHC experiments?
- The solution: Serial Powering or DC-DC power conversion.
  - Serial Powering of the ATLAS pixel detector – an example
  - Serial Powering ingredients (some):
    - Voltage regulators
    - Protection Schemes
    - Data transmissions issues

Cassical (parallel) powering scheme

- V_1,V_2 supplied to *n* modules from power supply through ~50m cables.
- Well tested and widely used configuration.
- Substantial power loss in the cables (typically 50%).
- cables contribute significantly to material budget of the detector.



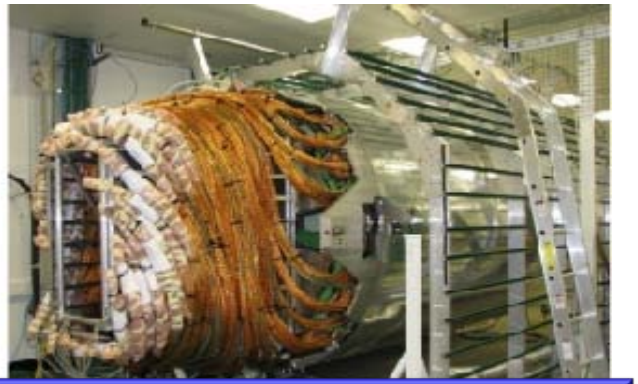
Tracker powering at LHC

- Current silicon trackers of ATLAS and CMS burn 50% power in cables!
- CMS strip tracker:
  - ASIC supply voltages: 2.5V and 1.25V.
  - Front-end power: 33kW.
  - Total current: 15kA (ATLAS SCT+TRT 12kA).
  - Loss in cables: 34kW.
- Cables are dimensioned to carry this current.

CMS Tracker Endcap TEC+

ATLAS Liquid Argon Cal FEE

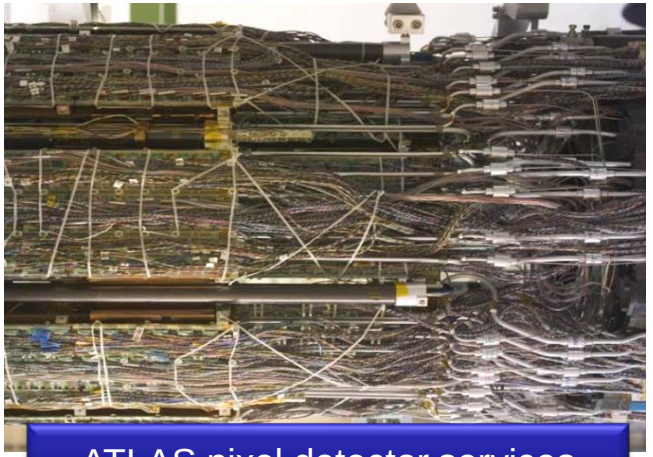
ATLAS Inner Det. Cables



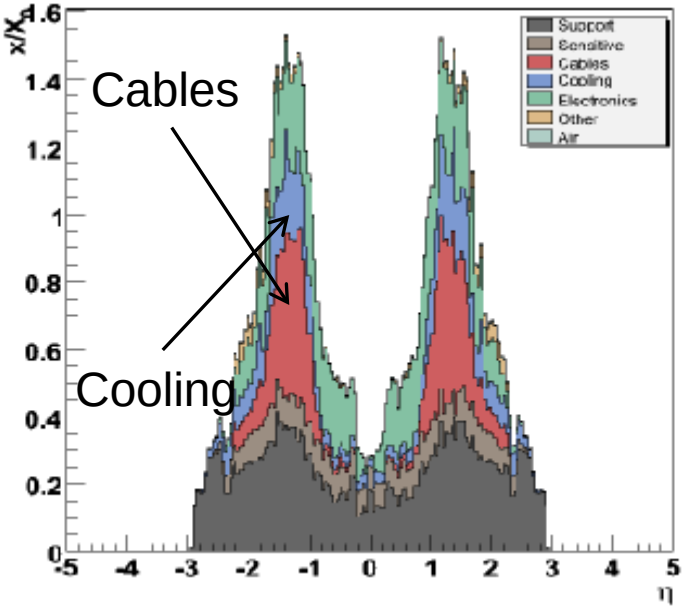
Tracker before insertion into CMS

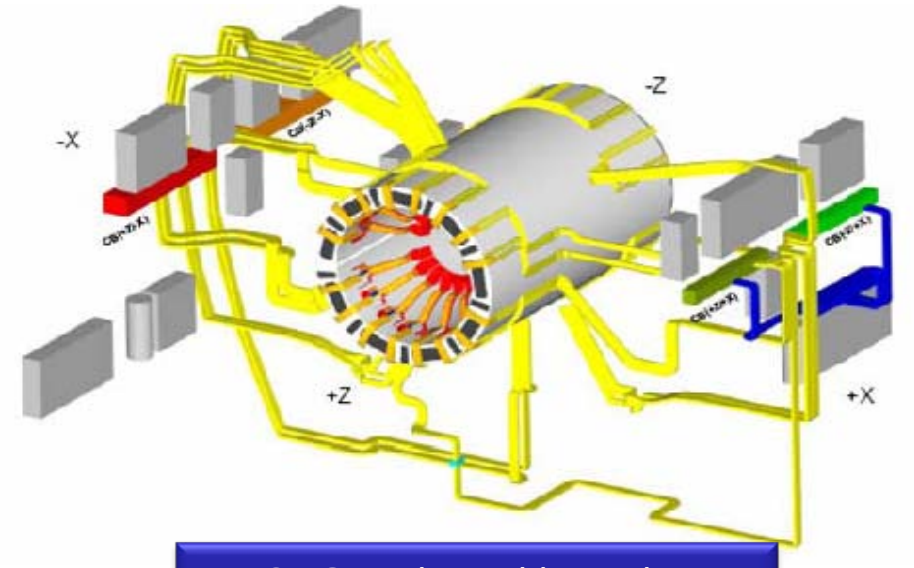
Tracker services at LHC

- Total cable cross section is fixed:
  - Cable loss scales with *current*^{2}.
  - Services are dominating the material budget in certain areas.
  - No space for more cable cross section.
  - Replacing of cables is very difficult.



ATLAS pixel detector services





CMS tracker cable routing

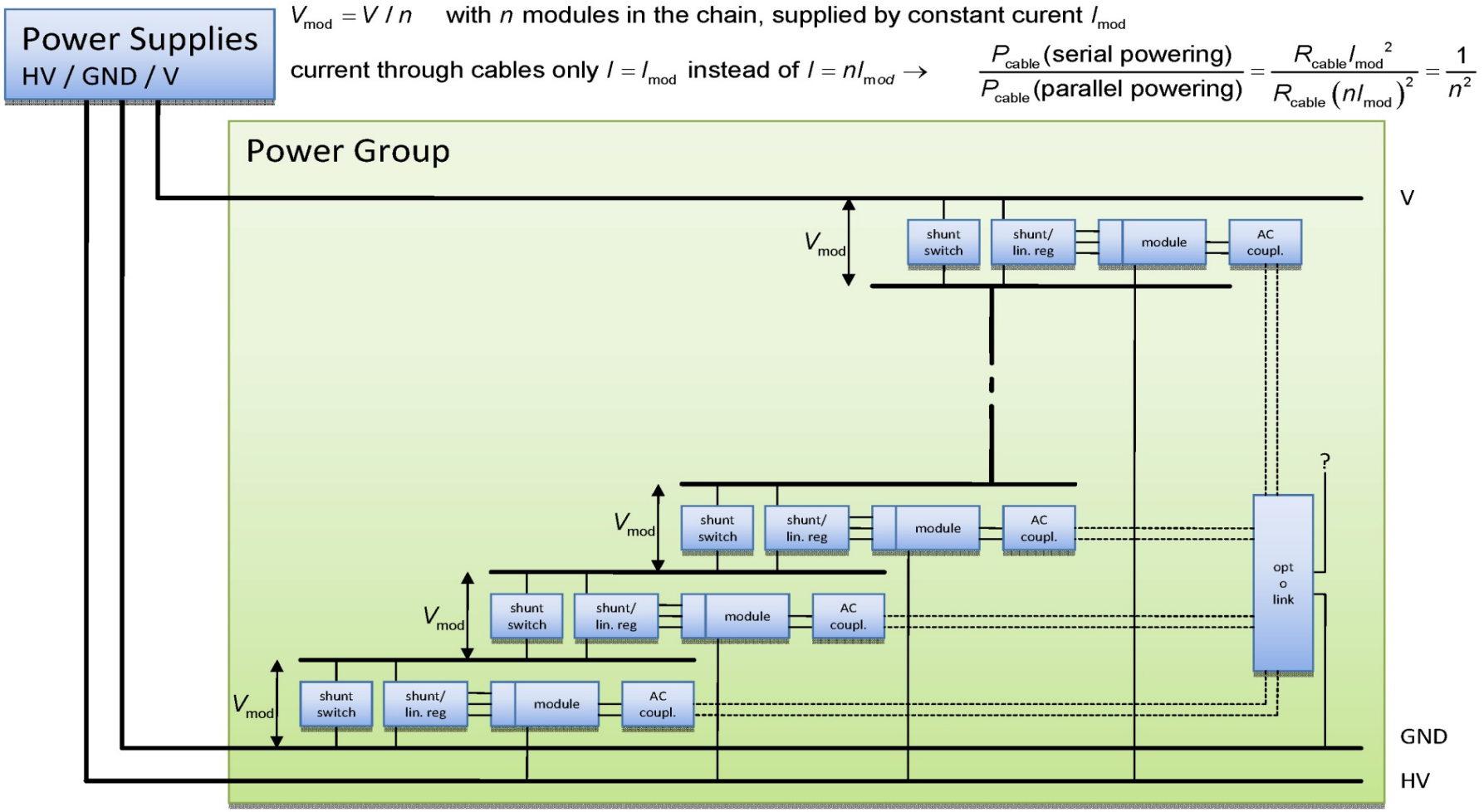
Tracker powering for SLHC

- Powering will be even more critical at SLHC trackers:
  - ASICs run at about 1.3 V (assuming 130nm CMOS)
  - Front-end power stays roughly the same: ATLAS: 43-63kW, CMS. 35kW
  - Total current goes up: ATLAS 33-48.5A, CMS: 27kA
  - If we need to send 2-4 times more current through the same cables → 4-16 x cables loss (‚power efficieny' drops to 12.5% or less)
- These estimates are driven by the requirement for high granularity, raiation tolerance and low noise and take already into account imprvements due to smaller ASIC fearure size!

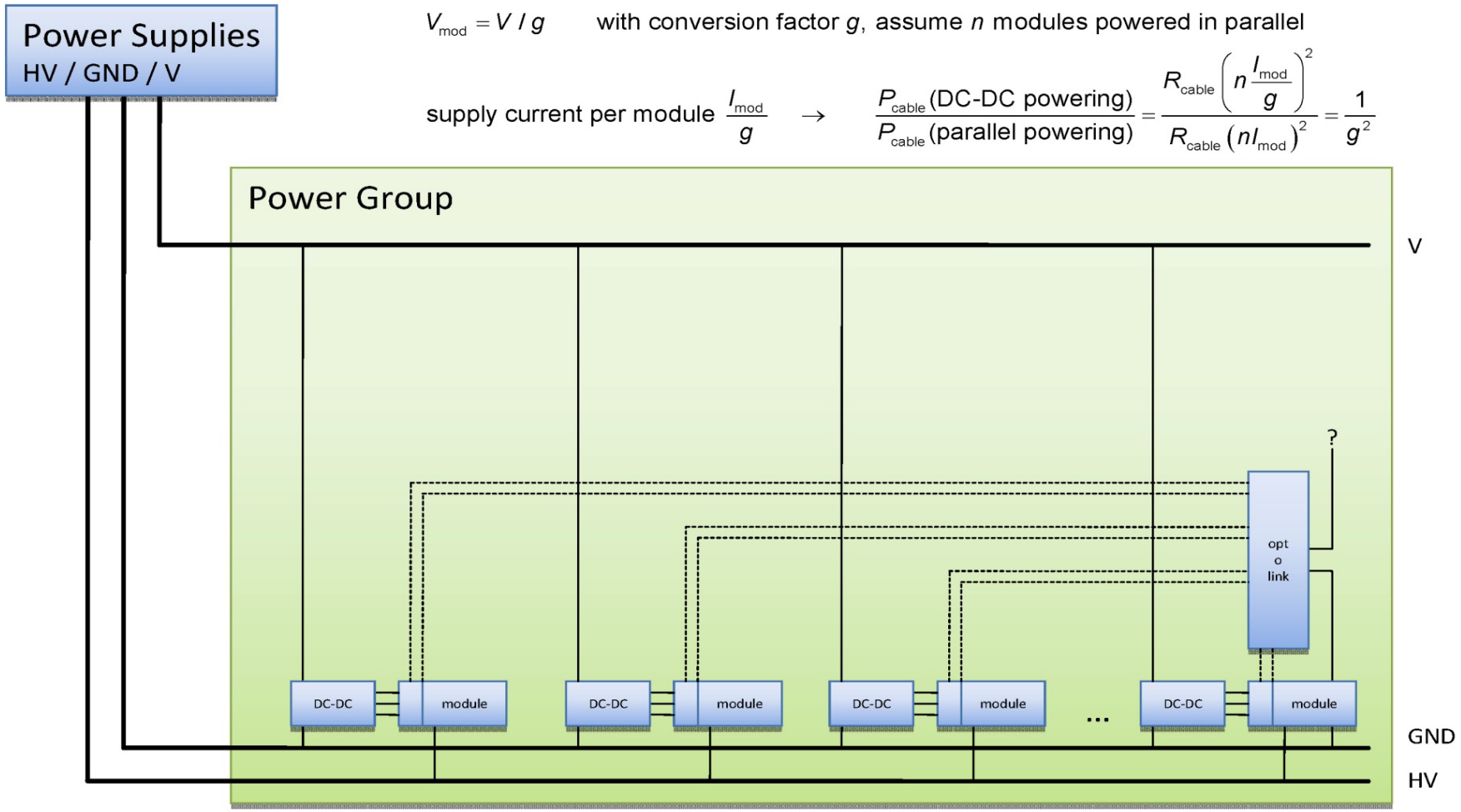
➔ since cable loss scales with $current^2$ we need to transmit power at lower current!

  - This approach allows to reduce cable cross-section even furter to save material

Serial Powering



DC-DC Power Conversion



Comparison of Serial Powering and DC-DC Power Conversion

	Serial Powering	DC-DC Conversion
efficiency	65 – 85 % (to be measured on real systems)	
power loss in cables	~(# modules in chain)$^{-2}$	~(conversion factor)$^{-2}$
supply of different voltages	add voltage regulator	add converter
supply of different currents	current = max. needed current	no problem
scalability in #modules	adapt input voltage	add converter or increase current capacity
FE ASIC	shunt and regulation circuitry partly incorporated in FE ASIC	can be fully decoupled from FE ASIC or partly incorporated
system ground potential	different for every module	one ground level
data/control links	need AC coupling	any coupling
slow control (voltage reading, ...)	different reference potential for each module	as in conventional systems
reliability	need protection against failure of module or power circuitry in chain + over-voltage protection	converter failure leads to loss of modules possiblity to switch off individual modules
start-up	all modules in chain at once	operation of individual modules possible
noise	voltage fluctuations in chain	switching noise
rad-hard transistors at full input voltage (10-50 V)	bypass transistors (slow)	switching transistors
material budget	shunt/lin. regulators (inside FE ASIC), bypass transistor, AC coupling	converter

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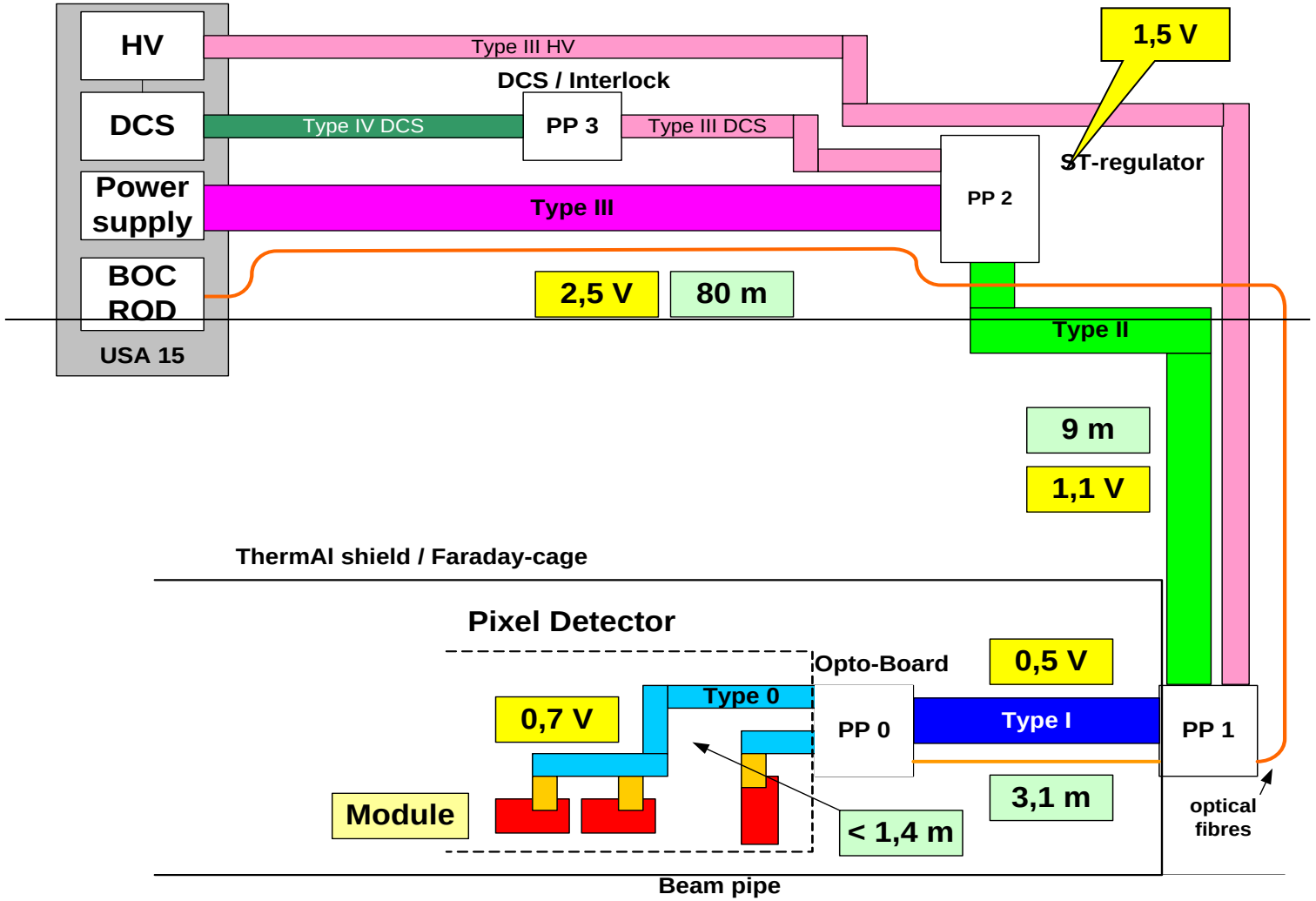
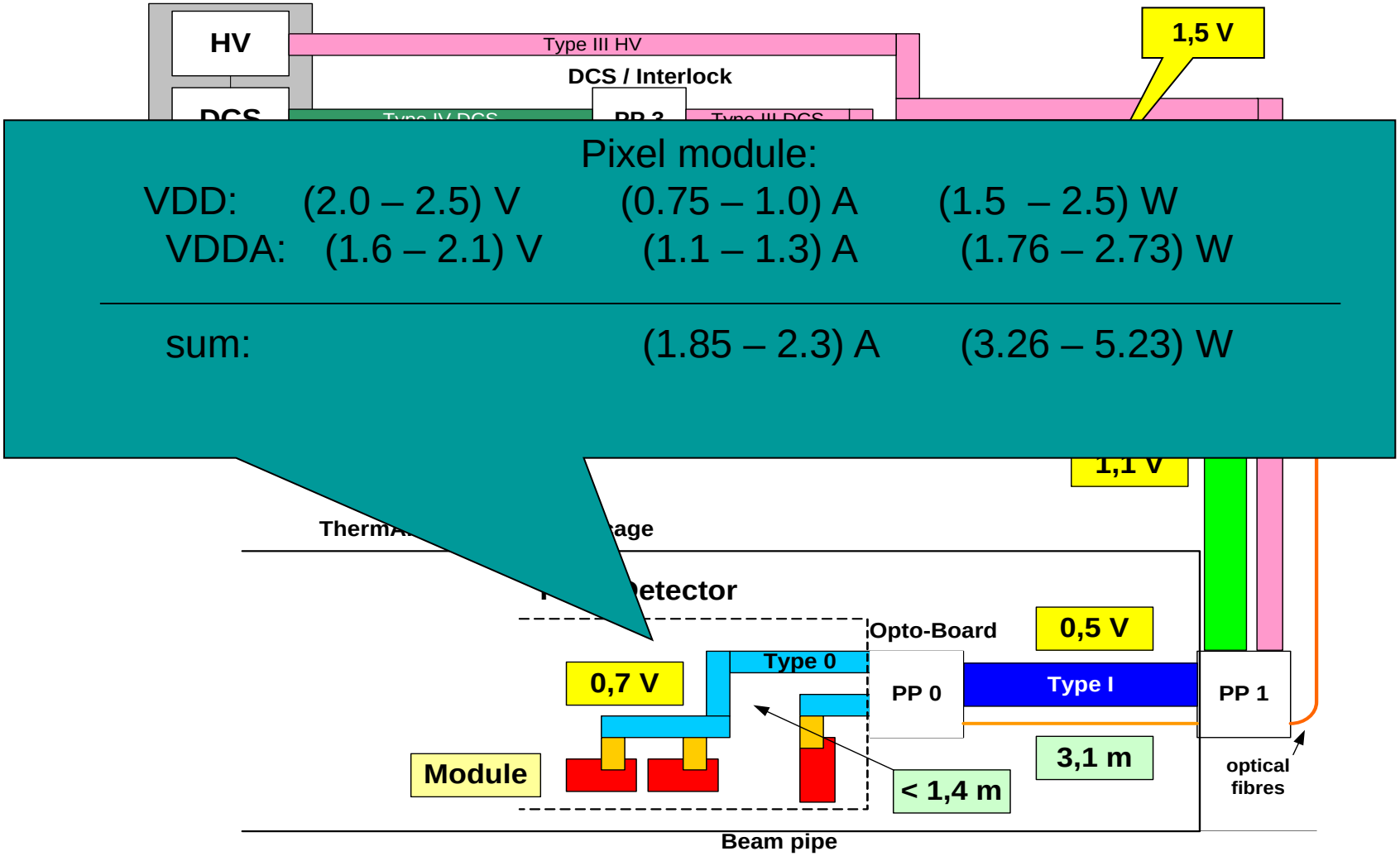
SP for ATLAS Pixel

An example

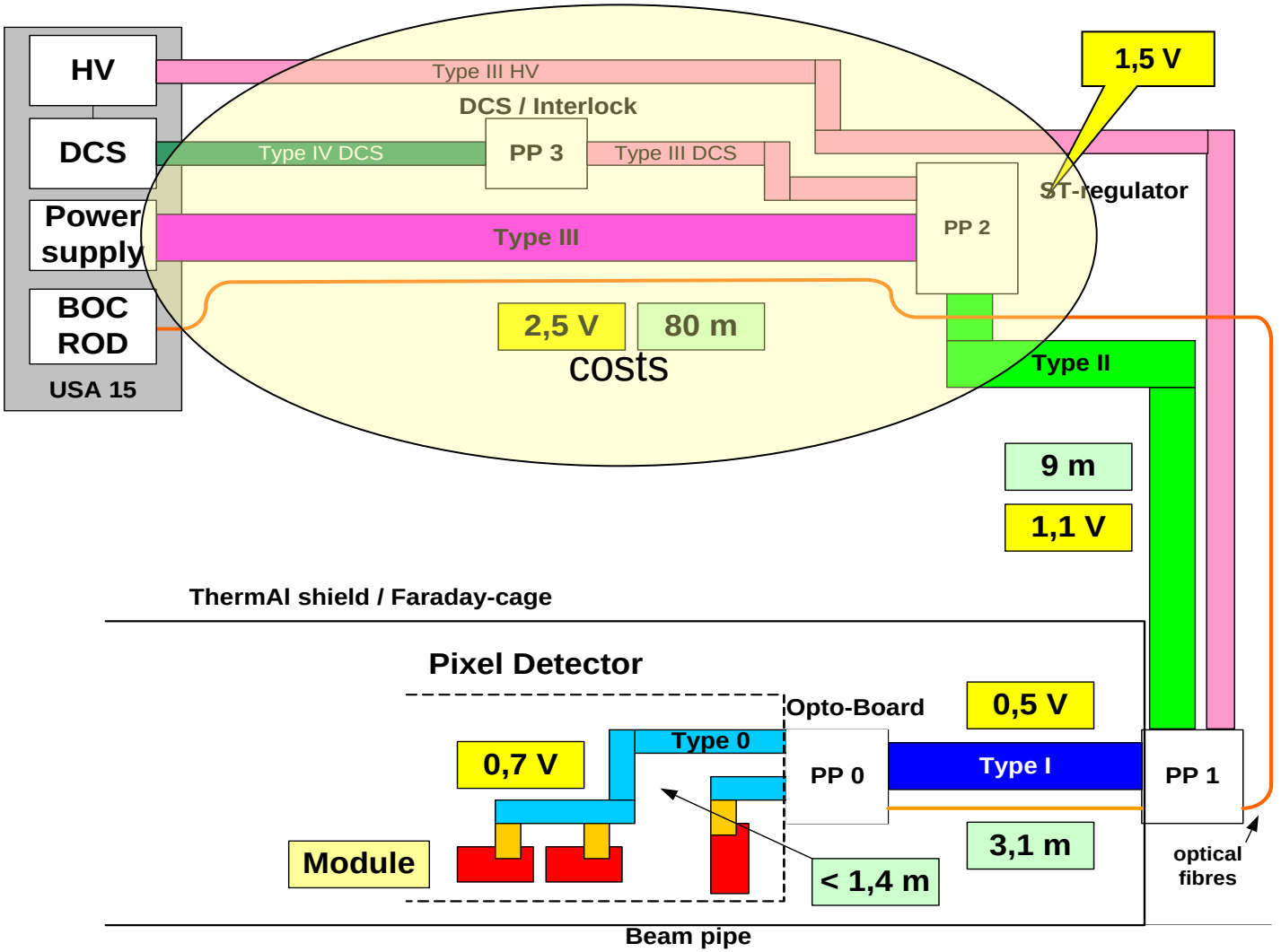
Service chain for ATLAS pixel detector



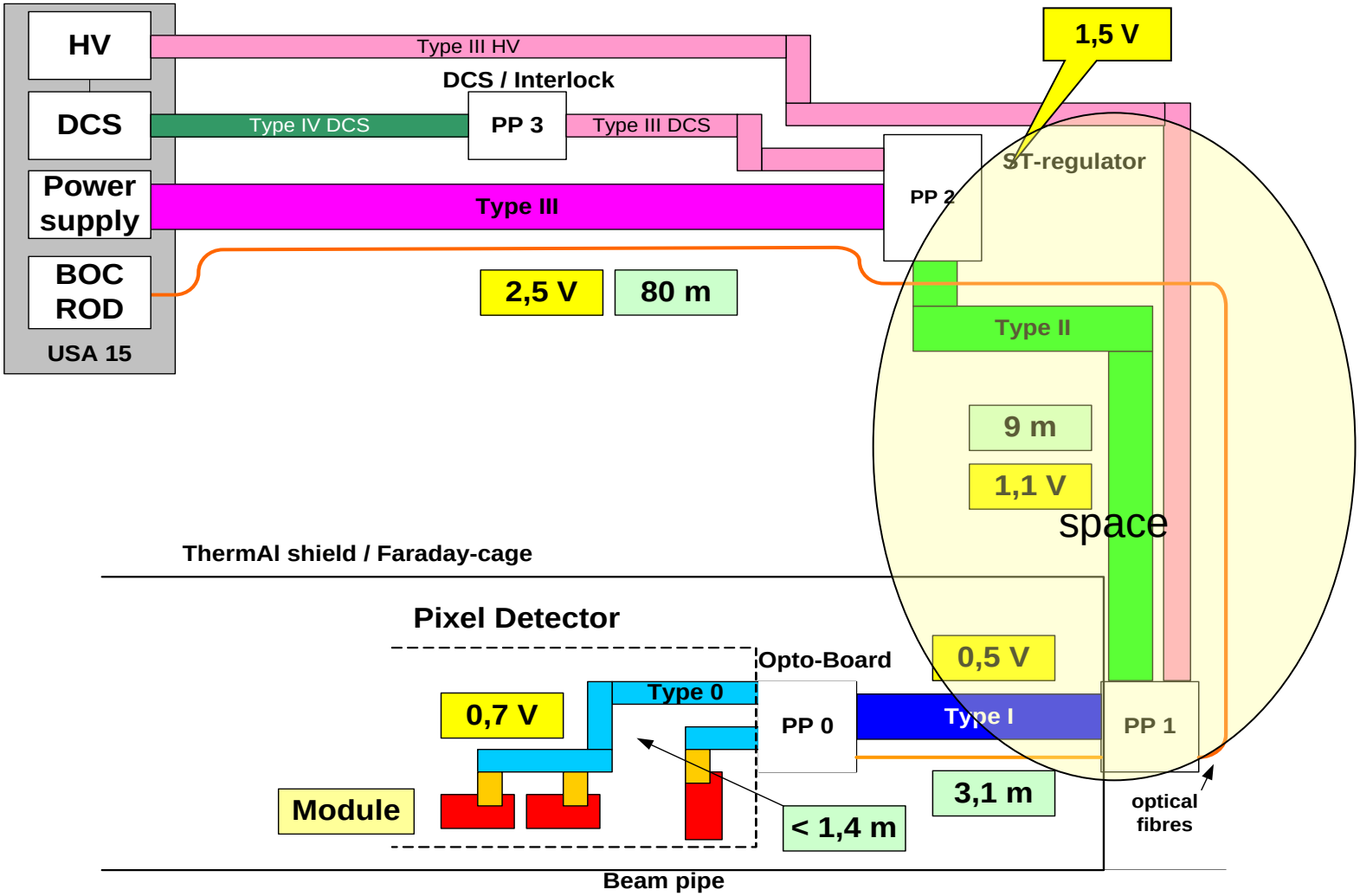
Service chain for ATLAS pixel detector



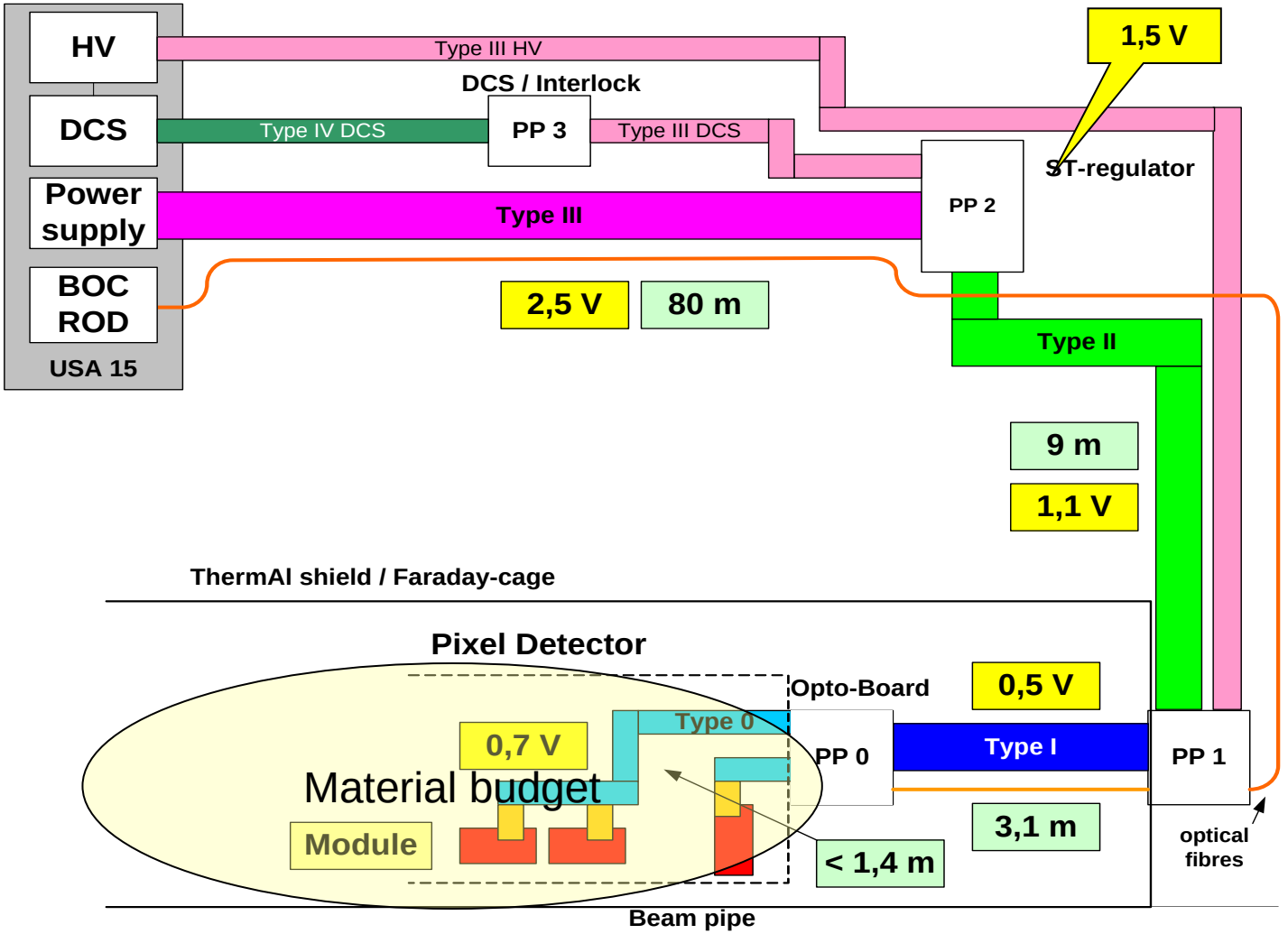
Service chain for ATLAS pixel detector



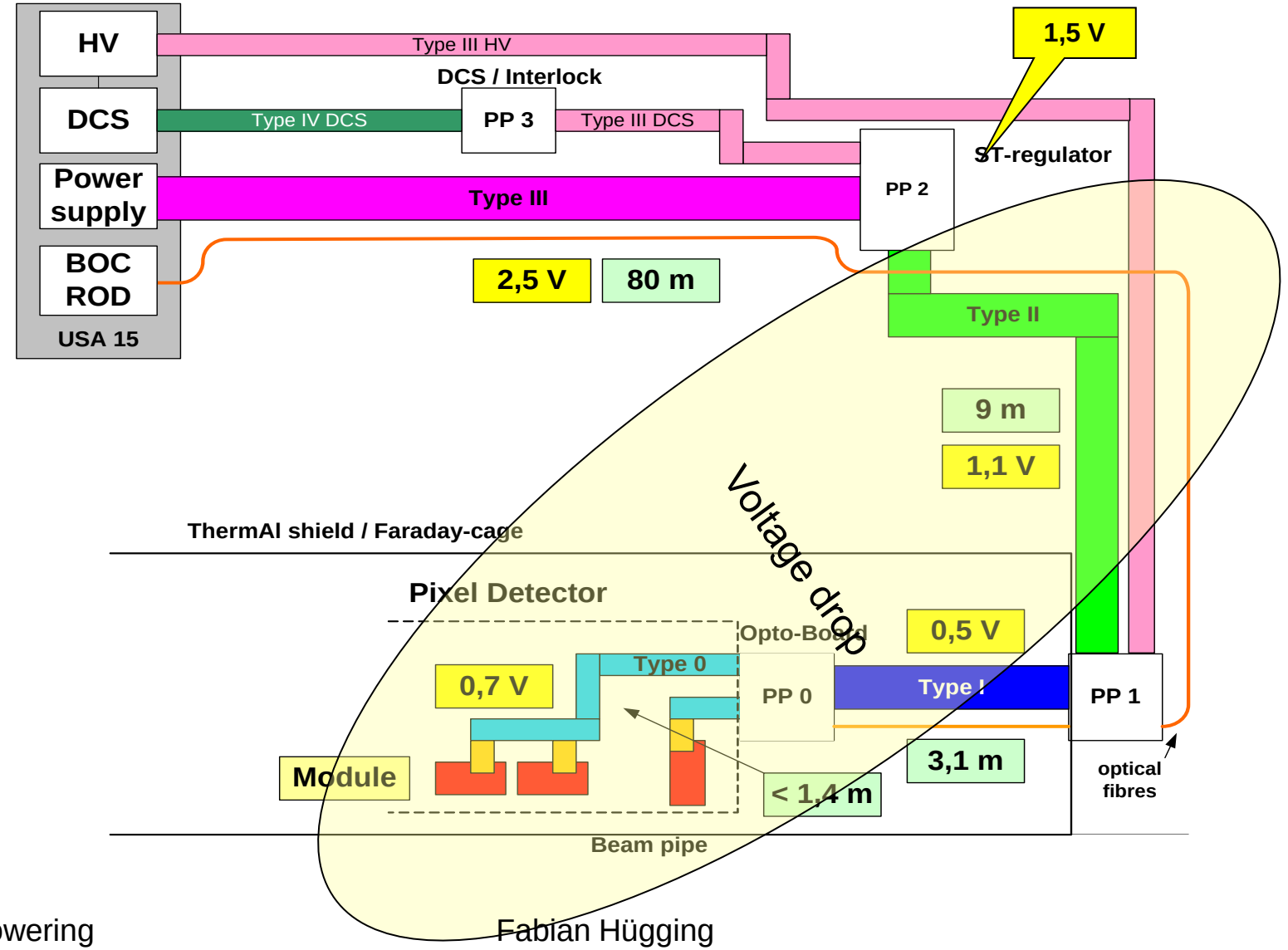
Service chain for ATLAS pixel detector



Service chain for ATLAS pixel detector

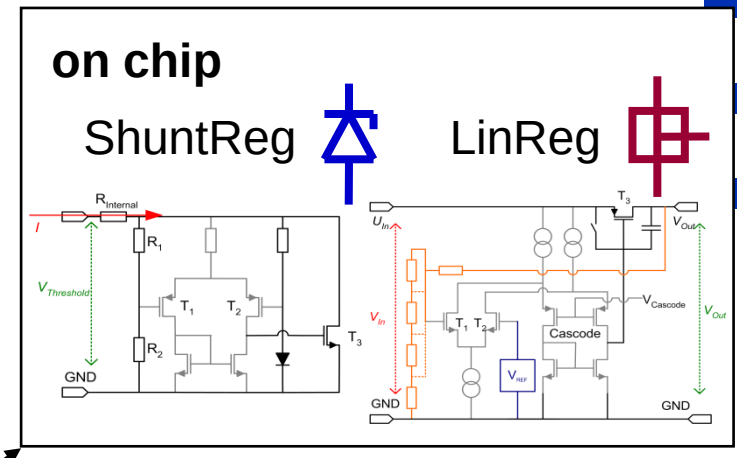


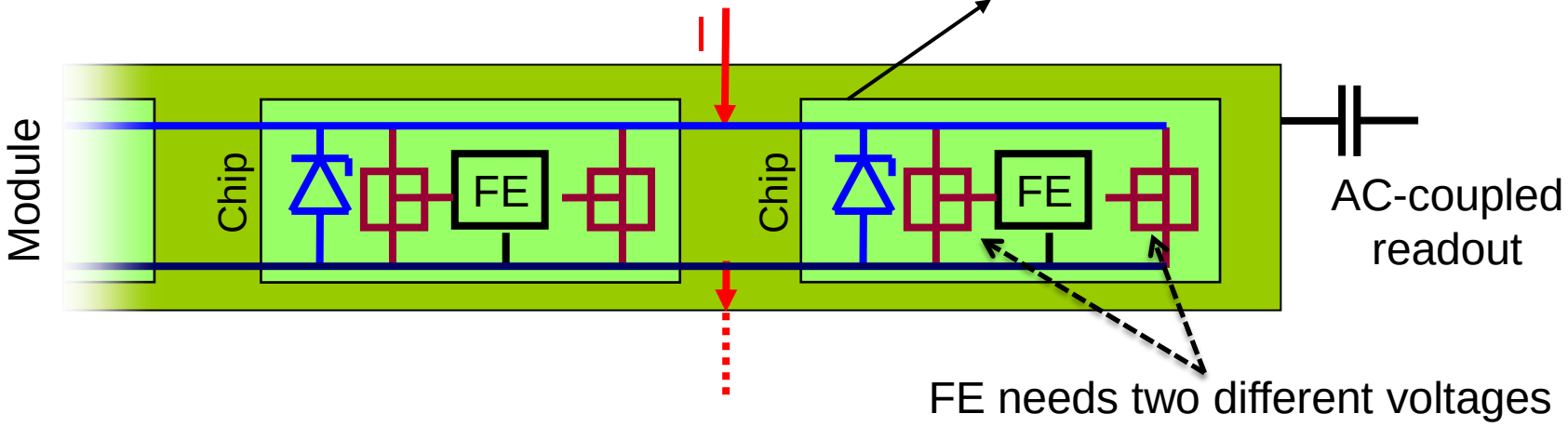
Service chain for ATLAS pixel detector



Basic Principle

- Constant current through all modules
- Voltages generated **on chip** by
  - **Shunt regulators**
    - **Current -> Voltage**
  - **Linear regulators**
    - **Voltage->Voltage**





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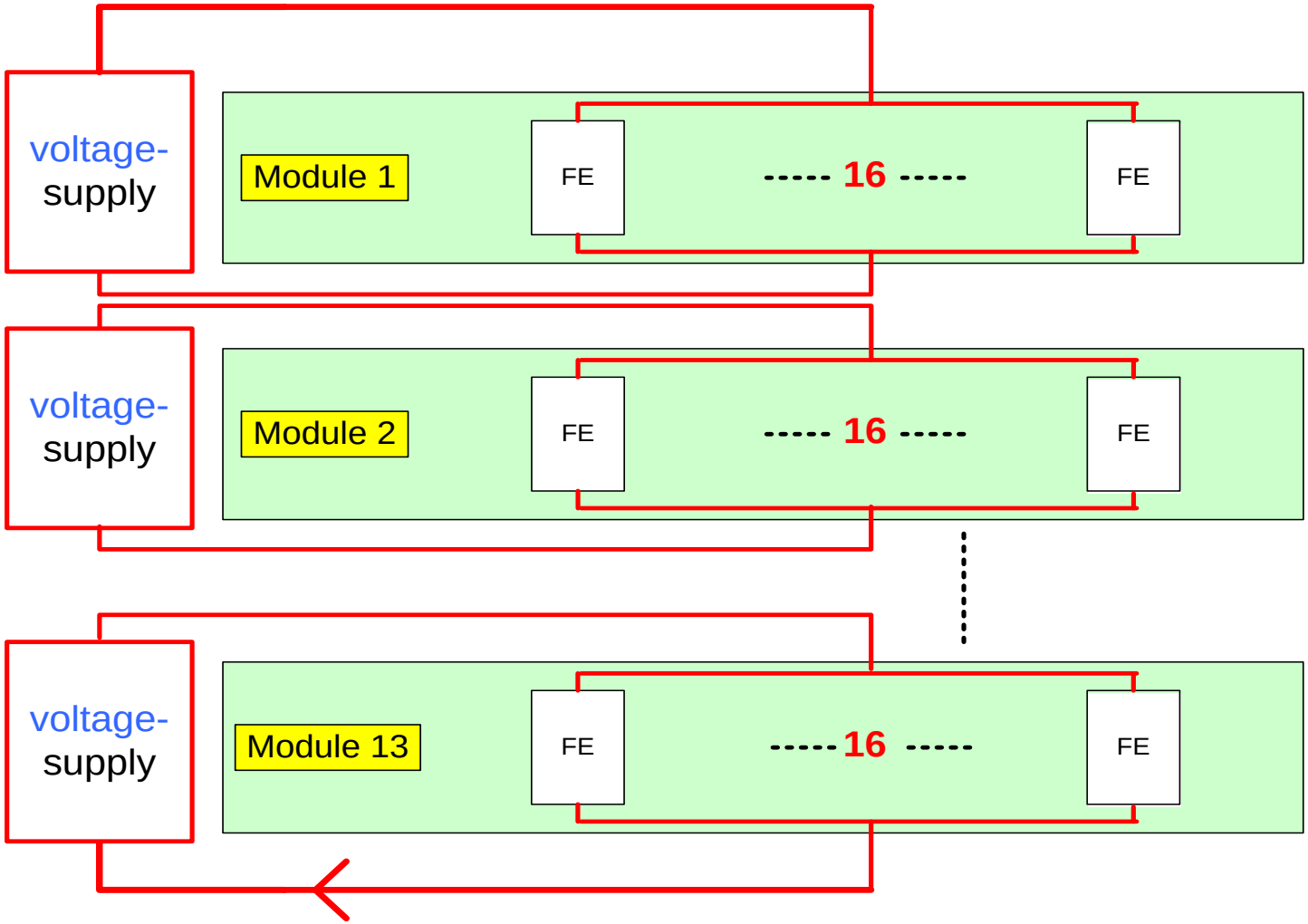
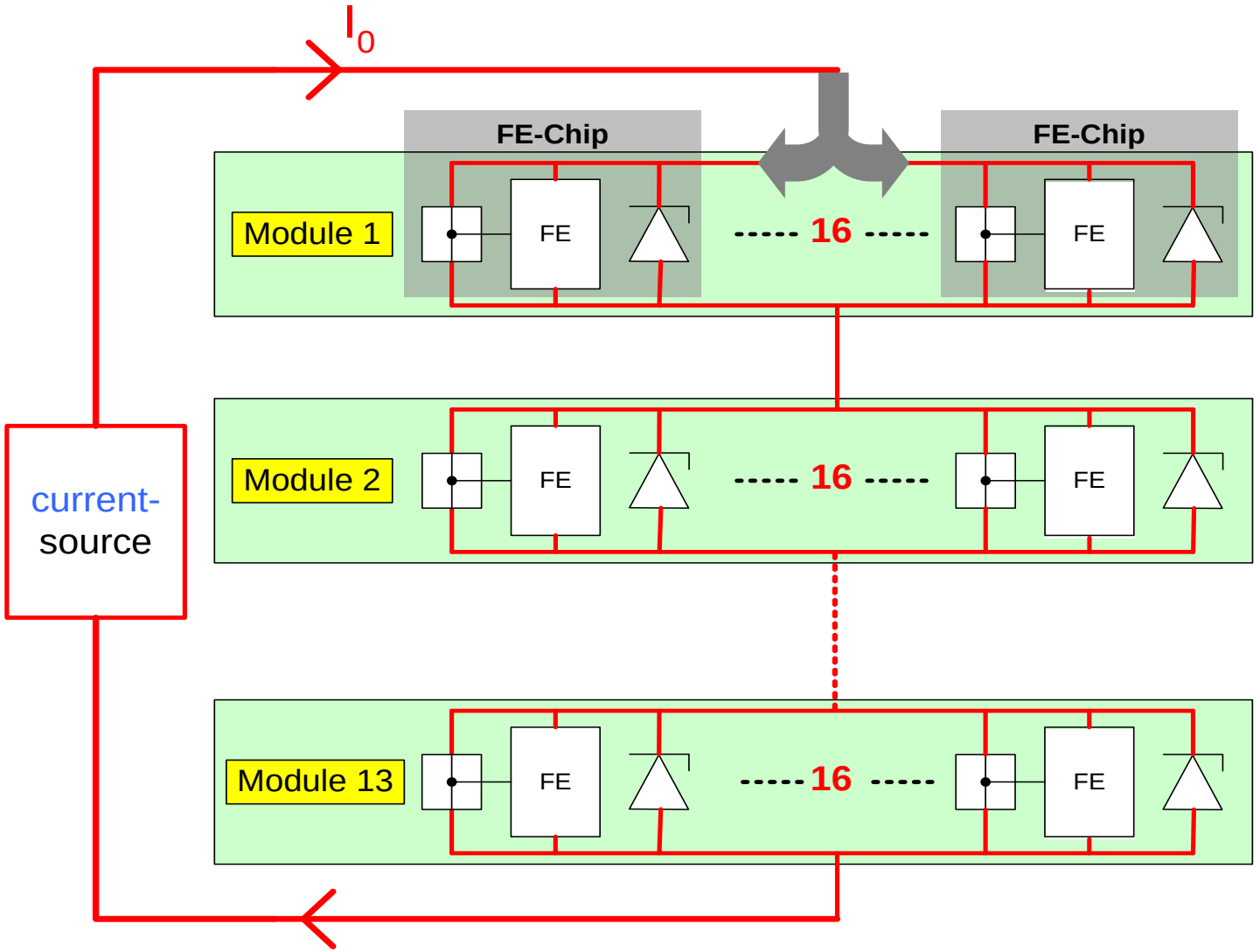
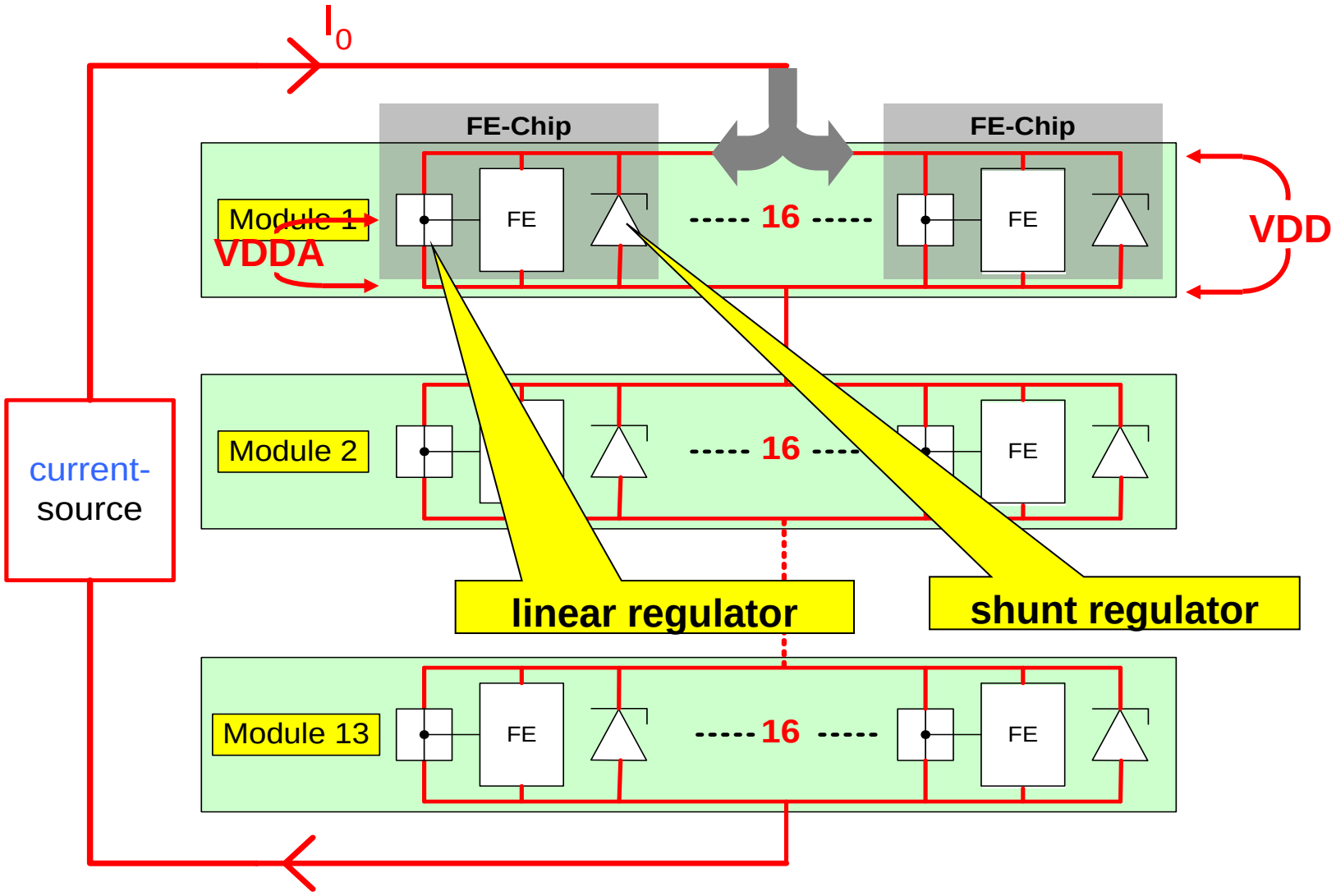
Serial-Powering



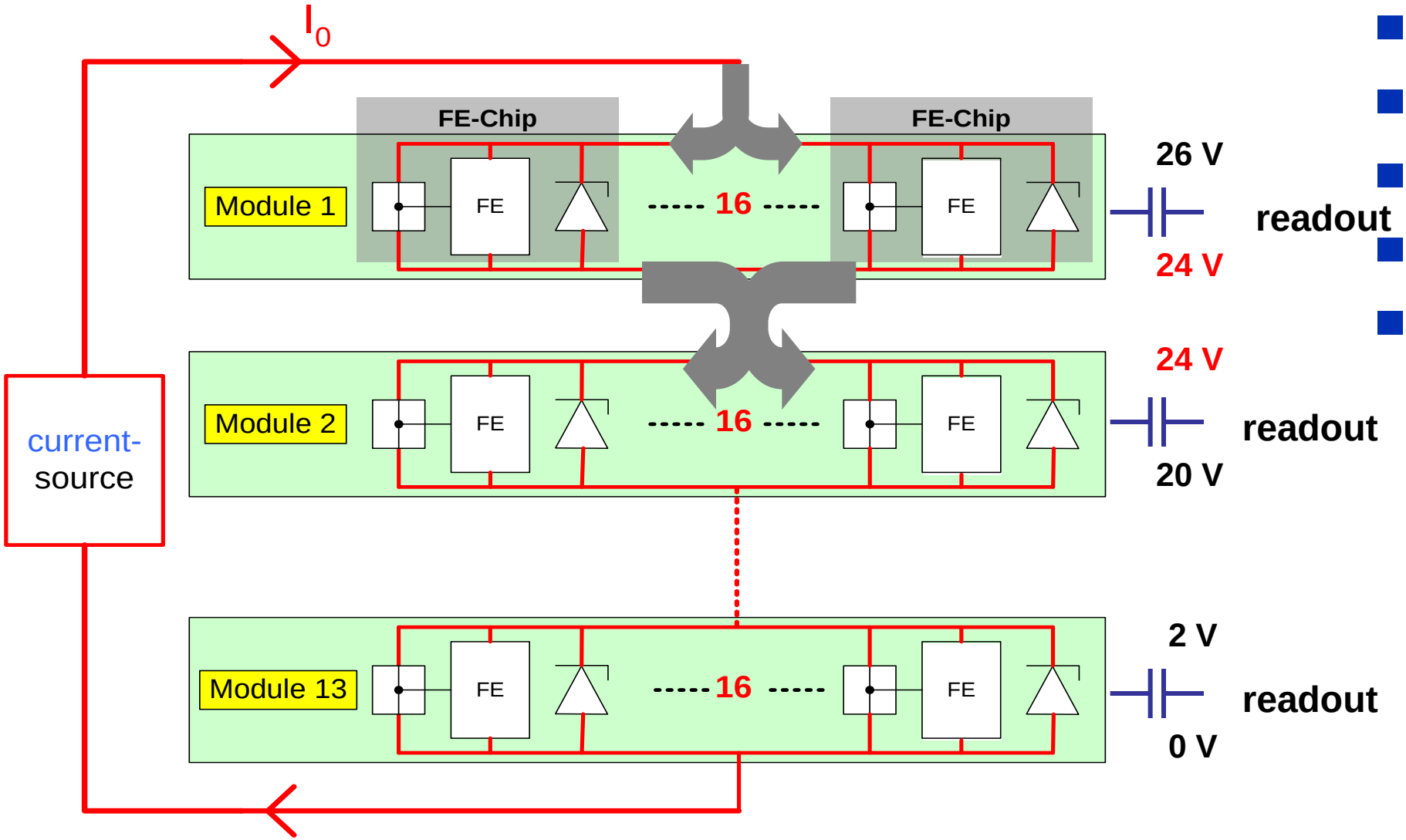
Serial-Powering



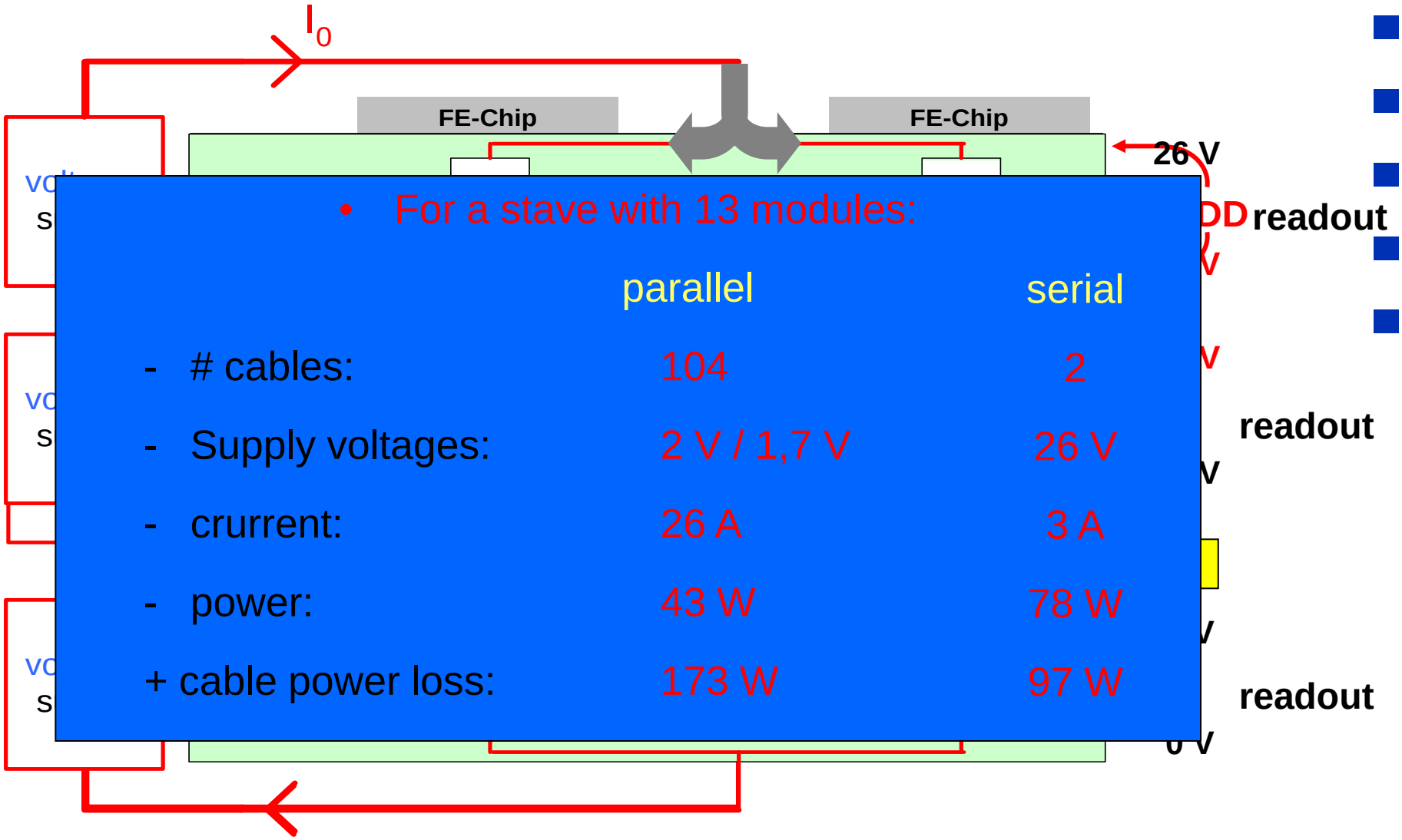
Serial-Powering



Serial-Powering



Serial-Powering

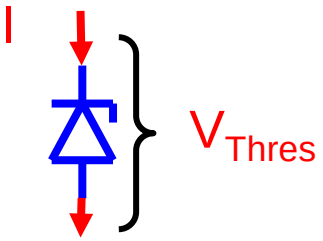


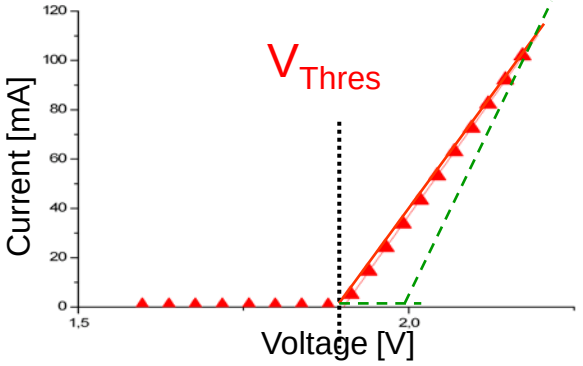
- For a stave with 13 modules:

	parallel	serial
- # cables:	104	2
- Supply voltages:	2 V / 1,7 V	26 V
- crurrent:	26 A	3 A
- power:	43 W	78 W
+ cable power loss:	173 W	97 W

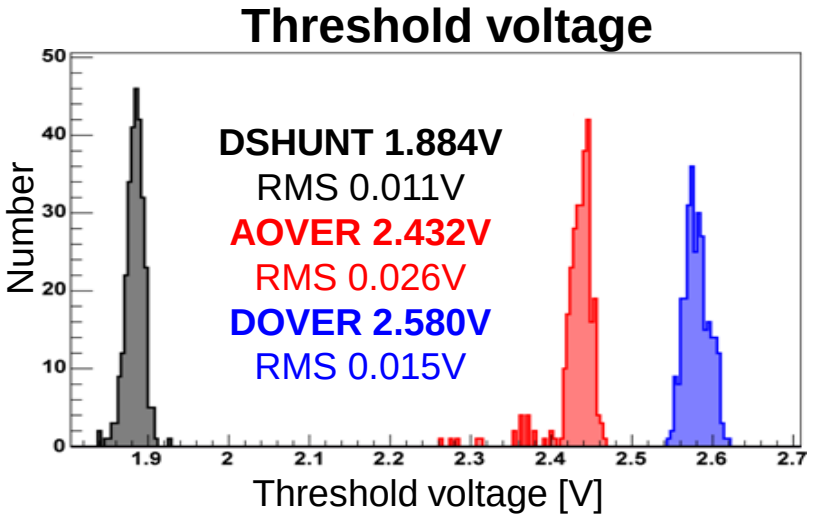
Shunt Regulators I3

- Important properties:
  - Threshold voltage
  - Resistance
  - Spread of threshold voltages and resistance



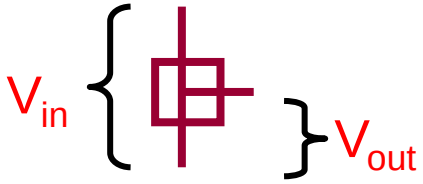


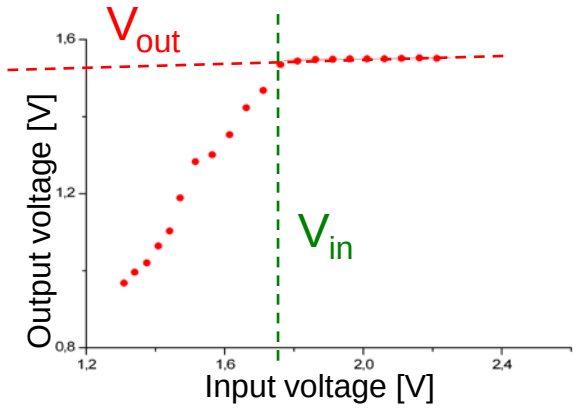
- 3 shunt regulators on chip:
  - DShunt (2.0V), AOver (2.4V) and **DOver (2.7V)**
- Measurement on ~280 chips on a production wafer:
  - Threshold voltages as expected
  - Resistances ~1Ω with small spread (RMS <0.15Ω)



Linear Regulators I3

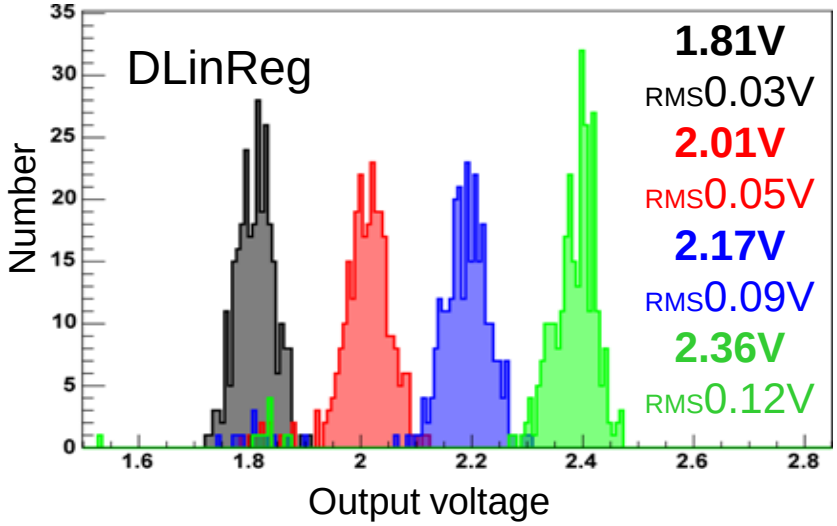
- Important properties:
  - Output voltage
  - Voltage drop (Vin –Vout)
  - Stability vs input voltage or vs load





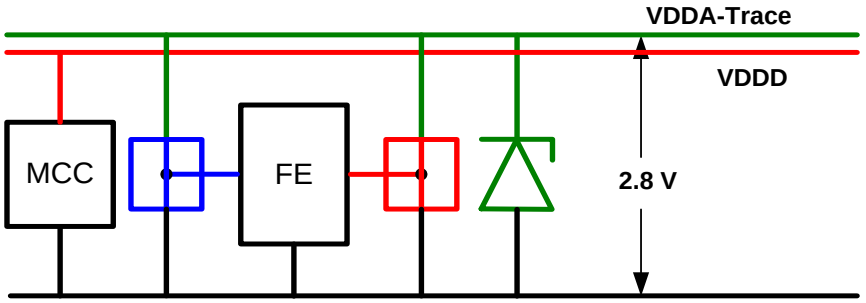
- 2 linear regulators on chip:
  - ALinReg (1.5V-1.8V) and DLinReg (1.8V-2.4V), both in 4 steps
- Measurement on ~280 chips on a production wafer:
  - Good separation between output voltages
  - Voltage drop ~230mV (ALinReg) and ~160mV (DLinReg)
  - Stability $\Delta V_{out}/\Delta V_{in}<0.2$
  - Stability $\Delta V_{out}/\Delta I<0.1\Omega$

Output voltage



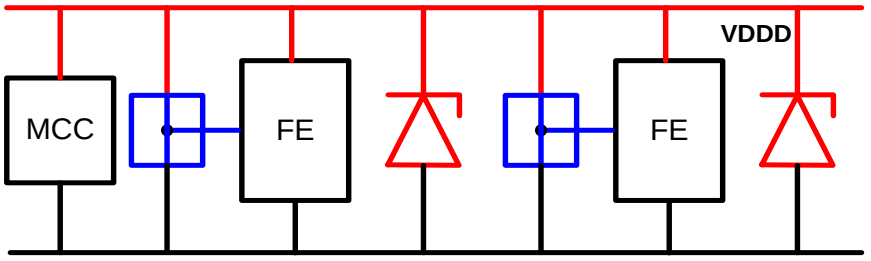
SP schemes within FE-I3

A+D linear regulated



- pros:
  - Suplly voltages more flexible
  - Individual chips are better seperated
  - Modules can beoperated with constant current and constant voltage
- cons:
  - More power loss
  - Higher risk for indiviual chips

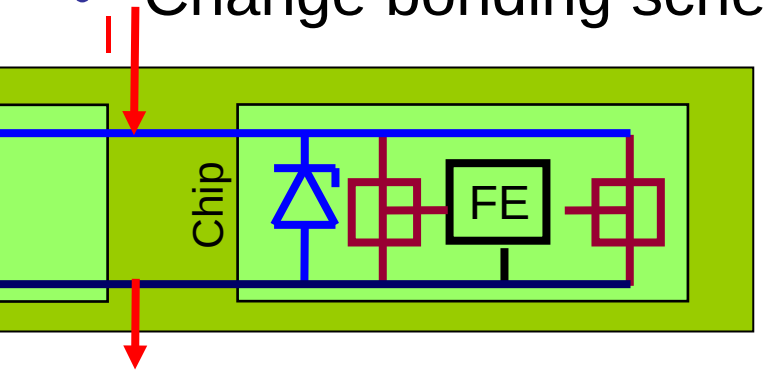
only VDDA linear regulated



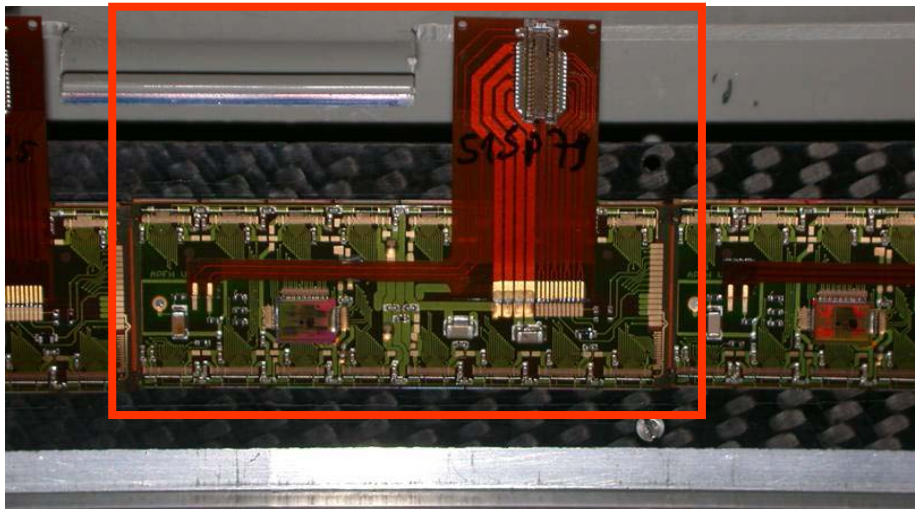
- pros:
  - Lower power loss
  - MCC and FEs are on the same digital potential
- cons:
  - Digital supply voltage defined by design of shunt regulator
  - Cross talk between chips possible

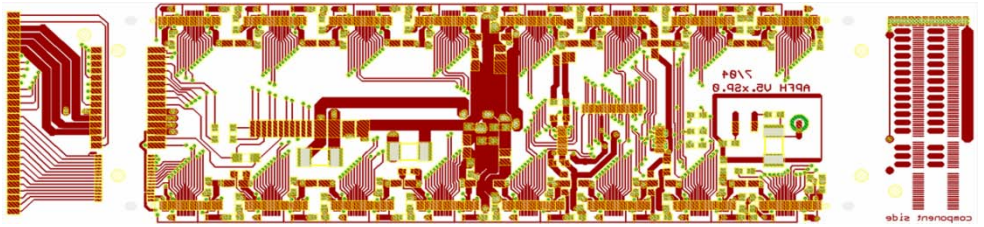
Single Serial Powering module

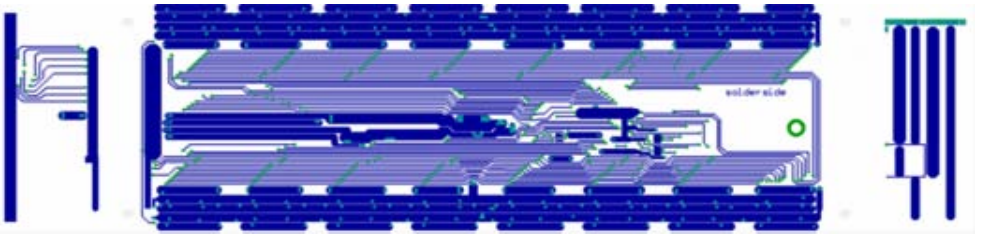
- Using already available production chips and dummy/damaged module
- Change bonding scheme / Dedicated flex hybrid



Module



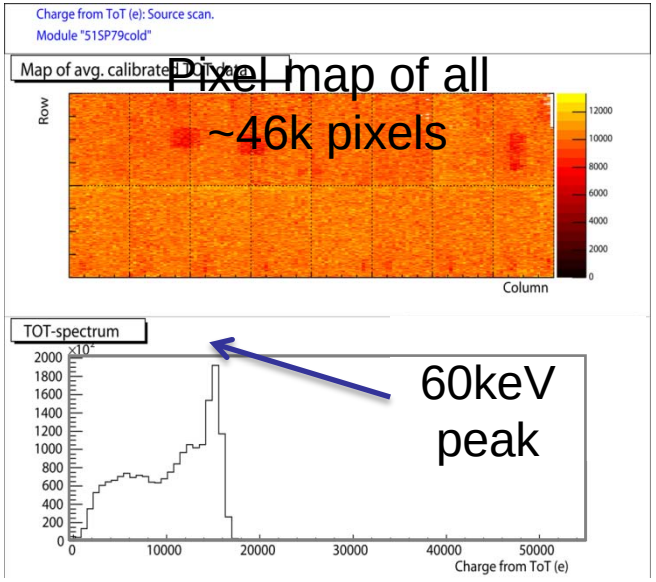




Performance of Single I3 modules

- Single Serial Powering Module performance as good as Parallel Powering Modules (esp. noise)?

Source scan with ^{241}Am as a qualitative proof



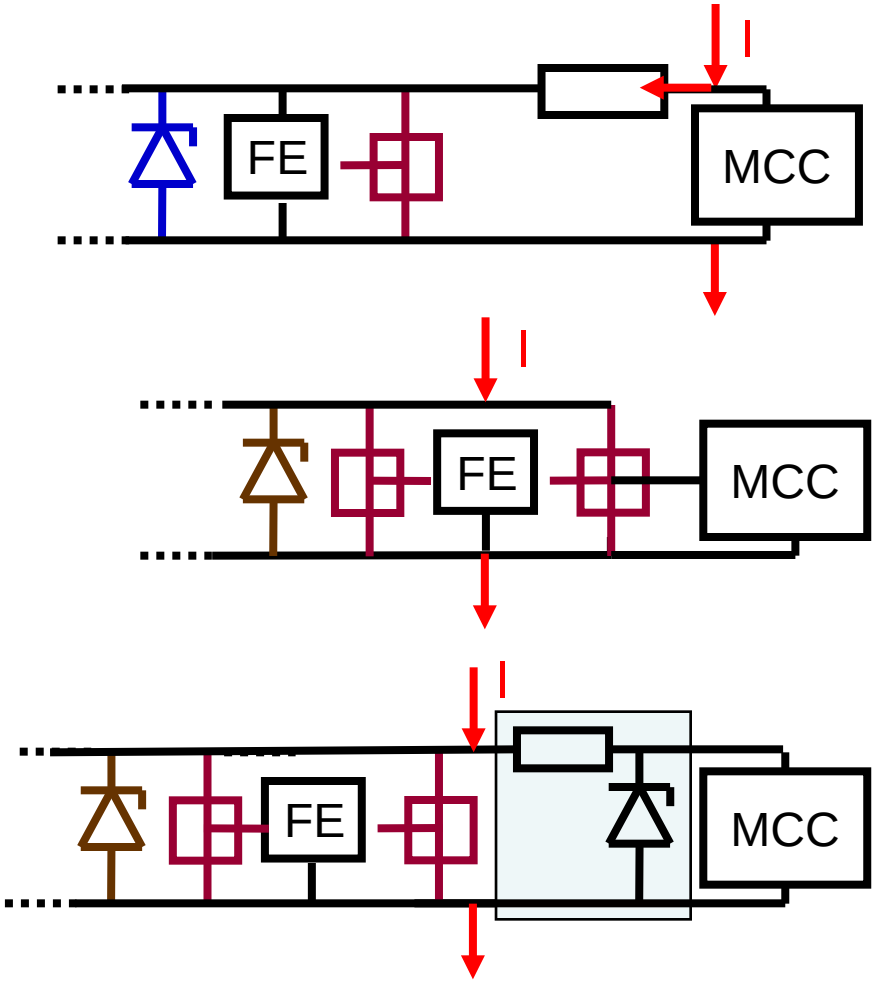
Some perfomance data as quantitative proof

	Serial	Parallel
Threshold	4226e$^-$	4169e$^-$
Dispersion	90e$^-$	64e$^-$
Noise	186e$^-$	183e$^-$
In-Time-Th.	5624e$^-$	5532e$^-$
Overdrive	1451e$^-$	1344e$^-$
Crosstalk	0.93% (n)	<1%
ToT@20ke$^-$	30.2ns	28.6ns

- **Fully working, no difference to PP-Modules**

Comparison of Serial Powering Schemes

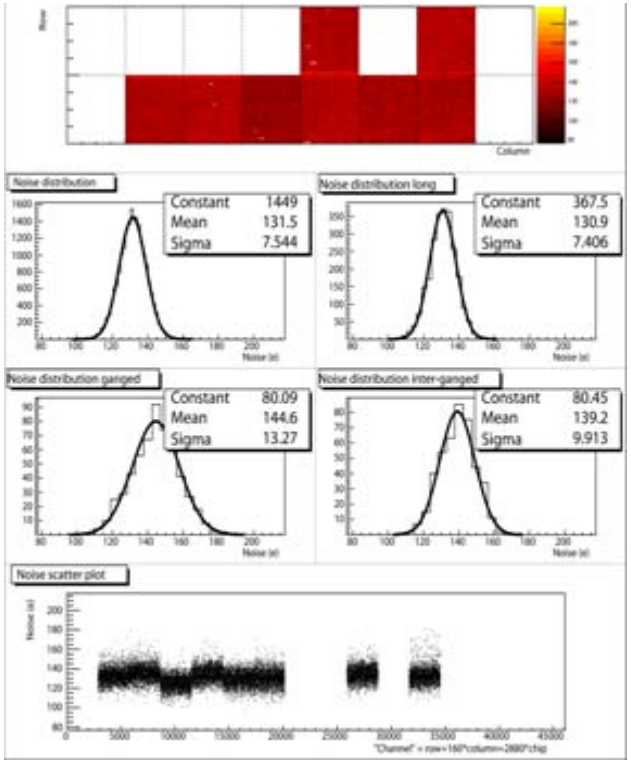
- Basic Scheme
  - Uses: DSHUNT 2,0V and ALINREG 1,6V, MCC ~2,0V
- Extended Scheme
  - Uses: DOVER 2,7V, ALINREG 1,6V and DLINREG 2,0V for FE+MCC
- MCC Extended Scheme
  - Separate Regualtor for MCC



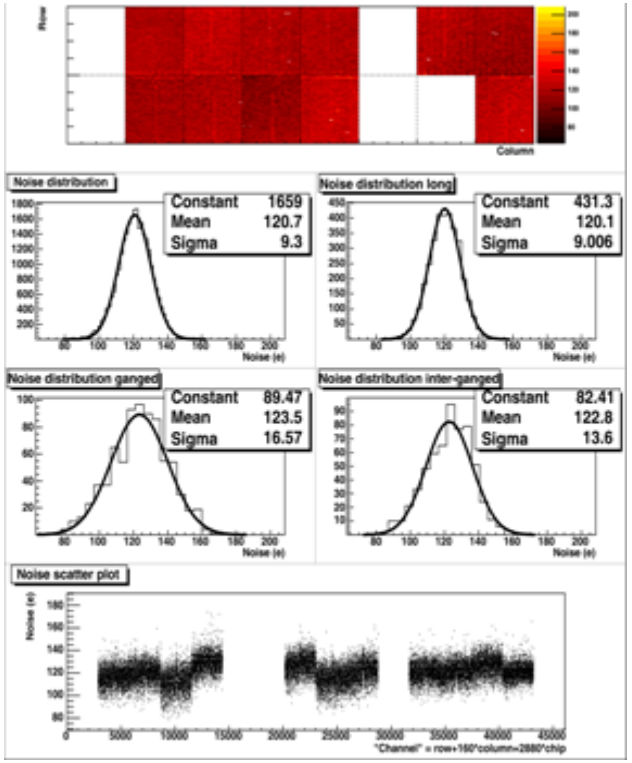
Comparison of Serial Powering Schemes

- Three **I3** Modules with different schemes
  - Noise map:

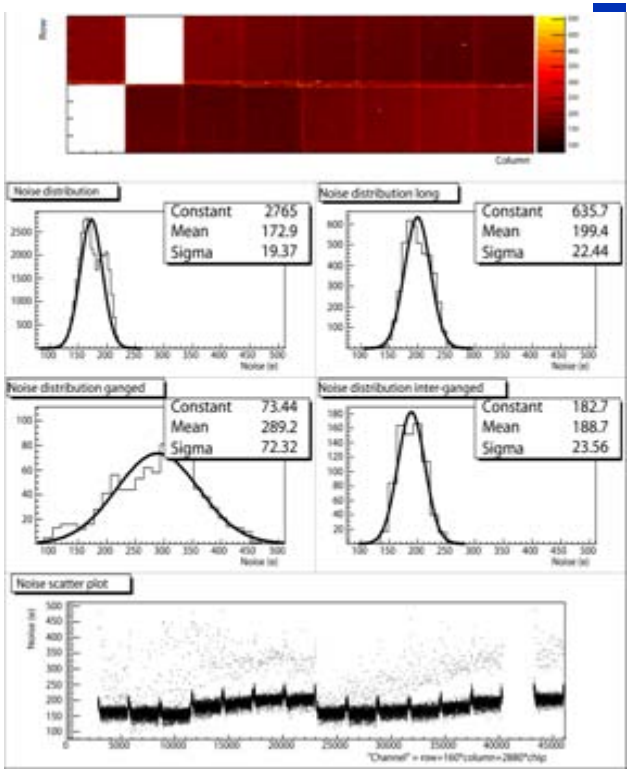
Basic
(no sensor)



Improved
(no sensor)



separate MCC-Regulator



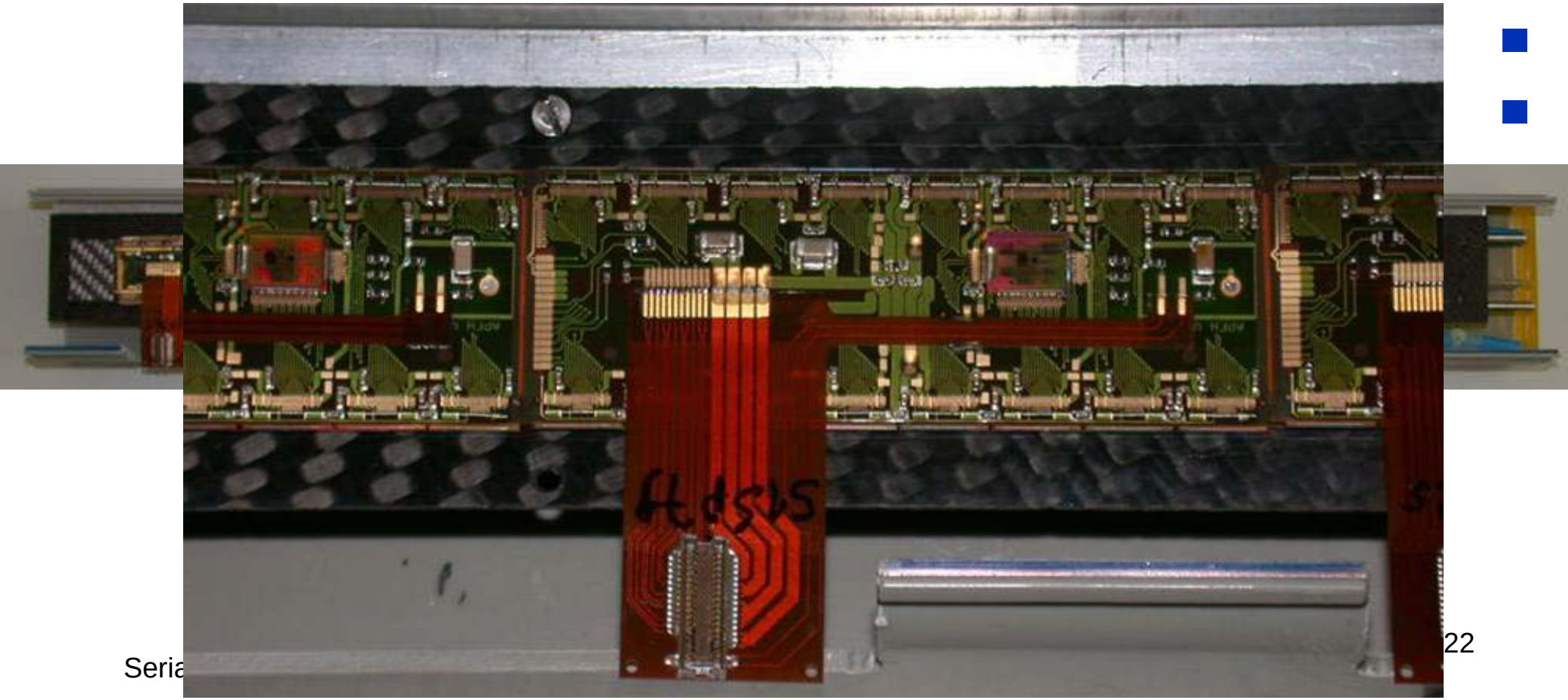
Comparison of Serial Powering Schemes

	Basic (no sensor)	**Extended** (no sensor)	**MCC Extended**	**Parallel Powered Module** (510970)
Threshold [e^-]	4143	4132	4194	4189
Dispersion [e^-]	52	51	73	75
Noise [e^-]	134	121	179	196

- No difference between schemes, no difference to PP modules
- Decided to use the improved scheme, simple, flexible and DLinReg can handle extra load

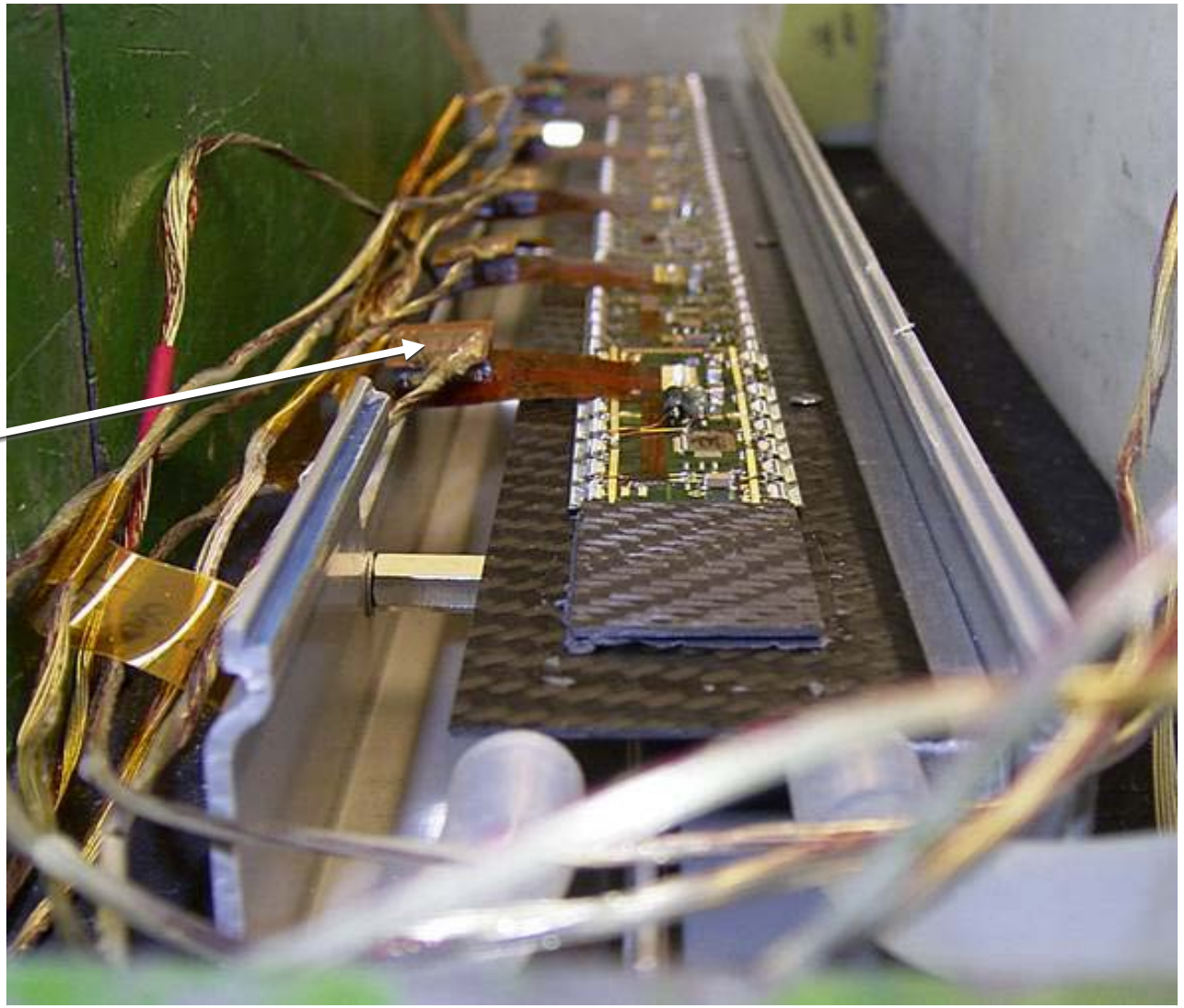
Serial Powering Dummy Half-Stave

- 6 Modules (4 with full Serial Powering scheme)
  - Dummy carbon-support-structure with cooling pipe



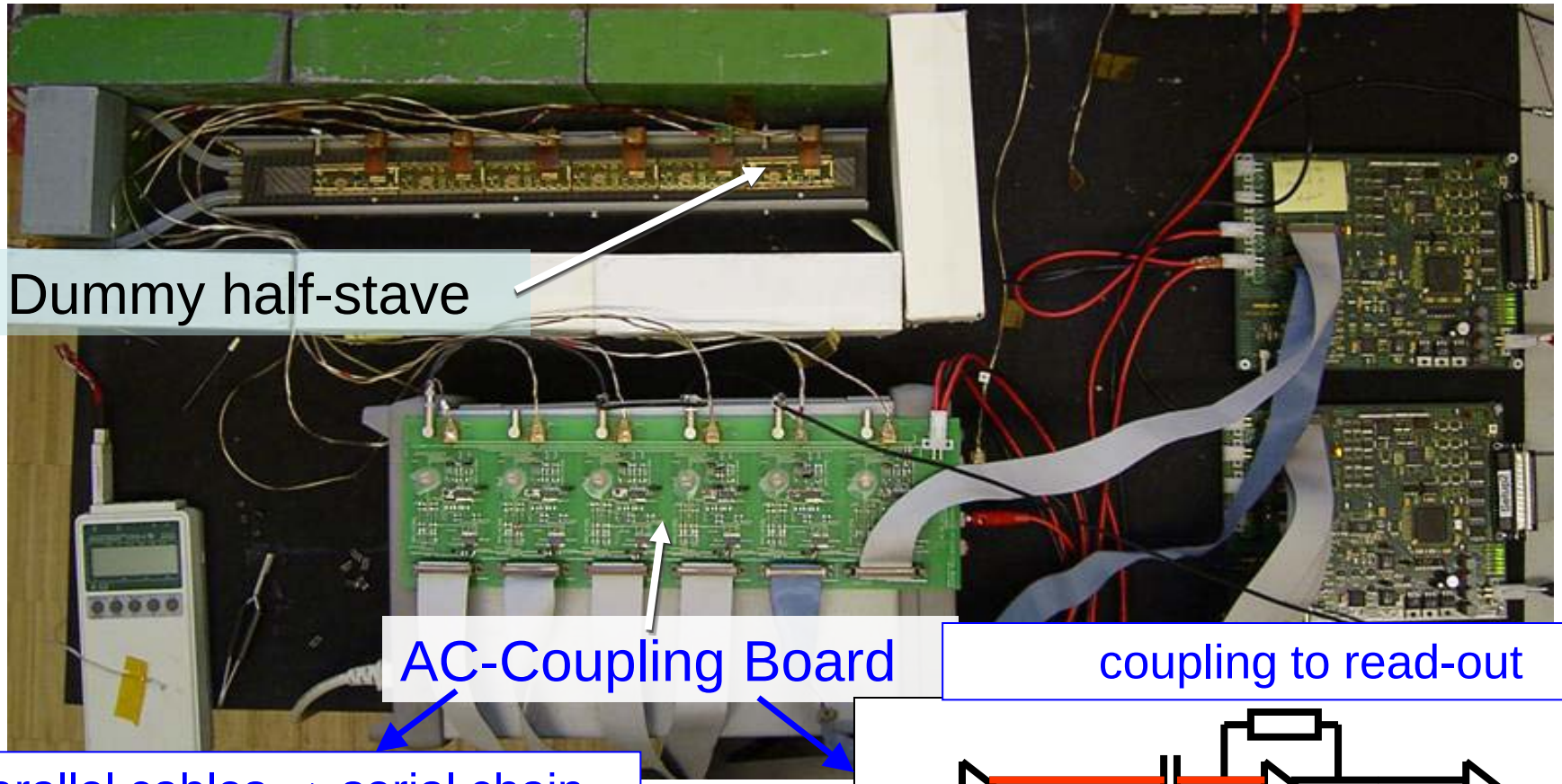
Serial Powering Dummy Half-Stave

PP cables,
serial routing done by
AC-Coupling Board



Serial Powering Dummy Half-Stave

- AC-Board & 2 std. module test systems: full read-out

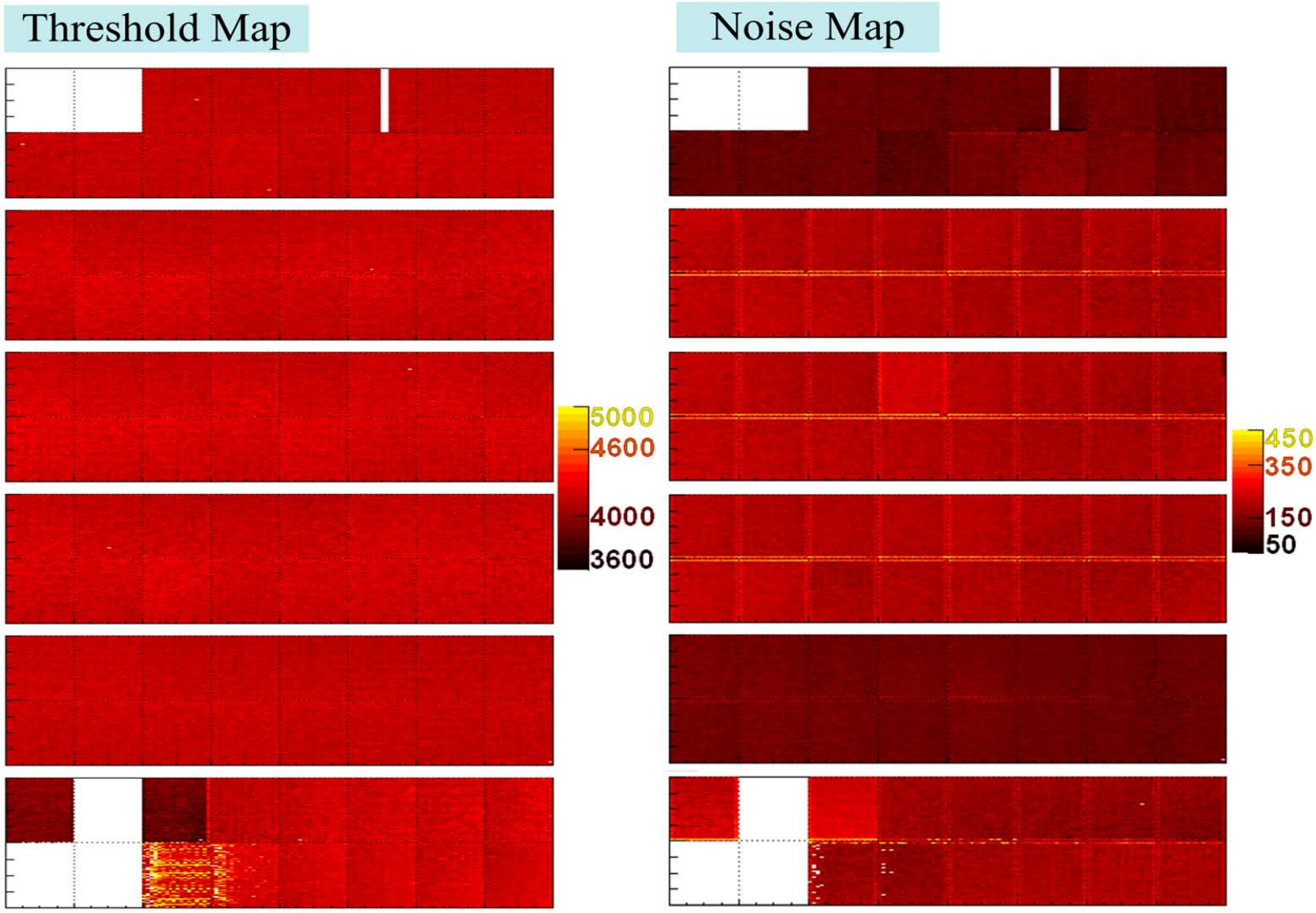


Noise Measurements on Dummy Half-Stave

- **Full half-stave operation, as good as single module operation?**

- Pseudo-parallel read-out:
  - XCK and STROBE to all six modules at the same time
  - Threshold scan performed on all modules, read-out of two modules at the same time

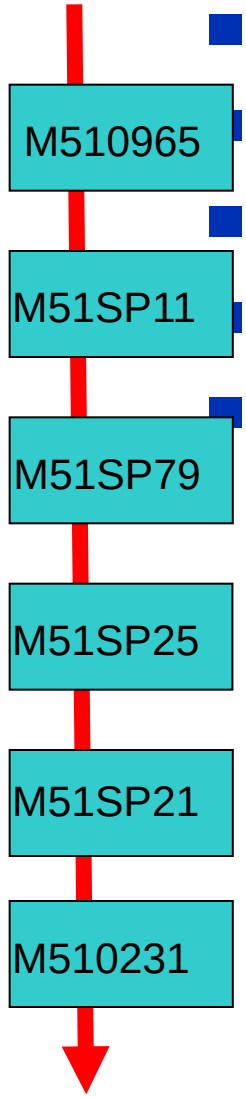
Noise Measurements on Dummy Half-Stave



Noise Measurements on Dummy Half-Stave

Threshold [e^-] (Dispersion [e^-])	Noise [e^-] (Δ to single SP powered [e^-])
4134 (57)	127 (4.4)*
4156 (69)	182 (-0.6)
4173 (70)	186 (-0.3)
4162 (70)	184 (-4.4)
4132 (58)	133 (0.0)*
4160 (91)	172 (-5.3)

*no sensor



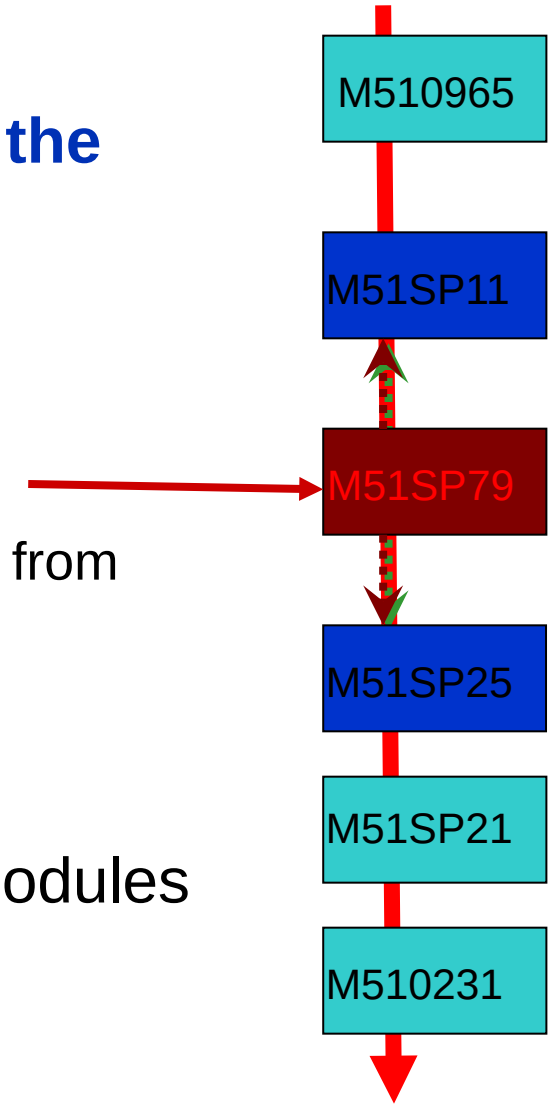
- **No difference to single-module operation and to Parallel Powered modules**

Induced Noise Pickup

- **Do other modules pick up noise through the power lines?**

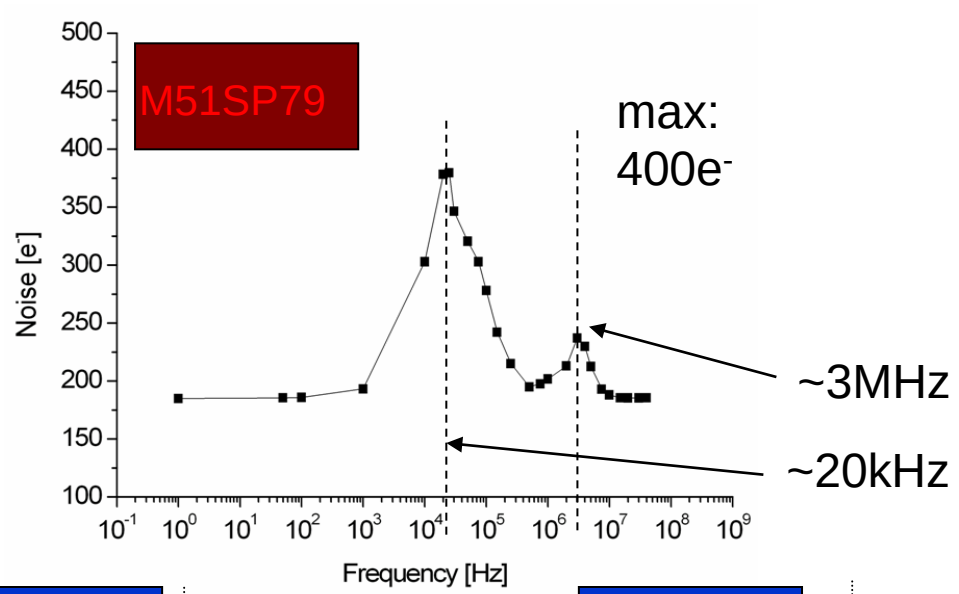
- Noisy module achieved by
  1. setting **threshold to 0**
  2. a **parallel, switching load**
     300mA to 500mA, frequencies up to 40MHz

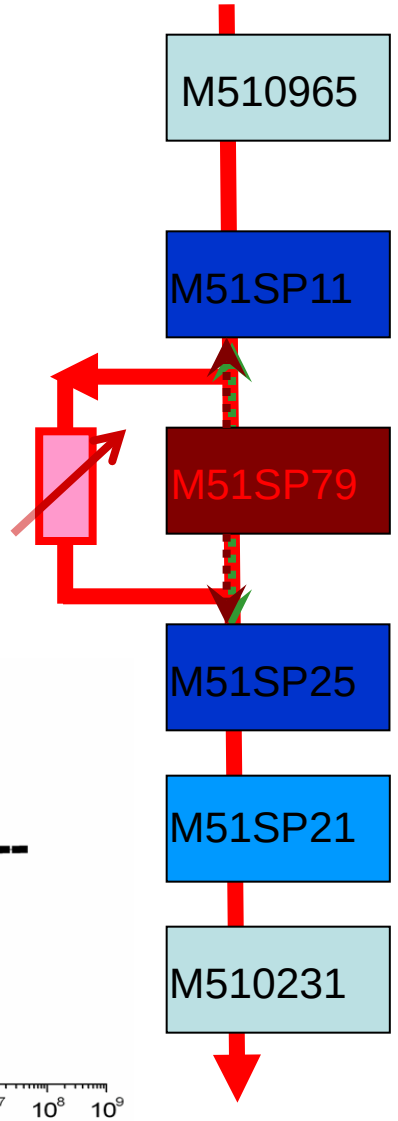
- “Parallel” threshold scan performed on all modules



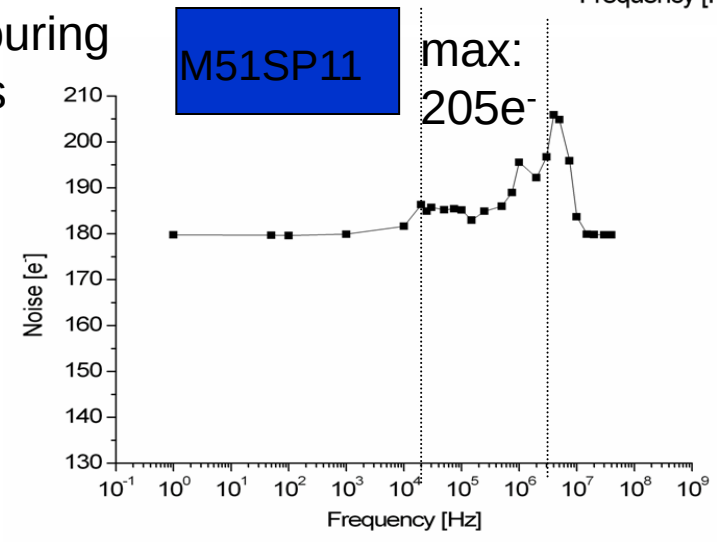
Induced Noise Pickup: frequency dependence

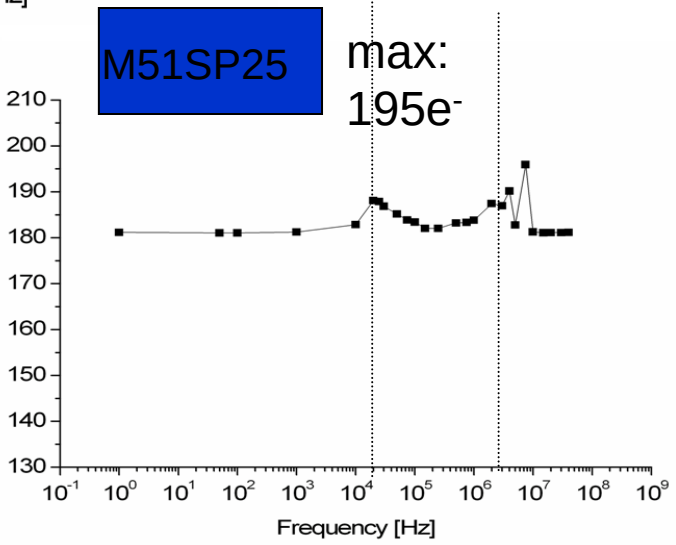
Module parallel
to switching load





Neighbouring
modules





Induced Noise Pickup: threshold=0 on 1 module

Noise difference [e^-] to normal half-stave operation

Thresh=0	M510965	M51SP11	M51SP79	M51SP25	M51SP21	M510231
M510965	noisy	6.0	-0.2	-0.6	9.7	-0.4
M51SP11	13.5	noisy	2.1	9.4	1.6	2.0
M51SP79	1.7	10.2	noisy	1.8	1.3	1.6
M51SP25	1.6	5.4	1.7	noisy	15.2	1.7
M51SP21	13.3	-0.4	-0.3	-0.4	noisy	-0.2
M510231	2.7	9.0	2.9	9.5	19.7	noisy

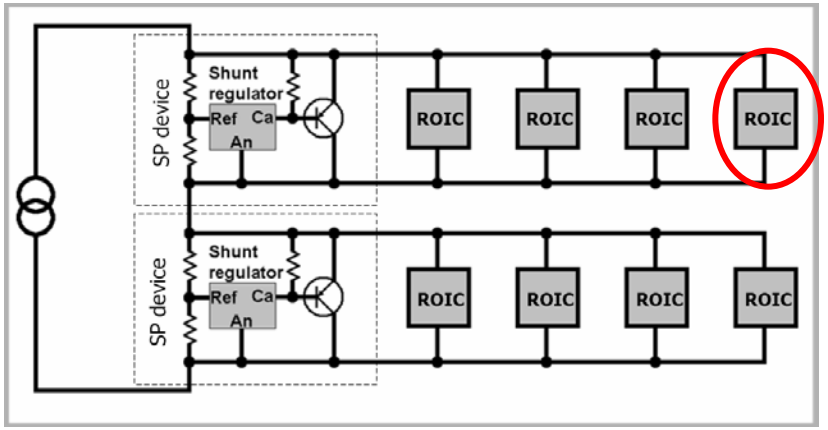
Voltage Regulators

On-chip or Off-chip Regulators?

- Figure of merit (FOM) for silicon detectors (load resistance) x (active area)
  - of order of 10Ω.cm^2 for pixel and 100Ω.cm^2 for strip detectors.
- FOM for converters: ε/(1-ε) x (output resistance) x (rad. Thickness) x (area)
  - Ratio of converter/detector gives the radiation thickness penalty for using converters in active areas.
  - Typical FOM of external converters are in the order of 1-5%RL.Ω.cm^2 at 80% efficiency.
  - This gives a penalty of 0.5%RL per layer for pixels and ~0.05%RL for strips.
- But a penalty >0.2%RL per layer is regarded as too severe! → only strips can use external converters!
- Pixel detectors must use internal (on-chip regulators) which usually have a FOM of less than 0.5%RL.Ω.cm^2 (just the external blocking capacities)

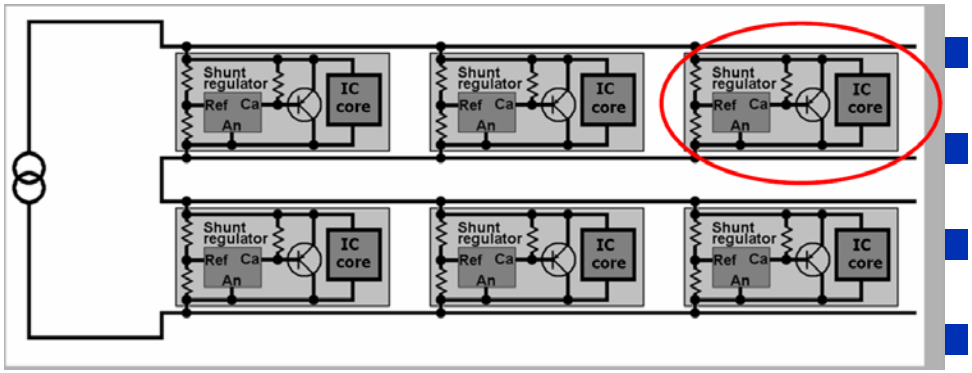
Serial Powering Schemes

1) External shunt regulator + transistor



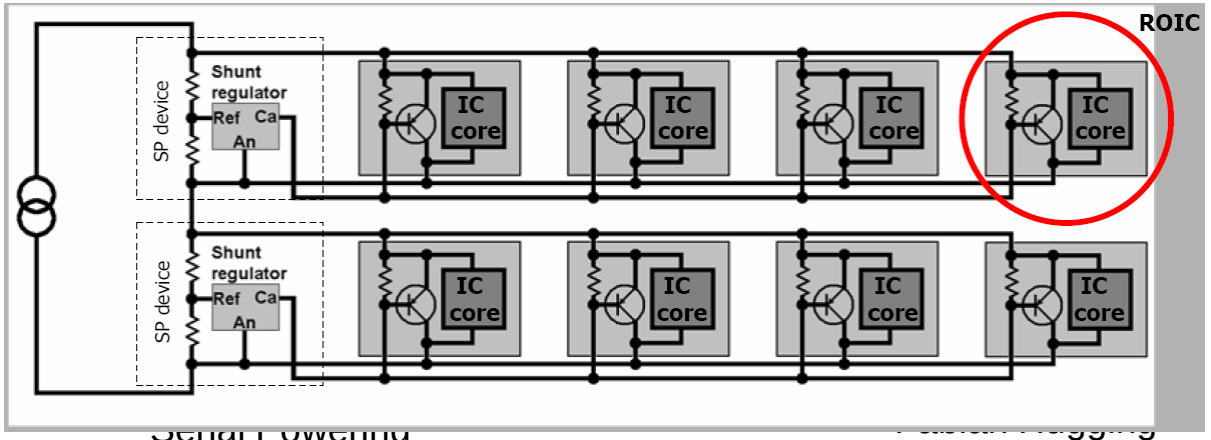
implies a **high current shunt**
SP device enables to operate non SP-ROIC in SP mode

2) Internal shunt regulator + transistor in each ROIC



Disadvantage: many power supplies in parallel
Matching issue can cause hot spots and potentially kill chips
adjustment/trimming scheme needed

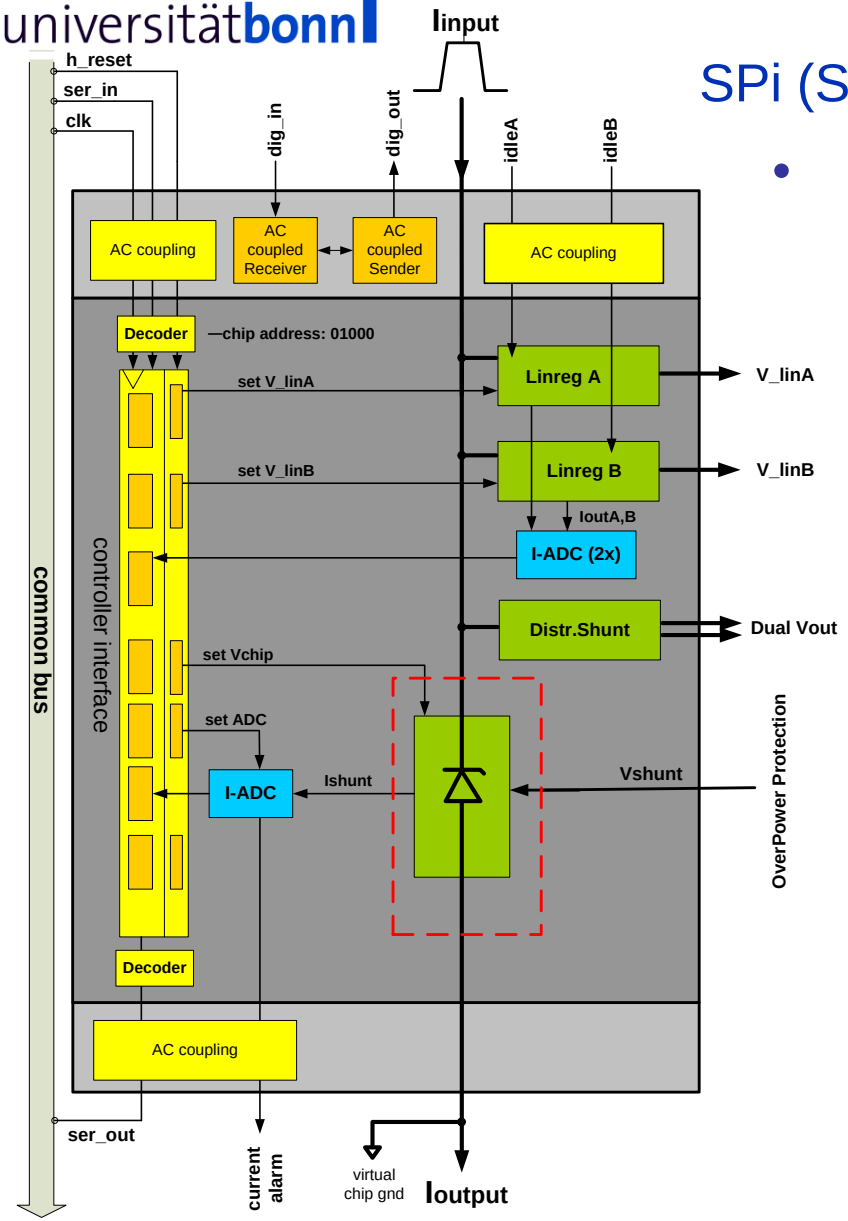
3) External SR + parallel shunt transistor in ROIC



feedback however **more challenging** and depends on implementation

choice of architecture **not obvious**,
detailed studies anticipated by various groups
scheme (2) can be realized by any ROIC standalone
External Converters can cover scheme (1) and (3)

SPi – Architecture Overview



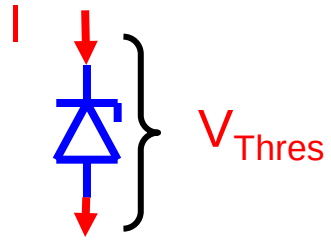
SPi (Serial Powering interface): versatile SP chip:

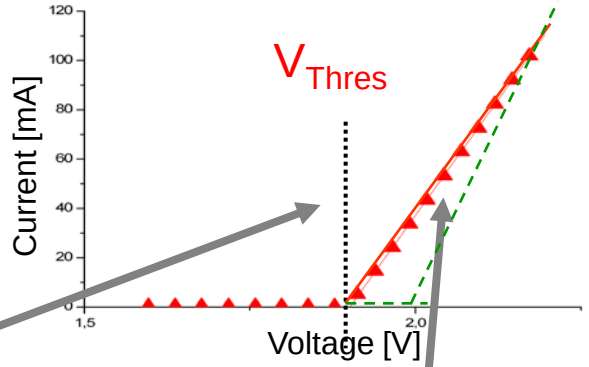
- list of basic features:
  - **shunt** creates Vchip (scheme1) , distr. shunt (scheme3)
  - communication via **multi drop** bus (each SPI chip has 5bit address) reduces number of str.-lines for SPI to minimum of 2 (3)
  - spare AC coupled interfaces (**comports**)
  - **ADC**s to monitor shunt and LR current
  - **2x LinReg**: separate analog / digital supply to hook up some chips (1-3) for tests. Not proposed as a scaleable solution for a whole module (linregs should be part of ROIC, as e.g. in the ABCn)
  - **OverPower** protection (avoids detector hot spots) (chip feature, needs external control)
  - **radtol. design** techniques, TSMC 025MM process

On Chip Shunt Regulators - FE-I3

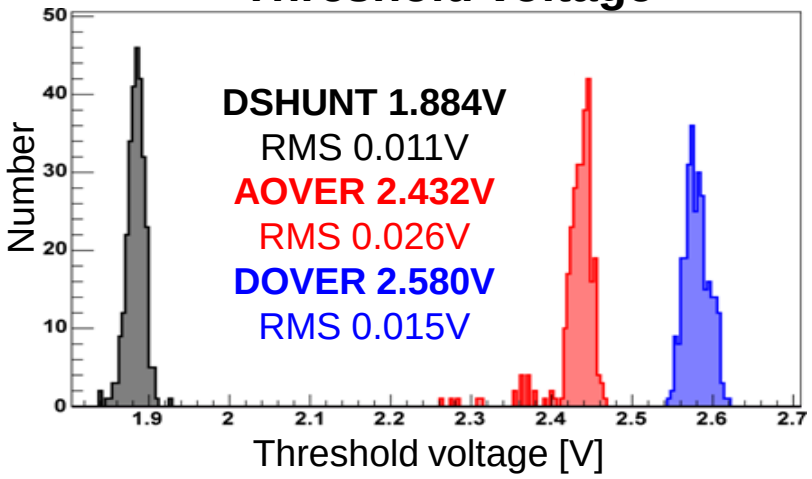
Designed by Laurant Blanquart

- Important properties:
  - Threshold voltage
  - Resistance
- 3 shunt regulators on chip:
  - DShunt (2.0V), AOver (2.4V) and DOver (2.7V)

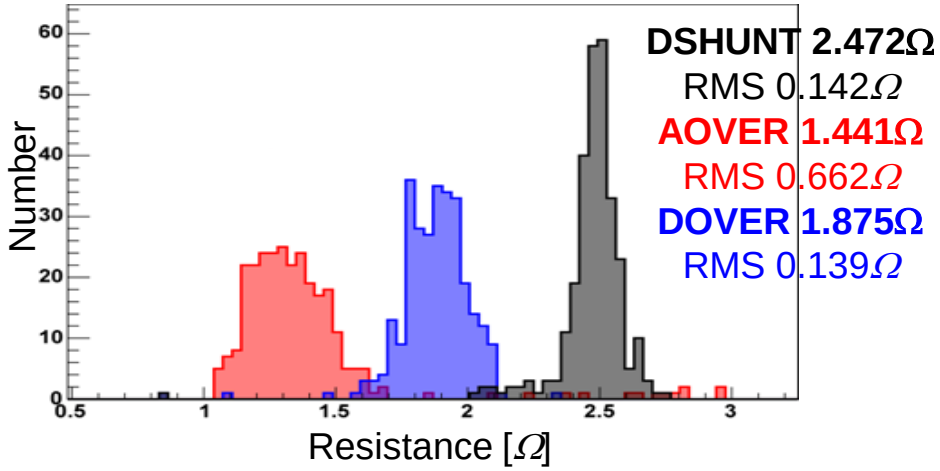




Threshold voltage



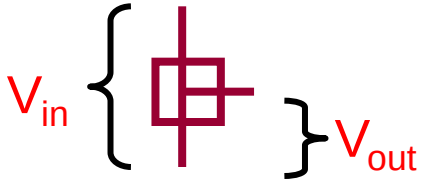
Resistance

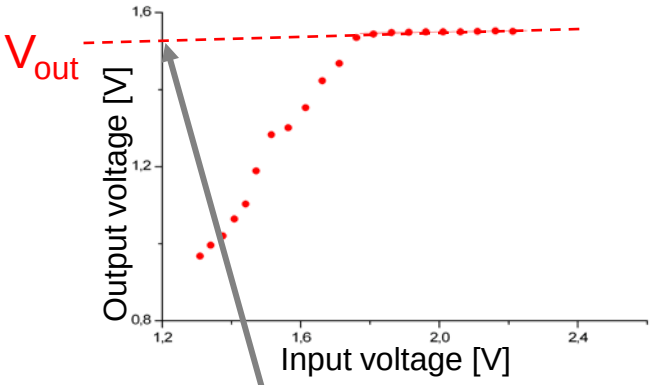


On Chip Linear Regulators - FE-I3

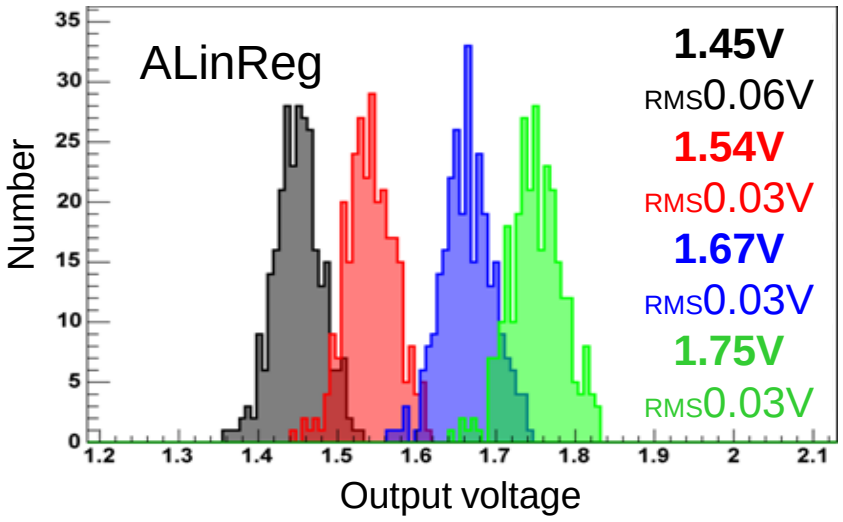
Designed by Laurant Blanquart

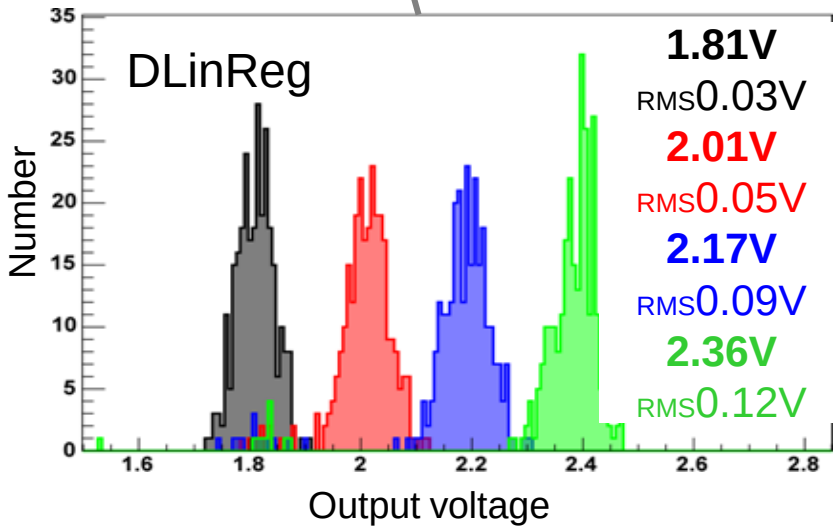
- Important properties:
  - Output voltage
  - Voltage drop ($V_{in} - V_{out}$)
  - Stability vs input voltage or vs load
- 2 linear regulators on chip:
  - ALinReg (1.5V-1.8V) and DLinReg (1.8V-2.4V), both in 4 steps



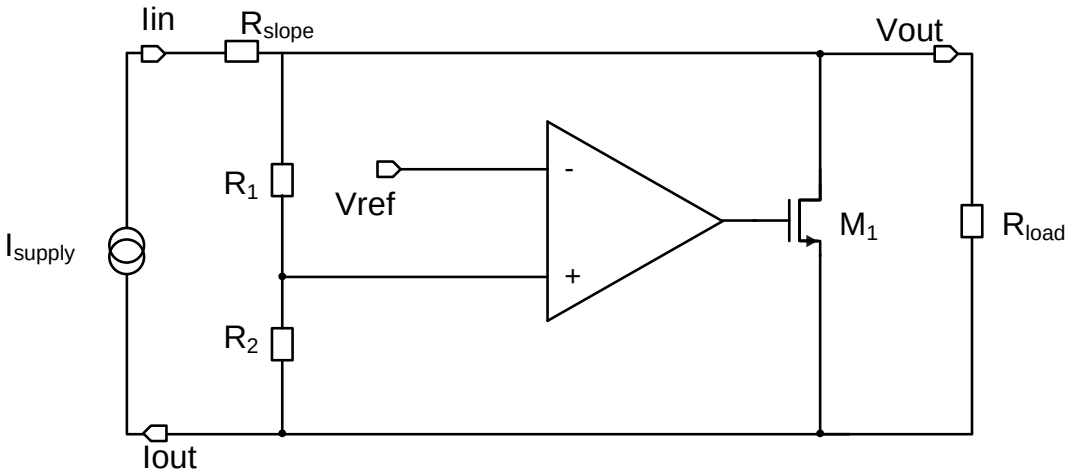


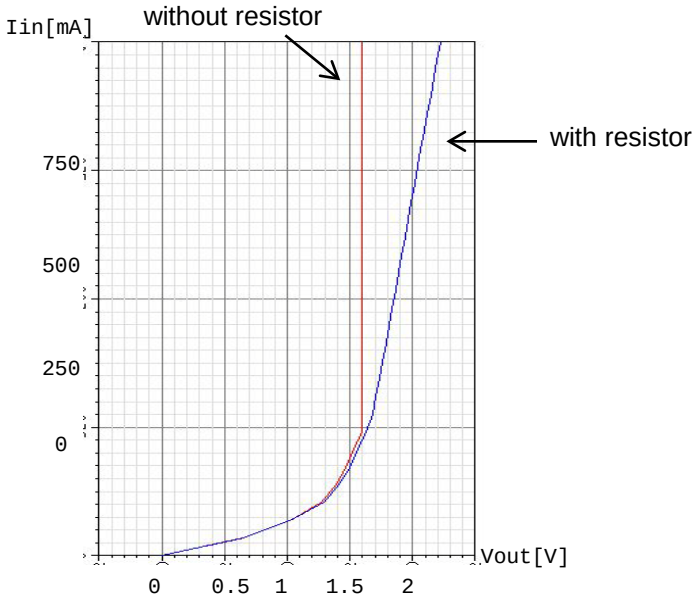
Output voltage of 277 chips:





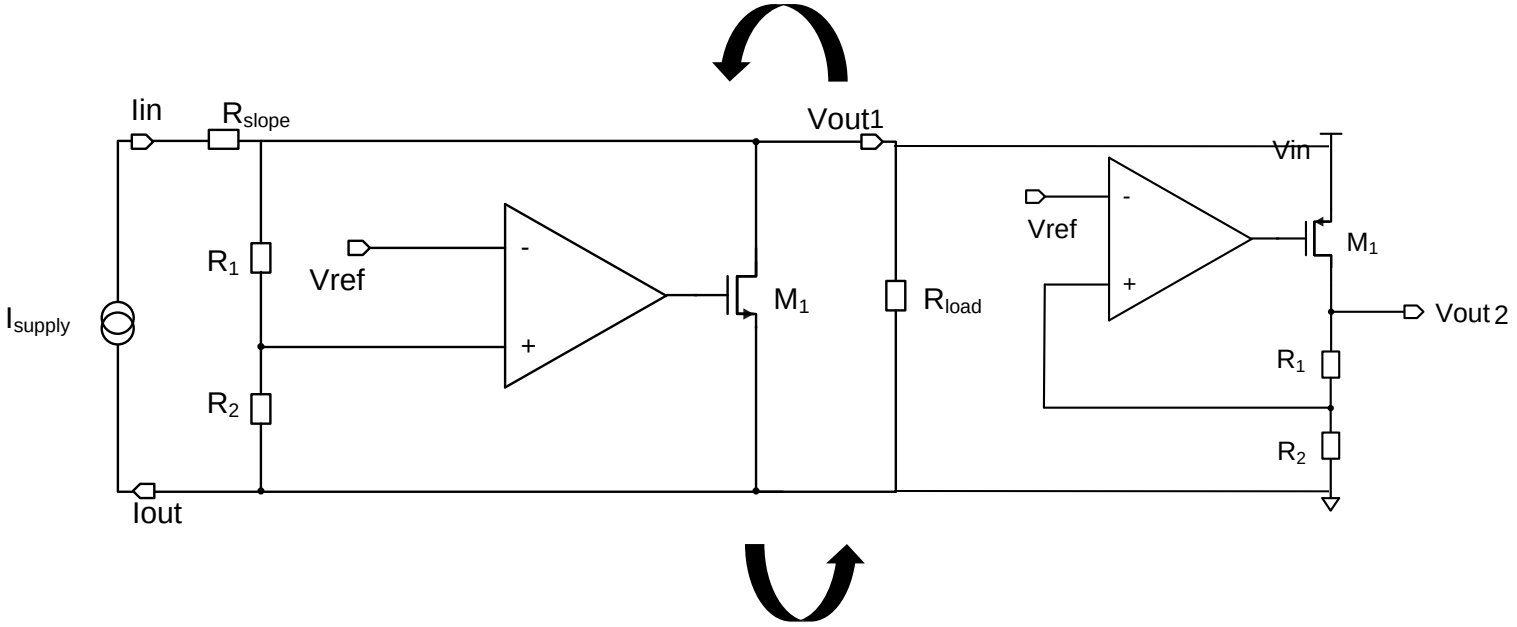
Shunt Regulator (FE-I3 approach)





- Shunt regulator generates a constant output voltage out of the current supply
- current that is not drawn by the load is shunted by transistor M1
- Very steep voltage to current characteristic
- Mismatch & process variation will lead to different Vref and Vout potentials
- Most of the shunt current will flow to the regulator with lowest Vout potential
- Potential risk of device break down at turn on
- Using an input series resistor reduces the slope of the voltage to current characteristic I=f(V)
- R_{SLOPE} helps distributing the shunt current between the parallel placed regulators
- R_{SLOPE} does not contribute to the regulation and consumes additional power

LDO Regulator (FE-I3 approach)

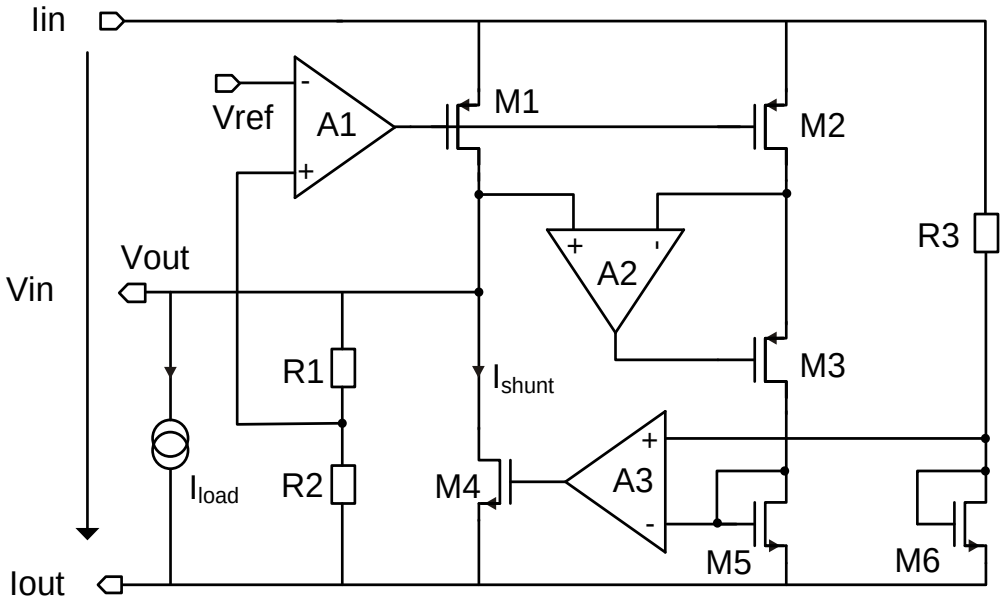


- Second supply voltage of lower potential is genareated by a LDO regulator powered by the shunt regulator
- The LDO power transistor operates like a regulated series resistor which controls the voltage drop between input output voltage to have a constant output voltage

- Change order of regulation chain
- R_{SLOPE} replaced by the LDO power transistor
- Shunt transistor connected to the LDO output

LDO Regulator with Shunt Transistor (ShuLDO)

Simplified Schematic

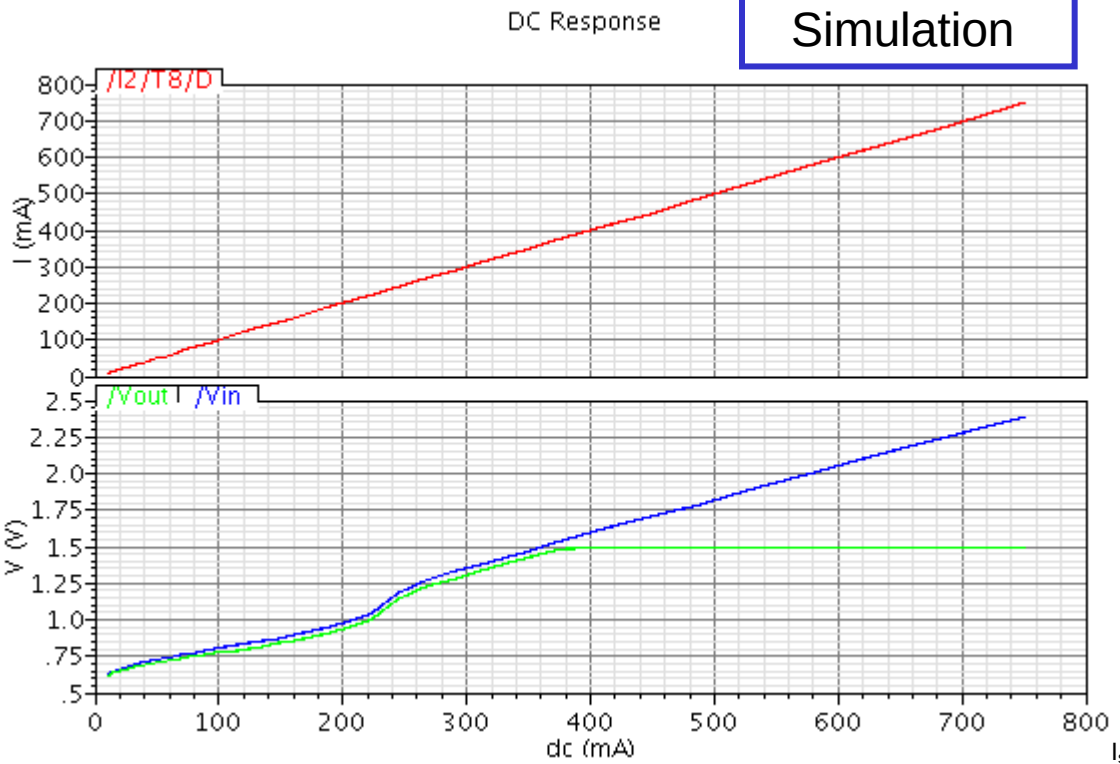


- Combination of LDO and shunt transistor
- M4 shunts the current not drawn by the load
- Fraction of M1 current is mirrored & drained into M5
- Amplifier A2 & M3 improve mirroring accuracy
- Ref. current defined by resistor R3 & drained into M6
- Comparison of M5 and ref. current leads to constant current flow in M1
- Ref. current depends on voltage drop V_{lin} which again depends on supply current Iin

- „Shunt-LDO“ regulators having completely different output voltages can be placed in parallel without any problem regarding mismatch & shunt current distribution
- Resistor R3 mismatch will lead to some variation of shunt current (10-20%)
- „Shunt-LDO“ can cope with an increased supply current if one FE-I4 does not contribute to shunt current e.g. disconnected wirebond → ref current goes up
- Can be used as an ordinary LDO when shunt is disabled

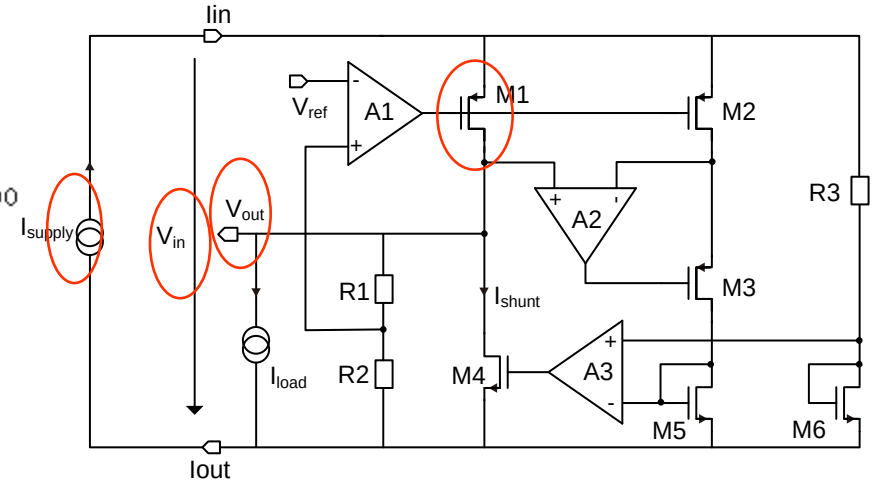
ShuntLDO Voltage Current Characteristic

Simulation



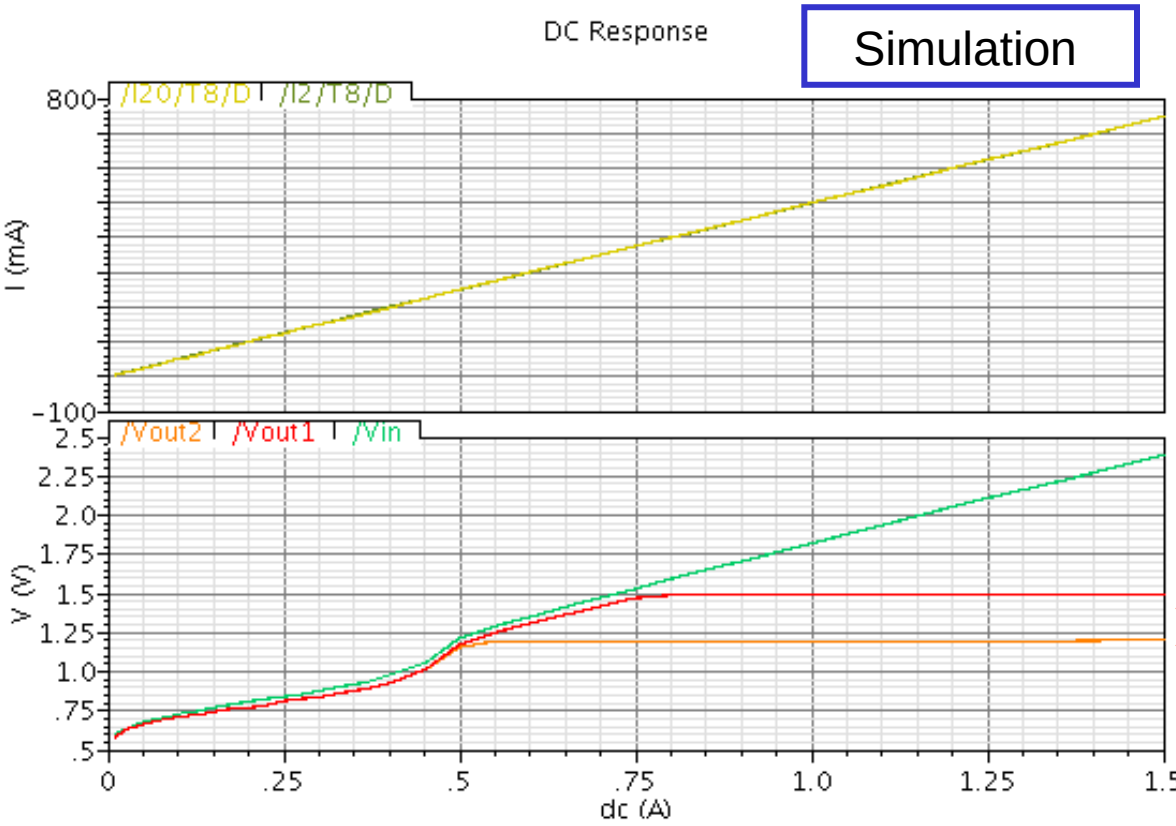
Current flowing through the regulator
(Power PMOS transistor M1)

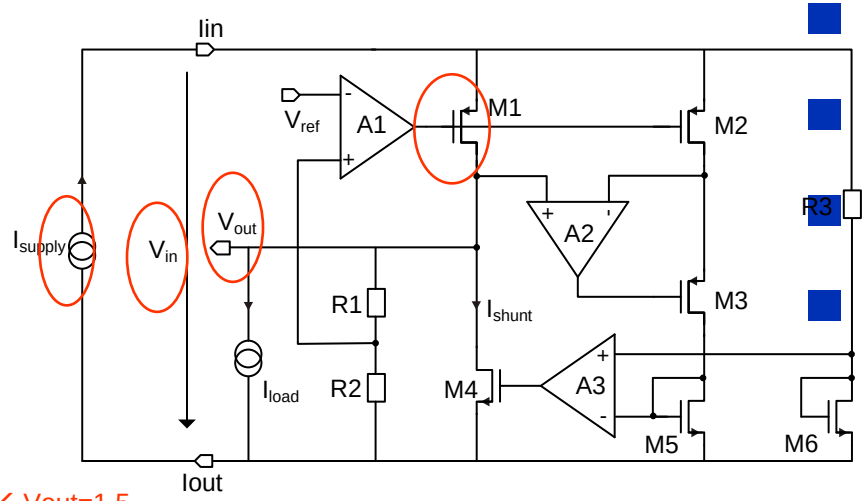
Vout Regulator output voltage (green)
Vin potential between Iin & Iout (blue)



- linear voltage to current characteristic
- slope is defined by reference resistor R3 divided by the current mirror aspect ratio 2kOhm/1000=2Ohm
- Output voltage stays stable as soon the amplifiers are saturated and the final value is reached.

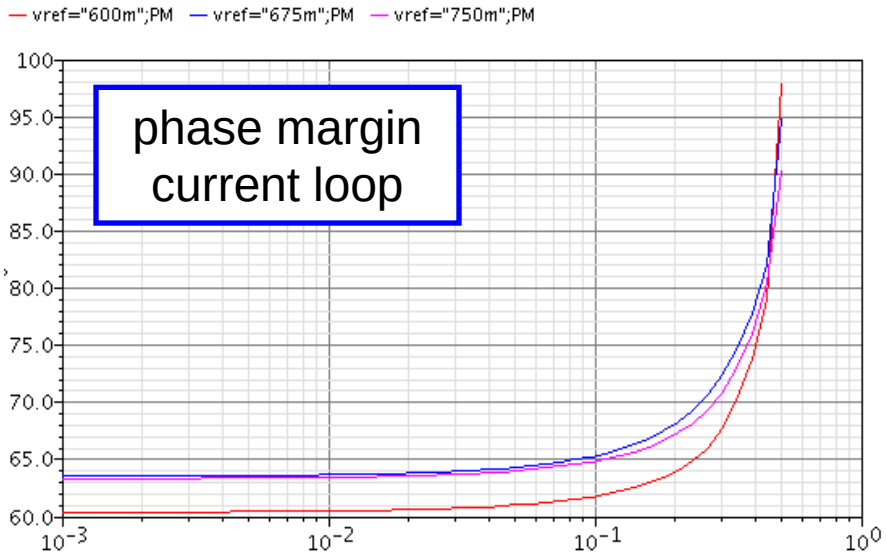
Parallel Regulator Operation

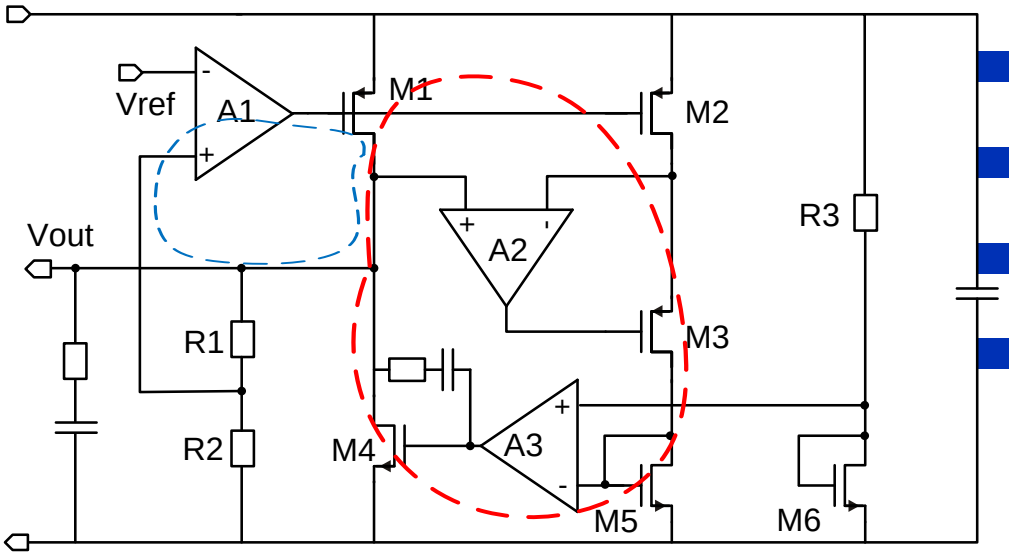




- 2 regulators placed in parallel with Vout1=1.2 and Vout2=1.5
- Output voltages settle at different potentials
- Current flowing through the regulator stays the same

Stability





Regulator consists out of two control loops:

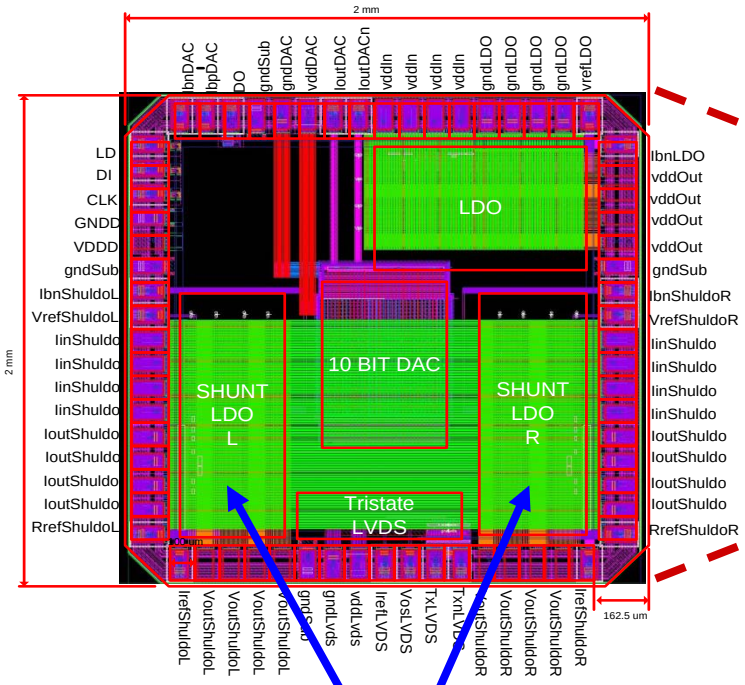
- A voltage based control loop for the output voltage regulation

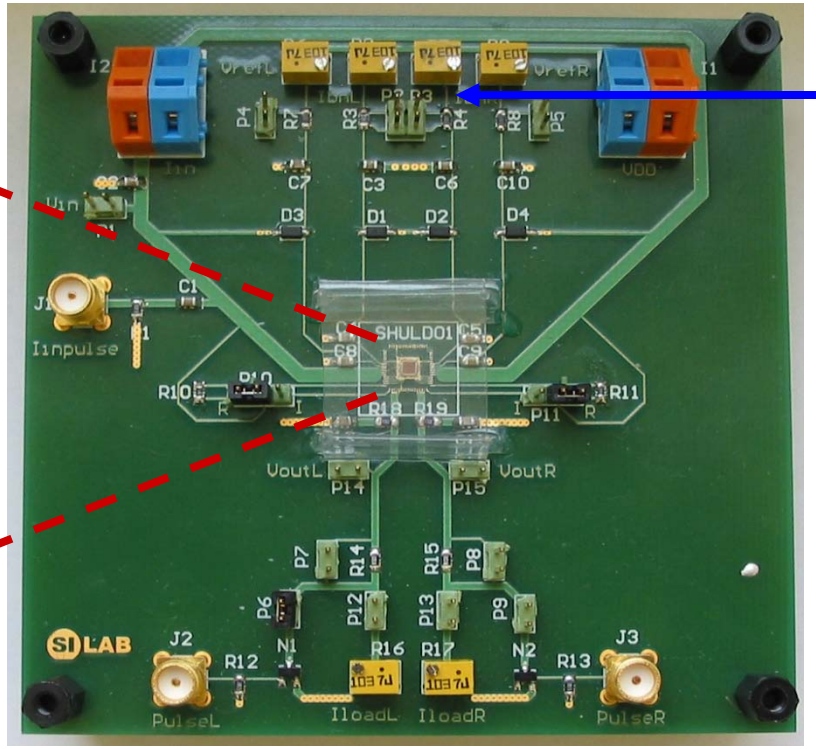
ESR of output capacitor used for stabilization (off-chip components)

- A current based control loop for the shunt current regulation

Stabilization by Pole-Zero Compensation (small on-chip components)

Setup for Test Measurements

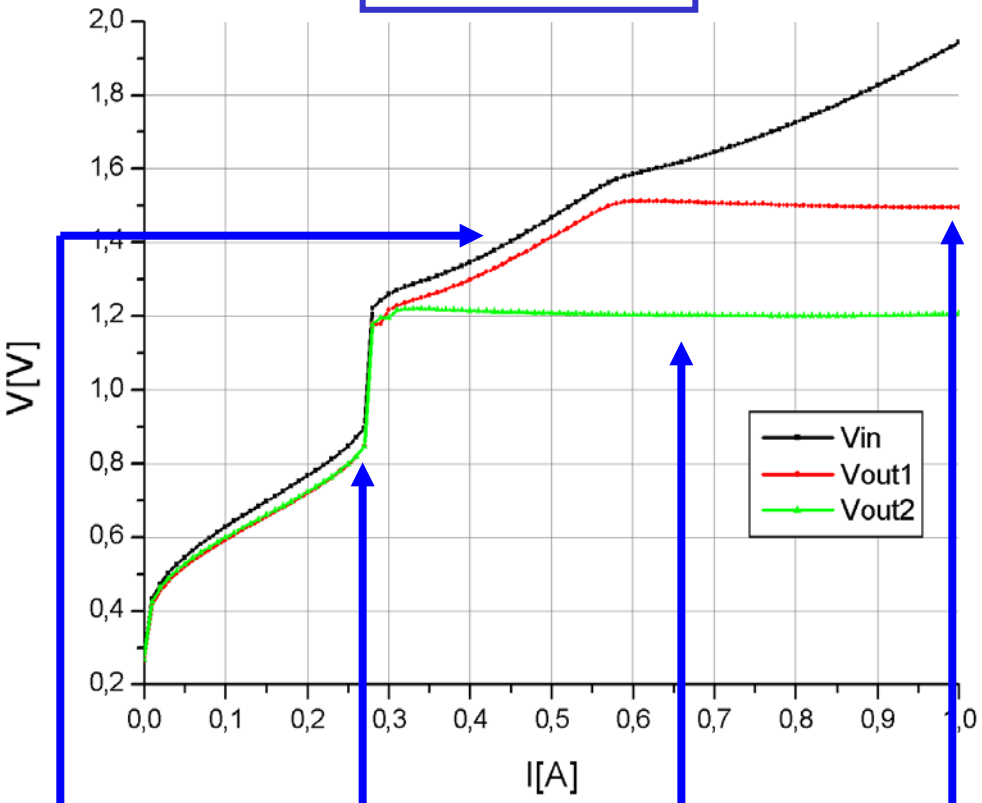




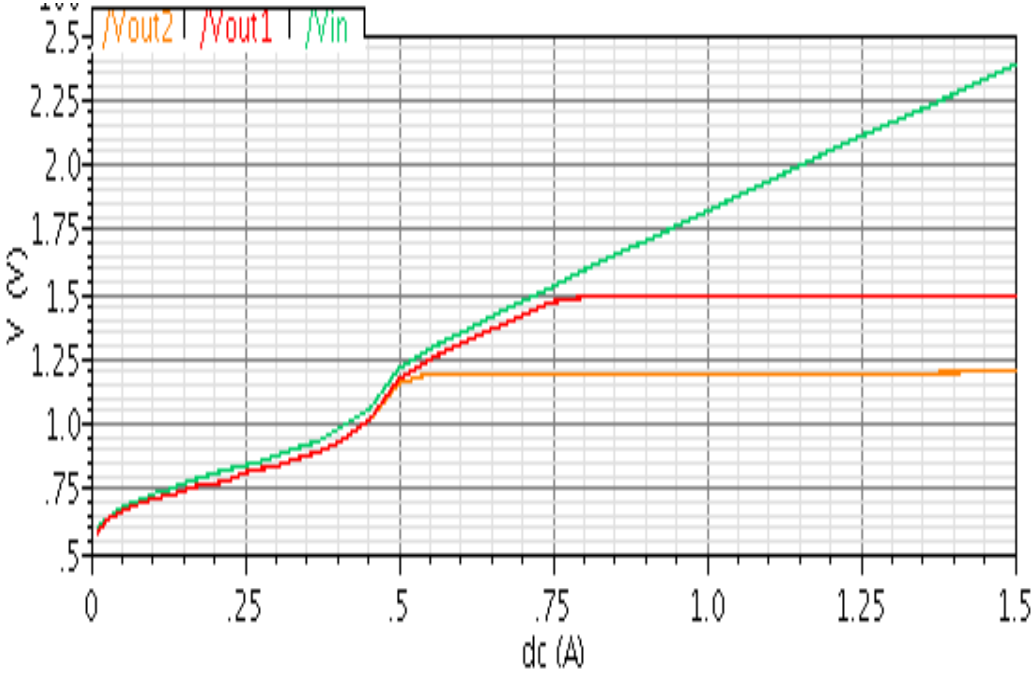
- Two Shunt – LDO regulators are connected in parallel on-chip
→ avoid influence of PCB parasitics
- biasing & reference voltage is provided externally
- input & load current is provided by programmable Keithley sourcemeter
- input & output voltages are measured automatically using a Labview based system

Two Shunt-LDO parallel connected on-chip

Measurement



Simulation



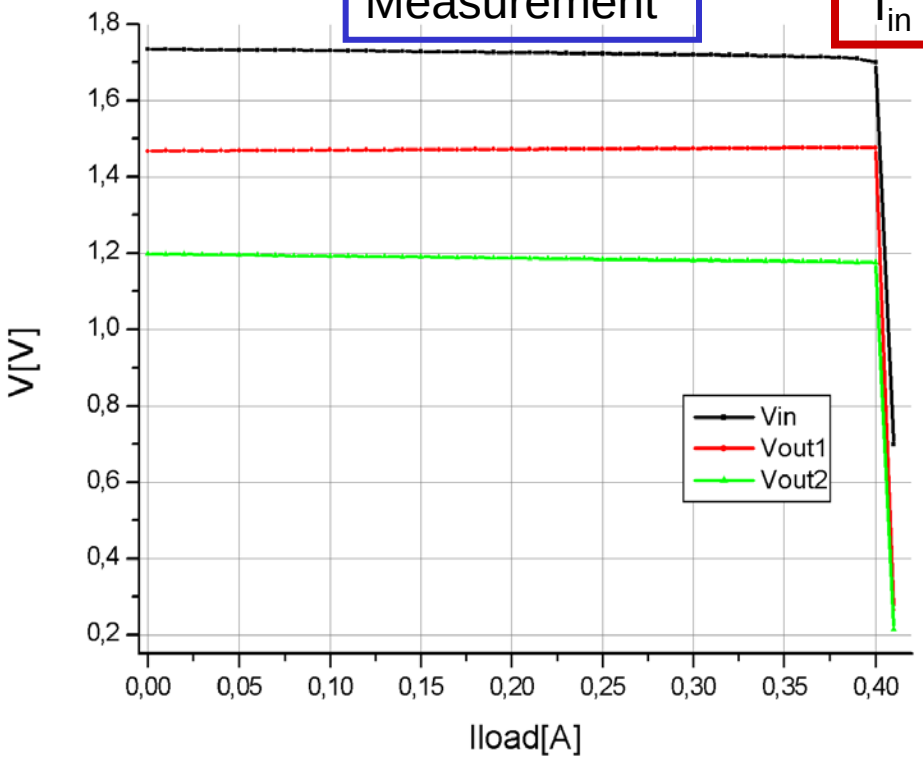
- Saturation point is reached for smaller input currents and is more abrupt than in simulation
- Non constant slope of Vin
- Vout1 and Vout2 slightly decrease with rising input current

→ IR drop on ground rail leads to smaller effective reference voltage

Load Regulation Measurement

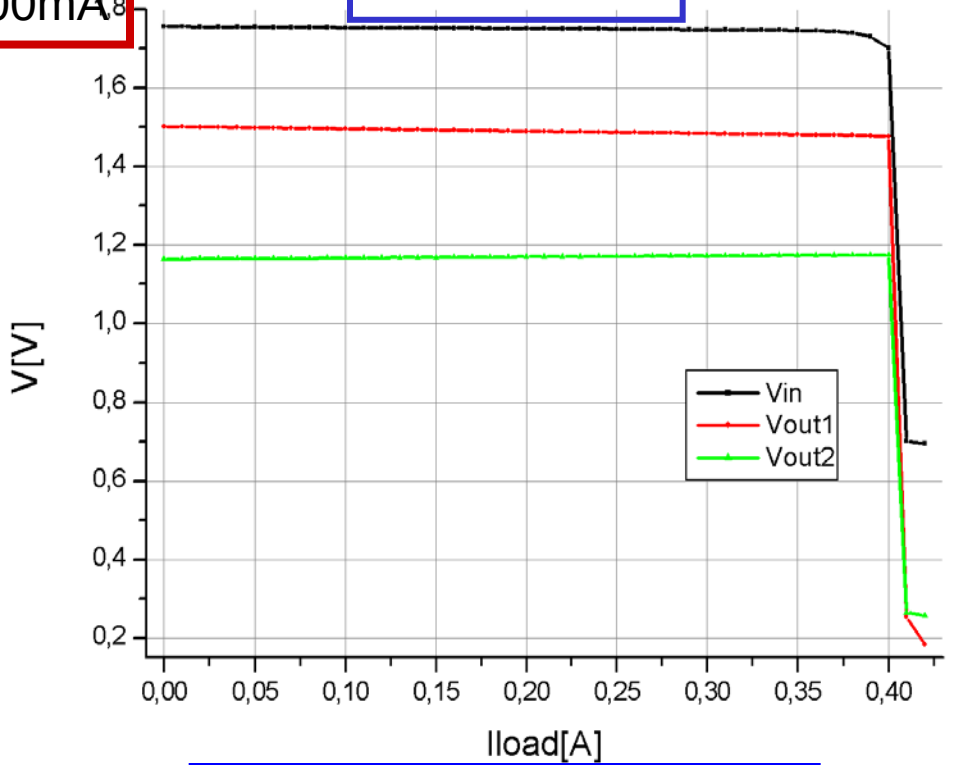
Measurement

I_{in} = 800mA



1.5V output voltage sees a fix load I=400mA
1.2V output has variable load Iload

Measurement

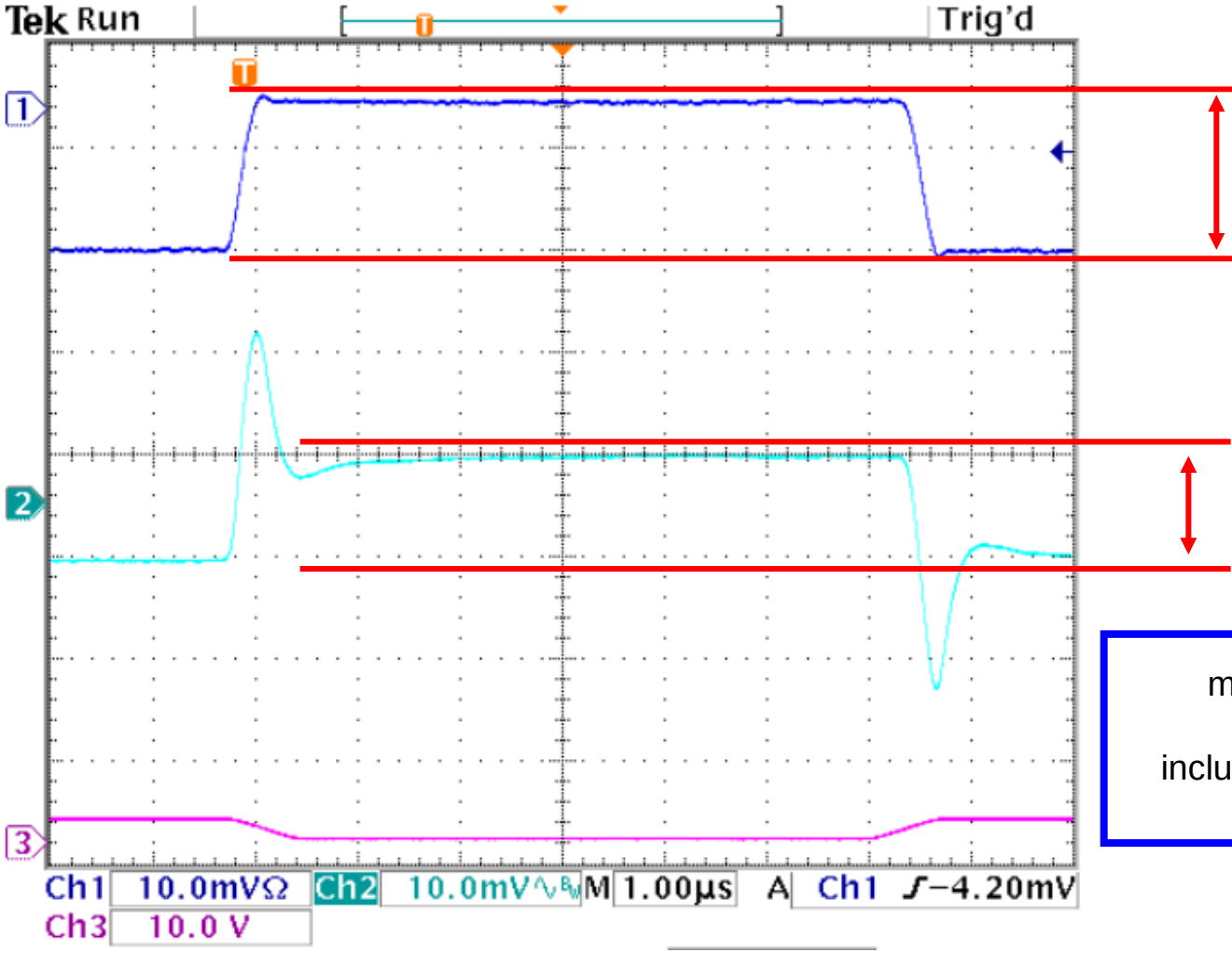


1.2V output voltage sees a fix Iload=400mA
1.5V output has variable Iload

Input & output voltages collapse when the overall load current reach the input current value

Effective output impedance of R = 50-60 mOhm (incl. wire bonds & PCB traces)

Load Transient Behaviour

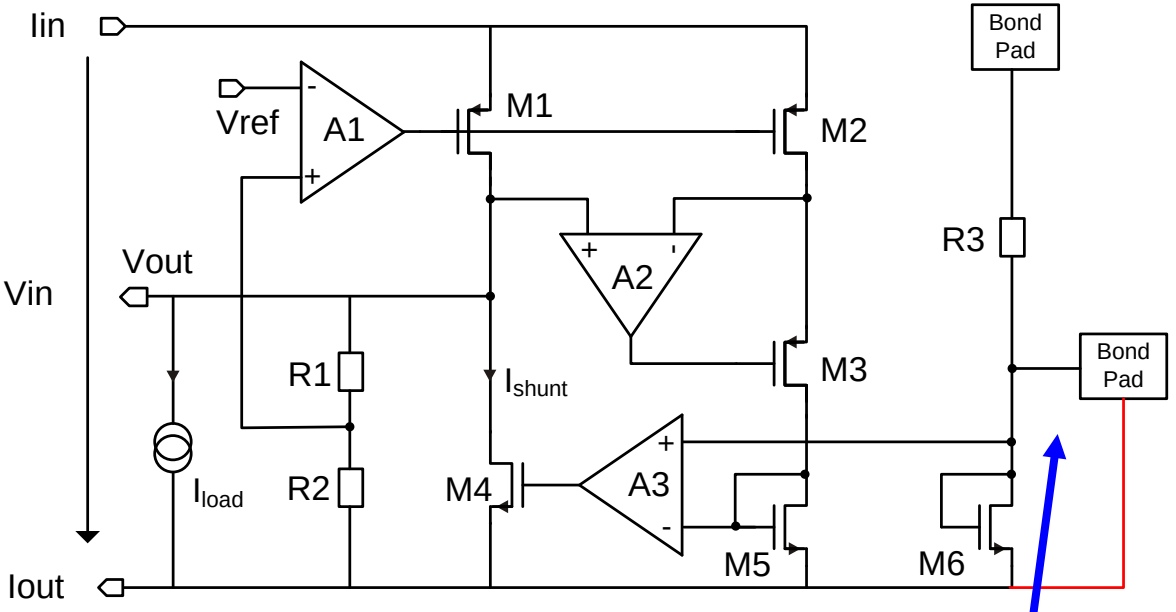


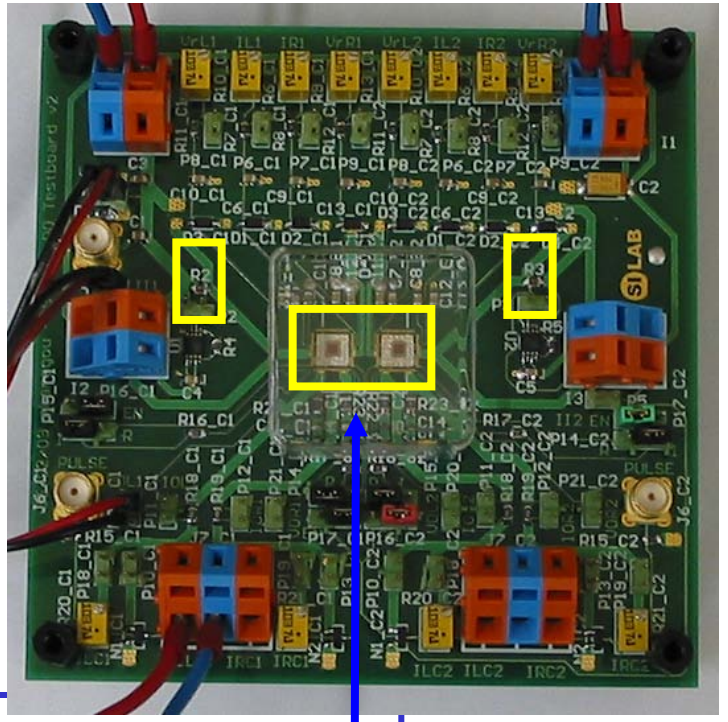
load current pulse of 150mA
15mV measured across
100mOhm

10mV output voltage change

measured output impedance
Rout=66mOhm
including wire bonds & PCB traces

Setup for Measurement of Shunt Currents

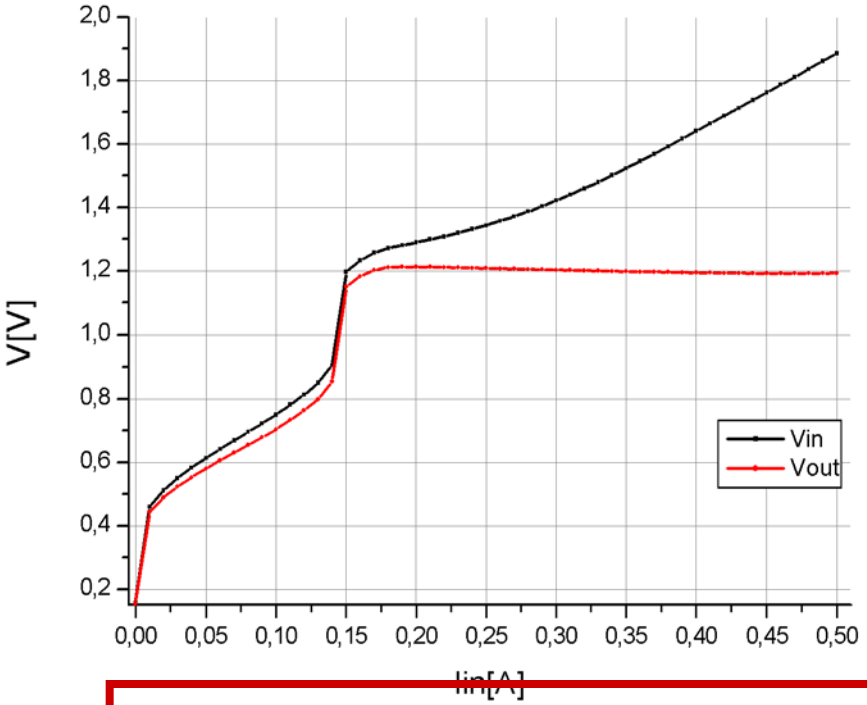




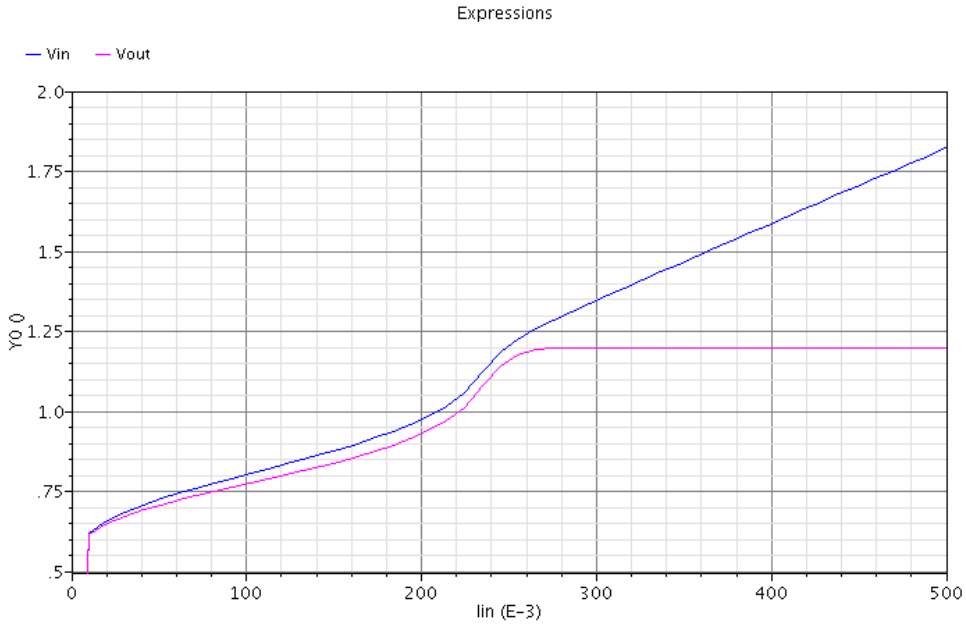
- direct measurement of shunt current distribution is not possible
  → regulators are connected in parallel on-chip
- shunt capability can be switched-off by defining zero reference current
→ use of special dedicated bond pads
- two SHULDO test chips connected in parallel on PCB level
→ each test chips has one operational regulator and one regulator switched-off
- shunt current is measured by 10 mOhm series resistors & instrumentation opamp

Single Shunt Operation

Measurement

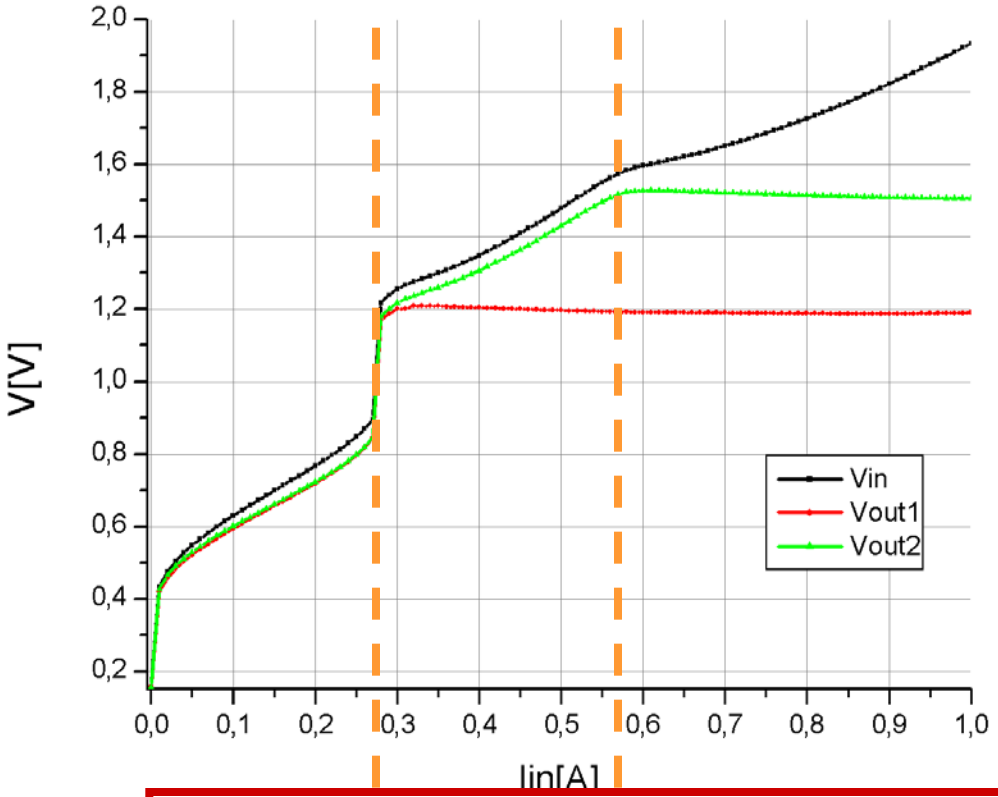


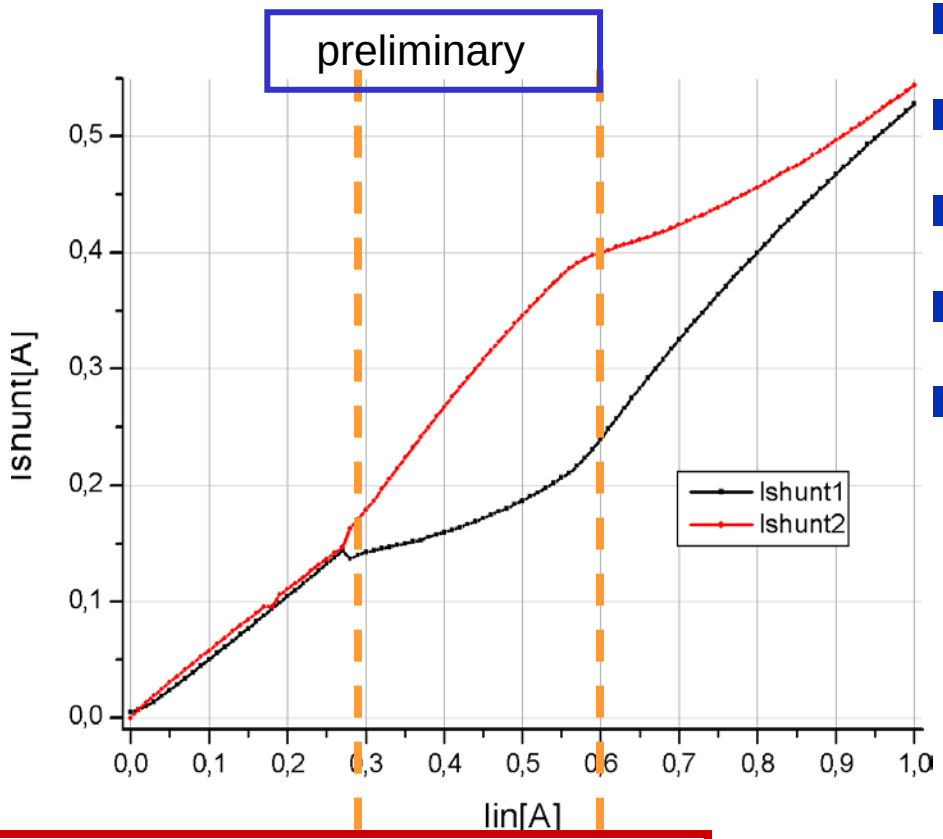
Simulation



Input voltage potential level around ~1.9 is reached with half of the current (500mA) with respect to parallel operation of two regulators
→ Shunt capability of 2nd regulator is switched-off

Current Distribution Measurement





- Unbalanced shunt current distribution unless both regulators are saturated
- More shunt current is flowing through the regulator which saturates first
- Non-constant slope of input Voltage closely related to shunt current distribution

Power efficiency

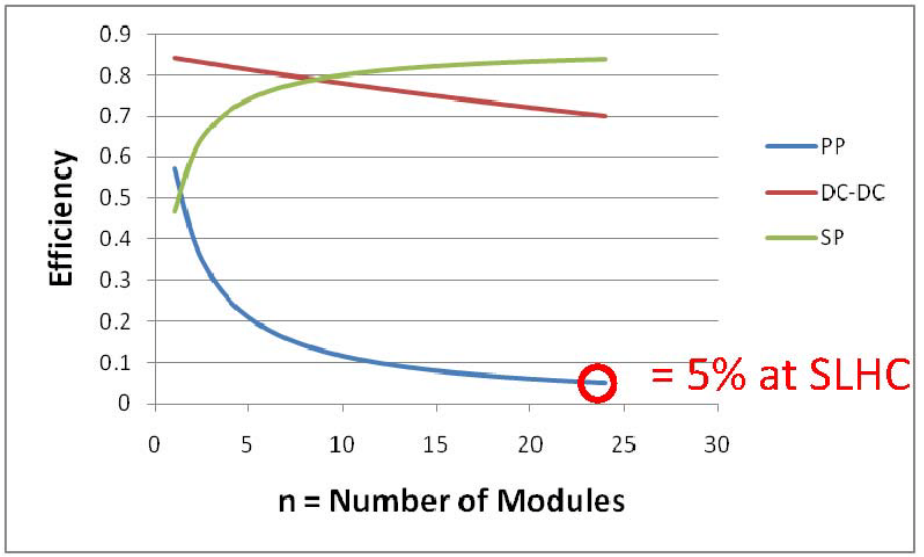
- Power efficiency comparison between SP and DC-DC using realistic scenario for ATLAS strip detector:
  - is defined as power needed by FE / power delivered to FE
  - for DC-DC decreases with number of modules
  - for SP increases with number of modules
- Both are feasible in terms of power efficiency

I = hybrid ABC-X current = 1.5A
V=ABC-X (130 nm) voltage = 1V
m=Vin/Vout for DC-DC = 10
n = number of modules on stave
$\varepsilon = P_{out}/P_{in}-1$ = 0.15
$\delta = I_{shunt}/I$ = 0.15
R = cable resistance = .5 Ω

$$\text{PP Eff} = \frac{nIV}{nIV+(nI)^2R}$$

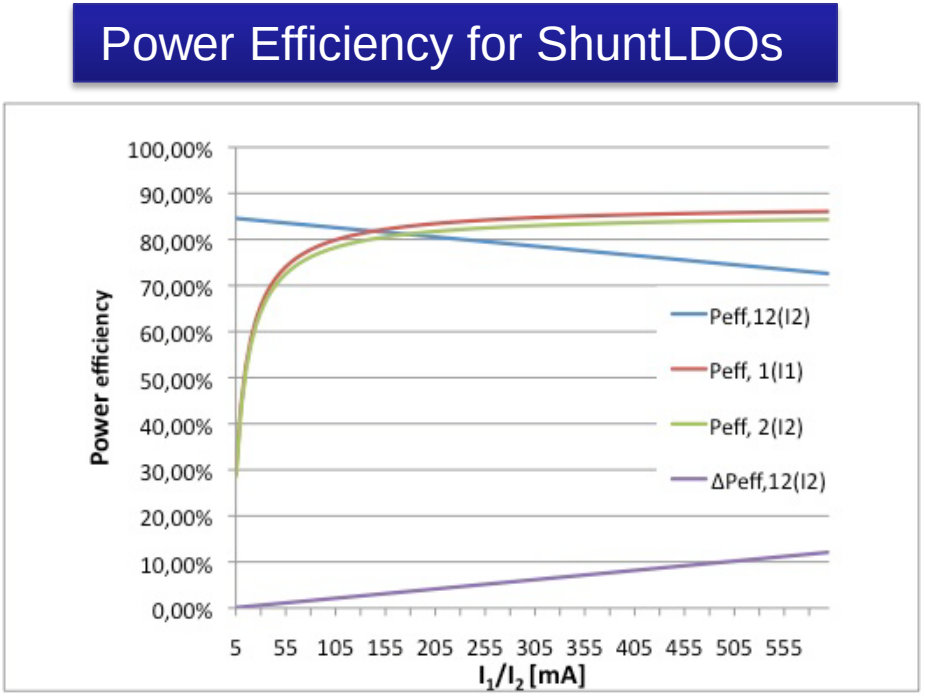
$$\text{DC-DC Eff} = \frac{nIV}{nIV/(1-\varepsilon)+(nI/m(1-\varepsilon))^2R}$$

$$\text{SP Eff} = \frac{nIV}{nIV/(1+\delta)+(I/(1+\delta))^2R}$$



Power efficiency

- SP power efficiency calculation is more complicated is you consider the 2 voltage needed usually for the FE electronics:
- Calculated here for ATLAS Pixel FE (FE-I4) in 130nm technology using two ShuntLDOs:
  - Two output voltages at 1.4 V (analog supply) and 1.2 V (digital supply), dropout voltage 0.2 V and shunt current 10 mA, no cable factor included.
  - Total current consumption ~600mA
  - Power efficiency for both voltages alone is well above 80%.
  - But power efficiency for both out voltages at the same time depends as well on the amount of current needed by the lower supply voltage!
- is around 80% for a digital current consumption of 250mA



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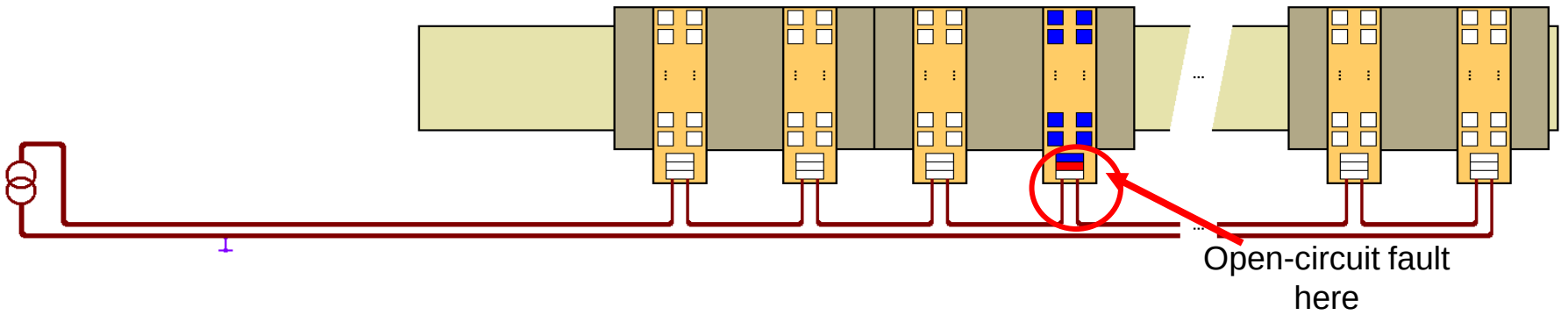
Protection schemes

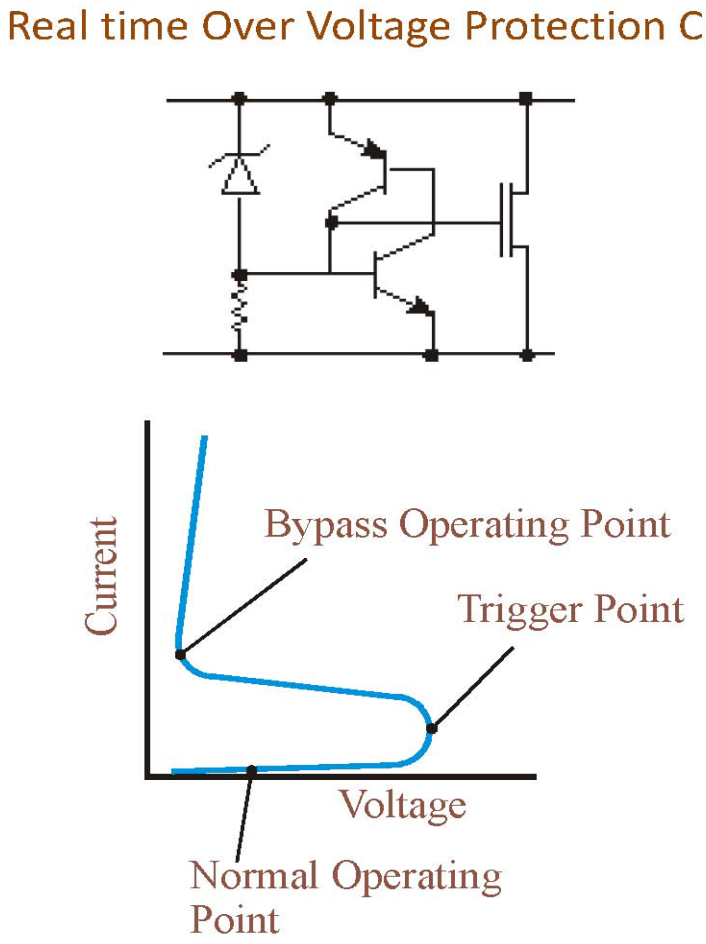
Serial Powering Protection

- What is needed in case an “open” develops in a chain of modules?
  - Real Time Local Protection/Current Bypass
    - Current source power supply is too far away for voltage limit to protect stave
    - 200 meters/ (2/3c) ~1 us. Assume open leaves ~ 10pf, and I ~ 1 amp, then voltage across short ~ 1 A x 1 us/ 10pf = 100kV → likely may spark and could!
  - Slow Control enabled bypass
    - Need a short that can bypass module in case it develops pathological behavior that adversely affects performance of stave
    - Short should be sufficiently low in impedance the resulting voltage across it will be low enough to disable module circuitry (i.e. small compared to normal module operating voltage, ideally < 100 mV)
  - Protection circuitry should not introduce additional stave failure modes



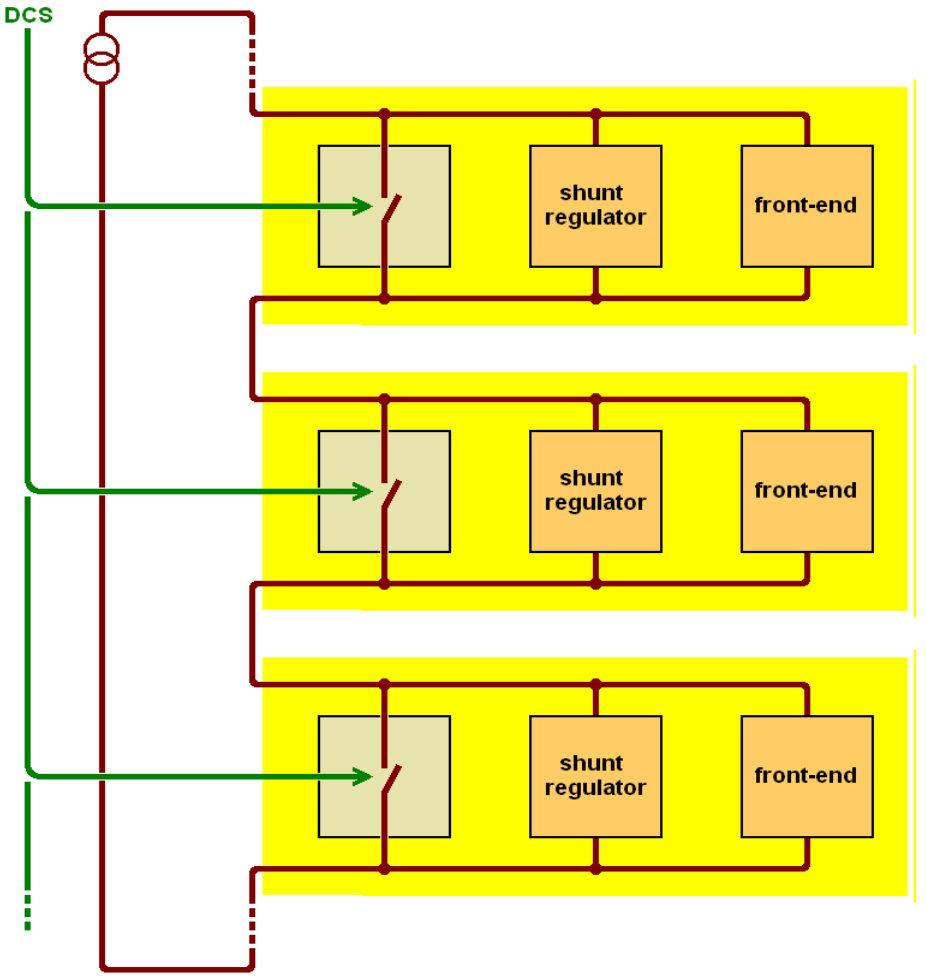
Real time overvoltage protection – crowbar circuit

- When an over-voltage condition occurs the low current zener starts conducting and triggers the pnp-npn latch (similar to a thyristor).
- One option is to use high current PNP-NPN BJTs.
- Our current preferred option is to use low current BJTs. The NPN base drives a custom FET that conducts most of the current. There are more possibilities to find radiation tolerant (i.e. high f_t) low current BJTs than power BJTs



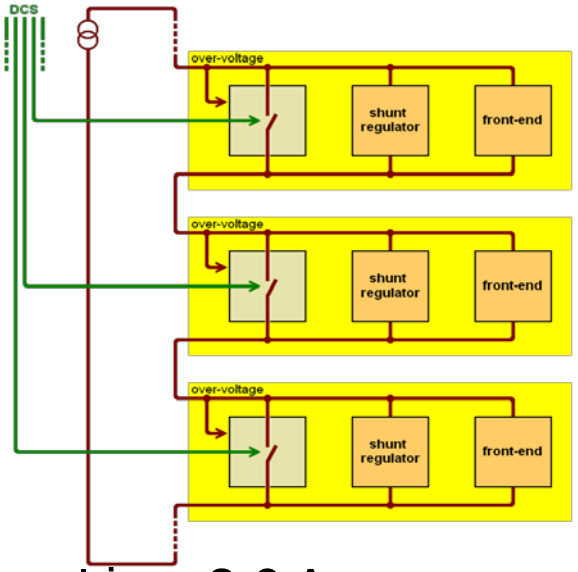
Protection schemes

- Target specifications:
  - Less than 100mV across each module when it is “off”.
  - Switching one module on/off will not affect its neighbours.
  - During normal operation (all modules working) protection draws no power.
  - Extra module components use about 10mm^2 hybrid area.
  - Each module can automatically, independently and very quickly shut down in a fault condition.
  - The Detector Control System (DCS) will control power to each module.

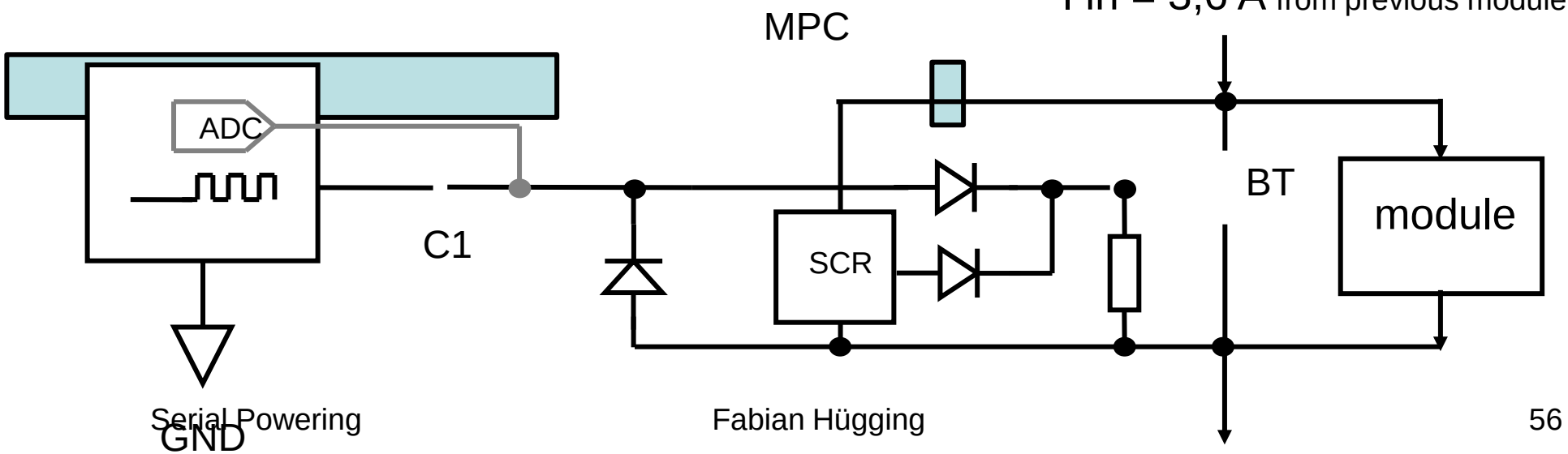


Protection schemes

- Tailored for pixel detectors using custom made ASIC
- Separate line from each module to end of stave allows each module voltage to be measured.
- Uses an SCR to latch into shorting state on over-voltage.

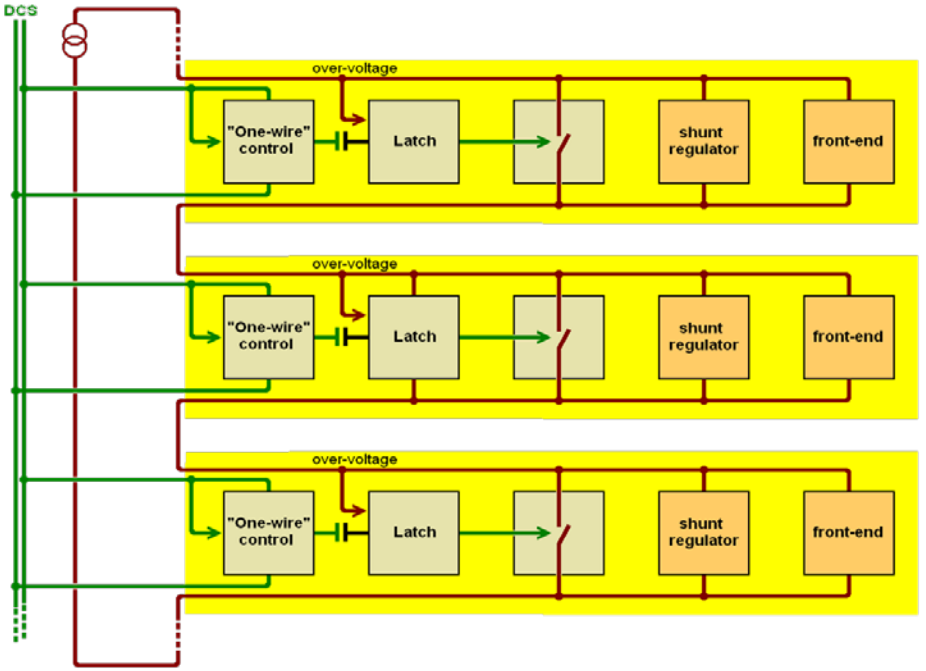


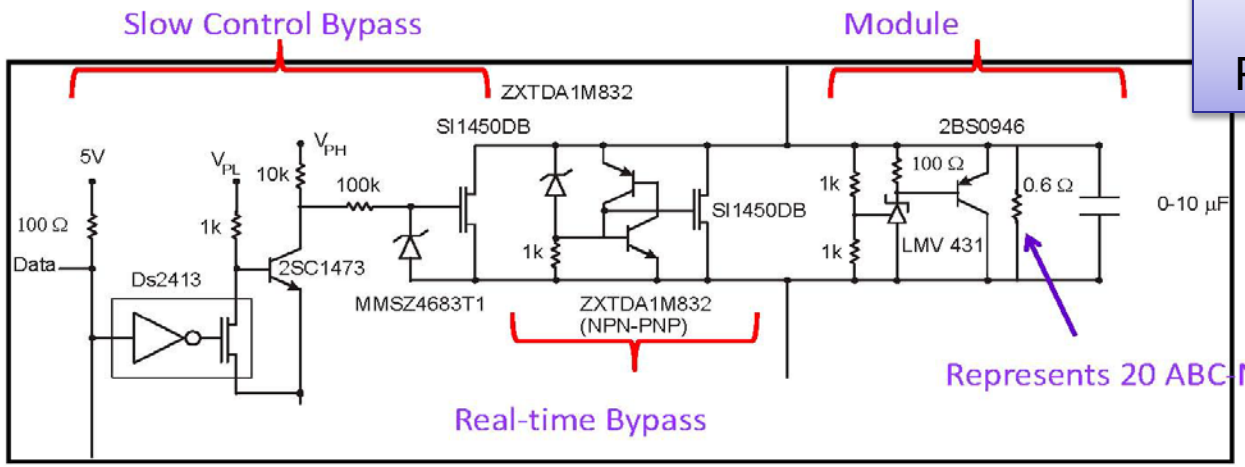
I in = 3,6 A from previous module



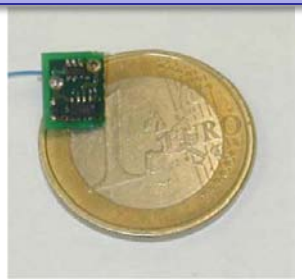
Protection schemes

- Tailored to strip detectors.
- Separate component used for over-voltage and DCS.
- One line DCS control.





Discrete Component
Real Time Bypass Prototype



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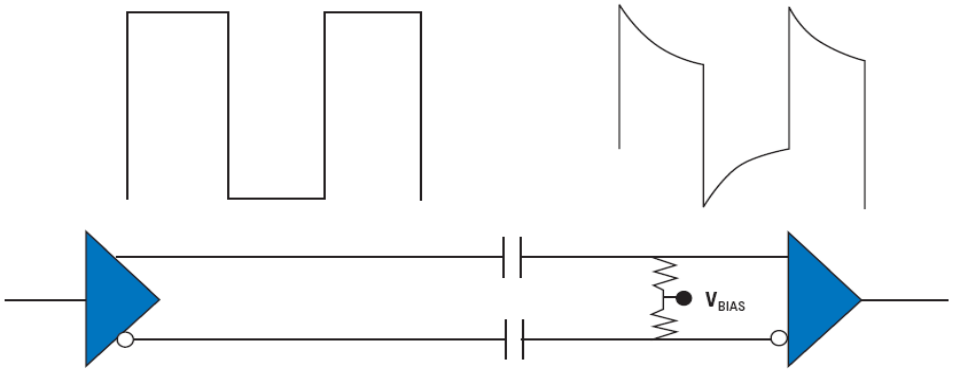
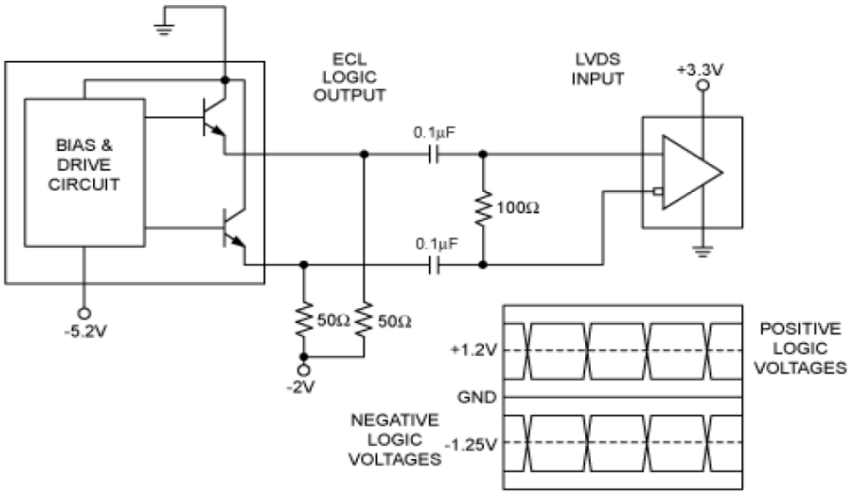
Data transmission

AC-coupling

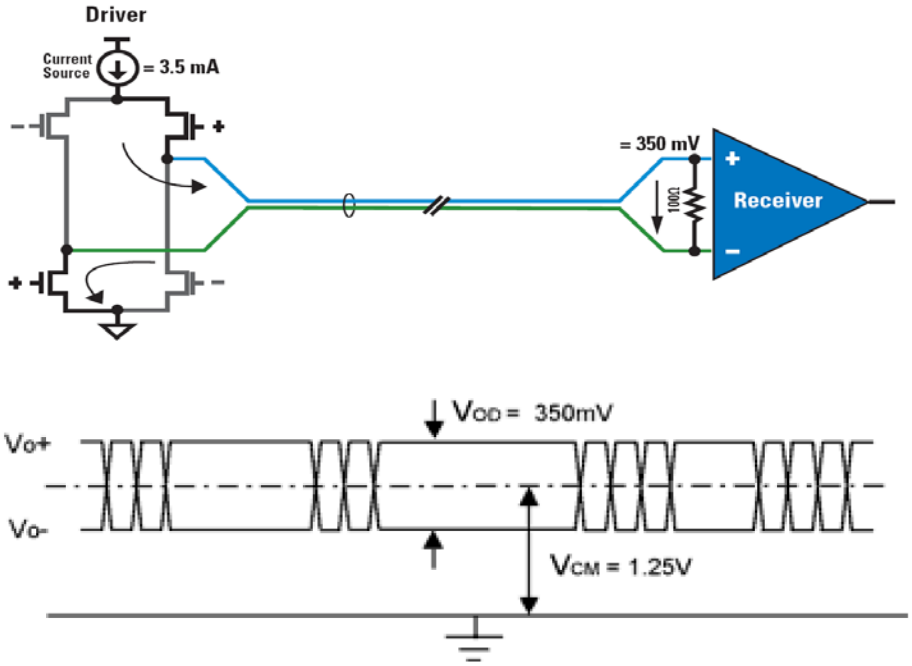
- What?
  - Termination techniques where capacitors are put in series with both signals of the differential pair
- Why?
  - Optimal common-mode voltage at the receiver input
  - Level shifting
  - Guard against differences in ground potential
- How?

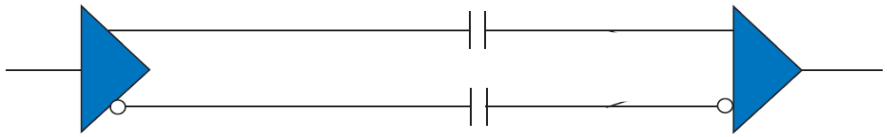
$$C = \frac{(7.8 \times \text{Run Length} \times \text{Bit Period})}{R}$$





AC-coupled LVDS link



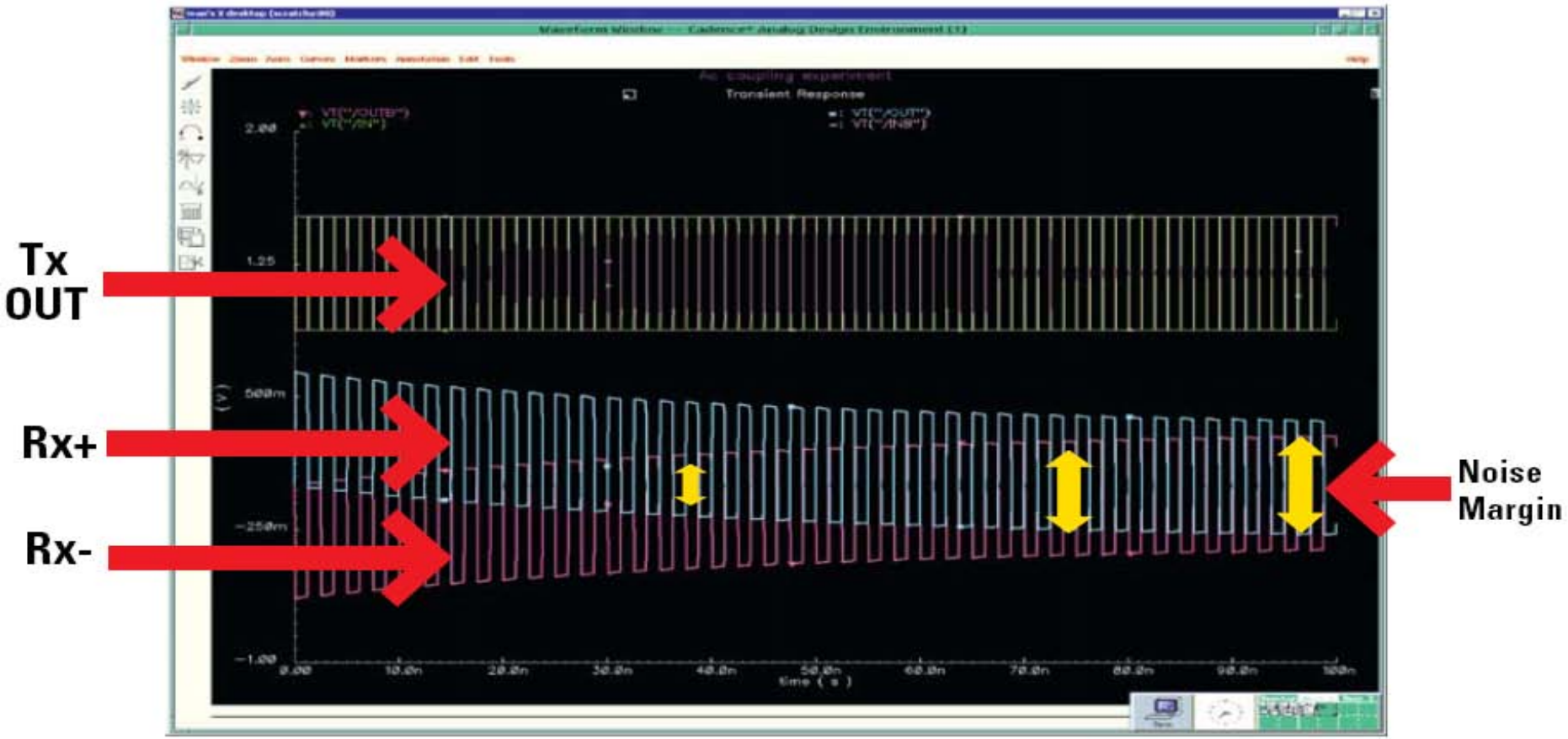


- On the TX side nothing changes
- V_{CM} (RX) is undefined
- V_{ID} is not centered around 0V

- V_{CM} (RX) = V_{CM} (TX) ± gnd shifts ± noise
- V_{OD} and V_{ID} are centered across 0V

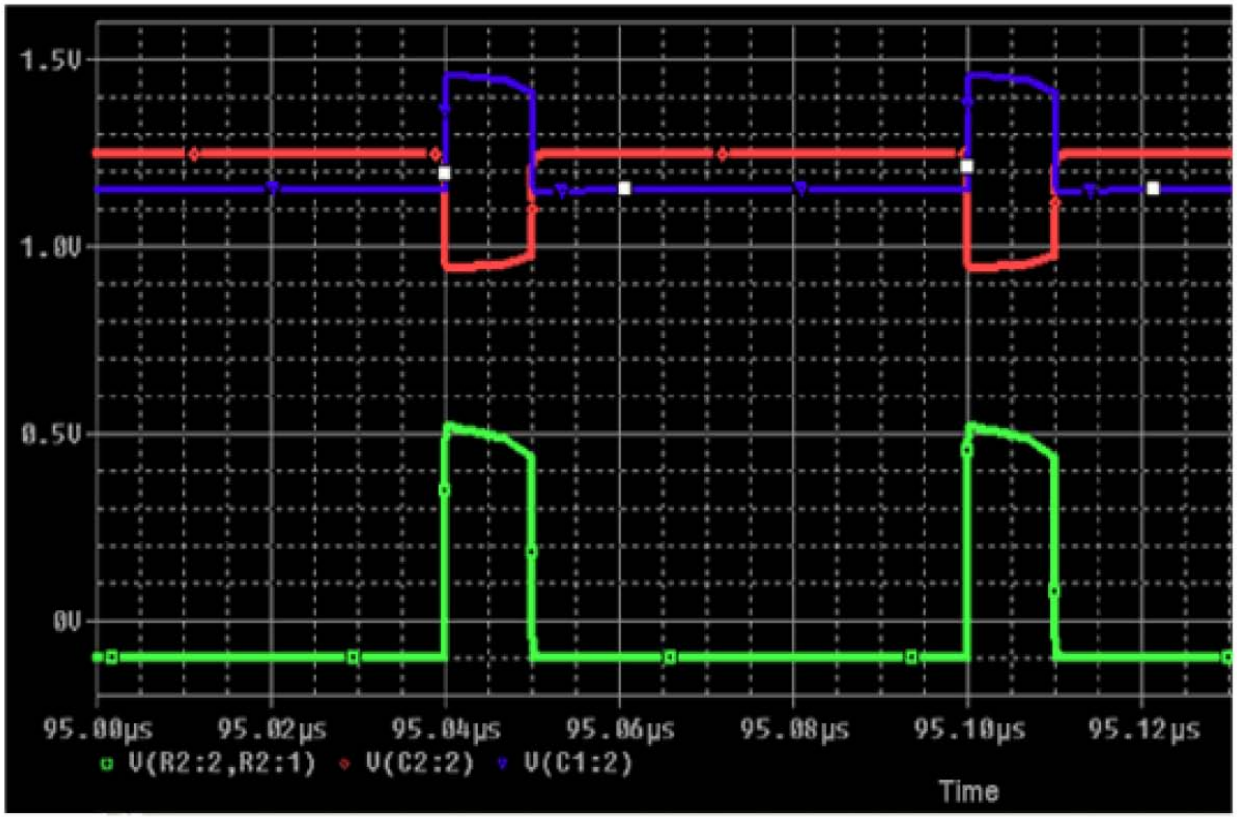
- Self-biased receiver inputs to set V_{CM}
- DC-balance to have V_{ID} centered across 0V

AC-coupling & DC-balance



When AC-coupling is used, current flows into the termination only during transitions. Without transitions, the charge on the 2 receiver inputs will slowly decay towards the same value, thereby reducing noise margin. Same situation at start-up (see picture on the right) -> DC–balance guarantees frequent transitions

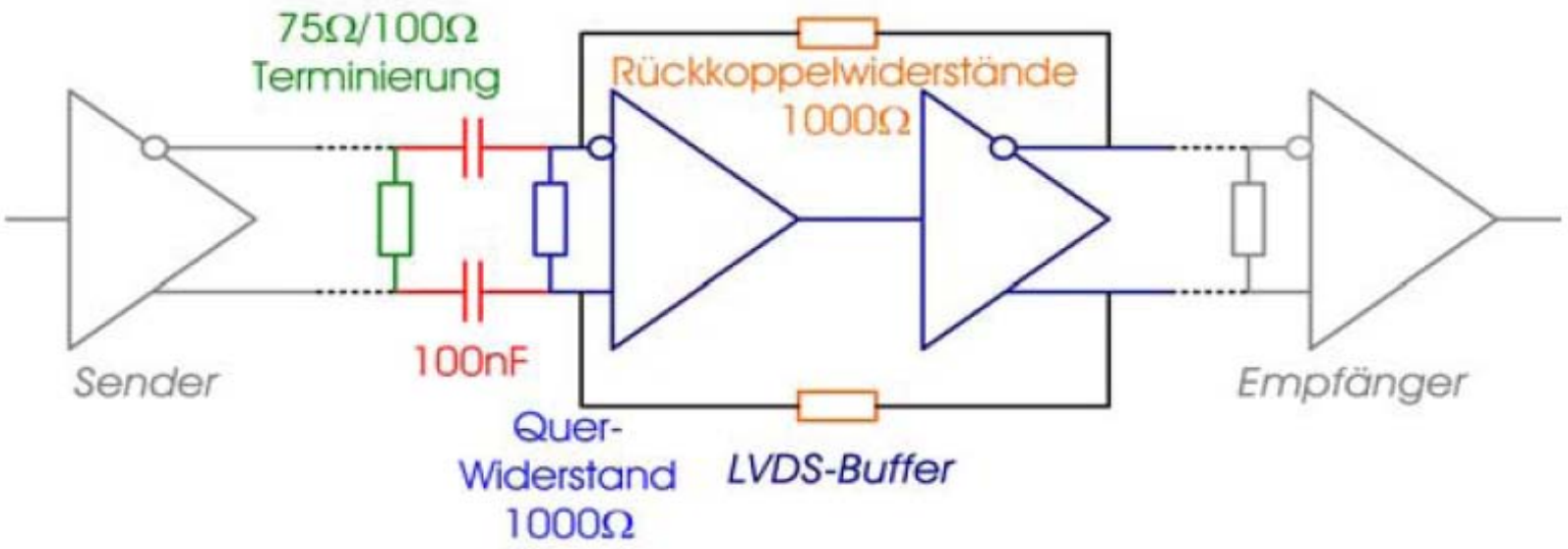
AC-coupling & DC-balance



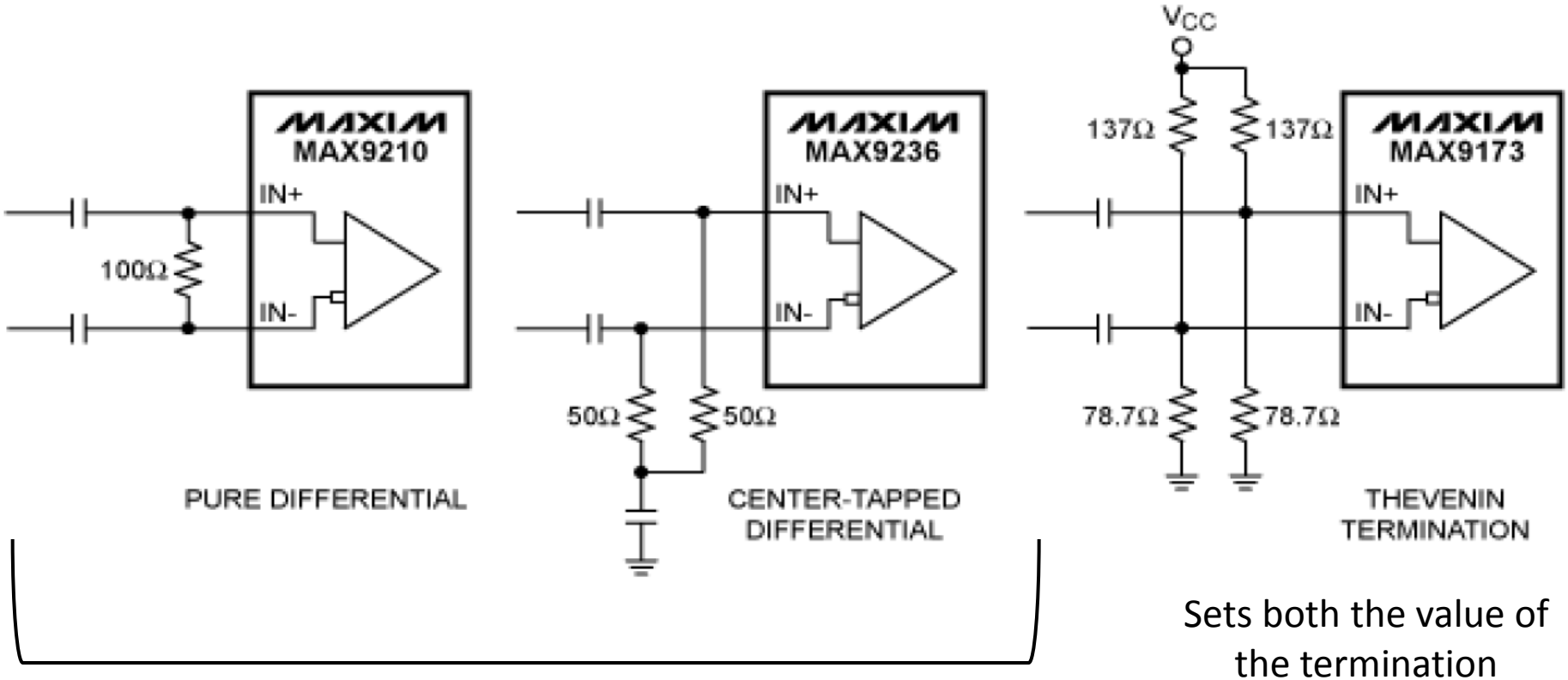
Non DC-balanced signals result in a V_{ID} not centered around 0 and skewed

AC-coupled LVDS link with feedback

- The feedback keeps the last state received
  - No need for self-biasing of the inputs
  - No need for DC-balancing
  - Acts as a fail-safe (keeps the output in the last state)



AC-coupling & termination

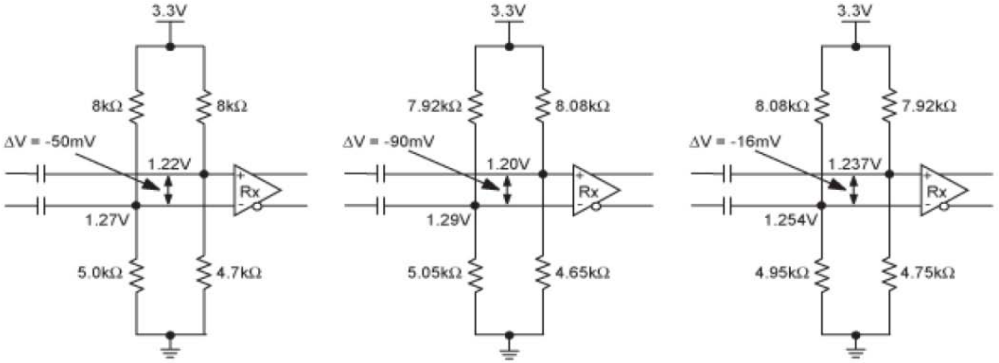


Self-biased LVDS receiver inputs

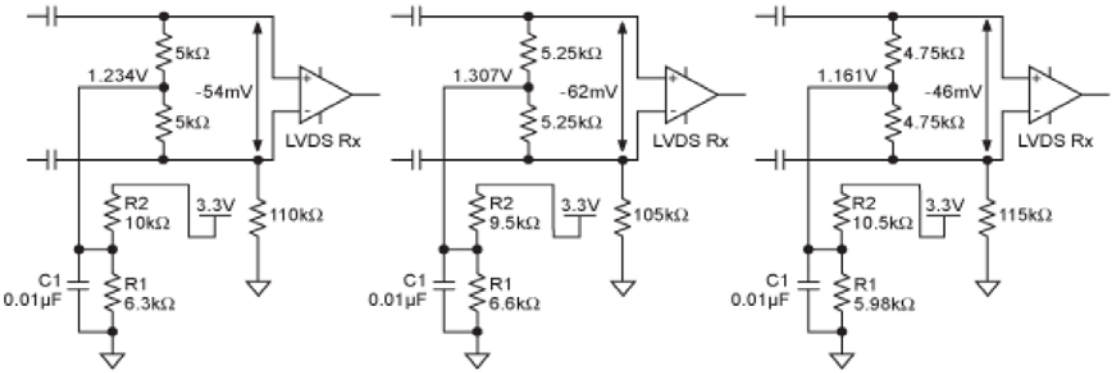
Sets both the value of the termination resistor and V_{CM}

AC-coupling & fail-safe

- When using the parallel fail-safe approach, Thevenin termination is required
  - If this configuration is not used, the DC voltage at the receiver inputs is almost VCC, which is outside the common-mode voltage range for the LVDS device
- A scheme like the one on the side puts together
  - Termination resistor
  - Biasing of the inputs
  - Fail-safe



- Differences in R value due to process variation can be a problem
  - More robust design against process variation is shown on the bottom



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The End