PLL design for clock multiplier in MAPS

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Outline

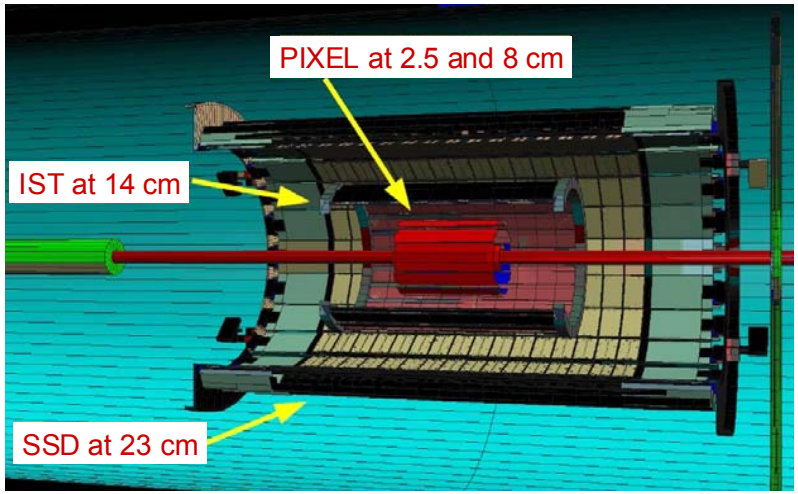
- *MAPS (Monolithic Active Pixel Sensors) in STAR experiment*
- *PLL architecture*
- *Building blocks*
- *Measurements*
- *Conclusion*

Extension of MIMOSA-26 to STAR

- **Final HFT (Heavy Flavour Tracker) - PIXEL sensor :**
  - Ladder equipped with MIMOSA-26 chip with active surface × ~1.7
    - 1088 col. of 1024 pixels → 1.1 million pixels
  - Pitch : 18.4 µm → (~20.0 x 18.8 mm²)
  - Integration time 200 µs
  - After power-on and configuration, the sensors are run continuously
  - The sensors readout path requires sending data over 6-8 m LVDS link at 160 MHz
  - Design from now → fab. Feb. 2010
  - 1st physics data expected in 2011/12

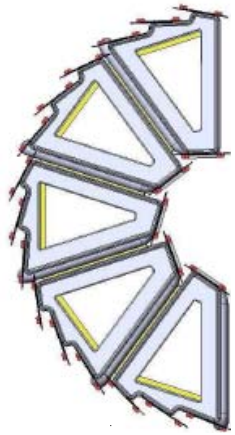
- ***Option :***
  - *A low frequency clock at 10 MHz will be multiplied to 160 MHz in each sensor by a PLL*
  - *The same clock will also equip an optional 8b / 10b data transmission block*

See Guy Dozière's talk



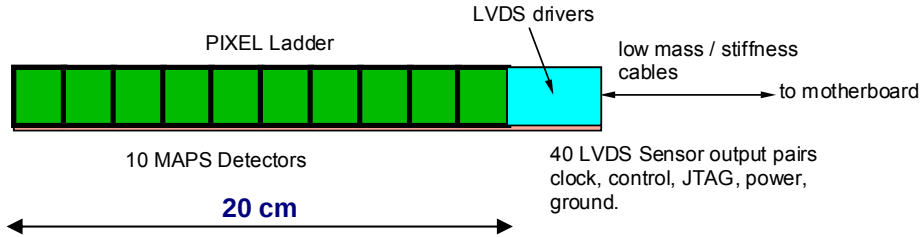
STAR Detector Upgrade

Pixel Vx Detector



Inner Layer:
10 ladders

Outer Layer: 30 ladders
10 sensors / ladder

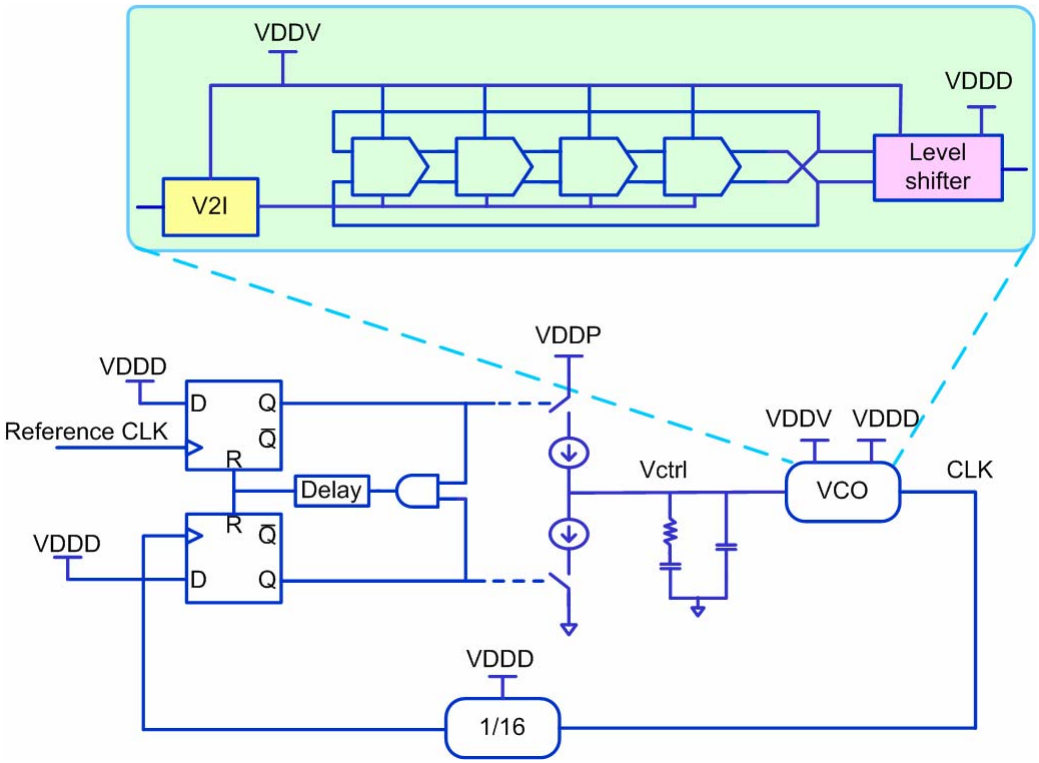


Ladder

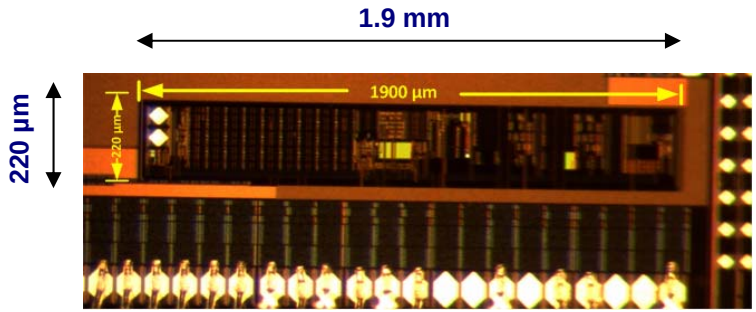
Architecture of the PLL

- **The first PLL prototype has been designed and manufactured in a AMS 0.35 µm CMOS process**

- **The PLL requirements for clock multiplier in MAPS are :**
  - Period jitter less than a few tenth of ps rms
  - Low power consumption
  - Specific form factor



PLL, 8b/10b

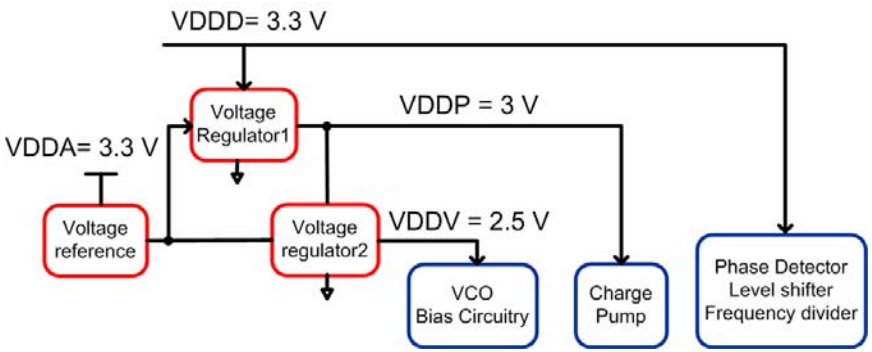


PLL Characteristics

- **Various noise sources within the PLL contribute to the jitter and phase noise**
  - Electronic noise (thermal and 1/f noise)
  - Supply and substrate noise
- **For high frequencies system, the effect of electronic noise is typically much less pronounced than that due to substrate and power noise**

F.Herzel and B.Razavi, IEEE Trans. On Circuits And Systems-II: Analog and digital signal processing, vol. 46, N°.1, January 1999

- **In MAPS, supply and substrate noise is a major noise source**
  - It results mainly of voltage fluctuations on the supply lines due to large current transients in digital and mixed circuitries ($Pdigital_{mean}$ ~ 200 mW in M26)
- **The VCO has the most significant contribution to noise**
  - Design architecture less sensitive to supply and substrate noise
  - Electronic noise minimized in the design
- **Two voltage regulators were implemented to provide stable voltage supplies to the analog part**

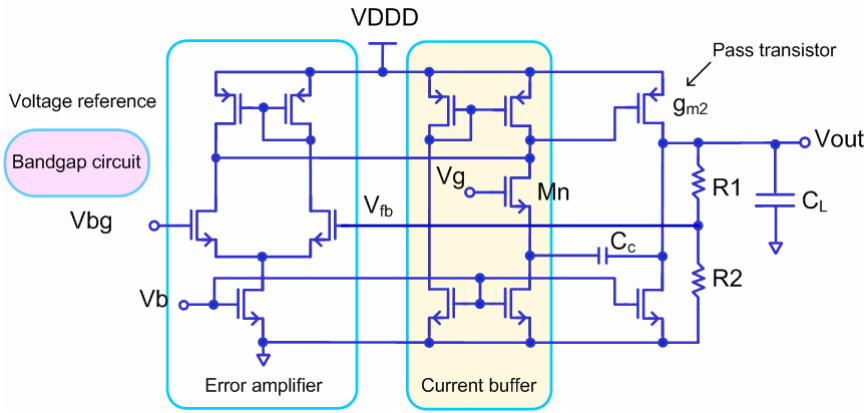


Power supplies distribution

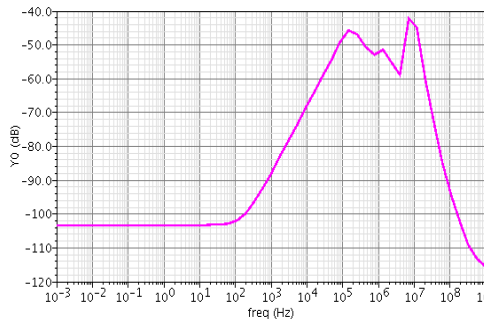
Building Blocks

- **The voltage regulator topology :**
  - It is composed of the voltage reference provided by a bandgap circuit, the error amplifier, the pass transistor, the voltage divider R1-R2 and the load capacitor
  - It is similar to a two-stage amplifier
  - A high PSSR for the two-stage amplifier will reduce the output ripple of the regulator
  - The regulator structure uses a current buffer in series to the miller compensation capacitor to break the forward path and compensate the zero
    - very efficient both for gain-bandwidth improvement and for high frequency PSRR
    - slight increase of complexity, noise and power consumption

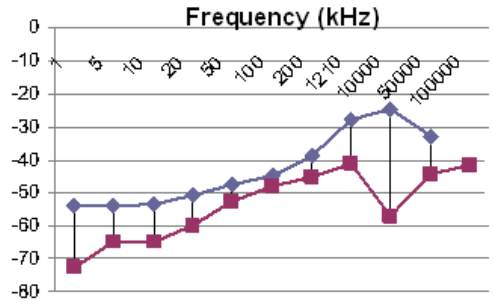
G. Palmisano and G. Palumbo, IEEE Trans. On Circuits And Systems-I: Fundamental, theory and applications, vol. 44, N°.3, March 1997



Voltage regulator schematic



Sim. : PSNR of VCO supply



Meas. : PSNR for VCO supply (in red) and for CP supply (in blue)

In the closed-loop configuration,
the output ripple can be estimated by :

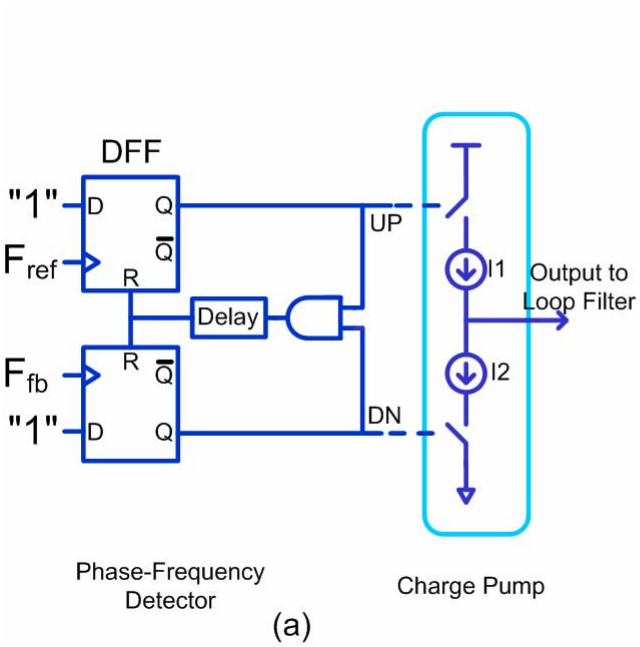
$$Vout_R \cong \frac{1}{\beta}\left(Vbg_R + \frac{VDDD_R}{PSRR}\right)$$

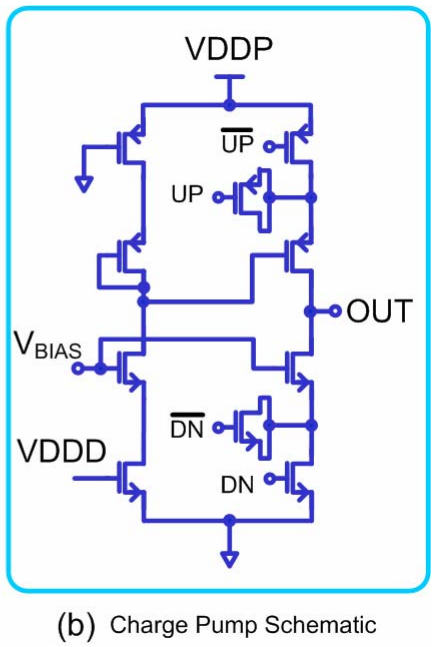
Voltage regulator area	**0.15 mm²**
Static current consumption	**780 µA**
Maximum output current	**14 mA**
PSNR	**< - 30 dB**

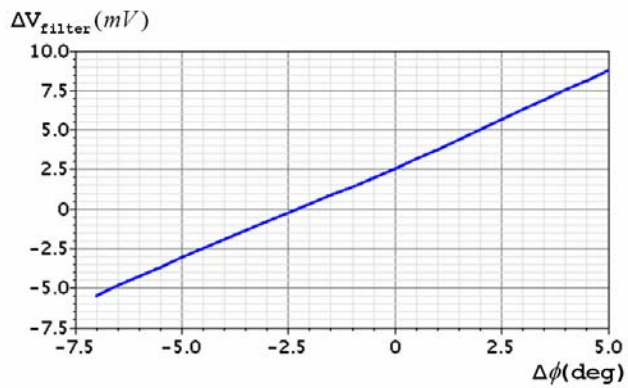
Performance summary

Building Blocks

- **The phase-frequency detector and charge pump structure :**
  - In order to avoid the dead-zone around the zero-phase error leading to increased noise, the state where UP and DN pulses are «high» simultaneously is enlarged by inserting a delay in the reset path
  - Optimized Delay
    - To minimize the dead zone and to limite the perturbation on the control voltage in the steady-state of the PLL
  - Dummy switch structure in the CP reduces the charge injection and the clock feedthrough mismatch

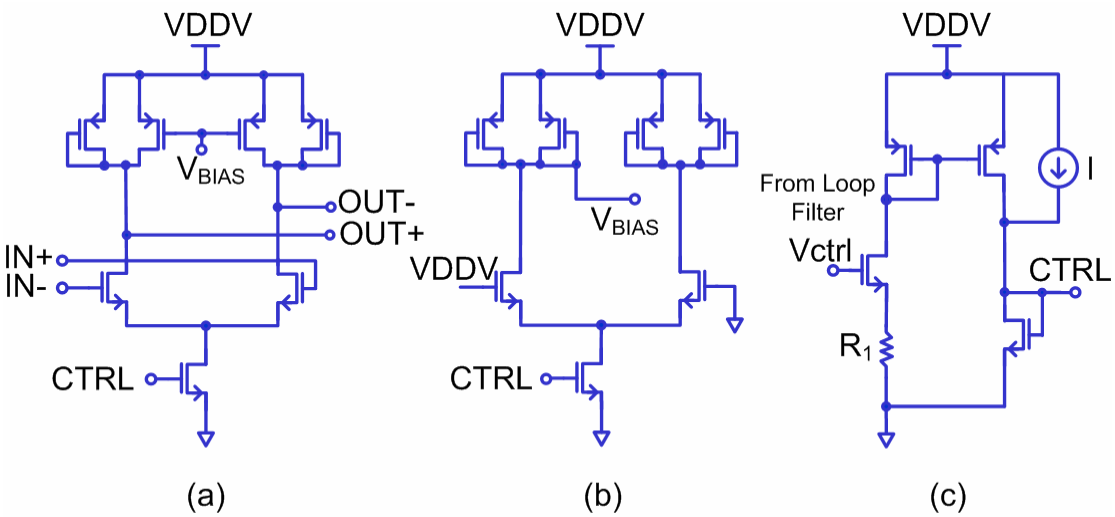




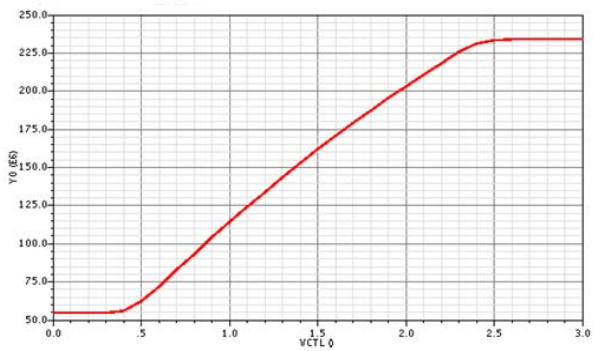


Building Blocks

- **The voltage controlled oscillator topology :**
  - The delay cell contains a source coupled pair with symmetric resistive loads
  - Linear controllable resistors are desirable to achieve supply noise rejection in differential cell
  - By using symmetric loads, the first order noise coupling term are cancelled out, reducing the jitter caused by the common-mode noise present in the supply line
  - The cell delay changes with VBIAS which is generated dynamically by a replica bias circuit
  - A controllable tail current in the delay cell and in the bias circuit is used to adjust the cell delay
  - The output voltage swing is relatively maintained constant by varying the active resistance of the load in such a manner that the variation is inversing to the observed current change
  - The voltage to current converter provides a first order linear relationship between the oscillation frequency and the control voltage



VCO tuning range : 60 – 230 MHz



Control Voltage Vctrl (V) versus Freq. (MHz)

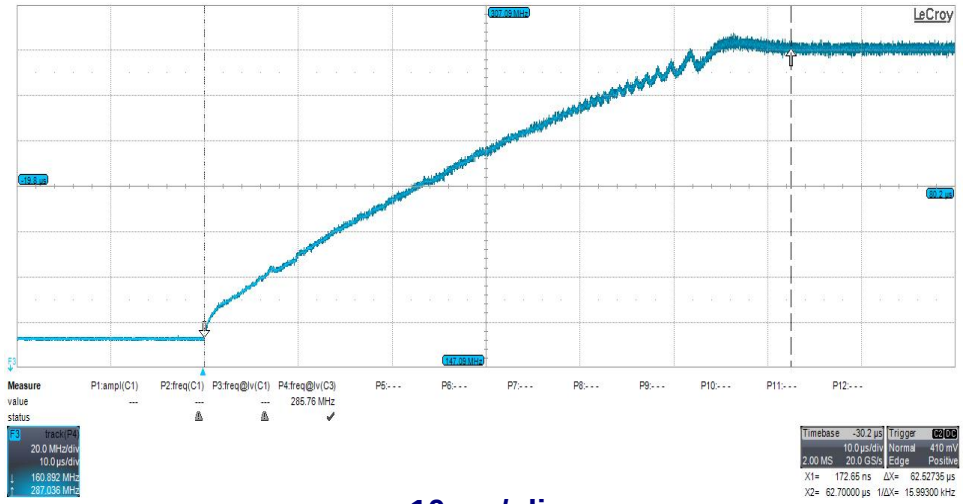
PLL Measurements

- **Locking range :**
  - 138 – 300 MHz (operating frequency = 160 MHz)
  - Frequency range shift compared with the simulation results
  - Relatively stable in temperature

- **Locking time :**
  - 60 µs
  - Good agreement with the simulation

Temperature (°C)	Lower limit (MHz)	Upper limit (MHz)
0	130	295
20	138	298
45	140	297

PLL locking range as function of temperature



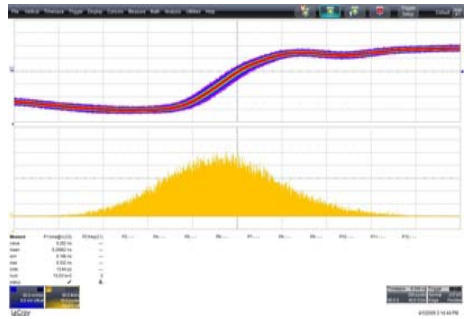
10 µs / div

PLL locking time : the reference clock jumps from 10 MHz to 16.7 MHz

Measured Clock Jitter

- **Jitter as function of the reference frequency at room temperature, with a stable 3.3 V supply voltage :**

Reference freq.(MHz)	9	10	12	14	16	18
PLL clock (MHz)	144	160	192	224	256	288
Period jitter (ps rms)	13	14	12	13	12	12
Period peak-peak jitter (ps)	124	126	113	107	97	111
Cycle to cycle jitter (ps rms)	23	22	23	21	22	22
Cycle to cycle peak-peak jitter at 10^{-12} BER (ps)	323	317	326	293	318	307



Period jitter

- **Period jitter at 160 MHz with a peak amplitude of 400 mV square wave on the power supply line as function of the perturbation frequency :**

Noise frequency (kHz)	0.1	1	10	100	1000	10000
Period jitter (ps rms)	19	19	16	16	16	15
Period peak-peak jitter (ps)	148	131	140	113	132	127

Conclusion and Perspective

- **The power consumption has been estimated at 7 mW**
  - On-chip voltage regulators increase the power consumption of 20 %
- **The period jitter is less than 20 ps rms in a emulated noisy power supply environment**
  - The PLL can be employed as clock multiplier in MAPS
- **In the future, the same PLL clock will also equip a serial transmitter block**
  - The PLL jitter should be optimized by characterising the transmission system with cable connections and receivers in order to ensure the data transmission with low error rate
  - Programmable loop bandwidth

PLL performance summary

Technology	**0.35 µm CMOS process**
PLL die area	**0.42 mm^2**
Multiplication factor	**16**
Locking range	**138 MHz – 300 MHz**
Power supply requirement	**3.0 – 3.6 V**
Power consumption (estimated)	**7 mW at 160 MHz**
Period jitter	**14 ps rms**
Period jitter with noise	**16 ps rms**
Locking time	**60 µs**