Microelectronics at IN2P3 & IRFU

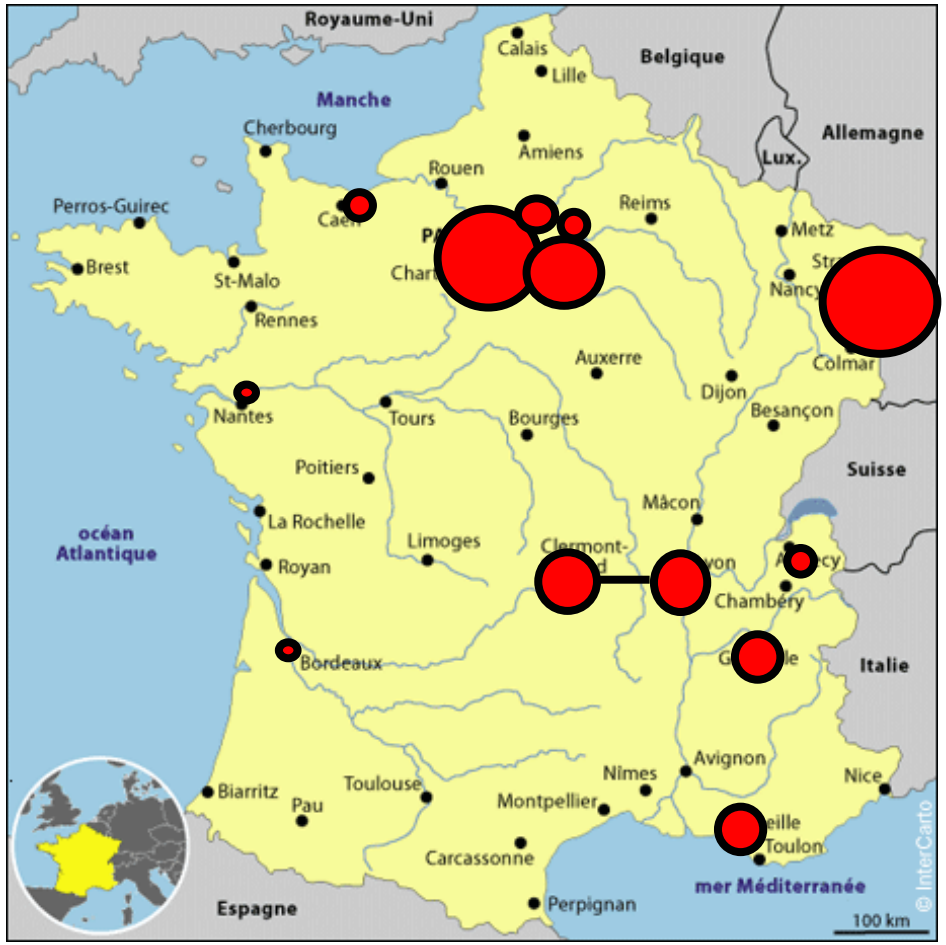
C. de La Taille

IN2P3 Micro-Electronics Coordinator

Microelectronics at IN2P3

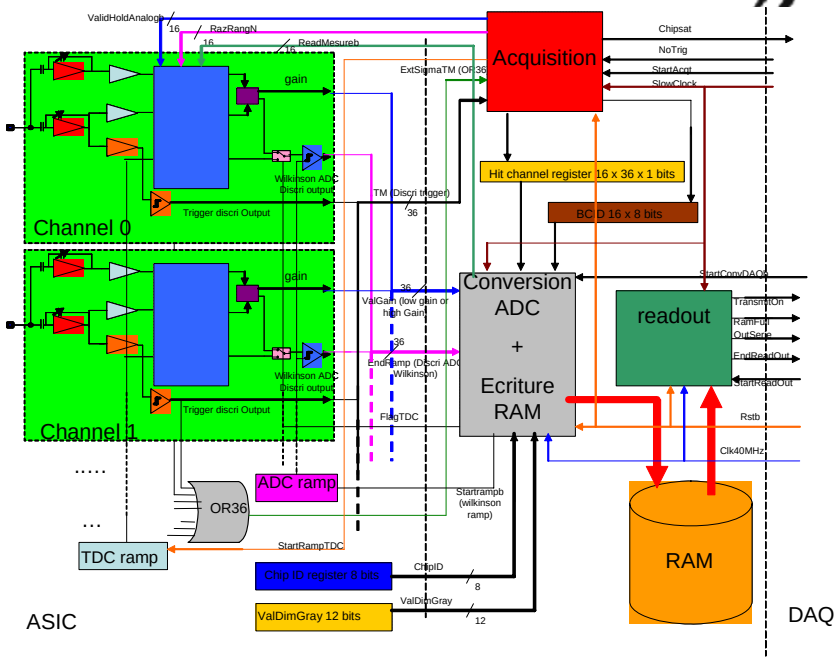
- Large force of micro-electronics engineers (~50)
  - Experience in designing and building large detectors
  - Common Cadence tools
  - But scattered in ~15 labs

- National organization :
  - Building blocks : « club »0.35µm SiGe
  - Networking 0.35 and 130 nm
  - Creation of poles with critical mass (~10 persons)
    - Orsay (OMEGA)
    - Clermont-Lyon (MICHRAU)
    - Strasbourg (IPHC)



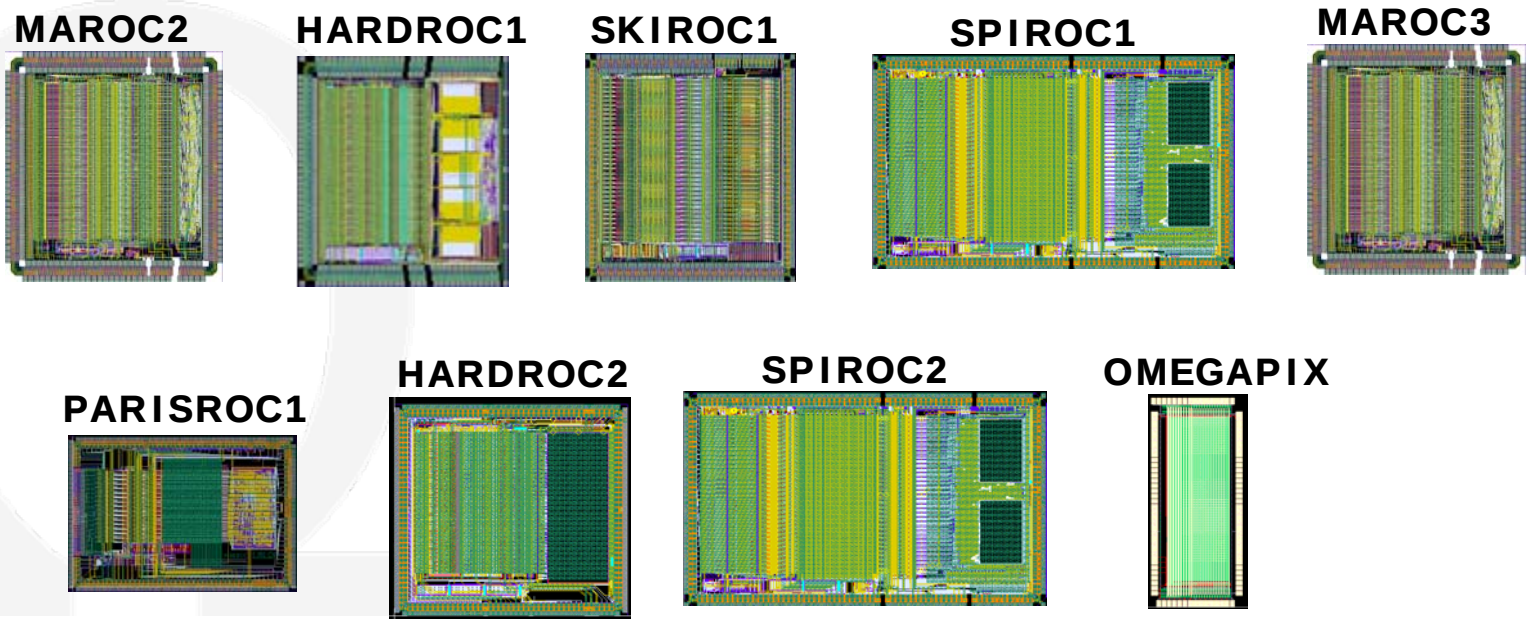
Motivation for poles

- Continuous increase of chip complexity (SoC, 3D…)
  - Minimize interface problems
- Importance of critical mass
  - Daily contacts and discussions between designers
  - Sharing of well proven blocks
  - Cross fertilization of different projects
- Large R&D activity
  - ILC detectors
  - sLHC starting (3D electronics)
  - astrophysics



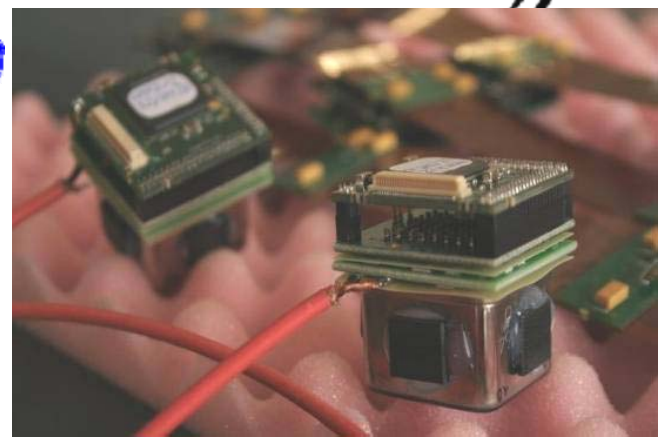
Recent chips at OMEGA Orsay

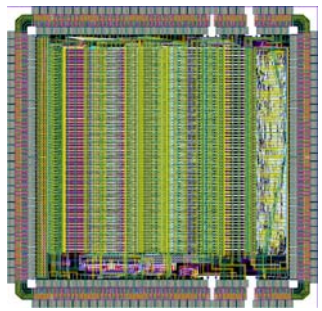
- Several chips developped for ATLAS LAr, OPERA, LHCb, CALICE in BiCMOS 0.8µm and installed on experiments
- Turn to Silicon Germanium 0.35 µm BiCMOS technology in 2005
- Readout for MaPMT and ILC calorimeters
- Very high level of integration : System on Chip (SoC)
- Start of 3D integrated 130nm electronics for sLHC pixels
- Adaptation of MAROC for EUSO spatial application

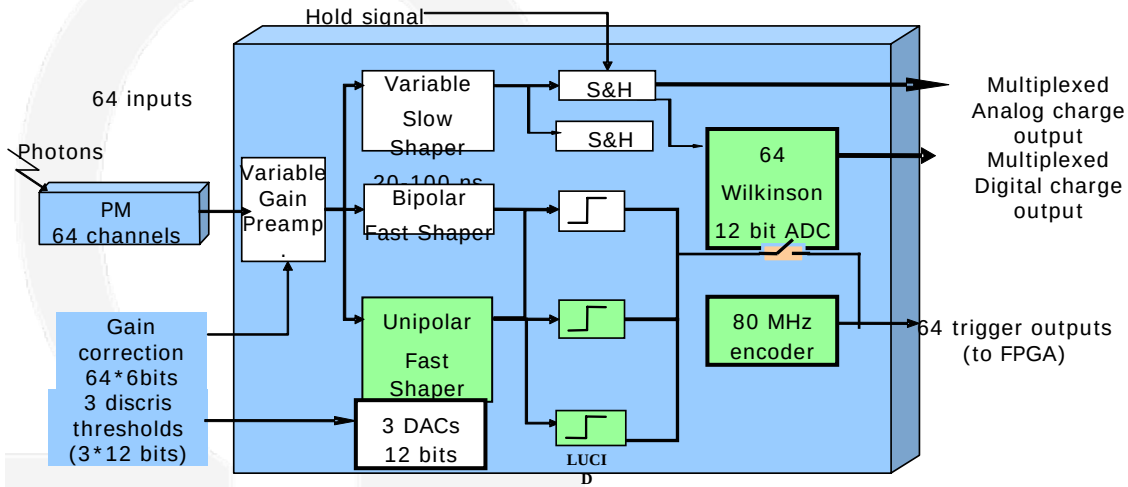


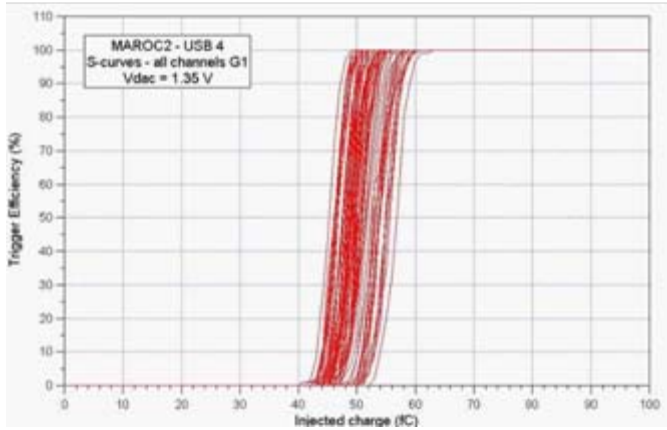
MAROC : MultiAnode Read-Out Chip

- Complete front-end chip for 64 channels multi-anode photomultipliers
  - 6bit-individual gain correction
  - Auto-trigger on 1/3 p.e. at 10 MHz
  - 12 bit charge output
  - SiGe 0.35 µm, 12 mm^2, Pd = 5 mW/ch
- Bonded on a compact PCB (PMF) for ATLAS luminometer (ALFA)
- Also equips Double-Chooz, medical imaging… Project for JEM-EUSO



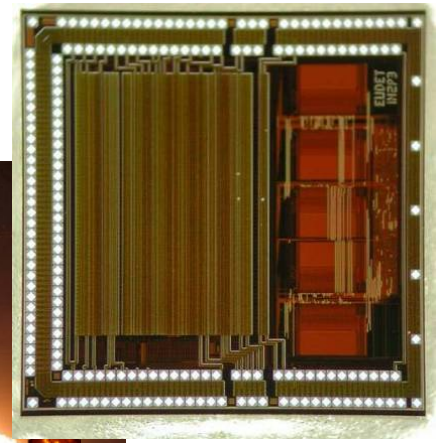




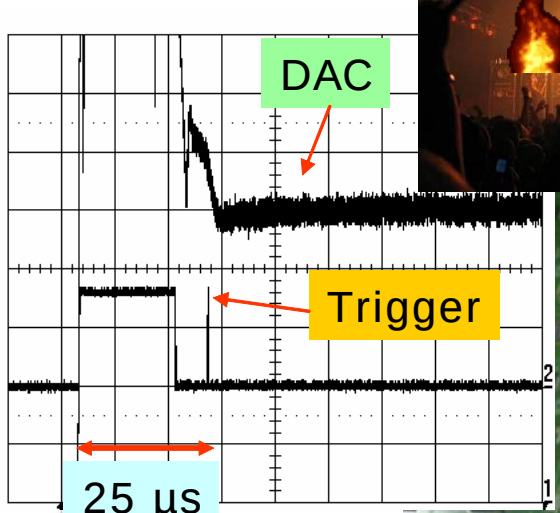


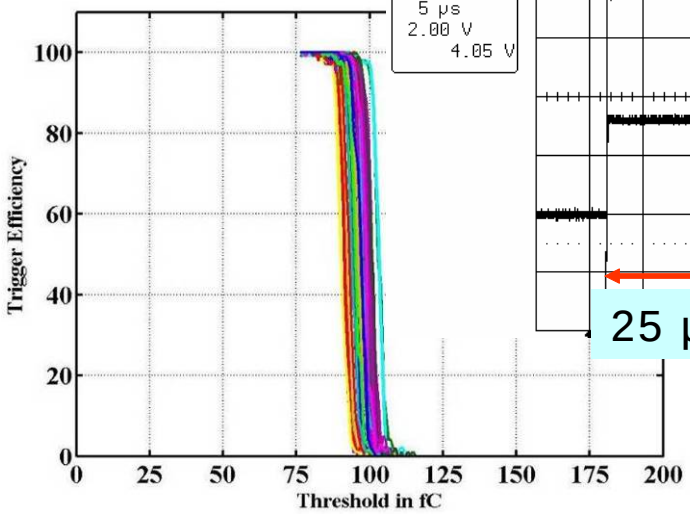
HaRDROC : ILC DHCAL readout

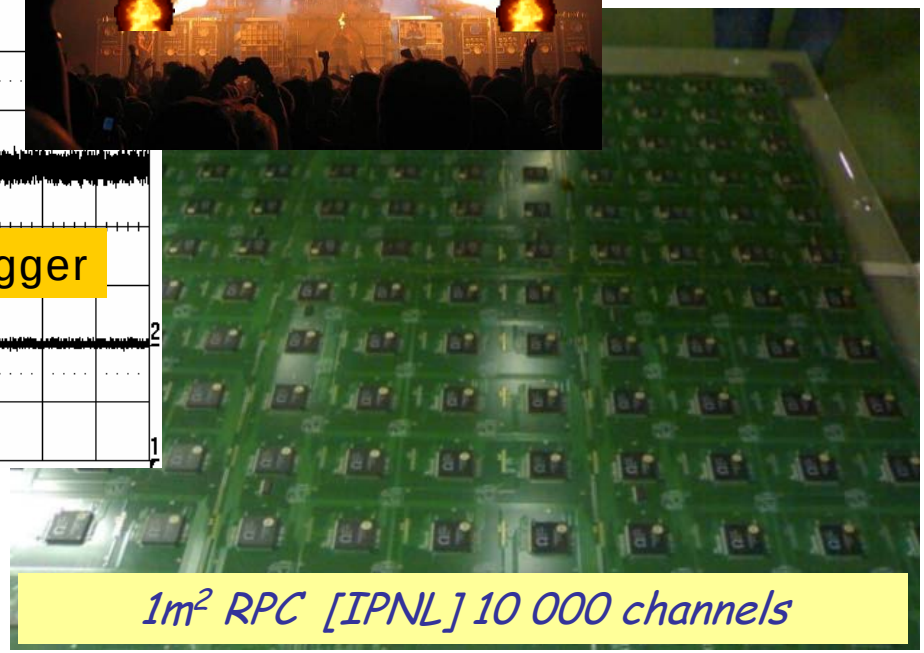
- Hadronic Rpc Detector Read Out Chip
  - 64 inputs, preamp + shaper+ 3 discris
  - Full power pulsing => 7 µW/ch
  - Fully integrated ILC sequential readout
  - Chip embedded in detector
  - AMS SiGe 0.35 µm
  - in beam in 2008-2009
  - 5000 chips to be produced in 2010



HaRDROC it's gonna heat ! =>Power pulse





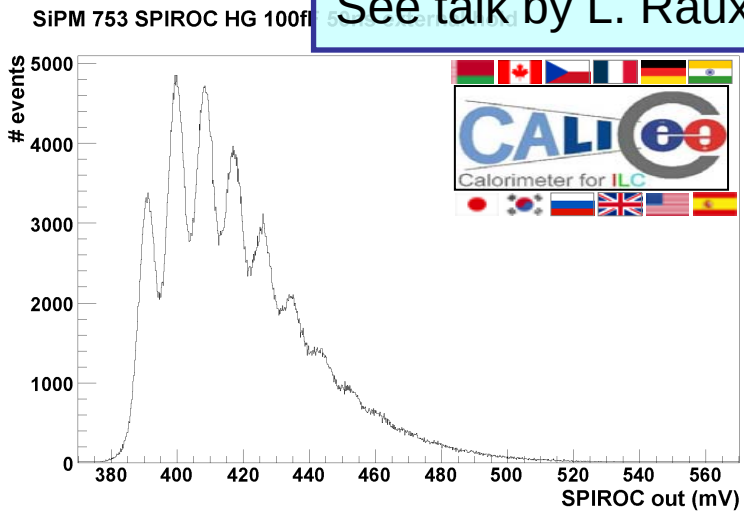


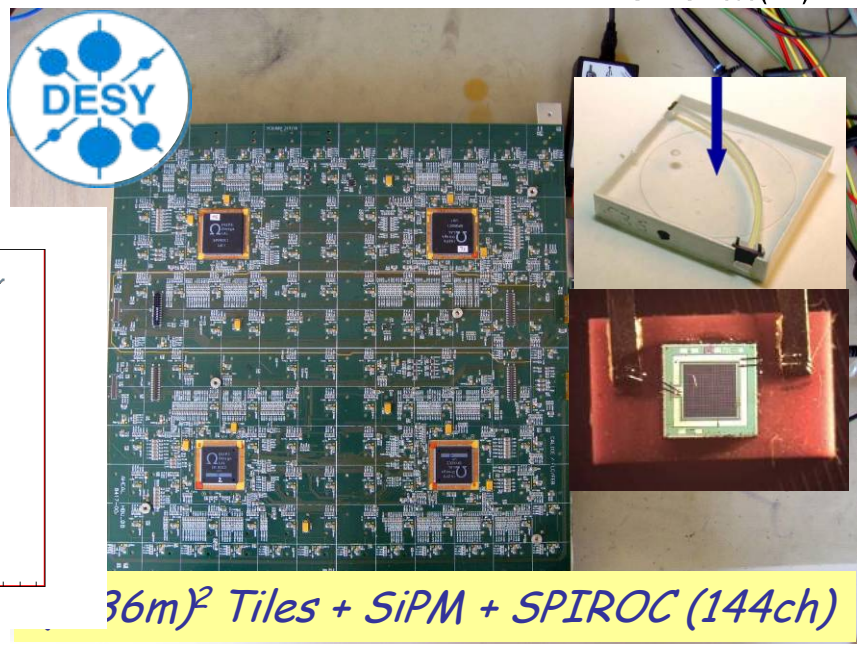
1m² RPC [IPNL] 10 000 channels

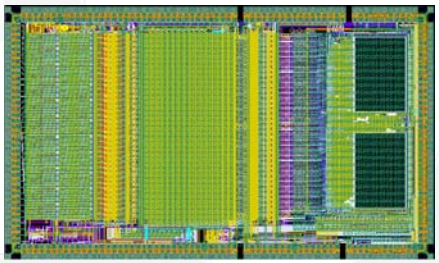
SPIROC : ILC AHCAL & ECAL readout

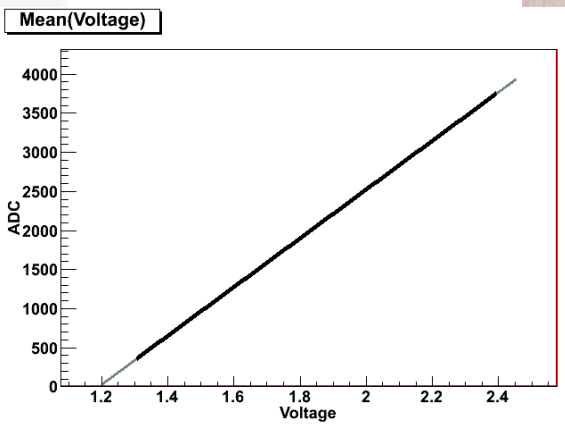
- SPIROC : Silicon Photomul. Integrated Readout Chip
  - 36 channels
  - Internal 12 bit ADC/TDC
  - Charge measurement (0-300 pC)
  - Time measurement (< 1 ns)
  - Autotrigger on MIP or spe (150 fC)
  - Sparsified readout compatible with EUDET 2nd generation DAQ
  - Pulsed power -> 25 µW/ch
  - Also External users (PET, hodoscopes, µ-imaging… (@ Aachen, Napoli, Pisa, Roma…)

See talk by L. Raux







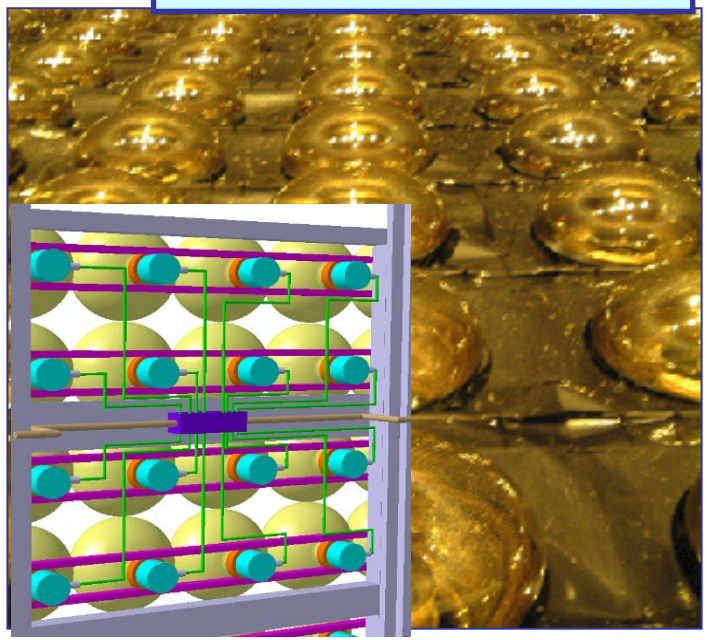


(36m)² Tiles + SiPM + SPIROC (144ch)

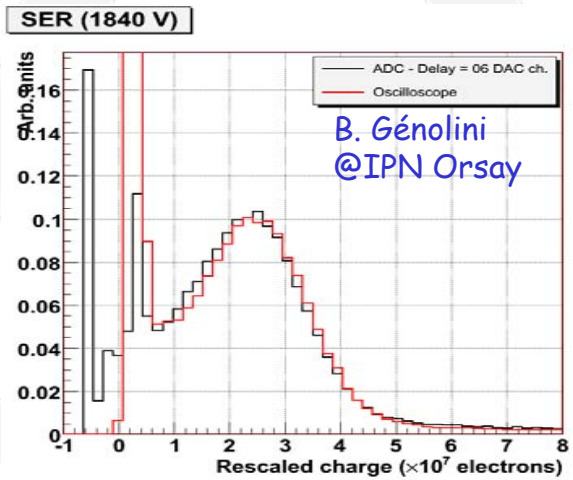
PARiSROC for PMm²

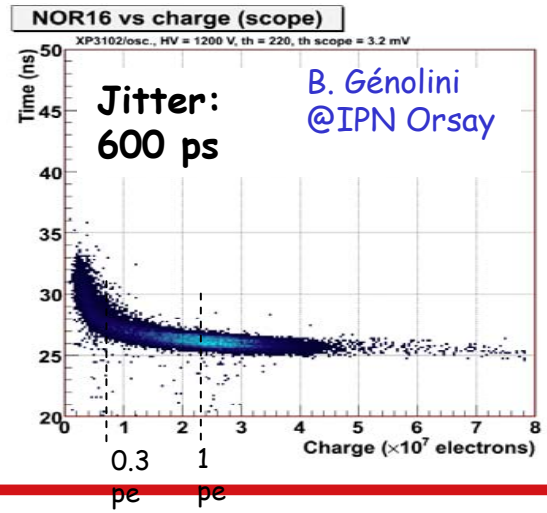
- Photomultiplier ARray Integrated SiGe Read-Out Chip
  - Replace large PMTs by arrays of smaller ones (PMm2 project)
  - Centralized ASIC 16 independent channels
  - Auto-trigger
  - Charge and time measurement (10-12 bits)
  - Water tight, common high voltage
  - Data driven : « One wire out »
- Application in large Water Cerenkov
  - Chip studied by MENPHYNO, DUSEL, LENA…

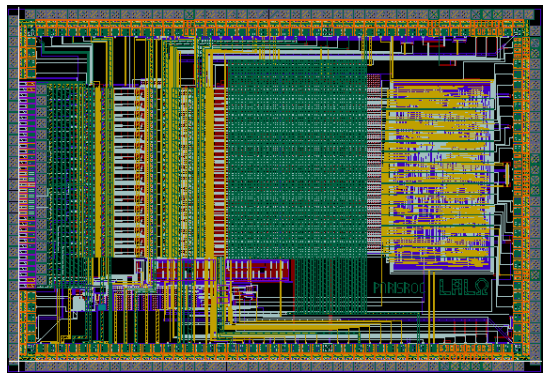
See talk by S. Conforti



Joël Pouthas IPN Orsay





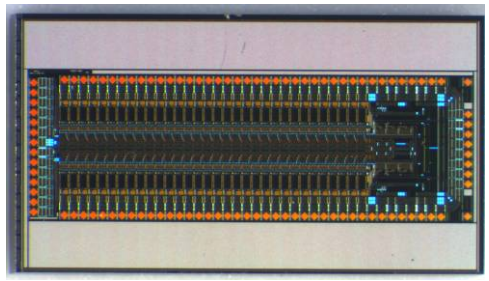


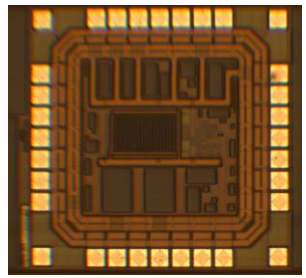
Front-End R and D in HEP
(Room temperature and Cryogenic Temperature)

See talk by H. Mathez

Main analog blocks
- Charge Sensitive Amplifier
- Shapers
- Buffer

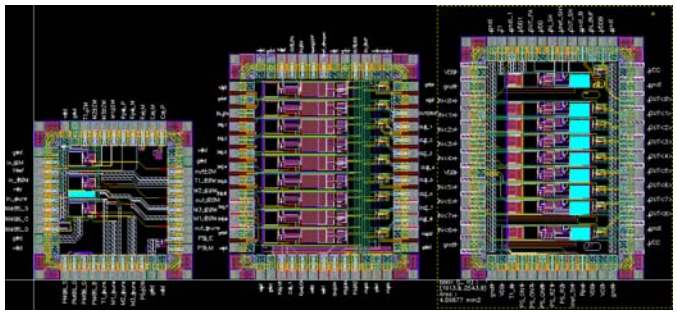
Analog /digital Asic

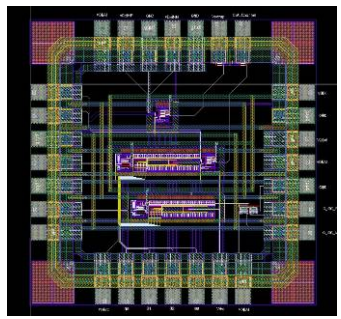




Full diff CSA

- ILC (DHCAL et ECAL)
- INNOTEP (medical imaging project)
- Beam profiler for hadrontherapy
- T2K



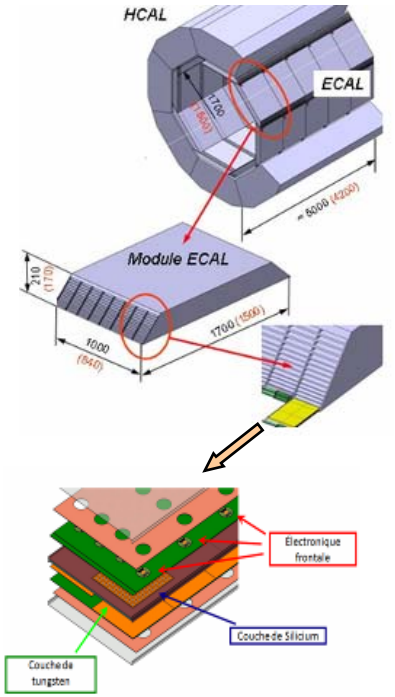


AMS 0.35 CMOS and BiCMOS proce

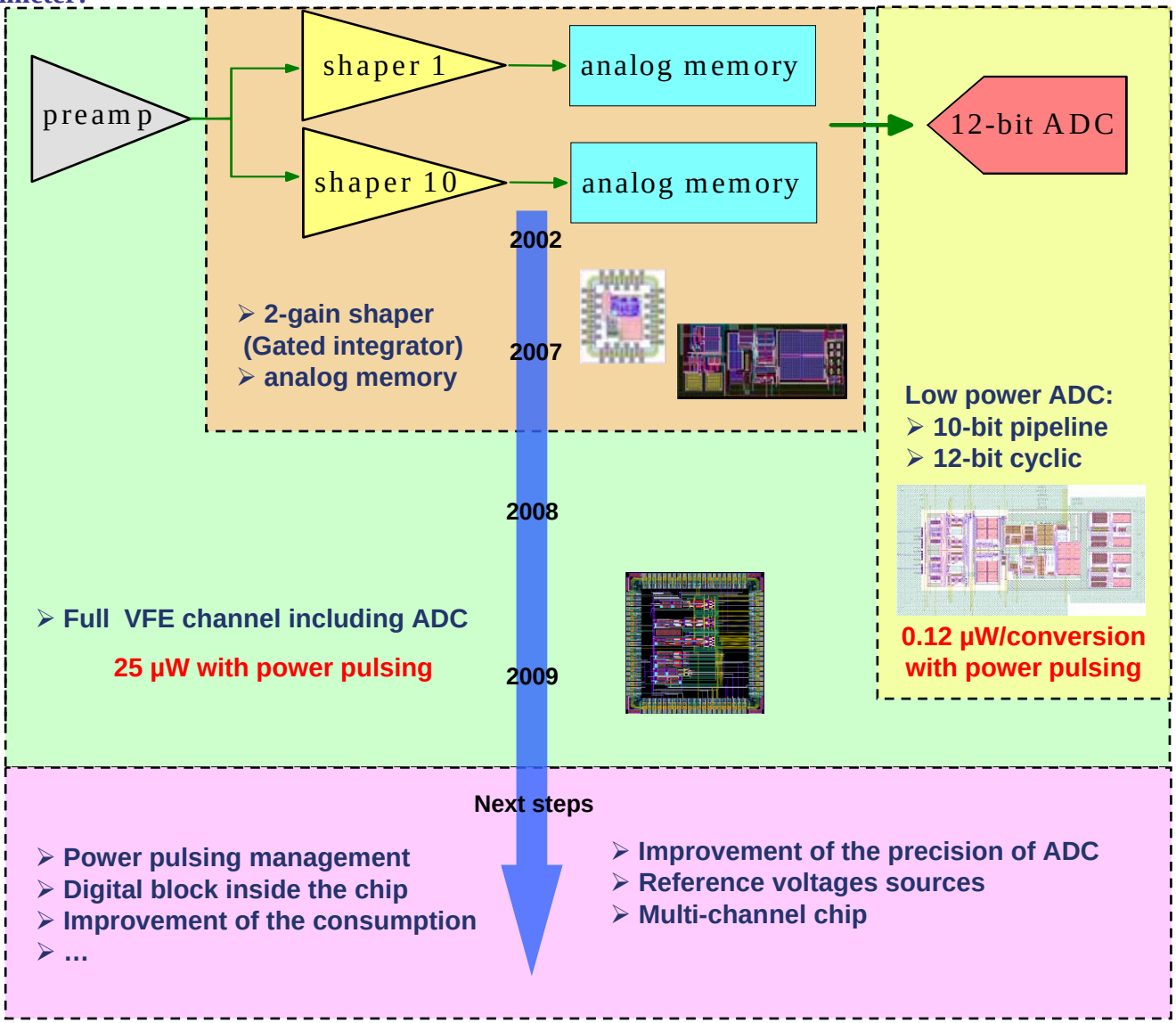
R&D dedicated to ILC/Calice

Very-front-end electronics of SI-W calorimeter:

- Dynamic range of 15 bits
- Global precision > 8 bits
- Embedded multi-channels chips
- > 100.10^6 channels
- Ultra-low power : 25 µW per channel

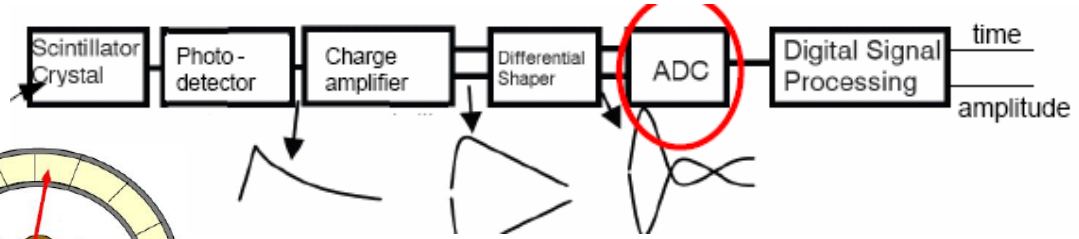


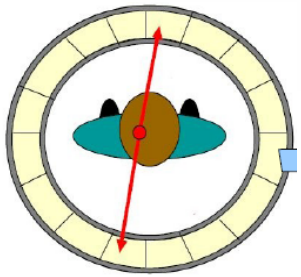
The embedded VFE chip inside the sandwich structure of the Ecal detector



INNOTEP (AMS 0.35µm SiGe)

See talk by S. Crampon

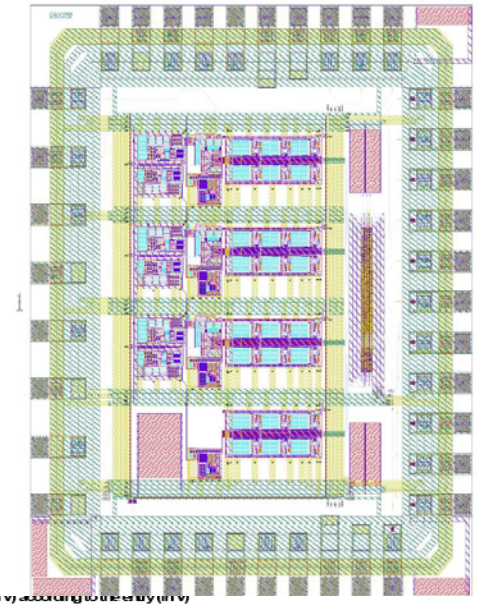


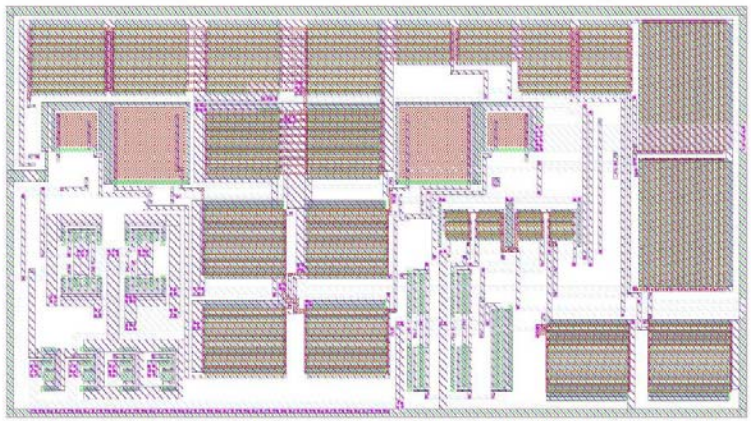


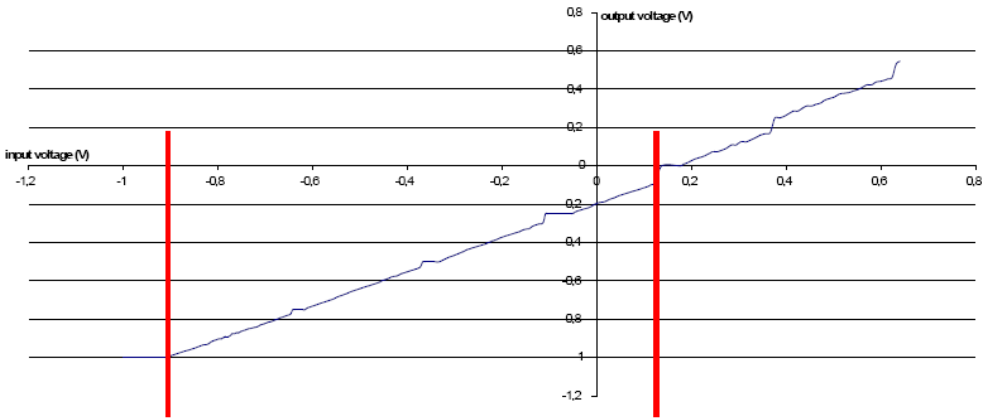
Detector ring

100 Mhz 8 bits ADC (S. Crampon thesis)
First version tested, need for an iteration

Fast preamplifier and 40ns shaper (tested)
Used for a 40 channels demonstrator.



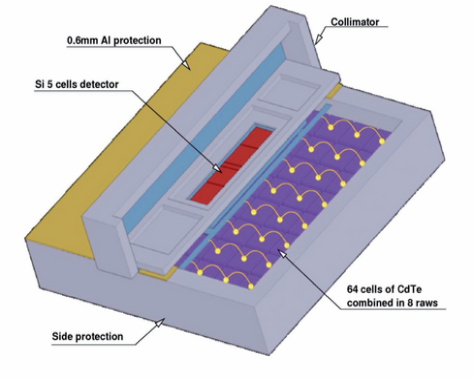


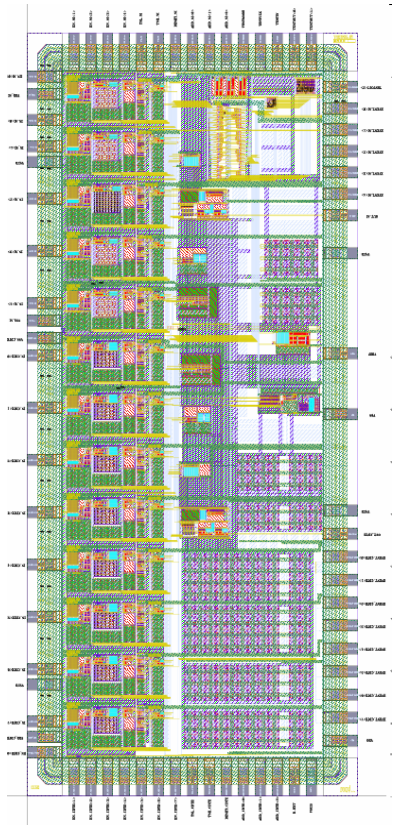


Technology transfer

TARANIS Project through CESR in Toulouse via MIND/C4I

Experiment goal : Measurement of the energetic electrons generated by atmospheric thunderstorms, space electronics (µsatellite)





Front-end analog blocks (CSA, Shapers, comparators) come from several projects (INNOTEP, ILC T2K)

2 types of detectors : CdZnTe and Si diode

- TOF : 1ns resolution
- TOF PET : very high timing resolution << 200ps
- Very High speed ADC >> 500Ms/s… 1 GMs/s ?
- Beam profiler : high counting rate (100Me/s)
- Very fast preamplifier and shapers

Microelectronic part of the EREBUS project

"Intelligent sensor to limit the nitration of industrial process and the rejection of VOC (Volatile Organic components)"

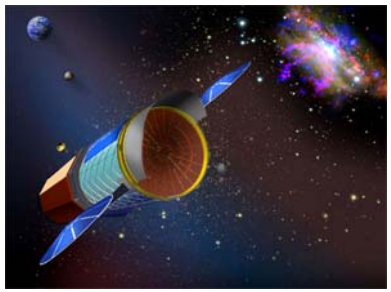
- Preamplifier, shaper, ADC and treatment.

- Technology transfer

  EUREKA Project

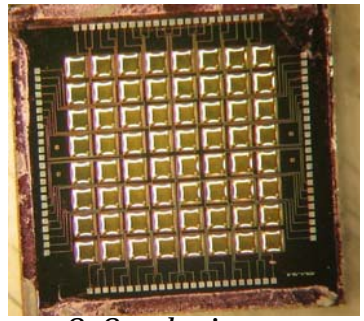
  PhD student "bourse CIFFRE"

LT Mux for XRAY micro calorimeters Matrix



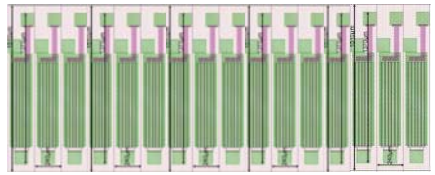
Satellite IXO

- **Target: IXO** satellite (ESA)
- **High resolution** (5eV @ 6kEV) **XRay spectro-imager**
- **fine pitch:** 4000 pixels
- Calorimeter Matrix manufactured by **CEA/LETI**
- Detector temperature : 50 to 100mK
- Photon by photon detection => high speed FE



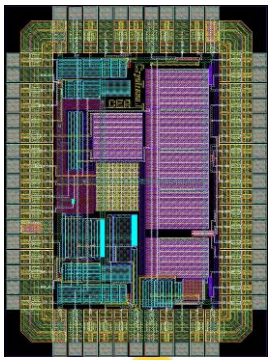
8x8 calorimeter matrix prototype

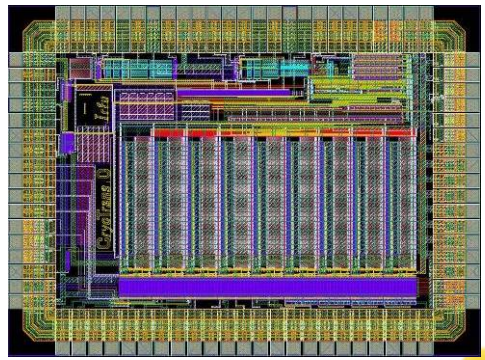
- Front_End electronics close to the detector:
- **Must operate @ 4K**
- Amplify and multiplex the detector pulses
- Low noise, low power **(30µW/channel)**



Multi HEMT chip.

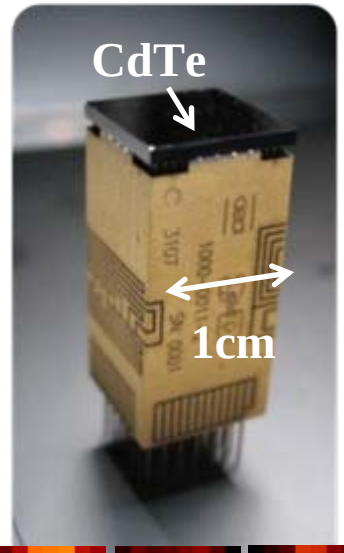
- **Technological choices:**
  - HEMT (from CNRS/LPN) for the first stage (impedance adaptation + gain).
  - AMS 0.35µm SiGe chip for extra gain + 32=>1 mulitplexing:
    - Behavior of SiGe @ 4K evaluated on previous chips.
    - 2 prototype circuits submitted in July 2009.

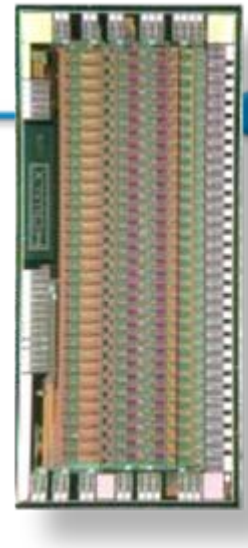




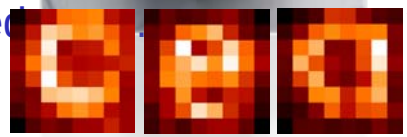
Idef-X 2.E for ECLAIRs.

- For SVOM/ECLAIR: Gamma Ray Burst satellite.
- CdTe Detectors.
- 32 channels. 2.2 mW/ ch.
- Slow control => many parameters tunable
- Self triggered / 1 Thresh/channel.
- **1µs-10µs** selectable shaping.
- Peak detector. Mux Output.
- Sparsification and zero-supress.
- ~200mV/fC**.** 50ke- linear range (220 keV CdTe)
- 60 e- rms noise with detectors.
- Rad-tolerant > 200krad. Use of Latch-up hardened
- Space qualification in progress.

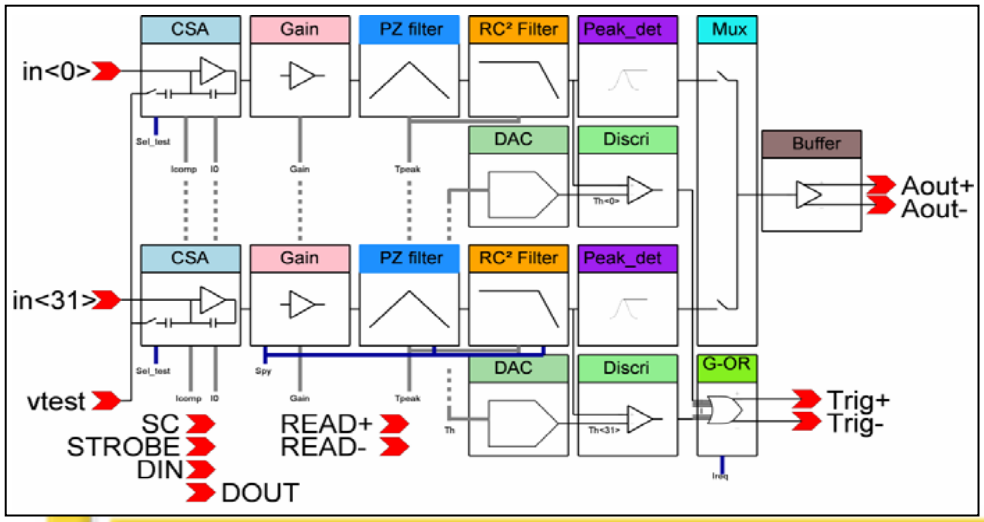


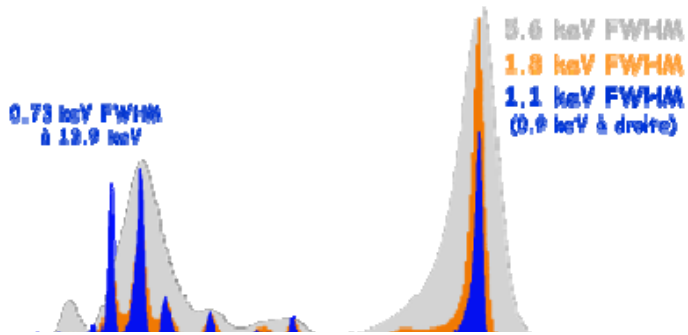


AMS0.35µm CMOS EPI. 18mm^2. 2000 chips manufactured



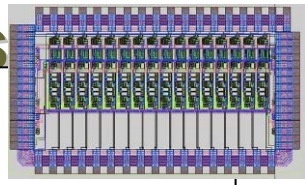
60keV picture from ^{241}Am source + mask (Caliste 64)



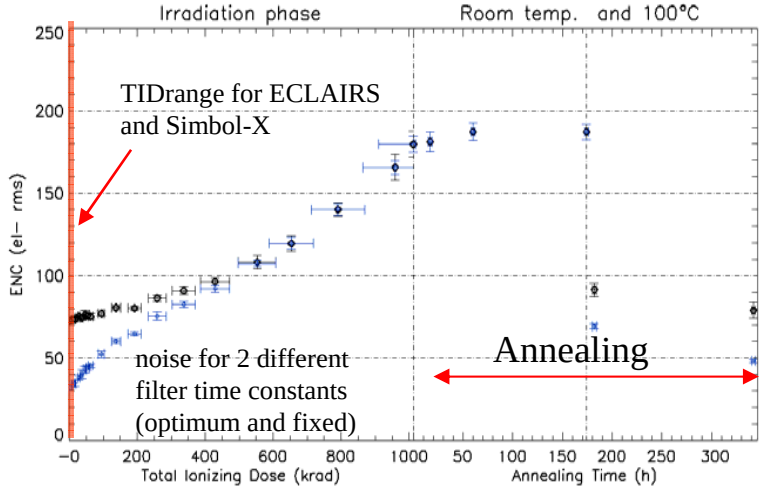


Noise and threshold 5x better than with the previous generation

IDeF-X family : radiation hardness



- IDeF-X V1.0
  - TID: Irradiation with 60CO @ 500rad/h up to 1 Mrad

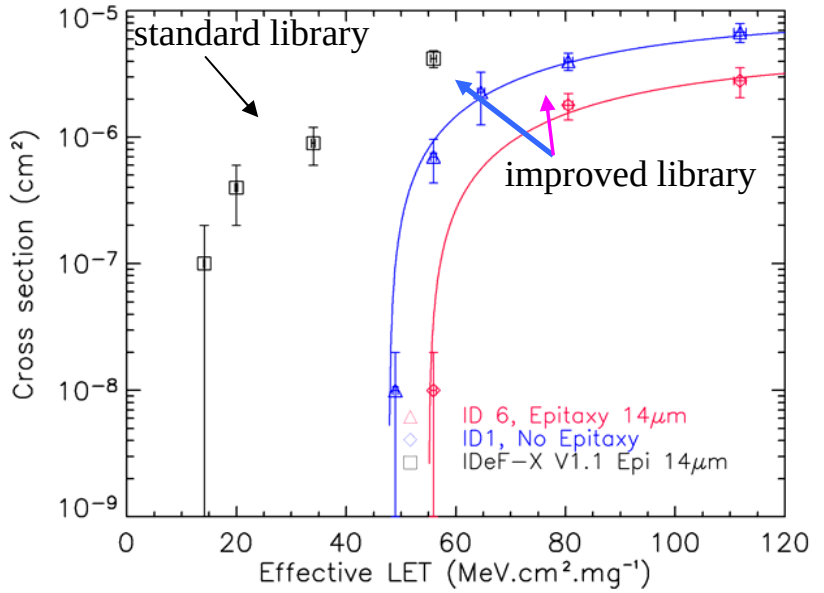


- Up to 1 Mrad: no visible effect excepted on noise performances => Noise increase cleared by annelaing.

For ECLAIRs and SIMBOL-X (TID<10krad)

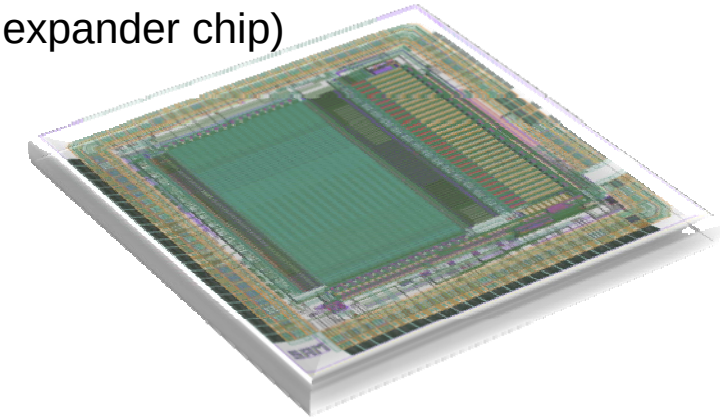
New digital library to improve hardness against SEL:

Test on Idef-X V2.E => no anti latchup circuit required for the ECLAIRs mission.

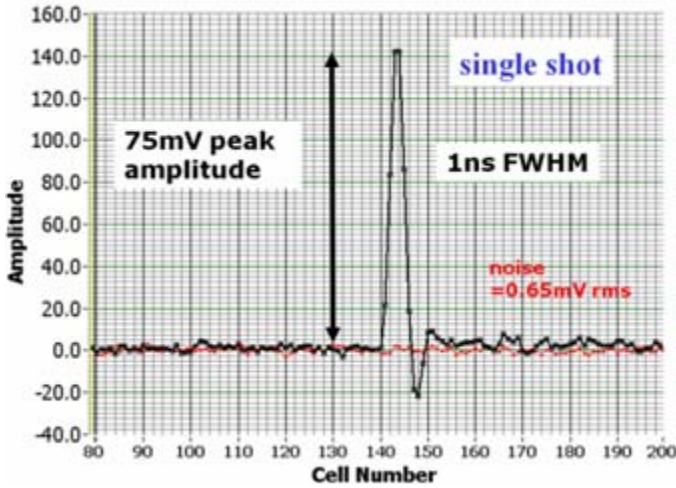


The SAM (swift analog memory) chip for the HESS2 experiment:

- Readout for the fast PMTs of the HESS2 camera
- High RO speed Gsample/s analogue memory (time expander chip)
- Number of ch 2
- Number of cells/ch 256
- **Sampling Freq 0.7-3.2GS/s**
- Readout Speed >16 MHz
- BW **450 MHz**
- PW 300 mW
- Dynamic range 12.6 bits rms
- Simultaneous R/W No
- Smart Read pointer Yes
- 6000 chips manufactured: 95% Yield
- New chip under design => Cerenkov Telescope Array



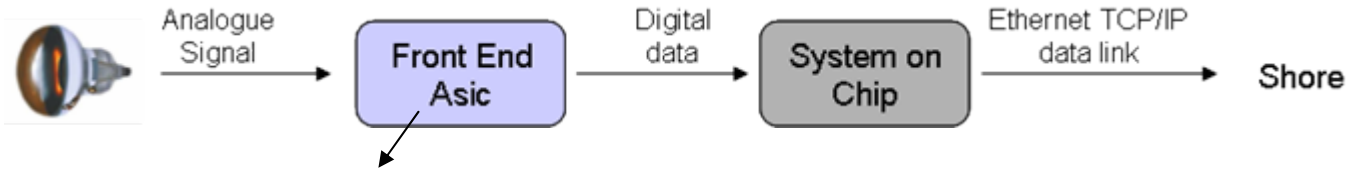
AMS CMOS 0.35µm.
50k transistors, 11mm²



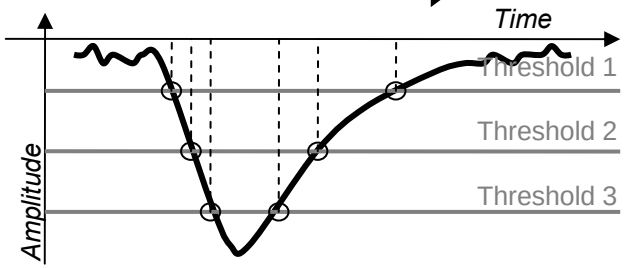
Narrow pulse sampled by SAM @ 3.2GS/s

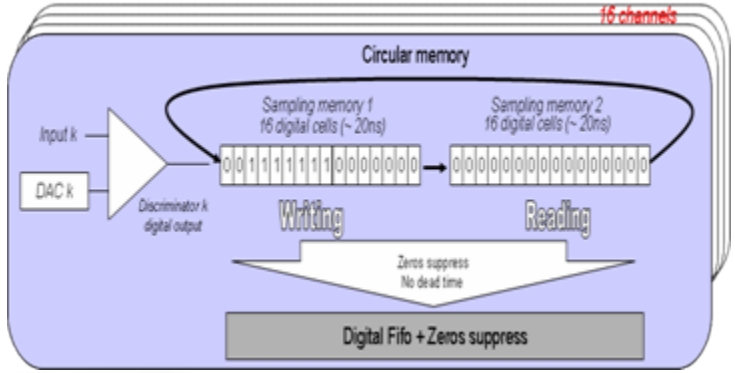
SCOTT: RO chip for the PMT of the Km³ neutrino submarine detector

-In the frame of KM3NET: (FP6 & FP7): baseline design



-SCOTT: based on the generalized TOT (time over threshold) concept:





•No amplitude coding, but:

• Time coding for each threshold crossing (1ns precision)

•16 independent discriminators channels with threshold set by 10 bit DACs.

• Versatile design, can be configured by slow control:

-1 PMT => 16 coding channels (~1 GS/s 4bit ADC(linear or nonlinear scale depending on the thresholds)

- 16 PMTs => 1- coding channels: (~TDC)

•Zero supress

•Derandomization (FIFO).

•Data driven readout

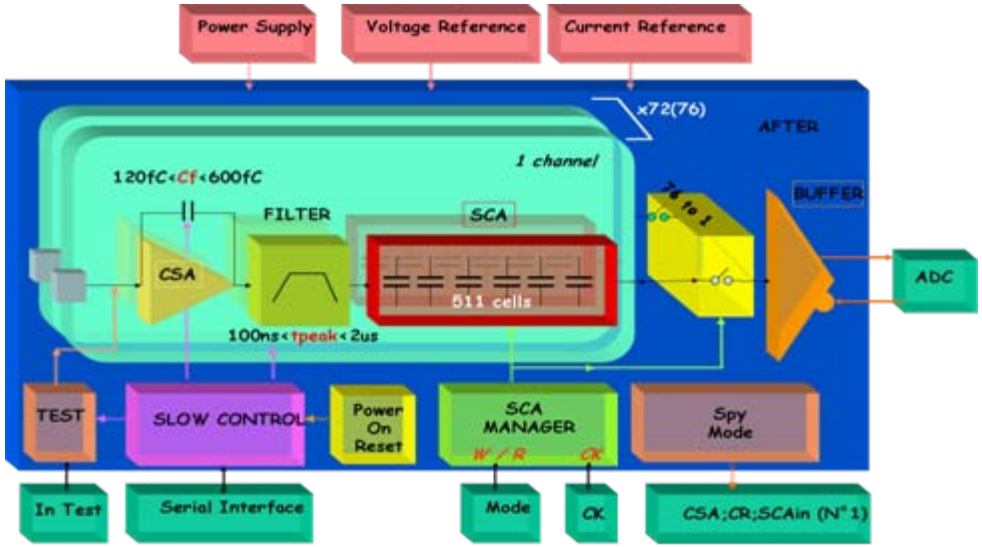
•SCOTT0= SCOTT single shot version prototyped in dec 2008 => concept validated.

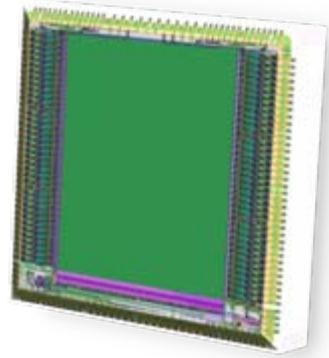
•AMS BiCMOS 0.35µm.

•SCOTT1 (with final RO) submitted sept. 7th 2009.

The AFTER chip for the TPC of T2K

Design to read the 120.000 Micromegas pads of the TPC of T2K.
Combine a low noise Front-end & and a large depth and S/N SCA.
Installation @ Tokai in progress. Start at the end 2009.





AMS CMOS 0.35µm
7.8 x 7.4 mm²
500.000 transistors
6000 chips manufactured
85% Yield

Main Design features

- **72** channels x **511** analog memory cells;
- F_{write}: **1-100MHz**; F_{read}**: 20MHz**
- **4** Charge Ranges (120fC to 600fC)- 1% INL
- Supports positive or negative input signals
- **16** Peaking Time Values (**100ns to 2µs**)
- Constant dead time (2ms to read all the SCA)
- **S/N >11 bit rms.**

AGET: A future improved AFTER

- Based on AFTER
- 1 discri/channel, 1 threshold/channel
- Multiplicity output. Autotriggerable.
- On chip zero-supress
- New 50ns shaping & “high energy” ranges
- New modes of readout
- Prototype submission: end of 2009

Monolithic Active Pixel Sensors (MAPS): A Long Term R&D

- **Main objective: ILC, with staggered performances**
  - MAPS applied to other experiments with intermediate requirements

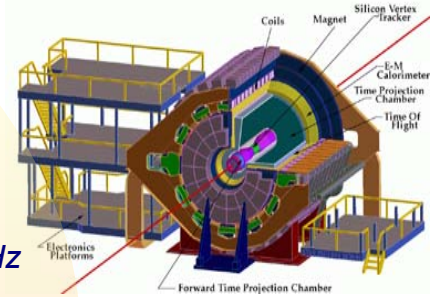
EUDET 2007/2009

Beam Telescope

- FP6 EUDET Project (DESY-Hamburg, Germany)
  - Surface: 6 x 2 cm^2
  - Read-out speed: A. 20 MHz → D. at 100 MHz
  - Temp. & Power: No constraints
- STAR Experiment (RHIC – Brookhaven, USA)
  - Surface: ~1600 cm^2
  - Read-out speed: A. 50 MHz → D. up to 250 MHz
  - Temp. & Power: 30°C, ~100mW/cm^2
- CBM Experiment (GSI – Darmstadt, Germany)
  - Surface: ~500 cm^2
  - Read-out speed: D. 15 x 10^9 pixels/sensor/s
  - Rad Tol: 1 MRad, > 10^{13} N_{eq}/cm^2
- ILC Experiment
  - 5-6 layers of detection: ~3000 cm^2
  - Read-out speed: D. 15 x 10^9 pixels/sensor/s
  - Temp. & Power: 30°C, ~100 mW/cm^2
  - Rad Tol: ~300 kRad, ~10^{12} N_{eq}/cm^2

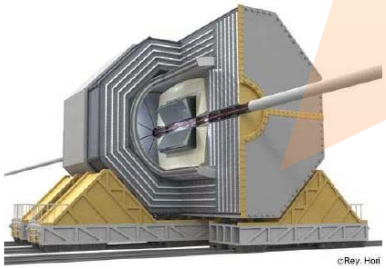
STAR 2010

Solenoidal Tracker at RHIC



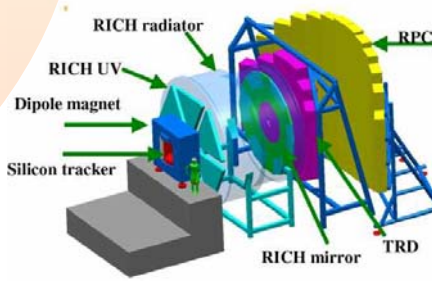
ILC >2012

Internatinal Linear Collider



CBM 2012

Compressed Baryonic Matter



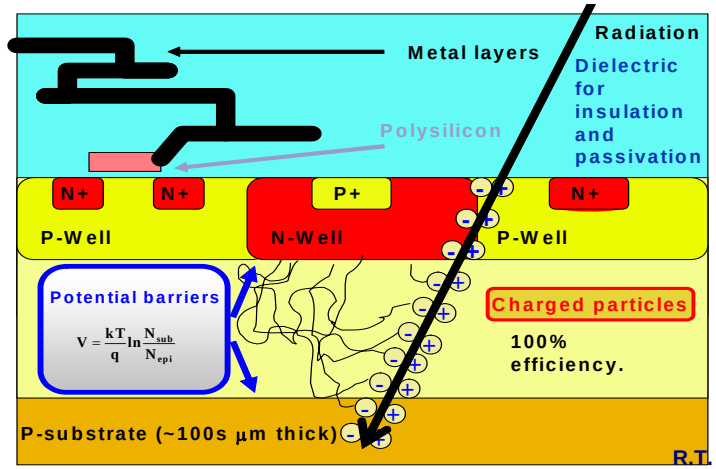
➔ **Spinoff: Interdisciplinary Applications, biomedical, …**

- Partnerships: GIS IN2P3/Photonis & GIS IN2P3/SAGEM & Ohio University & Michigan University…

Development of MAPS for Charged Particle Tracking

- ***In 1999, the IPHC CMOS sensor group proposed the first CMOS pixel sensor (MAPS) for future vertex detectors (ILC)***
  - *Numerous other applications of MAPS have emerged since then*
  - *~10-15 HEP groups in the USA & Europe are presently active in MAPS R&D*

- ***Original aspect: integration sensitive volume (EPI layer) and front-end readout electronics on the same substrate***
  - *Charge created in EPI, excess carries propagate thermally, collected by N_{WELL}/P_{EPI}, with help of reflection on boundaries with P-well and substrate (high doping)*
    - *Q = 80 e^-h / µm ➔ signal < 1000 e^-*
  - *Compact, flexible*
  - *EPI layer ~10–15 µm thick*
    - *thinning to ~30–40 µm permitted*
  - *Standard CMOS fabrication technology*
    - *Cheap, fast multi-project run turn-around*
  - *Room temperature operation*

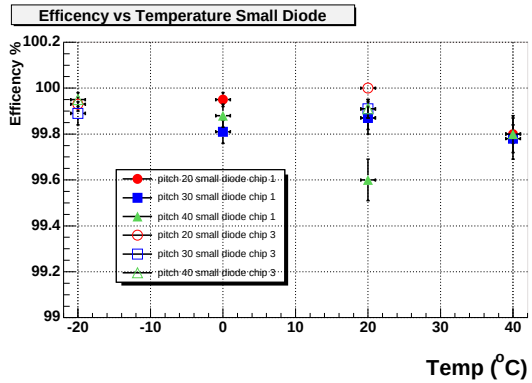


- ➔ ***Attractive balance between granularity, material budget, radiation tolerance, read out speed and power dissipation***

  BUT
  - *Very thin sensitive volume → impacts signal magnitude (mV!)*
  - *Sensitive volume almost un-depleted → impacts radiation tolerance & speed*
  - *Commercial fabrication (parameters) → impacts sensing performances & radiation tolerance*
  - *N_{WELL} used for charge collection → restricts use of PMOS transistors*

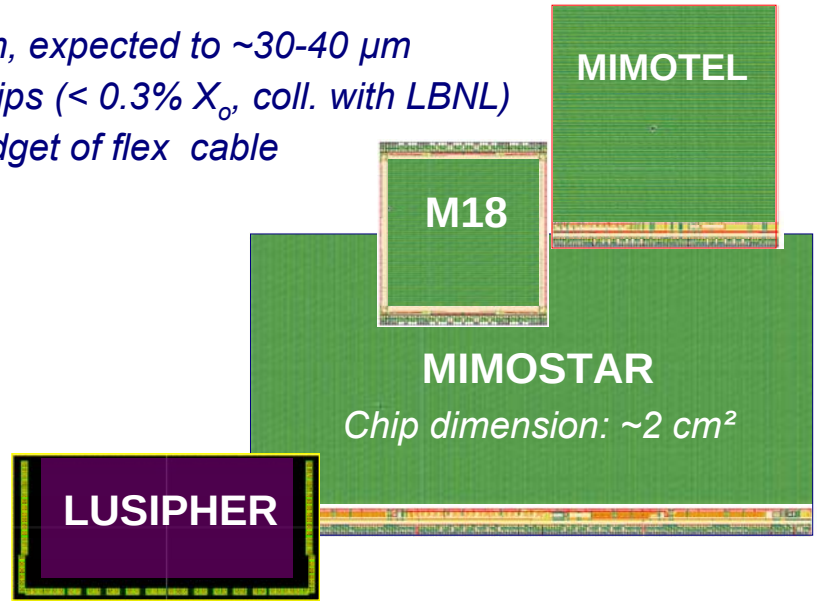
Achieved Performances with Analogue Readout

- ***MAPS provide excellent tracking performances***
  - *Detection efficiency ~100%*
    - *ENC ~10-15 e^- , S/N > 20-30 (MPV) at room temperature*
  - *Single point resolution ~ µm, a function of pixel pitch*
    - *~ 1 µm (10 µm pitch), ~ 3 µm (40 µm pitch) ➔ analogue output!*
  - *Radiation tolerance:*
    - *Ionising radiation tolerance: O(1 M Rad)*
    - *Non ionising radiation tolerance: 2x10^{12} N_{eq}/cm^2 (20 µm pitch) → 10^{13} N_{eq}/cm^2 (10 µm pitch)*
  - *System integration*
    - *Thinning (via STAR collaboration at LBNL) ~50 µm, expected to ~30-40 µm*
    - *Development of ladder equipped with MIMOSA chips (< 0.3% X_o, coll. with LBNL)*
    - *Edgeless dicing / stitching → alleviate material budget of flex cable*



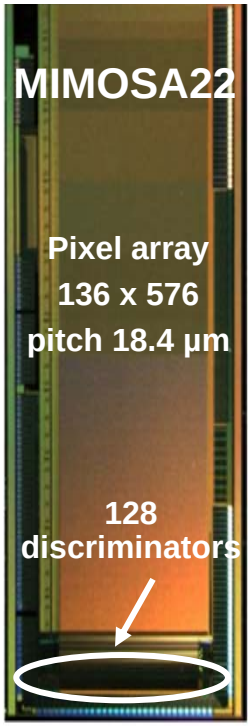
MAPS: Final chips:

- *MIMOTEL (2006): ~66 mm², 65k pixels, 30 µm pitch*
  EUDET Beam Telescope (BT) demonstrator
- *MIMOSA18 (2006): ~37 mm², 262k pixels, 10 µm pitch*
  High resolution EUDET BT demonstrator
- *MIMOSTAR (2006): ~2 cm², 204k pixels, 30 µm pitch*
  Test sensor for STAR Vx detector upgrade
- *LUSIPHER (2007): ~40 mm², 320k pixels, 10 µm pitch*
  Electron-Bombarded CMOS for photon and radiation imaging detectors



- **BUT: moderate readout speed for larger sensors with smaller pixel pitch!**

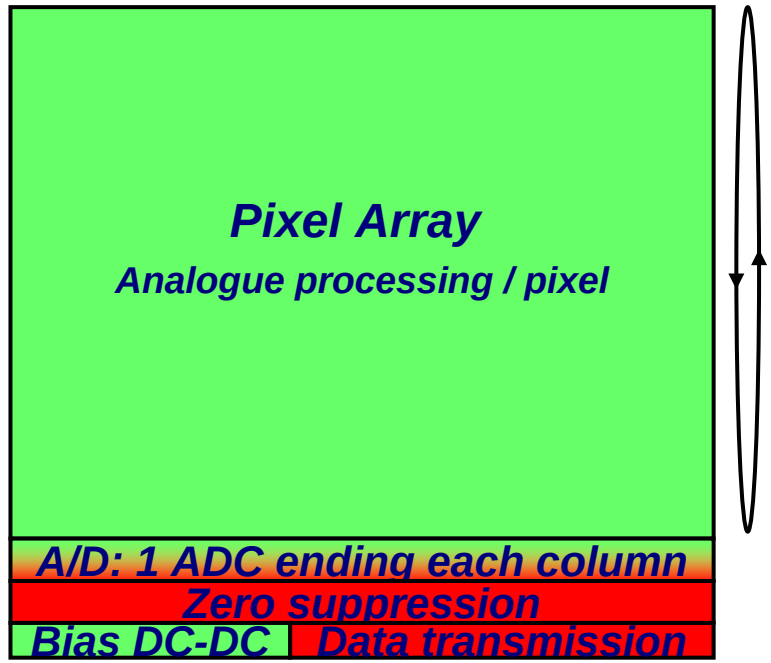
MAPS performance Improvement

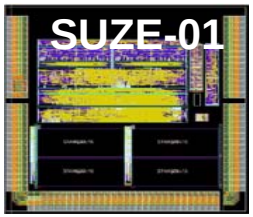


➔ *R&D on high readout speed, low noise, low power dissipation, highly integrated signal processing architecture with radiation tolerance*

❶ ***Architecture of pixel array organised in // columns read out:***

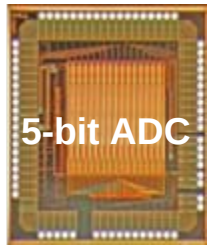
- *Pre-amp and CDS in each pixel*
- *A/D: 1 discriminator / column (offset compensation)*
- *Power vs Speed*
  - *Power ➔ Readout in a rolling shutter mode*
  - *Speed ➔ All pixels belonging to the same row are read out simultaneously*
- *MIMOSA8 (2004), MIMOSA16 (2006),* ***MIMOSA22 (2007/08)***





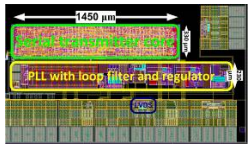
❷ ***Zero suppression logic:***

- *Reduce the raw data flow of MAPS*
- *Data compression factor ranging from 10 to 1000, depending on the hit density per frame*
- ***SUZE-01 (2007), see poster A. HIMMI***



❹ ***4–5 bits ADCs (~10^3 ADC per sensor)***

- *LPCC, LPSC, IRFU, IPHC collaboration*
- *Potentially replacing column-level discri.*
- *5 bits: σ_{sp} ~1.7–1.6 µm*
  4 bits: σ_{sp} < 2 µm for 20 µm pitch
- *Next step: integrate ADCs with pixel array*



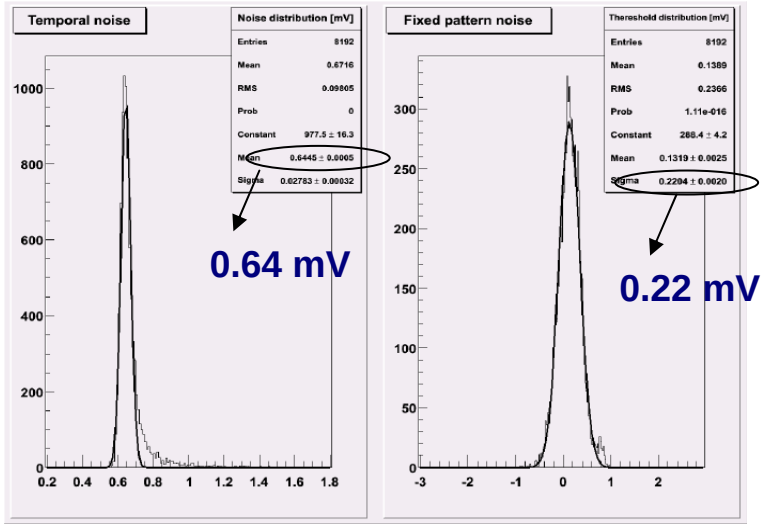
❸ ***Serial link transmission with clock recovery***

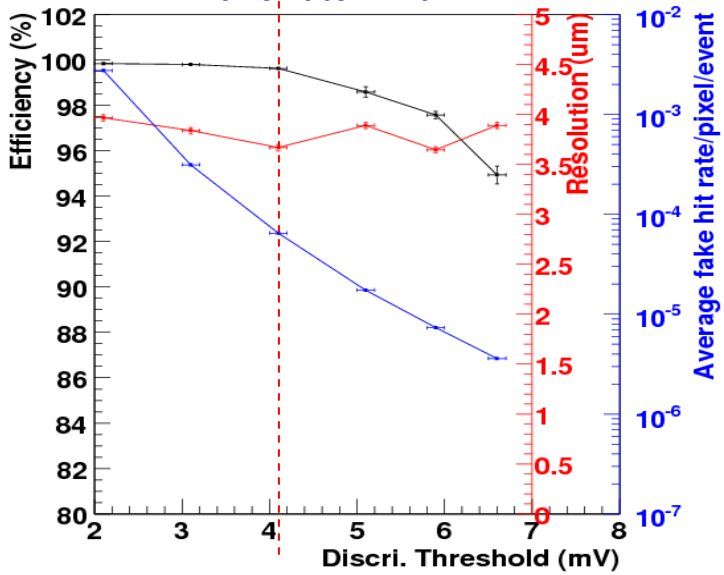
- *Prototype (2008-2009)*
- ***See poster I. VALIN***

❺ ***Voltage regulator & DC-DC converter***

MIMOSA22 & SUZE-01 Test Results

- ***MIMOSA22:*** ***(15 µm EPI) 136 x 576 pixels + 128 column-level discriminators***
  - **Laboratory test:**
    - *Temporal Noise: 0.64 mV ➔ 12 e⁻*
    - *FPN: 0.22 mV ➔ 4 e⁻*
  - **Beam test at CERN SPS (120 GeV pions)**
    - *Threshold ~ 4 mV ➔ 6 x σ noise*
      - *Detection Efficiency > 99.5%*
      - *Single point resolution < 4 µm*
      - *Fake rate < 10^{-4}*





- ***SUZE-01:***
  - **Lab. test :**
  - *Design performances tested at the nominal frequency with safety margin of 20%, at* room *Temp*
    - *No pattern encoding error, can handle > 100 hits/frame at rate ~200 ns per pixel row*
  - **Still to do :** *improve radiation tolerance (SEU, SEL) of digital circuits (including memories)*

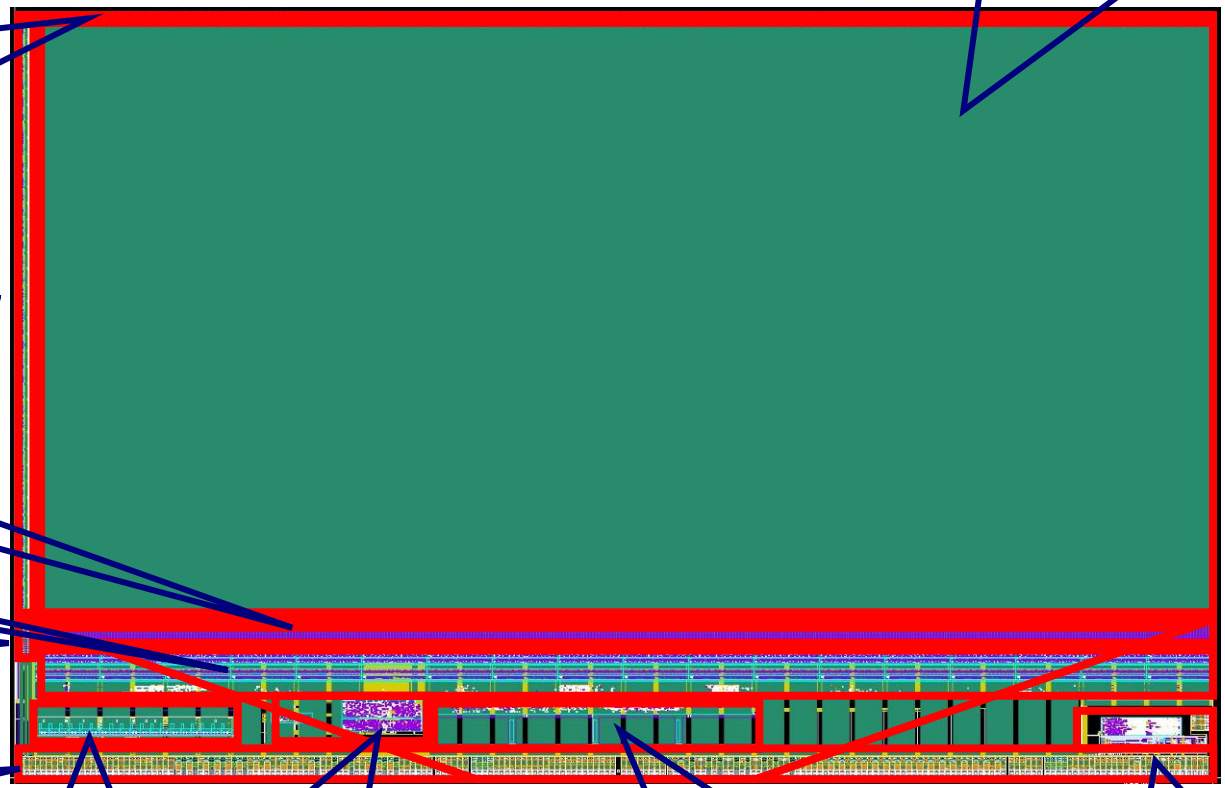
MIMOSA26: 1st MAPS with Integrated Ø

CMOS 0.35 µm OPTO technology

Chip size : 13.7 x 21.5 mm²

- Pixel array: 576 x 1152, pitch: 18.4 µm
- Active area: ~10.6 x 21.2 mm²
- In each pixel:
  - Amplification
  - CDS (Correlated Double Sampling)

- Testability: several test points implemented all along readout path
  - Pixels out (analogue)
  - Discriminators
  - Zero suppression
  - Data transmission



- Row sequencer
- Width: ~350 µm

- 1152 column-level discriminators
  - offset compensated high gain preamplifier followed by latch

- Zero suppression logic

- Reference Voltages Buffering for 1152 discriminators

- I/O Pads
  Power supply Pads
  Circuit control Pads
  LVDS Tx & Rx

- Current Ref.
- Bias DACs

- Readout controller
- JTAG controller

- Memory management
- Memory IP blocks

- PLL, 8b/10b optional

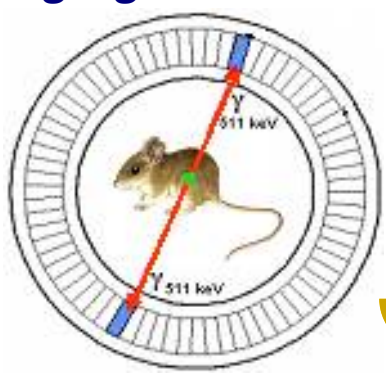
Summary MAPS

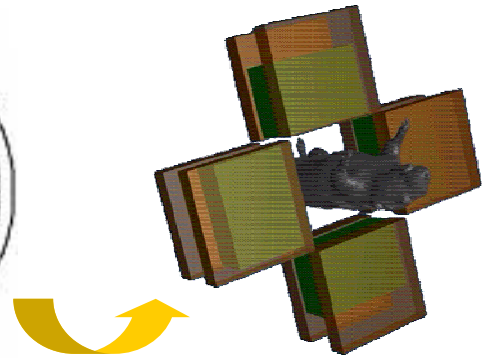
- ***The First reticule size MAPS with binary output and integrated zero suppression logic has been designed and fabricated***
  - *Small pitch pixel (18.4 µm), Large sensitive area (> 2 cm^2)*
  - *High binary read-out speed : ~10 K frames/s*
  - ➔ ***2D MAPS have reached necessary prototyping maturity for real scale applications:***
  - *STAR vertex detector upgrade: MIMOSA26x1.7 (may also equip EUDET BT, ~50 µm)*
  - *Architecture will be extended to MVD-CBM (SIS-100) and is proposed for Vx det.-ILC*
- ***The emergence of fabrication processes with depleted epitaxy / substrate opens the door to :***
  - *Substantial improvements in read-out speed and non-ionising radiation tolerance*
    - *Non-ionising radiation tolerance up to 10^{14} N_{eq}/cm^2 is expected*
  - *"Large pitch" applications ➔ trackers (e.g. Super LHC)*
- ***Translation to 3D integration technology :***
  - *Resorb most limitations specific to 2D MAPS*
    - *T type & density, peripheral insensitive zone, combination of different CMOS processes*
  - *Offer an improved read-out speed : O(µs) !*
  - *Many difficulties to overcome (ex. heat, power)*
  - *R&D in progress ➔ 2009/10 important step for validation of this promising technology*

µE for Biomedical Application

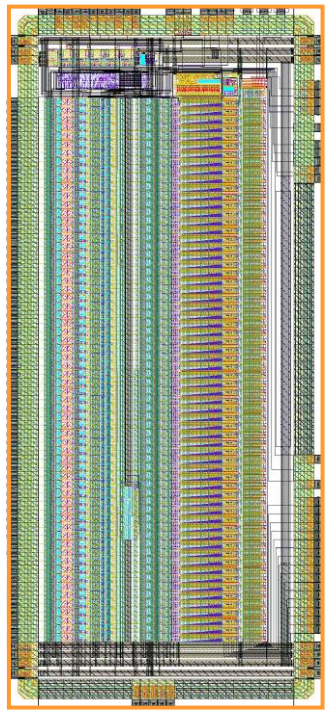
See talk by N. Olivier-Henry

- ***IPHC Imabio Project: small animal PET imaging***
  - *4 modules arranged around the animal*
  - *Matrix of 32 ×24 crystals / module*
    - *1.5mm×1.5mm×25mm LYSO(Ce)*
  - *Read at both ends by MCP photo-detectors*
    - *MCP (Multi Channel Plate)*
  - *3072 crystals and 6144 electronic channels*
  - *100 ASICs of 64 channels*



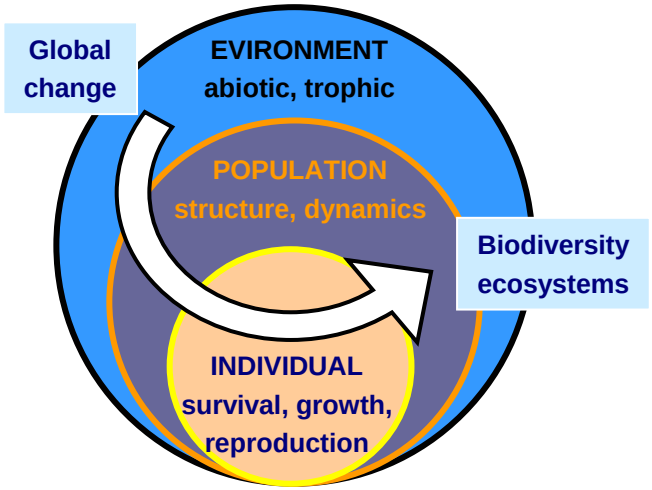


- ***IMOTEPAD64: 64 channels readout circuit***
  - *Chip dimensions: 3.68 x 8.26 mm², 100 µm pitch*
  - *Input dynamic range: 11 bits, ~ fC – 104 pC*
    - *Adjustable gain : 6 bits*
    - *Shaping time: 300 ns,*
    - *Analogue sampling, < 3 % nonlinearity*
  - *Time resolution: 625 ps ➔ ~ 200 ps (next generation)*
    - *Measured Jitter < 20 ps rms*
  - *Readout frequency: 100 kHz*
    - *CK: 50 MHz*

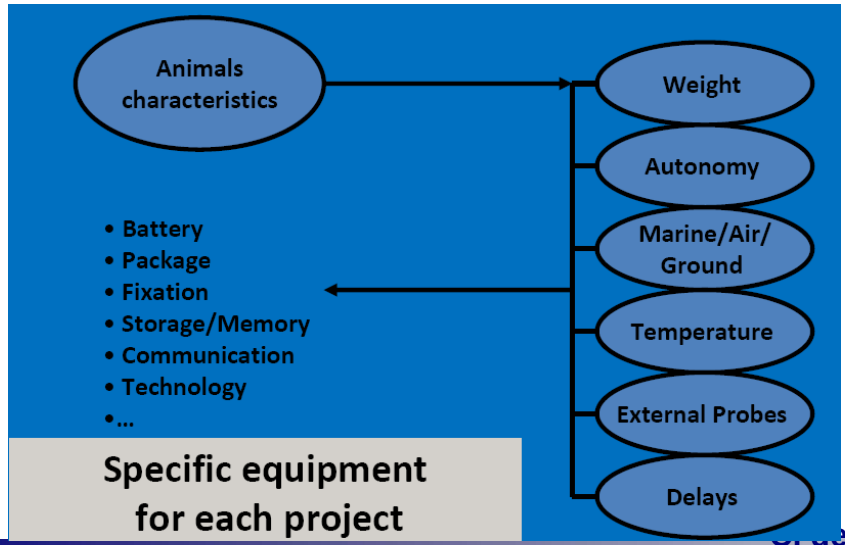


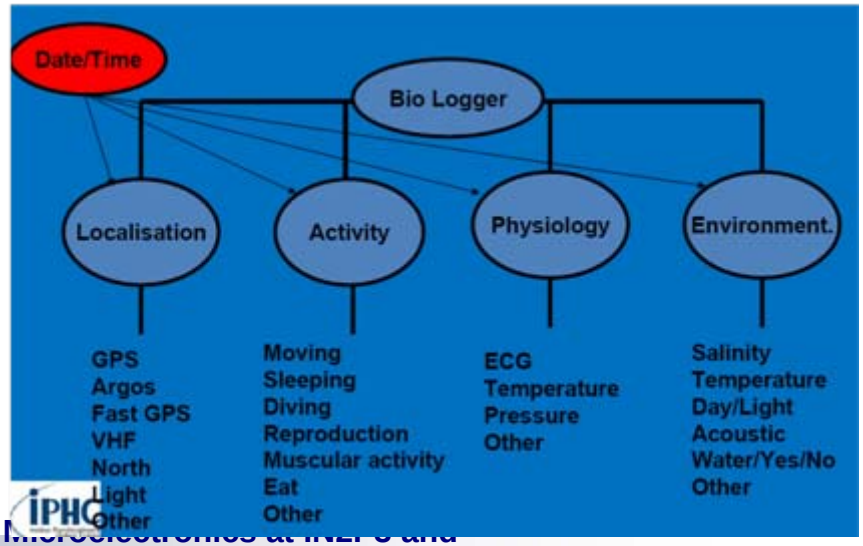
µE for Bio-logging

- IPHC ➔ Multidisciplinary laboratory ➔ 3 departments (DEPE, DSA, DRS)
- One of R&D activities: Bio-logging:



Large diversity of request
No standard technology
No standard development
Specific requirement for each project
Time to deployment short





ASIC for Bio-logging

- **Integration ➔ miniaturisation:**
  - Sensors + electronics ➔ final goal
    - Master sensors
      - Temperature (2), Pressure/Temperature, Light, Logical (water presence/counter)
    - Secondary sensors
      - Zeegbee, GPS, Acc 3D
    - Other sensors
      - ECG/ Analogue input, Digital compass

Access technology & IP

- **Low power design:**
  - Analogue & mixed design:
    - Ultra low power ADC design
  - Digital (Asynchronous ?) Design: from
    - Controller for sensor scanning and data storage

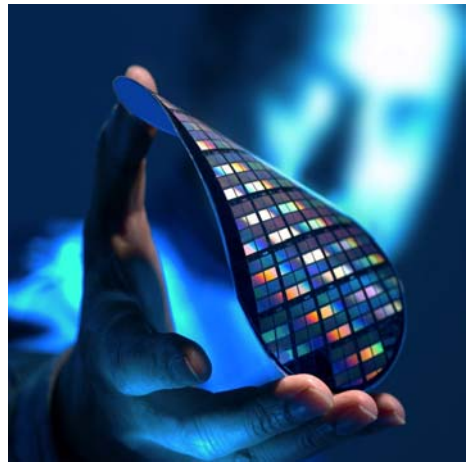
    to
    - Ultra low power Micro-controller:
      - for data compression and treatment
      - for complex trigger

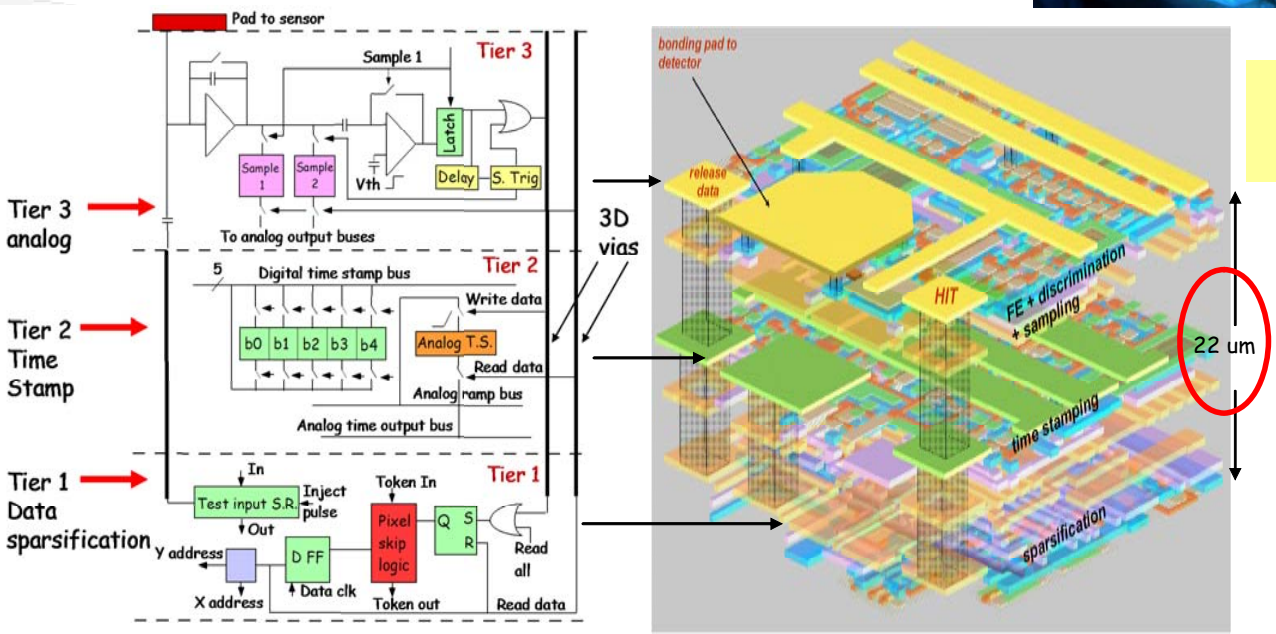
Collaboration

3D technology

- Increasing integration density
  - Large industrial market (imagers, processors, memories…)
  - Uses ~1 µm Through Silicon Vias
  - Requires wafer thinning to ~10 µm
  - A new major revolution coming up !
- Promoted into HEP by Ray. Yarema (FNAL)
  - IN2P3 joined FNAL 3D consortium
  - CPPM, IPHC, IRFU, LAL/OMEGA,LPNHE

See talk by JC Clémens



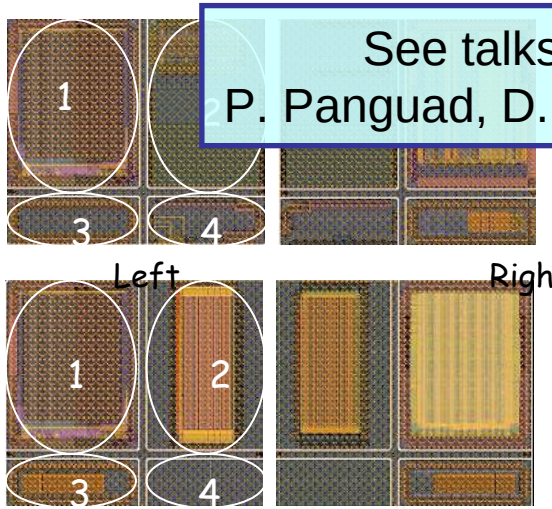


V1P1 3D chip by FNAL

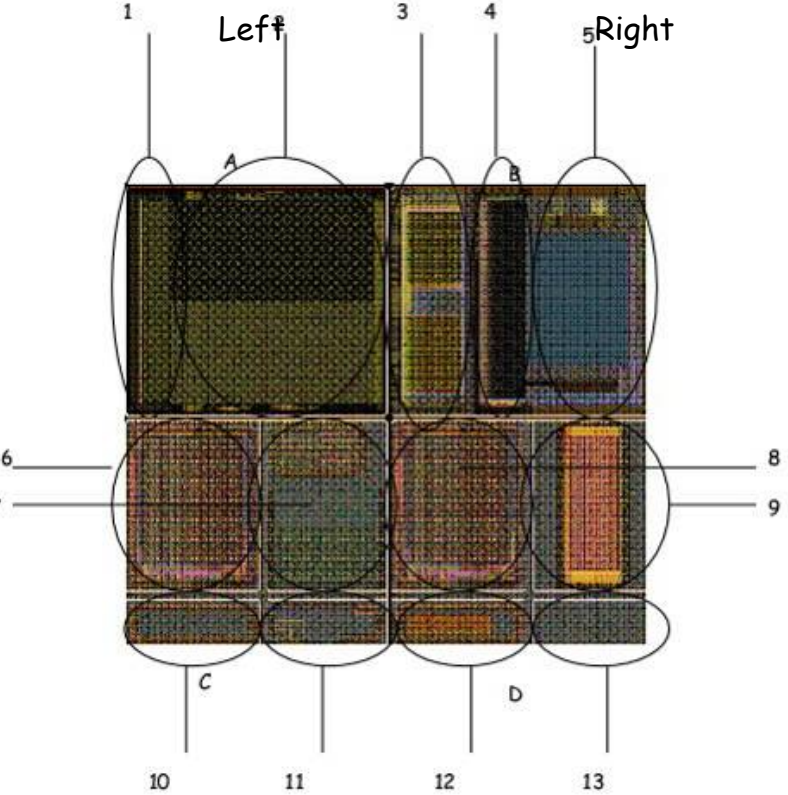
IN2P3 participation in 3D FNAL run

- CPPM/Bonn - ATLAS 2D pixel design based on earlier design in IBM 0.13 um (FEI4_prototype)
- CPPM – SEU resistant register and TSV/bond interface daisy chain to measure TSV and bond yield.
- CPPM/Bonn – ATLAS 3D pixel design foreseen for ATLAS upgrade
- OMEGA – 24x64 pixel array for SLHC

See talks by
P. Panguad, D. Thienpont



- IPHC_INFN CAIRN_1: - Multi purpose pixel sensor: ILC, bio-medical applications …
- IPHC_IRFU CAIRN_2: Prototype sensor for ILC with rolling shutter readout mode
- IPHC CAIRN_3: - Prototype sensor for ILC, 12 µm pitch, 5 bits time stamp
- IRFU-IPHC CAIRN_4: - prototype sensor fo ILC with rolling shutter readout mode
- CMP Memory: CMP Anti-latch up SRAM



Chips shown at TWEPP

- Fast ADCs & DACs for ILC: LPSC Grenoble (L. Gallin-Martell)
- 12 bits 35 MHz ADC : LPSC Grenoble (F. Rarbi)
  - Talk « building blocks » by F. Rarbi
- MicroMegas DHCAL readout : LAPP Annecy (R. Gaglione)
- DLLs for SNemo : LPC Caen (V. Tocut)
  - Talk « building bocks » by L. Leterrier
- Discri for FEI4 : CPPM Marseille (M. Mehouni)
- Analog memory for km3 : CPPM Marseille (L. Caponetto)
- ASPIC LSST readout : LAL+LPNHE (F. Wicek)
  - Talk « building blocks » by R. Sefri

Les études en cours

- Initialement pour l'expérience CLAS12 en développement : étude d'un TDC pour mesure de temps de vol pour scintillateur résolution inférieure à 100ps sur 0.35µm SiGe d'AMS
- Ce projet a rejoint les études pour PMm^2 Conception de la partie TDC de l'ASIC Omega PARISROC2, optimisation de la double rampe pour atteindre une résolution de 150ps sans temps mort local. Run en novembre 2009

Perspectives

- Adaptation des travaux réalisés pour PARISROC2 à l'électronique du projet CLAS12 (lecture par galettes de microcanaux)
- Préamplificateurs de charge pour l'expérience GASPARD (détecteurs Silicium) :
  - ~ 15000 voies
  - Quantité de matière minimale
  - Faible consommation
  - Faible bruit 150-200e^-
  - Dynamique 14 bits

Chips at Subatech [C. Renard]

- Low noise amplifier for CODALEMA in 0.35µm CMOS
  - Continuation of BiCMOS 0.8 µm charge preamp for CODALEMA radio detection of atmospheric showers
- Variant (simplified) of IDEFIX for 2012 ?

Chips at LPNHE [H. Lebbolo]

- ASPIC : Dual slope integrator CCD readout for LSST
  - Talk « building blocks » by R. Sefri
- CLASSIC : Clamp and sample variant for CCD readout for LSST
- ILC microstrip readout (SiLC collaboration + EUDET) IMC 130 nm
  - Talk « building blocks » by T. Hung Pham
- Low noise current preamp for photodiode telescope calibration
- Possible participation in SuperB for TDC

Conclusion

- Strong, experienced teams, gathered in poles to realize complex chips
- Designs in SiGe 0.35 µm, IBM & Chartered 130nm
- 3D developments with FNAL
- Thanks to Christine Hu (IPHC), Jean-Claude Clémens (CPPM), Eric Delagnes (IRFU), Jacques Lecoq (LPCClt), Hervé Mathez (IPNL) who provided slides for TWEPP
- Thanks to V. Chambert (IPNO), C. Renard (Subatech), H. Lebbolo who provided information for this talk

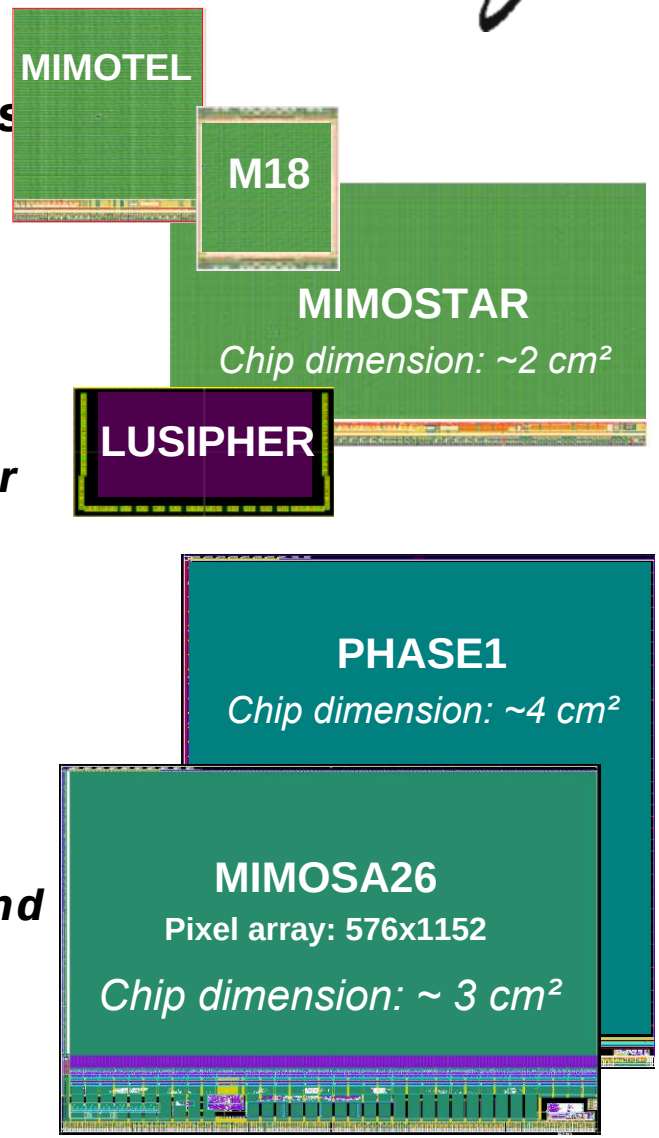
R&D Axes

See talks by
G. Dozère, I. Valin

- *In-pixel gain and radiation tolerance improvements:*
  - ***Simple 3T pixel with off line CDS ➔ in-pixel amplification + CDS without S/N degradation***
  - ***Ionising radiation: pixel special layout, increase readout speed***
    - ***Up to 1Mrad @ -20°C, $t_{r.o.}$ = 180 µs, no change to detection eff. ➔ crucial @ room temperature***
  - ***Non ionising radiation ➔ High resistivity sensitive volume ➔ faster charge collection***
    - ***Exploration of a technology with depleted epitaxial layer: MIMOSA-25 (2008) > 3x10^{13} N_{eq}/cm²***
    - ***Exploration of a new VDSM technology with depleted substrate: MIMO_LePix (2009/2010):***
      - ***Project driven by CERN for SLHC trackers also attractive for CBM, ILC and CLIC Vertex Detectors***
- *Readout speed improvements:*
  - ***Sensor organised for // columns read out + column-level discrimination:***
    - ***IPHC-IRFU Collaboration: MIMOSA8 (2004), MIMOSA16 (2006), MIMOSA22 (2007/08)***
  - ***Zero suppression circuit for data flow reduction:***
    - ***SUZE (2007): compression factor: 10-1000, function of the hit***

Final Chips

- *Analogue output MAPS*
  - ***MIMOTEL (2006): ~66 mm², 65k pixels, 30 µm pitch***
    - ***EUDET Beam Telescope (BT) demonstrator***
  - ***MIMOSA18 (2006): ~37 mm², 262k pixels, 10 µm pitch***
    - ***High resolution EUDET BT demonstrator***
  - ***MIMOSTAR (2006): ~2 cm², 204k pixels, 30 µm pitch***
    - ***Test sensor for STAR Vx detector upgrade***
  - ***LUSIPHER (2007): ~40 mm², 320k pixels, 10 µm pitch***
    - ***Electron-Bombarded CMOS for photo and radiation imaging detectors***



- *Digital output MAPS:*
  - ***PHASE1 (2008): ~4 cm², 410k pixels, 30 µm pitch***
    - ***Without data suppression, 1st MAPS with EUDET JRA1 readout***