

# Les ROC chips

Laboratoire : UMS OMEGA

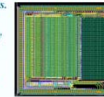
Sujet : aperçu des circuits complets réalisés par le pôle OMEGA : un nom de contact est associé à chaque circuit

*Omega*

## The ROC chips

### HARDROC / MICROROC

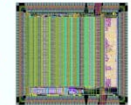
HARDROC is a 64-channel front-end ASIC designed to readout negative fast (<1ns) and short (<10ns) current pulses from various detectors (Multi Anode Photo Multipliers, Resistive Plate Chambers). HARDROC provides a semi-digital readout with three thresholds tunable between 10 fC up to 10 pC and integrates a 128-deep digital memory to store the 2 x 64 discriminator outputs as well as the bunch crossing identification coded over 24 bits. The three thresholds are set by three integrated 10-bit DACs. The gain of each channel can be tuned individually from 0 to 2 over 8 bits, allowing the compensation of non-uniformity between the 64 detector channels. Each channel can auto trigger down to 5 fC which corresponds to the 5  $\sigma$  noise limit. A multiplexed charge measurement up to 10pC is integrated and can be daisy chained. 872 slow control parameters allow versatility and various settings. The power consumption is about 1.5 mW/channel and the chip can be fully powered-down allowing a significant power reduction by disabling unused blocks. MICROROC is a variant of HARDROC and integrates an ultra low noise charge preamp (0.1 fC for a detector capacitor of 80 pF) allowing to set the threshold down to 1 fC.



Contact : Nathalie Seguin-Moreau

### MAROC

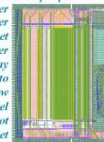
MAROC for "Multi Anode Read Out Chip" is a 64-channel chip designed to readout negative fast input current pulses such as those provided by Multi Anode Photo Multipliers. Each channel provides a 100% trigger rate for signal greater than 1/3 photoelectron and a charge measurement up to 30 photoelectrons (~5pC) with a linearity of 2%. The gain of each channel can be tuned between 0 and 2 thanks to an 8 bit variable gain preamplifier allowing to compensate the non uniformity between detector channels. A slow shaper combined with two Sample and Hold capacitors allows storing the charge up to 5pC as well as the baseline. In parallel, 64 trigger outputs are obtained thanks to two possible trigger paths : one made of a bipolar or unipolar fast (1.5 ns) shaper followed by one discriminator for the photon counting and one made with a bipolar fast shaper (with a lower gain) followed by a discriminator to deliver triggers for larger input charges (> 1pe). The discriminator thresholds are set by two internal 10-bit DACs. A digital charge output is provided by an integrated 8, 10 or 12 bit Wilkinson ADC. 828 slow control parameters allow versatility and various settings.



Contact : Sylvie Blin

### SKIROC2

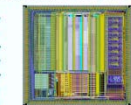
SKIROC2 is a 64-channel front-end ASIC designed to readout silicon PIN diodes. Each channel is made of a variable-gain and low-noise charge preamplifier followed by two shapers – one with a gain of 1 and the other with a gain of 10 – to provide a charge measurement from 0.2 fC up to 10 pC. A time tagging is performed by a 12-bit TDC ramp. The charges and times are stored in a 15-depth Switched Capacitor Arrays (SCA), the values of which are converted by a multi-channel 12-bit Wilkinson ADC and sent to an integrated 4 Kbytes memory. The analog value of the charge is also available on an output pin. The trigger chain is composed of a high gain fast shaper and a discriminator and allows each channel to auto trigger down to 0.2 fC. Thresholds of the 64 discriminators are set by a common 10-bit DAC and an individual 4-bit DAC per channel. Each discriminator output is sent to an 8-bit delay cell (delay time tunable between 100 ns and 300 ns) to provide the Hold signal for the SCA cells of the slow channel. The power consumption is about 1.5 mW/channel and each stage can be individually shut down when not used. 616 slow control parameters are available to set various configurations and ensure the versatility of the chip.



Contact : Stéphane Callier

### SPACIROC

SPACIROC (Spatial Photomultiplier Array Counting Integrated ReadOut Chip) is a 64-channel chip designed to readout negative fast input current pulses such as those provided by Multi Anode Photo Multipliers and for spatial and low power applications. The 64 inputs from MAPMT Anodes are amplified by an 8-bit variable gain preamplifier allowing to tune the gain of each channel between 0 and 4 and so to compensate the non-uniformity between detector channels. Each channel provides a 100% trigger rate for signal greater than 1/3 photoelectron. Charge measurements from 2pC up to 220pC are performed using a Time-over-Threshold. A fast Photon Counting (50 MHz) is done thanks to a fast shaper followed by a discriminator, the threshold of which is set by one internal 10-bit DAC. The digital part operates continuously and handles data conversion of each Photon Counting and Time-Over-Threshold channel. The digital data are transmitted via dedicated parallel communication links and within the defined Gate Time Unit (GTU). The ASIC data output rate is 40MHz. Spaciroc is radiation tolerant and its power consumption is lower than 1mW/channel.

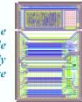


Contact : Sylvie Blin

### PARISROC

Parisroc is a 16-channel front-end ASIC designed to readout photomultiplier tubes (PMTs) in large scale applications such as water Cherenkov experiments. The concept of the ASIC is to combine an auto-trigger chip to 16 PMTs to obtain an autonomous macro-cell for large area of detection.

An adjustment of the gain of each channel compensates the gain variation of the PMTs and allows to use only one HV cable for the 16 PMTs. In the ASIC, the 16 channels are totally independent. In each channel, the auto-trigger starts the charge and time measurements which are then converted and stored.



Only the hit channels are read out by one serialized output. The time measurement is done by a 24-bit counter at 10MHz for the coarse time and a time to amplitude converter for the fine time, giving with a resolution better than 1 ns. The charge measurement is done by a 2 gain preamplifier followed by a shaper with variable shaping times (25ns, 50ns or 100ns). Charge and fine time values are converted by a 10 bit ADC.

Contact : Gisèle Martin-Chassard

### SPIROC / EASIROC

SPIROC is a dedicated very front-end electronics for an ILC prototype of hadronic calorimeter using SiPM. This ASIC is due to equip a 10,000-channel demonstrator in 2010. It embeds cutting edge features that fulfill ILC final detector requirements. It has been realized in 0.35 $\mu$ m SiGe technology.

It has been developed to match the requirements of large dynamic range, low noise, low consumption, high precision and large number of readout channels needed. SPIROC is an auto triggered (down to 50fC), dual gain, 36-channel ASIC which allows to measure on each channel the charge from one photoelectron to 2,000 photoelectron and the time with a 1ns accurate Time-to-digital Converter (TDC). An analogue memory array with a depth of 16 for each channel is used to store the time information and the charge measurement. A 12-bit Wilkinson Analogue-to-digital Converter (ADC) has been embedded to digitize the analogue memory content (time and charge on 2 gains).

The data are then stored in a 4 Kbytes RAM. A very complex digital part has been integrated to manage all these features and to transfer the data to the DAQ. In parallel, a "spin-off" chip, EASIROC, has been developed. EASIROC, standing for Extended Analogue Si-pm Integrated ReadOut Chip is a 32 channels fully analogue front end ASIC dedicated to readout SiPM detectors.

Its versatility allows its use in many photo detector experiments and is already used for PEBS, MuRAY, J-PARC and medical imaging.

Contact : Ludovic Raux



**IN2P3**  
Les deux infinis



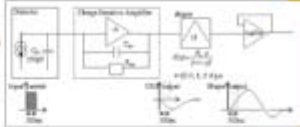
# Electronique à froid

- ❑ Evolution du circuit depuis 2007
  - ❑ Test à froid de différents blocs
  - ❑ Ajout de fonctionnalités
- ❑ Test en cours à l'IPNL sur détecteur 128 voies
  - ❑ 4 cartes de 4 circuits
  - ❑ Points délicats : filtrage des alimentations
- ❑ Perspectives 2015
  - ❑ Test au CERN sur chambre de 6x6x6 [m<sup>3</sup>]
  - ❑ Dynamique : -3fC à -1.2pC
  - ❑ Intégration 16 voies par chip

Circuit Liquid Argon Zygote IC LARZIC



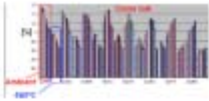
**New spécification (version 7):**

- 16-channel 3fC to 1.2pC (0.5µs pulse) CSA
- 1500e- ENC with 250pF Cdet
- Able to work in LAr vapours @ -150°C
- 6mA/channel



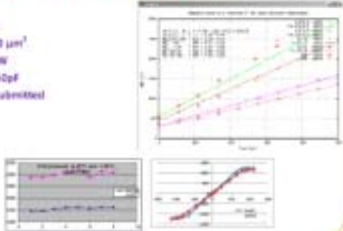
**Cold electronics (-150°C)**

**chip evolution**

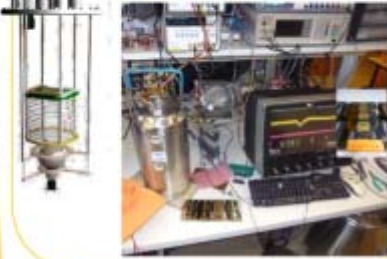
**Version 6 : LARZIC measures**

Version 6 :  
Power supply: 1.3V  
Die area: 200x300 µm<sup>2</sup>  
Consumption: 1.8mW  
ENC = 1400 e- @ 250pF  
NSS 2013 abstract submitted




**4x4x8 (128-channel) under test (2013)**

30cm drift chamber  
Labex LIO Funding for the prototype  
Test facility in Lyon (IPNL)  
Four cards of four ASIC to be tested



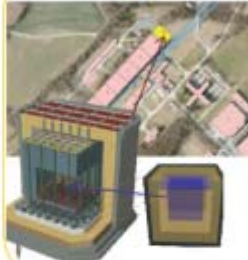
**i2c slave verified**



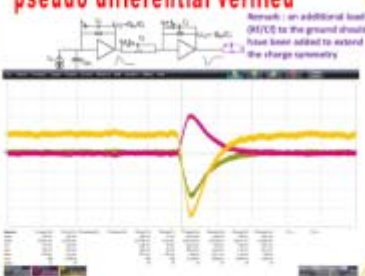
i2c slave with two 8-bit registers had been tested at ambient as well as at LN2 temperature (-200°C)

**2015 target : 8000 channels**

CERN EHM1 extension  
4x6x6 [m<sup>2</sup>] active area  
7680-channel => 480 ASIC of 16-channel each  
Input range from 3fC to 1.2pC, (only electrons input signal)



**pseudo differential verified**



Remark : an additional load (HV) to the ground should have been added to extend the charge symmetry

Contact : e.bechetoille@ipnl.in2p3.fr

Ecole de microélectronique de l'IN2P3  
Porquerolles —23/27 juin 2013




- ❑ **Projet de valorisation: circuit ALARMIC**
  - ❑ Mesure et surveillance de 3 gaz polluants sans fil
  - ❑ VFE, comparateurs et DAC très basse conso.
- ❑ **R&D: circuit TROPIC**
  - ❑ T&H et bloc numérique pour ADC 2GHz 6 bits
  - ❑ Application: filtrage optimal temps réel (TEP TOF)
- ❑ **R&D: TDC haute résolution**
  - ❑ Dédié aux chambres RPC à muons pour CMS
  - ❑ Résolution visée: 10 ps
  - ❑ Architecture basée sur la différence de périodes d'oscillation de 2 oscillateurs

Projets valorisation et R&D


**MICRHAU**

Bien que fortement impliqué dans les projets de physiques des particules de l'IN2P3 et leurs applications médicales, le pôle MicRhAu cherche à développer des partenariats avec des acteurs industriels et à explorer des pistes de R&D pour les projets futurs.

**Circuit ALARMIC: détection de gaz polluants**




**Circuit TROPIC: ADC 2GS/s 6bits, T&H en courant**



**TDC haute résolution**


Un R&D basé sur l'utilisation de chambres RPC multi-étages a été initié dans le but d'écouter les chambres à muons de CMS. La connaissance précise de l'instant de détection permet de remonter au point d'interaction. Le R&D électronique porte sur un TDC dont la résolution doit être de 10 ps avec un temps mort inférieur à 100 ps. La réflexion sur ce R&D a commencé en 2012 mais la conception et la fabrication seront réalisées en 2013.

La figure montre l'architecture du TDC ainsi que le chronogramme de la mesure de temps T. Cette architecture est basée sur la différence de périodes d'oscillation de 2 oscillateurs, elle a déjà été implémentée dans un FPGA.



Contact : royer@clermont.in2p3.fr

Ecole de microélectronique de l'IN2P3  
Porquerolles — juin 2013







IN2P3  
Les deux infinis

MICRHAU  
Pôle de microélectronique Rhône-Auvergne

# Les upgrades HL-LHC @ MicRhAu

- ❑ Trigger à muons ALICE : circuit **FEERIC**
  - ❑ Front-end analogique / Précision en temps
- ❑ Tracker CMS : circuit **PRACTIC\_32**
  - ❑ Front-end analogique multivoie
- ❑ TileCal ATLAS : circuit **FATALIC/TACTIC**
  - ❑ Front-end analogique à sortie numérique
- ❑ Tracker LHCb : circuit **PACIFIC**
  - ❑ Front-end analogique multivoie
- ❑ Tracker CMS : circuit **Concentrateur**
  - ❑ Circuit de traitement numérique
- ❑ MFT ALICE : circuit **SDS**
  - ❑ Circuit de traitement numérique

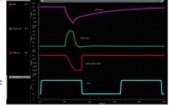
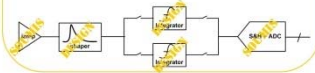
Le pôle MicRhAu est engagé sur l'ensemble des upgrades des expériences pour le HL-LHC, avec pour certaines expériences jusqu'à deux développements.

Upgrades HL-LHC

In progress

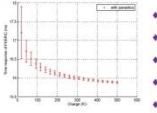
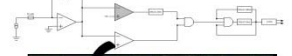

**PACIFIC : tracker LHCb**

- ◆ Chaîne de lecture complète pour SiPM
- ◆ 128 voies/circuits
- ◆ Collaboration : Barcelone, Valence, Cracovie, Pôle MicRhAu
- ◆ Consommation : 8 mW / voie
- ◆ Technologie : IBM 130 nm
- ◆ 1ère soumission version 8 voies : novembre 2013

**FEERIC : trigger à muons ALICE**

- ◆ Dynamique d'entrée :  $\pm 20$  fC à 5 pC
- ◆ Résolution en temps : 20 ps à 700 ps rms suivant la charge
- ◆ Consommation : 70 mW / voies @ 3 V
- ◆ 8 voies /circuit ► 3000 circuits pour l'ensemble
- ◆ Technologie : AMS 0.35  $\mu$ m

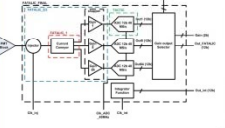
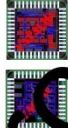
**FATALIC/TACTIC : TileCal**

**FATALIC 3 : Convoyeur de courant = Shapers**

- ◆ Dynamique d'entrée : 625 nA à 62.5 nA
- ◆ Impédance d'entrée :  $\infty$
- ◆ Shaper

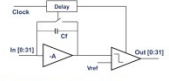
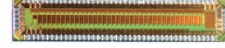
**TACTIC : ADC pipeline**

- ◆ Nombre de bit : 12
- ◆ Fréq. d'échantillonnage : 40 MHz (simu) ; 100 MHz @ 40 Mbit/s
- ◆ Consommation : 1 mW
- ◆ Technologie : IBM 180 nm

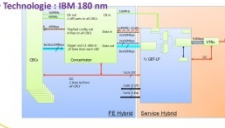
**PRACTIC\_32**

- ◆ Dynamique d'entrée : 1.2 fC à 10 fC
- ◆ Mode Electrons ou trous
- ◆ Circuit en simulation : 1200 e<sup>-</sup> et 1400 e<sup>-</sup>
- ◆ Fréq. d'horloge : 40 MHz
- ◆ Gain en conversion : 3.5 mV/fC et 8.5 mV/fC
- ◆ Alimentation : 1.2 V
- ◆ 32 voies /circuit
- ◆ Technologie : IBM 130 nm
- ◆ Dimension : 4.5 mm x 1 mm

**Concentrateur : tracker CMS**




- ◆ Dynamique d'entrée : 625 nA à 62.5 nA
- ◆ Impédance d'entrée :  $\infty$
- ◆ Shaping time : 25 ns
- ◆ Consommation : 20.4 mW
- ◆ Technologie : IBM 180 nm



**SDS : MFT ALICE**

Contact : nicolas.pillet@clermont.in2p3.fr

Ecole de microélectronique de l'IN2P3  
Porquerolles — 24/27 juin 2013

# Electronique intégrée pour applications en hadron thérapie



- ❑ Aperçu des circuits intégrés réalisés dans le cadre des problématiques de hadron thérapie
- ❑ un ASIC multivoie pour la lecture de SDD double polarité a été fondu et testé
- ❑ une deuxième version est prévue
- ❑ un ASIC multivoie mixed-signal pour l'étiquetage temporel et l'enregistrement de la position de hits provenant de fibres scintillantes a été soumis pour la fabrication en Juin 2013

Integrated electronics for hadron therapy

**Ion-range monitoring during ion therapy:**  
prompt- $\gamma$  detection using a Compton camera combined with a beam tagging device (hodoscope)

**The hodoscope provides:**

- time reference for time-of-flight measurements (signal/background discrimination): 1ns resolution
- spatial tagging of the incident ions in a beam crossing plane: 1mm resolution
- counting rate capability of  $10^7$  ion pulses/s

**Compton camera:**  
electronic collimation through the use of multiple scatter detectors and an absorber

**Classical Compton camera approach obtains the 3D information from cone intersections**  
A combined Compton camera/beam tagging device simplifies the reconstruction to the intersection cone/line

**Integrated electronics for the scatter detectors**  
detector used: double-sided SDD ( $C_d = 15$  pF)  
readout chain composed of a two-polarity CSA followed by two shapers in parallel  
slow shaper (11ns) for input charge measurements and SNR optimization  
fast shaper (15ns) for timing measurements  
two configurations are possible for P and N strips readout

**8 channels prototype realised in AMS C55 and successfully tested [3]**

**Performances summary:**  
 $10^7$  hits/s counting rate  
CSA ENC: 835 e<sup>-</sup> rms (electrons) 1186 e<sup>-</sup> rms (holes)  
CSA conversion gain (mean): 2.05 mV/IC (electrons) 1.88 mV/IC (holes)

**Upcoming**  
64 channels version with added functionalities (configurable shaping time and gain) to be submitted  
improved (switched) version of the CSA without feedback resistor for total noise reduction

**Beam tagging hodoscope**  
array of scintillating fibres coupled to multichannel PMs  
acquisition rate up to  $10^8$  events/s

**Integrated electronics for the hodoscope**  
- 32-channels ASIC (HODOPIC) based on two previous designs [4,5]

**Single channel features:**  
- 525 fC—25.2 pC input dynamic range  
- about 2 Ohm input impedance  
- readout chain composed of a current conveyor (configurable gain) followed by a current comparator and a CSA in parallel  
- a current steering bias tree settles the same reference current for all channels: 10b + 3b double-dynamic internal DAC i'C-configurable  
- time stamping feature via a divided-by-32 reference clock (internal DLL): 140 ps resolution  
- internal event FIFO memory stores tagging information  
- event-driven architecture: the triggering of one of the channel comparators latches the 32b hit-map and writes the tag into FIFO  
- channel's gain individually configurable via i'C for fibre ageing  
- any of the channels CSA could be configured to an output pad for monitoring of the injected charge  
- a 3-state 32b-wide bus allows the direct readout of the DLL internal state for debugging

8 channels readout ASIC for SDD readout: chip microphotograph

CSA single channel layout with a detail of the input transistor design

Beam tagging 2x128 scintillating fibers

[1] M.H. Richard et al, "Design guidelines for a double scattering Compton camera for prompt- $\gamma$  imaging during ion beam therapy: a Monte Carlo simulation study", IEEE Transactions on Nuclear Science, Vol 58, No.1 Feb. 2011

[2] J.Krimmer et al, "Real-time online monitoring of the ion range by means of prompt secondary radiations", ANIMMA 2013 Conference Record

[3] M.Dahoumane et al, "A low noise and high dynamic charge sensitive amplifier-shaper associated with silicon strip detector for Compton camera in hadrontherapy", IEEE Nuclear Science Symposium and Medical Imaging (NSS/MIC) Conference Record

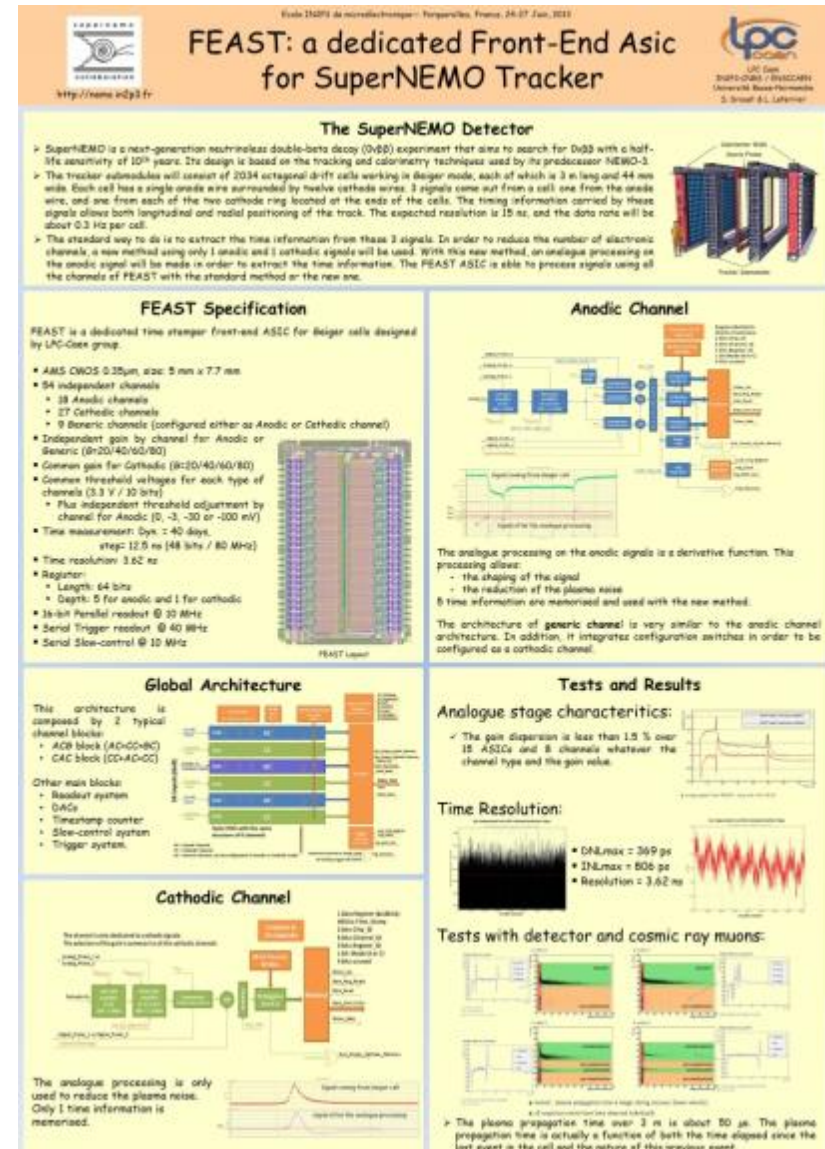
[4] S.Deng et al, "Front-end, multi-channel pmt-associated readout chip for hodoscope application", NIM A, Vol.695, No.0, 2012

Contact : caponetto@in2p3.fr

Ecole de microélectronique de l'IN2P3  
Porquerolles—23/27 Juin 2013

# FEAST: a dedicated Front-End ASIC for SuperNEMO Tracker

- **LPC Caen**
  - ✓ Service Electronique-Microélectronique  
S. Drouet / L. Leterrier (ASIC)  
F. Boumard / J. Langlois (Cartes de tests)
  - ✓ Service Instrumentation  
J. Brégeault (Logiciel d'acquisition)
  
- **SuperNEMO**
  - ✓ Physique du neutrino (Etude de la double désintégration  $\beta$  sans neutrino)
  - ✓ Démonstrateur SuperNEMO
    - Construction 2013-2014
    - $\approx 2000$  voies pour le tracker (150 ASICs)
  
- **FEAST**
  - ✓ Techno: AMS 0,35 $\mu$ m CMOS
  - ✓ ASIC pour le trajectographe
  - ✓ ASIC codeur de temps avec mise en forme analogique du signal à traiter
  - ✓ 54 voies indépendantes



**FEAST: a dedicated Front-End ASIC for SuperNEMO Tracker**

**The SuperNEMO Detector**

- SuperNEMO is a next-generation neutrinoless double-beta decay (0 $\nu\beta\beta$ ) experiment that aims to search for 0 $\nu\beta\beta$  with a half-life sensitivity of 10<sup>26</sup> years. The design is based on the tracking and calorimetry techniques used by its predecessor NEMO-3.
- The tracker submodules will consist of 2034 octagonal drift cells working in Geiger mode, each of which is 3 m long and 44 cm wide. Each cell has a single anode wire surrounded by twelve cathode wires. 3 signals come out from a cell: one from the anode wire, and one from each of the two cathode rings located at the ends of the cells. The timing information carried by these signals allows both longitudinal and radial positioning of the track. The expected resolution is 15 ns, and the data rate will be about 0.3 Hz per cell.
- The standard way to do is to extract the time information from these 3 signals. In order to reduce the number of electronic channels, a new method using only 1 anodic and 1 cathodic signals will be used. With this new method, an analogue processing on the anodic signal will be made in order to extract the time information. The FEAST ASIC is able to process signals using all the channels of FEAST with the standard method or the new one.

**FEAST Specification**

FEAST is a dedicated time stamping front-end ASIC for Geiger cells designed by LPC-Caen group.

- AMS CMOS 0.35 $\mu$ m, area: 8 mm x 7.7 mm
- 54 independent channels
  - 18 Anodic channels
  - 27 Cathodic channels
  - 9 Biometric channels (configured either as Anodic or Cathodic channel)
- Independent gain by channel for Anodic or Biometric (0/20/40/60/80)
- Common gain for Cathodic (0/20/40/60/80)
- Common threshold voltages for each type of channels (3.3 V / 30 bits)
  - Plus independent threshold adjustment by channel for Anodic (0, -3, -30 or -100 mV)
- Time measurement: 1 ns - 40 days, step: 12.5 ns (48 bits / 80 MHz)
- Time resolution: 3 nS rms
- Register:
  - Length: 64 bits
  - Depth: 5 for anodic and 1 for cathodic
- 16-bit Parallel readout @ 40 MHz
- Serial Trigger readout @ 40 MHz
- Serial Slave-control @ 10 MHz

**Anodic Channel**

The analogue processing on the anodic signal is a derivative function. This processing allows:

- The shaping of the signal
- The reduction of the plasma noise

5 time information are memorized and used with the new method.

The architecture of generic channel is very similar to the anodic channel architecture. In addition, it integrates configuration switches in order to be configured as a cathodic channel.

**Global Architecture**

This architecture is composed by 2 typical channel blocks:

- ACR block (AD-CO-BC)
- CAC block (CO-AD-OC)

Other main blocks:

- Readout system
- DACs
- Timestamp counter
- Slave-control system
- Trigger system

**Cathodic Channel**

The analogue processing is only used to reduce the plasma noise. Only 1 time information is memorized.

**Tests and Results**

**Analogue stage characteristics:**

- ✓ The gain dispersion is less than 1.5 % over 18 ASICs and 8 channels whatever the channel type and the gain value.

**Time Resolution:**

- DN<sub>rms</sub>max = 369 ps
- 2N<sub>rms</sub>max = 806 ps
- Resolution = 3.62 ns

**Tests with detector and cosmic ray muons:**

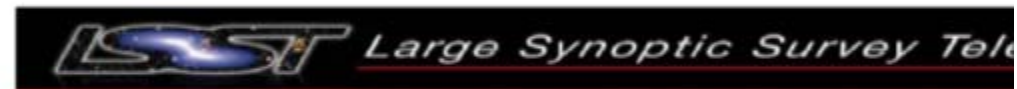
- The plasma propagation time over 3 m is about 50 ns. The plasma propagation time is actually a function of both the time elapsed since the last event in the cell and the nature of this previous event.



# ASPIC: Analog Signal Processing Integrated Circuit

LAL/LPNHE  
– LSST

Sujet/Domaine  
– Energie Noire  
– Supernovae




## ASPIC: Analog Signal Processing Integrated Circuit

Y. Tsvet<sup>1</sup>, H. Lebbolo<sup>1</sup>, M. El Berni<sup>1</sup>, A. Qureshi<sup>1</sup>, P. Antilogus<sup>1</sup>, J. Jeglot<sup>1</sup>, C. Juramy<sup>2</sup>, D. Martin<sup>3</sup>, S. Russo<sup>4</sup>

<sup>1</sup>Paris XI – CNRS / LAL    <sup>2</sup>Paris XI – CNRS / LPNHE

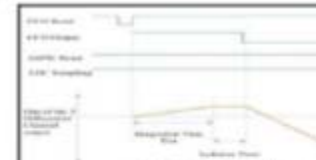
### LSST camera specifications

The 3.2 Gpixel LSST camera will be read out by means of 160 highly segmented 4k x 4k CCDs. A total of 3024 video channels will be processed by a modular, monolithic electronics package based on two custom multichannel analog ASICs now in development. Performance goals of 1 electron noise, 21% electronic crosstalk, and 40 mW total power dissipation per channel are targeted. The focal plane is organized as a set of 120 x 120 sub-modules ("rafts") with front end electronics housed in an enclosure lying within the footprint of the CCDs making up the raft. CCD surfaces within a raft are required to be coplanar to within 4 microns. The assembly of CCDs, sub-modules, electronics boards, and cooling components constitutes a self-contained and testable 144 Mpix imager ("raft tower"), and 21 identical raft towers make up the LSST science focal plane.



### Dual Slope Integration for CCD signals


The standard technique for analogue signal processing of CCDs, is "Correlated double sampling" (CDS), which removes thermal noise. The correlated double sampling is performed by integrating first the CCD and then the charge signal with opposite polarity during the same integration. The difference of these two integrations provides the CCD signal with the noise removed.



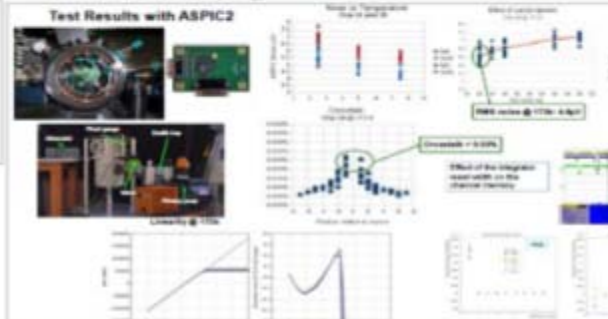
### ASPIC2

An integrated circuit, the ASPIC2, has been designed for CCD signal readout, with enhanced performances. It fulfills the preliminary requirements in post layout of the 1st LSST prototype.

#### ASPIC2 DIAGRAM



#### Test Results with ASPIC2



#### ASPIC2 Requirements

- 50kV / 1MHz or 70V rise noise (500ns integration)
- 500kHz Operation
- 0.85% Crosstalk (0.81% goal)
- 100ke<sup>-1</sup> Full Well capacity (150ke<sup>-1</sup> max)
- 0.5% linearity
- Differential outputs
- Output Drive = 50pF
- Supply 5V – 25mW/ch power dissipation
- temperature 173K.

### ASPIC3 & CABAC (Clock And Biases Asic for Ccd)

An ASIC called ASPIC3 was designed and is currently in production to fit with new CCD users. A CCD clocking & biasing integrated circuit called CABAC has also been designed.

#### ASPIC3 Updated Specs

- 50kV<sup>-1</sup> Full Well capacity
- 100MHz rise noise (500ns integration)
- 500kHz to 1MHz Operation range
- 1.4 to 0 gain range
- Operating temperature 173K(200K)
- Capacity 100k<sup>-1</sup> – 200k<sup>-1</sup> power dissipation
- Crosstalk 0.8% (0.75% goal)
- Conversion 0.1% (0.07% goal = 0.08% max)
- Differential outputs
- New integration timing
- The timing gain, increasing the gain over from 1.4 to 0.

#### CABAC Requirements

CCD Requirements	ASPIC3	CABAC
Gain	1.4 to 0	1.4 to 0
Capacity	100k <sup>-1</sup> – 200k <sup>-1</sup>	100k <sup>-1</sup> – 200k <sup>-1</sup>
Crosstalk	0.8%	0.8%
Conversion	0.1%	0.1%
Power	100mW	100mW
Temperature	173K	173K

#### CABAC Requirements

- CCD and Biases
- 0.5% Crosstalk
- 100k<sup>-1</sup> Full Well Capacity
- 100kHz to 1MHz Operation range
- 1.4 to 0 gain range
- 100k<sup>-1</sup> – 200k<sup>-1</sup> power dissipation
- Conversion 0.1% (0.07% goal = 0.08% max)
- Differential outputs
- New integration timing
- The timing gain, increasing the gain over from 1.4 to 0.

#### ASPIC3 New functionalities:

- Backdoor: Connection to all channels connects to ASPIC3. It allows to recover the 100MHz resolution of the existing line of ASPIC3 on CABAC in off-chip.
- Temperature Probe: Temperature Probe that reads the gain to probe of the first gain stage output or the second gain stage for CCD readout.
- Temperature Probe: Ties to the line to CABAC, allows us to monitor the temperature inside the ASPIC3.
- Substrate Clamping: By implementing a higher VDD gate at the entry of each channel, it is now simple to deactivate each channel in case of failure of the CCDs.
- Backdoor Programming: Provides flexibility and protection for startup configurations.

#### Test Results



ASPIC3 & CABAC  
A complete CCD (Clocking+Readout) system will be available in later 2014.



# IMOTEP pour IMagerie TEP

- IPHC - Groupe IMABIO
  - Plateforme AMISSA
- Sujet/Domaine
  - Circuit pour PM multivoies
    - Mesure d'énergie corrélée en temps
    - Dynamique d'entrée:  $2 \cdot 10^3$  à 1%
    - Dynamique  $10 \mu\text{s}$ , résolution 625 ps
- Interlocuteur
  - Xiaochao FANG

**Chaîne de lecture pour l'imagerie médicale : micro-tomographe à émission de positrons ( $\mu\text{TEP}$ )**

X. FANG, R. SEFRI, C. HU-GUO, C. COLLEDANI  
Institut Pluridisciplinaire Hubert Curie, 23 rue du Loess, 67037 Strasbourg

**Introduction**

Dans le cadre des développements de plateformes pour l'imagerie de précision et en particulier la nouvelle imagerie TEP, une exigence de performances de l'instrument de détection est toujours élevée par les chercheurs. Sous la forme de lecture et de traitement de données distribuées, il s'agit de créer une chaîne de lecture et de traitement des données hautement performante.

Le descripteur fondamental de cette chaîne est le circuit IMOTEP. Ce circuit permet de convertir des données numériques en temps de vol et de les traiter. Le circuit est capable de convertir une donnée numérique de 16 bits en temps de vol et de la convertir en temps de vol. Le circuit est capable de convertir une donnée numérique de 16 bits en temps de vol et de la convertir en temps de vol.

**AMISSA - A Multi-Channel Analog-to-Digital Converter**

**TEP: Principe général et flux**

**Circuit IMOTEP**

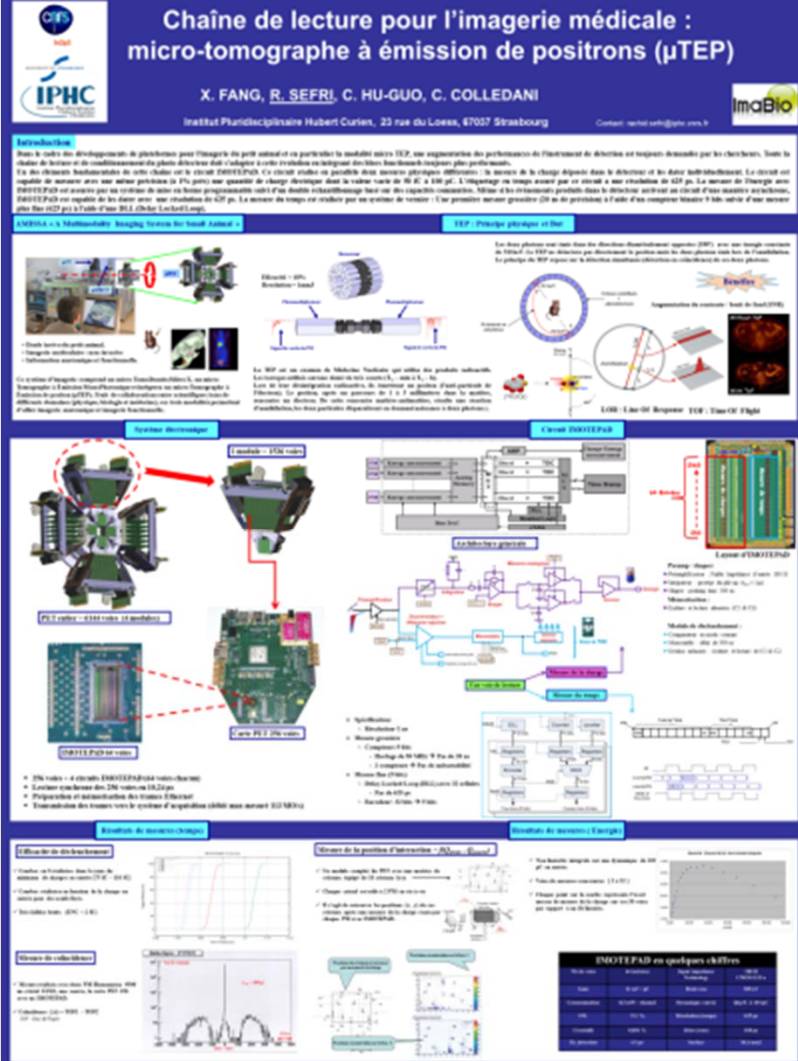
**Architecture globale**

**Flux de données**

**Caractéristiques**

**Conclusion**

**IMOTEP en quelques chiffres**




Paramètre	Valeur
Nombre de canaux	16
Temps de vol (ns)	100
Précision de mesure (ps)	625
Temps de lecture (ns)	10
Temps de traitement (ns)	10
Temps de conversion (ns)	10
Temps de lecture (ns)	10
Temps de traitement (ns)	10
Temps de conversion (ns)	10

# AROM

## Accelerated Read Out Mimosa

- IPHC - Groupe PICSEL
  - Upgrade ITS ALICE
- Sujet/Domaine
  - Pixels à discriminateur embarqué
    - Faible consommation
    - Grande vitesse de lecture
  - Etude de 3 architectures

- Interlocuteur
  - Hung PHAM



**A CMOS Pixel Sensor with In-Pixel Discrimination for ALICE-ITS Upgrade**  
Tianyang Wang, Pham Thanh Hung, Andrei Dorokhov, Christine Hu-Guo, Yann Hu  
Institut Pluridisciplinaire Hubert Curien

**ABSTRACT**

A new concept of CMOS Pixel Sensor (CPS) featuring in-pixel discrimination has been prototyped in a 0.18 μm CMOS Image Sensor (IS) process aiming to meet the requirements of ALICE-ITS upgrade. Each pixel consists of a sensing diode, a pre-amplifier and a discriminator within a pitch of 22x35 μm<sup>2</sup>, with direct binary output. It offers faster readout speed, lower power consumption and less inactive surface comparing to the column level discrimination. Three versions of discriminators have been implemented in their respective matrices to seek for the best compromise between performance and circuit implementation.

**INTRODUCTION**

The 0.18 μm OS process has been validated to be adequate for ALICE-ITS upgrade in respect of radiation hardness [1]. By utilizing this technology, two designs were prototyped driven by the specification of ALICE-ITS upgrade:

The first design inherits the architecture of column level discrimination from the ULTIMATE (MIMOSA 28) sensor [2] but using double row readout by implementing 2 discriminators per column.

The work focus on the second design whereas a discriminator is integrated inside each pixel. With pixel level discrimination, the analog signal is only used within the pixel and the analog buffer driving the column line is no longer needed. Thus, the static current consumption per pixel is largely reduced and also the readout time per row can be halved down to 100ns.

In the following part, the design of a prototype chip called AROM is going to validate the concept of in-pixel discrimination will be described.

**CIRCUIT IMPLEMENTATION**

**> Pixel**

The pixel includes two parts. The first part consists of the sensing diode and the pre-amplifier. The second part is the high precision discriminator with CDS. The pixel is fitted into an area of 22x35 μm<sup>2</sup>.

**1. Sensing and pre-amplification**

- Self-biased with feedback loop
- Validated performance in previous chips
- Noise floor ~23σ = ~1mV at the output

**2. Discriminator**

- Limitations
  - Inactive area available inside pixel
  - Close link between digital control signals and sensitive analog nodes
  - Simple circuitry is preferable
- Circuit design
  - Two amplifying stages = dynamic latch
  - Three different versions are implemented
  - Trade off between circuit implementation and performance
  - Same being used for the three versions
- Working principle
  - "Set"
    - Reset the amplifiers or discrimination line output
    - "read"
      - Apply the threshold voltage
      - Threshold voltage = V<sub>th</sub> - V<sub>th0</sub>
    - "latch"
      - Reset the latch on the read
      - Take decision on high level
    - "Set 0"
      - Read out the discriminated data

**> Routing of control lines**

- Sequencer placed at the bottom of the matrix
- No dead area is between when multiple chips are aligned side by side through chip stacking
- Cross like routing line
  - Generated vertically
  - Shared horizontally

**> Pixel layout**

- Elongated pixel with staggered diodes
- The red arrow indicates the control lines
- The double row readout employs the schematic of 2<sup>nd</sup> version of pixel

**> Organization of one matrix in AROM**

- Matrix read out in rolling shutter mode
- 8 digital outputs transmit 32 bits in 100ns through time multiplexing
- 4 analog outputs for sensing diode and pre-amplifier calibration (The signal is driven by an analog buffer)

**CHIP ORGANIZATION**

- Six matrices are implemented which can be selected individually
- Both single row readout (matrix of 32x32 pixels) and double row readout (matrix of 16x16 pixels) are attempted
- Separate matrices for testing the latch

**CONCLUSION**

- The chip AROM including row different versions of in-pixel discrimination has been submitted in April 2013 for exploring the new concept of binary pixel.
- According to simulation results, compared to column level, the new pixel can achieve:
  - ✓ 3 times less power consumption
  - ✓ 2 times less readout time(100ns/row)
  - ✓ Equivalent Fix Pattern Noise (~30σ/V)
- Test is planning in July
- Current consumption can be further reduced down to 10μA/pixel
- New chip AROM1 integrating 4 double row readout matrix of 64x64 pixels with internal bias and reference voltages programmed via JTAG will be submitted in August 2013

**REFERENCE**

[1] S. Senoussi et al., Charged particle detector performance of CMOS pixel sensors produced in a 0.18 μm process with a high-responsivity balanced base current IBS-2013. ...  
 [2] J. Vahlo et al. A vertex size CMOS pixel sensor dedicated to the STAR10T. 2013. arXiv:1307.7227v2  
 [3] J. Raab et al. First Test Results of MIMOSA 28, a First CMOS Sensor With Integrated Data Compression and Digital Output. 2009. IEEE Nuclear Science Symposium Conference Record.

# MIMOSA32 N1 & N2

## Etude du bruit "Random Telegraph Signal"

- IPHC - Groupe PICSEL  
– Upgrade ITS ALICE

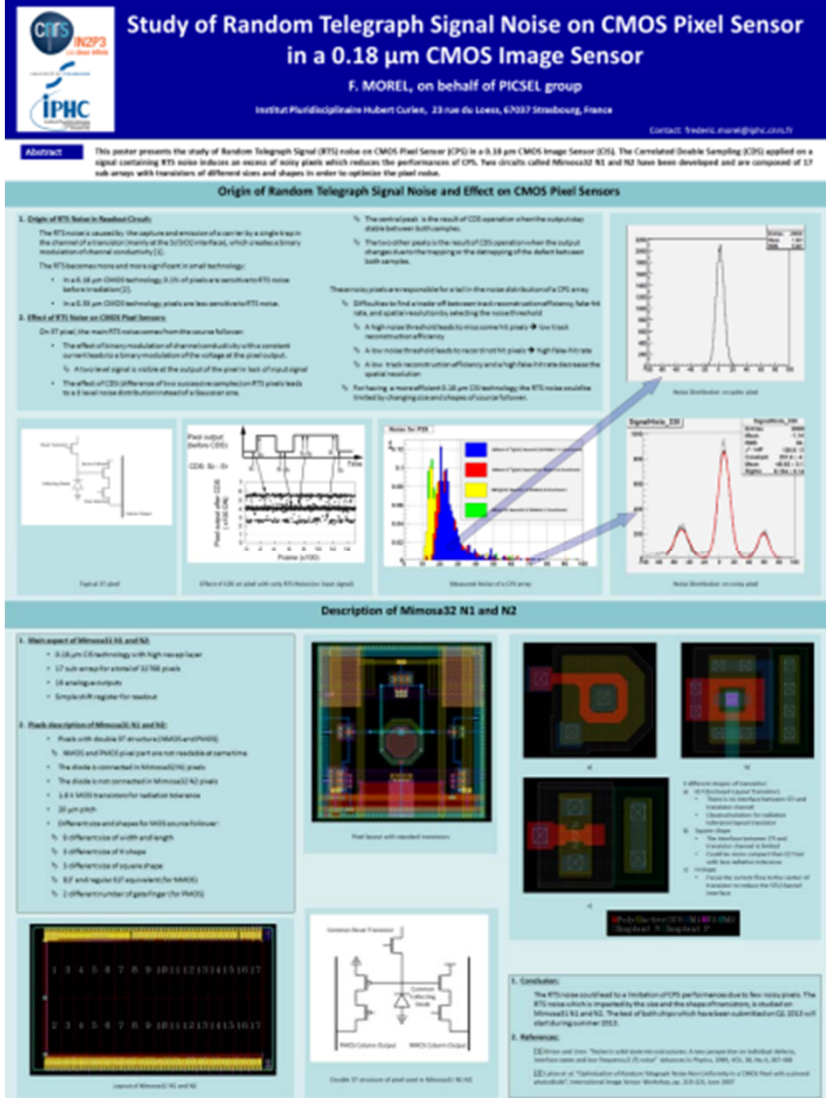
- **Sujet/Domaine**

- Optimisation des pixels

- SF pour lecture de la chaîne
- Etude en fonction de la taille et la géométrie du SF

- **Interlocuteur**

- Frédéric MOREL



**Study of Random Telegraph Signal Noise on CMOS Pixel Sensor in a 0.18  $\mu\text{m}$  CMOS Image Sensor**  
F. MOREL, on behalf of PICSEL group  
Institut Pluridisciplinaire Hubert Curie, 23 rue du Loess, 67037 Strasbourg, France  
Contact: frederic.morel@iphc.cnrs.fr

**Abstract:** This poster presents the study of Random Telegraph Signal (RTS) noise on CMOS Pixel Sensor (PS) in a 0.18  $\mu\text{m}$  CMOS Image Sensor (CIS). The Correlated Double Sampling (CDS) applied on a signal containing RTS noise induces an excess of noisy pixels which reduces the performances of CIS. Two circuits called Mimosas32 N1 and N2 have been developed and are composed of 37 sub-arrays with transistors of different sizes and shapes in order to optimize the pixel noise.

**Origin of Random Telegraph Signal Noise and Effect on CMOS Pixel Sensors**

**1. Origin of RTS Noise in Standard Circuits**  
The RTS noise is caused by the capture and emission of a carrier by a single trap in the channel of a transistor (mainly of the SOT/CC/FETs), which induces a binary modulation of thermal conductivity [1].  
The RTS becomes more and more significant in small technology:  
• In a 0.18  $\mu\text{m}$  CMOS technology, 3.5% of pixels are sensitive to RTS noise before readout [2].  
• In a 0.09  $\mu\text{m}$  CMOS technology pixels are less sensitive to RTS noise.

**2. Effect of RTS Noise on CMOS Pixel Sensors**  
On 37 pixel, the mean RTS noise comes from the source follower:  
• The effect of the modulation of thermal conductivity with a constant capacitance leads to a modulation of the voltage of the pixel output.  
• A thermal signal is visible at the output of the pixel (see output signal).  
• The effect of CDS (difference of two successive samples) on RTS pixels leads to a 3 level noise distribution instead of a Gaussian one.

The central peak is the result of CDS operation when the subpixel traps behave synchronously.  
The other peaks are the result of CDS operation when the output changes due to the trapping or the detraping of the defect between both samples.  
The noisy pixels are responsible for a tail in the noise distribution of a CIS array.  
• Difficulties to find a trade off between read-out efficiency, gate hit rate, and spatial resolution, selecting the noise threshold.  
• A high noise threshold leads to more correct hits but low read-out efficiency.  
• A low noise threshold leads to more correct hits but high hit rate.  
• A low read-out efficiency and high hit rate can decrease the spatial resolution.  
• For having a more efficient 0.18  $\mu\text{m}$  CIS technology the RTS noise could be limited by changing size and shapes of source follower.

**Description of Mimosas32 N1 and N2**

**1. Main aspect of Mimosas32 N1 and N2**  
• 0.18  $\mu\text{m}$  CIS technology with high read-out rate  
• 37 sub-arrays for a total of 3700 pixels  
• 18 analog outputs  
• Simple 40 registers for readout

**2. Pixel description of Mimosas32 N1 and N2**  
• Pixels with double 3T architecture (3T40 and 3T40S)  
• M40S and 3T40S pixel part are not readable at same time  
• The diode is connected to Mimosas32 N1 pixels  
• The diode is not connected to Mimosas32 N2 pixels  
• 3.8  $\times$  M40S transistors for readout balance  
• 30  $\mu\text{m}$  pitch  
• Different size and shapes for M40S source follower:  
• 3 differences of width and length  
• 3 differences of substrate  
• 3 differences of source shape  
• 8T and register 8T equivalents for M40S  
• 3 differences number of gates for the M40S

**3. Conclusion:**  
The RTS noise could lead to a limitation of CIS performances due to noisy pixels. The RTS noise which is impacting the size and the shapes of transistors, is studied on Mimosas32 N1 and N2. The test of both chips which have been submitted to CDS will start during summer 2013.

**4. References:**  
[1] Wilson and Chen, "Random telegraph noise in semiconductors: A new approach on individual defects, fluctuations and the frequency of capture", *Microelectronics Letters*, 2006, vol. 36, no. 6, pp. 547-549.  
[2] J. P. P. "The random telegraph signal: From the underlying physics to a CMOS pixel with correlated readout", *International Image Sensor Workshop*, pp. 3-9, 2011, June 2011.



# Réticule ITS1

## 180 nm Engineering Run

- IPHC - Groupe PICSEL
  - Upgrade ITS ALICE

- **Sujet/Domaine**

- Engineering Run / MPW
- Automatisation des procédures d'assemblage de 26 circuits

- **Interlocuteur**

- Grégory BERTOLONE

**An Engineering Run in a 0.18µm CMOS Imaging Sensor (CIS) process for the ALICE ITS Upgrade**  
 G. BERTOLONE, C. COLLEDANI, F. MOREL  
 Institut Pluridisciplinaire Hubert Curie, 23 rue du Loess, 67037 Strasbourg, France  
 Contact: gregory.bertolone@iphc.cnrs.fr

**Abstract**  
 An engineering run in a 0.18 µm CMOS Imaging Sensor (CIS) process, organized by CERN and IPHC, was submitted in Spring 2013. In a reticule size of 23.5x31 mm<sup>2</sup>, 26 circuits were implemented. They were mainly designed by CERN, RAL, and IPHC/IRFU. The reticule integration and optimization were performed at IPHC for a non-sacrificial dicing. The total surface of the circuits and the scribe lines represents 99.7 % of the reticule area. This paper introduces the assembly method used for the submission and presents some of the circuits designed by the IPHC/IRFU collaboration.

### Reticule Integration and Optimization process

- 1. Preparation of the Floor Planning**  
 Each laboratory submitted to IPHC a list of chips and an estimation of each die size. With these Black Boxes, IPHC elaborated the reticule Floor Planning (FP) in order to:
  - Respect the foundry reticule specifications and the dicing company constraints
  - Minimize the unused area
 IPHC also prepared the Cutting Plan (CP) as as the dicing is non-sacrificial. The dicing will be done in 3 cutting steps. After each cutting, several chips will be picked up from the reticule.
- 2. Reticule assembling procedure:**  
 When chips were ready, designers sent their gds and DRG waver files to IPHC. Then:
  - A standard verification protocol was applied on each gds:
    - ✓ Checking of duplicated cells name and PFD errors or warnings
    - ✓ Insertion of a dedicated prefix for all cells of the same chip (for eg: \_S2\_ for S2\_sensors)
  - Checking the compatibility between the layers in the gds and the process options. Each gds was automatically inserted in the reticule at its predefined position. The final gds creation process was performed with dedicated tool scripts (created by IPHC) and CalibreDRV tool (~15 min for 26 chips, 1 GB of data) in place of a classical stream-in-out flow.
  - An automatic Biting between each chips was done via Calibre script
  - A Calibre DRG was performed on the whole reticule (~930 for a multi-machine DRG run). The DRG errors were sorted and analyzed according to the individual waver files provided by the designers.
- 3. Submission**  
 IPHC and CERN managed the reticule waver form and all the administrative foundry documentation for the tape-out.

City	Total Area (mm <sup>2</sup> )	Area Ratio %
IPHC/IRFU	16	20%
CERN	7	20%
<b>TOTAL</b>	<b>23</b>	<b>40%</b>

	Area (mm <sup>2</sup> )	Ratio
Reticule Area	686.80	100
Chips Area	646.80	97
Scribe Area	17.86	2.7
Unused Area	664.37	98.7
Unused Area	2.13	0.3

**Legend:**  
■ CERN  
■ IN2P3/IRFU  
■ RAL

**Techniques and Tools**

- 0.18µm CIS process with 8 Layers Metals and 1 Poly
- Cadence PDK Flow (Virtuoso IC 6.1.5 and Encounter) + DRG/DRV tools for Calibre / PVS
- Final gds ~ 1 GB
- Submitted: April 2013
- Delivery: June 2013
- 26 wavers produced with 7 different values of EP1 reactivity



23.5 mm

31 mm

- **M02A32 (IPHC)**: In-pixel discrimination
  - Comparing 3 types of digital pixels
- **M02A32 (IPHC)**: In-pixel ADC
  - Comparing 3 types of different (ramp, SAR) in-pixel 3-bits ADCs
- **M02A32-THRA (IPHC/IRFU)**: Single Row Read Out
  - Validating the architecture of a full chain from charge collection to signal discrimination (implementation of STAR-PXL chip)
  - 136 col of 300 pixels (22 \* 33 µm) & 128 discriminators
- **M02A32-THRB1 (IPHC/IRFU)**: 2 Rows Read Out
  - Validating a double-row readout approach
  - An Architecture derived from M02A32-THRA but with double-row rolling shutter read-out mode and the row sequencer placed at the bottom of the matrix
  - 84 columns of 128 pixels & 112 discriminators
  - 2 chips with same footprint, but different pixel pitch for the matrix:
    - 22\*33 µm for M02A32THRB1 (from IPHC)
    - 22\*32 µm for M02A32THRB2 (from IRFU)
- **M02A32-FEE1 (IPHC)**: In-pixel amplification & CD0
  - Optimizing the signal over noise ratio (SNR) in-pixel circuitry
- **M02A32-N (IPHC)**: In-pixel noise investigation
  - Identifying and studying the noise sources (mainly RTS like)
  - 2 chips: 1 with sensing nodes, 1 without sensing nodes
- **M02A32 (IPHC)**: Charge collection optimization
  - Understanding the influence of the sensing node parameter on charge collection and optimizing SNR for various pixel dimensions (pixel & suber layers)
- **M02A32 (IPHC)**: Signalification Circuitry
  - Validating the data compression architecture with 1D input
  - 2D translation of STAR-PXL, signalification circuitry

1 See other IPHC content for more explanation about these chips

# MIMOSA 34 & CERNWIET

## Nouveaux procédés de fabrication

### Monolithique & Hybride

- IPHC - Groupe PICSEL

- R&D avancée

- Sujet/Domaine

- CMOS sur substrats HRES
- Capteurs/Flex ultraminesces

- Interlocuteur

- Wojciech DULINSKI

**New fabrication and packaging technologies for CMOS pixel sensors: closing gap between hybrid and monolithic approach**

Wojciech Dulinski, on behalf of PICSEL team  
Institut Pluridisciplinaire Hubert Curien, 23 rue du Loess, 67037 Strasbourg, France  
Contact: wojciech.dulinski@iphc.cnrs.fr

Monolithic CMOS Pixels (MAPS) integrate on the same silicon substrate the radiation sensor element with the processing electronics. Their fabrication is possible through easy access to commercial high-volume foundries, resulting in low costs and high yield. However in the standard implementation these devices suffer from two major limitations. First, only NMO5 transistors are allowed on top of the active area. Second, even high-resistivity substrate cannot be fully depleted because of voltage limitation of CMOS transistors. In order to overcome both limitations, we propose new CMOS fabrication procedures recently available for low-volume users.


Existing technologies for fully depleted MAPS fabrication: **smart use of standard Image Sensors CMOS or dedicated process**

**TOWER Jazz CMOS Image Sensors: Quadruple Well Process**

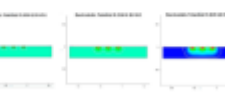
How to improve MAPS radiation hardness (particularly in case of larger pitch) or provide thicker detector layer (X-rays imaging application)?

**More depletion, by applying negative voltage to the substrate! But, if you want to keep small size of collecting Wells in order to minimize parasitic capacity (!), there is no straightforward solution...**

*(different approach than proposed by Tom Pook)*



Novel solution, based on AC-coupled diode (MIM cap)



Prototype PEGASUS sensor just arrived and ready for tests!  
Fabricated on variety of wafers: epi 40 μm/2kΩ cm, bulk > 500 Ω cm...

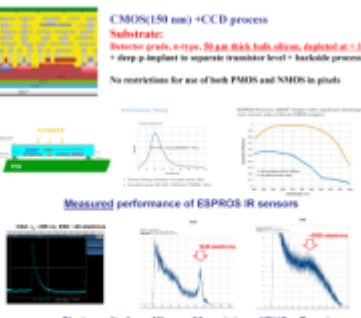
**ESPROS Photonics Corporation (EPC), Switzerland: example of "fabless" CMOS foundry**

Principle: process developed and owned by company at TCAD level, available for external users as a standard MPW or engineering run. Fabrication is subcontracted at real silicon foundry, post processing (if needed) included. All transparent to users, for a highly specialized structures and comparable costs...

CMOS(150 nm) +CCD process

Substrate: Intrinsic grade, n-type, 20 μm thick bulk silicon, depleted at 0 V, + deep p-implant in separate transfer level + backside passivation

No restrictions for use of both PMOS and NMOS in pitch

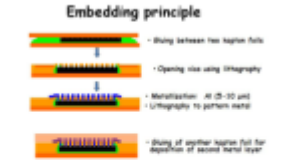


Measured performance of ESPROS IR sensors

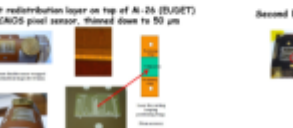
First results from Mimosas21 prototype IPHC - Bern...

Total thickness of monolithic CMOS sensors can be very small: typically 15 μm for active silicon and 8 μm for interconnections (several metal-insulator layers). Therefore MAPS can be thinned down to less than 50 μm, without losing their tracking performance. This allows very small material budget and construction of non-planar (cylindrical) detector layers: this silicon is quite flexible. In order to demonstrate feasibility of large area, ultra-light (< 5 % radiation length) sensor readers we develop novel packaging method. Thinned sensors (<50 microns) are embedded in polymer (kapton) film, electrical connection pads are implemented by metal deposition and metal lithography (no wire bonding).

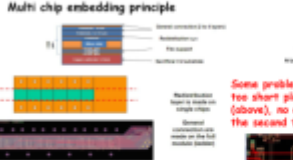
**Embedding principle**




First redistribution layer on top of Al-26 (EURET) CMOS pixel sensor, thinned down to 50 μm



**Multi chip embedding principle**



Some problems in the first iteration: too short plasma etching of glass layer (above), no electrical contacts... But the second try works: see results!



Lithographic details of interconnecting metal lines between 40 μm thick Al deposited on top of the pixel sensor

"Shadows" of metal deposited by glow discharge in visible light

Micro-photography of metal deposited by glow discharge using 10 kV X-ray PMMA

# MIMADC

## ADC 3 bits intégrés au pixel

- IPHC - Groupe PICSEL  
- R&D avancée
- Sujet/Domaine
  - Pixels à discriminateur embarqué
    - Faible consommation
    - Grande vitesse de lecture
  - Etude de 3 architectures

- Interlocuteur
  - Yang ZHOU

**A CMOS Pixel Sensor with 3-bit Pixel-Level ADCs for ILD Vertex Detector**  
W. Zhao, Ch. Hu-Guo, Y. Hu  
Institut Pluridisciplinaire Hubert Curien, 23 rue du Loess, 67037 Strasbourg, France

**Abstract:** CMOS pixel sensors (CPS) are foreseen to equip the ILD vertex detector where the priority is given to granularity, material budget, readout speed and power consumption. We report on a design of a CPS prototype integrated with 3-bit pixel-level ADCs (Analog-to-Digital Converters) for the outer layers of the vertex detector. The in-pixel functionalities include a particle sensing diode with amplification, a sample-and-hold, and an ADC. This architecture implemented in 180-nm CMOS allows to achieve a high spatial resolution with low power dissipation. A prototype chip, MIMADC, has been designed to evaluate the conception of CPS integrated with pixel-level ADCs.

**MIMADC**

- MIMADC prototype contains three millions of pixels with different ADC structures, one with SAR (Successive Approximation Register) ADC, and other two with 3-bit Pixel-Level ADCs.
- In-pixel processing functionalities including a particle sensing diode with amplification, a sample-and-hold, and an analog-to-digital converter are implemented within a 180-nm pixel.
- All modules are read out in one by one using column-parallel structure.
- The digitized results are sent to the readout system via a 2.5-Gbps driver.
- MIMADC is implemented in 180-nm CMOS process through TSMC process. The additional 3-bit pixel-level ADCs are used to evaluate the feasibility of the in-pixel ADCs.
- 3-bit Pixel-Level ADCs are implemented in 180-nm CMOS process through TSMC process. The additional 3-bit pixel-level ADCs are used to evaluate the feasibility of the in-pixel ADCs.

**3-bit Pixel-Level SAR ADC**

- Device Architecture
  - A 180-nm pixel matrix with 3-bit pixel-level SAR ADCs.
  - Each pixel consists of a 180-nm pixel-level SAR ADC, a pre-amplifier, and a 3-bit SAR ADC.
  - On-chip digital logic is implemented at the bottom of the matrix.
  - On-chip digital logic is implemented at the bottom of the matrix.
  - On-chip digital logic is implemented at the bottom of the matrix.
- Pixel Circuits
  - The pre-amplifier consists of a differential pair of PMOS transistors. The gain is controlled by the bias current of the PMOS transistors.
  - The SAR ADC is implemented with a 3-bit SAR ADC.
  - The SAR ADC is implemented with a 3-bit SAR ADC.
  - The SAR ADC is implemented with a 3-bit SAR ADC.
- Reference Circuits
  - The SAR ADC is implemented with a 3-bit SAR ADC.
  - The SAR ADC is implemented with a 3-bit SAR ADC.
  - The SAR ADC is implemented with a 3-bit SAR ADC.

**3-bit Pixel-Level SS ADC**

- Device Architecture
  - A 180-nm pixel matrix with 3-bit pixel-level SS ADCs.
  - Each pixel consists of a 180-nm pixel-level SS ADC, a pre-amplifier, and a 3-bit SS ADC.
  - On-chip digital logic is implemented at the bottom of the matrix.
  - On-chip digital logic is implemented at the bottom of the matrix.
  - On-chip digital logic is implemented at the bottom of the matrix.
- Pixel Circuits
  - The pre-amplifier consists of a differential pair of PMOS transistors. The gain is controlled by the bias current of the PMOS transistors.
  - The SS ADC is implemented with a 3-bit SS ADC.
  - The SS ADC is implemented with a 3-bit SS ADC.
  - The SS ADC is implemented with a 3-bit SS ADC.
- Reference Circuits
  - The SS ADC is implemented with a 3-bit SS ADC.
  - The SS ADC is implemented with a 3-bit SS ADC.
  - The SS ADC is implemented with a 3-bit SS ADC.

**SS ADC with in-pixel Memory**

- Device Architecture
  - A 180-nm pixel matrix with 3-bit pixel-level SS ADCs.
  - Each pixel consists of a 180-nm pixel-level SS ADC, a pre-amplifier, and a 3-bit SS ADC.
  - On-chip digital logic is implemented at the bottom of the matrix.
  - On-chip digital logic is implemented at the bottom of the matrix.
  - On-chip digital logic is implemented at the bottom of the matrix.
- Pixel Circuits
  - The pre-amplifier consists of a differential pair of PMOS transistors. The gain is controlled by the bias current of the PMOS transistors.
  - The SS ADC is implemented with a 3-bit SS ADC.
  - The SS ADC is implemented with a 3-bit SS ADC.
  - The SS ADC is implemented with a 3-bit SS ADC.
- Reference Circuits
  - The SS ADC is implemented with a 3-bit SS ADC.
  - The SS ADC is implemented with a 3-bit SS ADC.
  - The SS ADC is implemented with a 3-bit SS ADC.

**Simulation Results & Conclusion**

Metric	SAR ADC	SS ADC with in-pixel memory	SS ADC with in-pixel memory
Technology	180-nm CMOS	180-nm CMOS	180-nm CMOS
Area Size	180 μm	180 μm	180 μm
Conversion Time	180 ns	180 ns	180 ns
Power	180 μW	180 μW	180 μW
ADC Type	SAR ADC	SS ADC	SS ADC
Column Circuits	SAR Logic	Memory	Memory
Peripheral	2.5-Gbps Driver	2.5-Gbps Driver	2.5-Gbps Driver

The final prototype, called MIMADC, which features of 180-nm pixel-level ADCs integrated with pre-amplifier and sample-and-hold, has been implemented in 180-nm CMOS process. The MIMADC prototype contains three millions of pixels with different ADC structures: SAR ADC, SS ADC, and SS ADC with in-pixel memory. The in-pixel ADCs are used to evaluate the feasibility of the in-pixel ADCs. The preliminary fabrication experimental results are expected to be achieved in the future.

## COunter for Monitoring the Energy and Type of charged particles in High flux

- IPHC - Groupe PICSEL
  - Space Radiation Monitoring

- Sujet/Domaine
  - Dosimetry
  - High flux environment

- Interlocuteur
  - Yang ZHOU

**Development of a CMOS Pixel Sensor for Space Radiation Monitor**  
 Y. Zhou, J. Baudot, C. Duverger, Ch. Hu-Guo, Y. Hu and M. Winter  
 Institut Pluridisciplinaire Hubert Curie, Université de Strasbourg, 67037 Strasbourg, France  
 Contact: yang.zhou@iphc.cnrs.fr

**ABSTRACT**  
 With the purpose of monitoring simultaneously the proton and electron environment using a single sensitive device, we propose a CMOS pixel sensor featuring a 50  $\mu\text{m}^2$  sensitive area, counting capability up to  $10^6 \text{ cm}^{-2} \text{ s}^{-1}$  and with a minimal error due to pile-up of two close particles impacts on the sensor. The proposed architecture includes a 64x64 square pixel matrix with 50  $\mu\text{m}$  pitch size, an on-chip level 2-bit ADC to provide an appropriate energy resolution, and an embedded digital logic that already calculates the particle properties from the hit information provided by the pixels. To validate experimentally the proposed performance, a first prototype has been designed and fabricated in a 0.55  $\mu\text{m}$  process without the integrated digital processing part in the year 2012. The device simulation and design architecture are presented.

**INTRODUCTION**  
 The need for light, miniaturized and virtually real-time radiation monitors has become a general trend for space-related applications. CMOS Pixel Sensors (CPS), being insensitive to soft electronic systems, match these requirements well and offer additional advantages including low power, low weight, low fabrication cost and scalability to volume.

Previous works by the PICSEL group at IPHC demonstrated that CPS have excellent performance for charged particle tracking in high energy physics. In this context, the pixelated sensor generally provides spatial resolution with the counting signal stacks typically over one or two orders of magnitude. For space radiation monitoring, we propose to exploit the granularity in order to separate and count many particle impacts in a single frame as well as to estimate the energy deposited over a wide-dynamic range.

**Design study and performance simulation**

- Space radiation environment on Medium Earth orbit (MEO) sensors
  - Radiation:  $100 \text{ pSv} \cdot \text{h}^{-1}$  ( $10^6 \text{ cm}^{-2} \text{ s}^{-1}$  particles  $\text{cm}^{-2}$ )
  - Protons:  $100 \text{ keV} \sim 400 \text{ MeV}$ ;  $10^7 \sim 10^8$  particles  $\text{cm}^{-2} \text{ s}^{-1}$
  - Energy range up to 400 MeV
  - Sensor frame size up to  $1 \text{ cm}^2$
- Main sensor design features choice:
  - Sensitive area =  $50 \mu\text{m}^2$
  - Pitch =  $50 \mu\text{m}$ , 64x64 pixels in total
  - Operation speed = 20  $\mu\text{s}$  per frame

**Four main simulation for the complete response of the proposed CPS**

- Count of Energy deposited in sensitive area (Medium Earth simulation)
  - CPS model producing pixel signal
  - Parameterization of the sensor test results performed with the MIMOS CPS sensor
  - Range of measured signal in each pixel:  $300 \text{ pC} \sim 10 \text{ nC}$
- Optimization of pixel signal over 3 bits
  - 1.5k  $\text{MeV} \cdot \text{cm}^{-2}$
  - Range:  $200 \text{ pC} \sim 10 \text{ nC}$
- Data processing algorithm: timing of readout
  - Channelization
  - Sensi ADC counts in each channel
  - Sensi ADC counts in each channel
  - Sensi ADC counts in each channel
  - Sensi ADC counts in each channel

**Estimated performances**

- The estimated sensor performance with respect to the dose and particle flux measurement under the following conditions:
  - Each frame contains a number of particles uniformly distributed between 1 and 20.
  - There is a 20/70 mix of electrons and protons, with uniform energy distribution between 1 and 400 MeV.
  - Particles are detected normally incident on the pixel test bed.

**COMETH: 2 sensors for Monitor the Energy and Type of charged particles in High flux**

- This project is funded by COMETH
- $64 \times 64$  pixel CMOS technology
- $50 \times 50 \mu\text{m}^2$  sensitive area
- $10^6 \text{ cm}^{-2} \text{ s}^{-1}$  counting rate
- 12-bit on-chip 2-bit ADC
- 64x64 square pixels (pitch =  $50 \mu\text{m}$ )
- 200  $\mu\text{m}$  to 400  $\mu\text{m}$  energy range
- $10^7 \sim 10^8$  particles  $\text{cm}^{-2} \text{ s}^{-1}$  counting rate
- 1.5k  $\text{MeV} \cdot \text{cm}^{-2}$  energy range
- 1.5k  $\text{MeV} \cdot \text{cm}^{-2}$  energy range

**Architecture**

- A multi-stage block is used as charge sensing element
- The active area is divided into 4 sub-pixels to improve the signal-to-noise ratio
- The 12-bit ADC is implemented in a 0.55  $\mu\text{m}$  CMOS technology
- A double sampling circuit is used up to a Conversion Time (CT) of 100 ns
- A double sampling circuit is used up to a Conversion Time (CT) of 100 ns

**Signal and Nuclear treatment**

- The nuclear signal (count of  $\alpha$ ) collected by the detector is processed into voltage drop on the diode, amplified by the CS stage and input to the ADC stage
- The effect of the amplifier CS and the read noise of the detector are removed by the combined double sampling circuit
- The read noise of ADC is reduced by selecting a large value of CT (100 ns) for the CPS while the operation time of A is grouped in  $10^3 \sim 10^4$
- Global pixel performance characteristics
- First overall voltage gain is about 1.3 mV/alpha (MIP is 100 $\mu\text{m}$  ionized by the CS stage)
- Change in Voltage Gain (VG) is about 10% for the signals less than 100 MeV
- RISE time  $\sim 10$  ns in the ADC channel is about 10 ns for the signals less than 100 MeV

**ADC**

- Architecture
- Successive approximation structure is chosen for the trade-off between power and speed
- A simple 12-bit DAC is used to generate the same signal level for every comparison
- Based on the "charge redistribution" principle, a capacitor DAC is implemented and the external voltage (V<sub>IN</sub>, V<sub>REF</sub>, V<sub>OUT</sub>) can be used to adjust the DAC architecture

**ADC implementation**

- The reference 31 and 32 are the signals 01 and 00
- 32 stores upper part signal on D11, 30 measured the effect of the bit on D11
- $V_{OUT} = V_{REF} \cdot D_{11} / 2^{11}$ , the effect of the bit on D11
- Complementary output (Other charge 31-30)

**Conclusion and perspectives**

We proposed a CMOS Pixel Sensor architecture which aims at monitoring proton and electron fluxes up to  $10^6 \text{ cm}^{-2} \text{ s}^{-1}$  in 10 particles/frame for the operation speed of COMETH in real time. Simulation shows that the building block can be fabricated with a 0.55  $\mu\text{m}$  technology. The sensor performance can be achieved globally through the energy deposition measurement per particle up to 30 MeV nuclear energy. Implementation beyond this energy would require a strategy requiring several sensors equipped with various diodes.

The prototype COMETH without the fabrication and its counting logic was fabricated during summer 2012. In 2013 we will establish the dose measurement and particle count performance. Then, a fully functional demonstration will be designed, and the final sensor design system will be finalized.



## CPPM

Equipe microélectronique  
(conception - mesure - test)

- ATLAS / LHC et HL-LHC
  - IBL ( phase 0)
    - circuit FEI4
  - phase 1 et 2
    - Solution en 65nm
    - Solution en techno 3D
    - Solution en HV CMOS
- Imagerie
  - Rétine artificielle
  - Sonde intracérébrale

Ecole IN2P3 de microélectronique - 2013

### R&D Microélectronique au CPPM

F. Bompard, P. Breugnot, A. Caldas, D. Feugeron, F. Gensolen, S. Godot, Fléon, J. Liu, M. Menouni, P. Olive, P. Pangaud, A. Wang

Le Centre de Physique des Particules de Marseille (CPPM) est fortement impliqué dans le développement des circuits front-end pour la physique des particules (ATLAS) et valorise ses compétences dans des projets pluridisciplinaires (imagerie médicale, robotique).

---

#### ATLAS HL-LHC

Dans le cadre de la conception des futurs pixels du détecteur ATLAS pour HL-LHC, plusieurs défis doivent être relevés :

- taille de pixels réduite,
- lumiosité élevée (1 Gr/cm<sup>2</sup>),
- tolérance aux radiations à 10 Mrad (1 Grad),
- bande passante de sortie 1-3 Gbit/s,
- circuits intégrés complets (50 transistors), de grande taille et à faible consommation (14 W/cm<sup>2</sup>) pour instrumenter de grandes surfaces tout en limitant le matériel.

Pour cela nous développons 3 axes technologiques : le 65 nm, le HV-CMOS, et le 3D.

---

#### 65 nm

##### Electronique 65nm pour pixels hybrides

Dans la continuité des circuits FE-I3 et FE-I4, respectivement en technologie 250nm et 130nm, qui équipent les deux détecteurs ATLAS, la technologie 65nm devrait permettre d'étendre une table de pixel de 2x25x125 cm<sup>2</sup>.

Le circuit prototype ATPEXSA a permis de caractériser la tenue aux irradiations de la technologie en termes de tolérance aux SEEs et deses.

(PS ESRN proton 24 GeV)	type	taille	SE	SEI	SEB
123.4.4.200	SE	400 μm	2.8	1.0	1.0
123.4.4.200	SEI	250 μm	2.8	1.0	1.0
123.4.4.200	SEB	125 μm	2.8	1.0	1.0

Conclusions des tests :

- Traite résistance aux SEE
- Apparition d'erreurs à partir de 400 Mrad sur les DFF (en prévision de 1.2 à 2 années pour l'installation de la partie supérieure de la table de pixel des PROX droits).

En cours :

- Etude de test pour caractériser la tenue aux radiations de blocs monolithiques élémentaires
- conception de nouvelles mesures et blocs IP (12 bits/AD, ref tension, capteur ?)
- collaboration avec le LAPP depuis mars 2013

#### HV

##### Electronique HV pour pixels monolithiques

Deux prototypes en technologie AMS 0.13μm HV et un prototype en technologie GlobalFoundries 0.13μm BCDiBite ont été réalisés.

Les circuits CPPM v1 et v2 sont des modules de 60x60 pixels. Chaque pixel a pour taille 35x35 μm, ce qui correspond à 1/3 de la taille des pixels du FE-I4. La chaine analogique comprend un préamplificateur avec gain découplé. Chaque groupe de 3 pixels est relié par un multiplexeur capable à un pixel FE-I4. Le circuit CPPM v2 est une matrice de 78x24 et utilise la même technologie que celle utilisée pour le projet.

Les circuits CPPM ont été collés directement sur les circuits FE-I4. Ainsi chaque avertissement du CPPM donne l'information nécessaire pour être traité par les pixels du FE-I4. Cette information est déjà décodée et convertie (SE/ID) par le CPPM. Prochaine étape : circuit HVCMOS entièrement autonome (senseur + détection analog. + traitement numérique + bloc de lecture) - solution 3D ?

Tests :

- Radiation de 10<sup>12</sup> protons/cm<sup>2</sup> (technologie existante en grand volume)
- Radiation de la matrice.

#### 3D

##### Electronique 3D-IC pour pixels hybrides

En 2009, le 1<sup>er</sup> run 3D-IC HW pour le community HEP fut organisé par le FNRS, avec 15 participants (France, Germany, Italy, Italy and United States). Le projet est basé sur la technologie CHAVEZED 130nm Low Power avec une utilisation des TSVs en TEGAZOON.

FEI4-3D (CPPM) : transfert technologique du circuit FEI4\_3D. FEI4-3D (CPPM) : 30k register + comparateur + senseur des données et Data register. SEU-3D (CPPM) : 50k memory blocks. General test structures (CPPM) : TSV + 30 Data chain (seu, param.). HV operated with on-chip BackMetal (B). Transistor (Low et HT) proches des TSV. Test de stress radiologique (Tens, Cos, Dos, DPF).

Les circuits 3D ont été testés et l'échange de données entre « tiers » a été démontré. Les parties analogiques ont été amenées jusqu'à 500V sans dégrader les performances. Les circuits indépendants 2D ont été testés avec succès jusqu'à 400Mrad (proton).

---

#### ATLAS IBL

##### FEI4-B

FEI4-B est le circuit front-end qui constituera la nouvelle couche interne de pixels du détecteur ATLAS (Invertable B-Layer). Après la phase de conception qui s'est achevée à l'automne 2011 par l'envoi en fabrication, s'en est suivie la phase de tests et de caractérisation du circuit au cours de laquelle les composants conçus au CPPM (cristaux globulaires, membranes de configuration des pixels, convertisseurs A/N 10bits multivoies (GADC), capteur de température associé (TEMPSENS) ont pu être testés sur table et en irradiation au PS CERN (proton 24 GeV).

Caractérisation et test SEU des registres (5.5 10<sup>11</sup> protons/cm<sup>2</sup>)

Test capteur de 1<sup>er</sup> en direct

Conclusions des tests :

- les mémoires SEU ont montré la cross-section d'un facteur 40.
- les GADC et TEMPSENS fonctionnent en moins d'une heure à 600 Mrad.

Qualification et production du FEI4-B :

- la procédure de calibration GADC, nécessaire pour compenser l'effet de la dérive des variations des références de tension et courant, a été définie et la routine associée sera implémentée prochainement sur une plateforme de l'instrument de base.
- GADC et TEMPSENS sont utilisés pour la production des modules et des modules en mesure les courants de base des détecteurs (cristaux ou TSV), la température du circuit, la tension d'alimentation externe, et la tension d'entrée du pixel de calibration.

#### PIXSIC

Sonde Intracérébrale PIXSIC optimisée pour l'imagerie du cerveau in vivo chez l'animal adulte et lors de ses mouvements.

A. sonde silicium haute résolution : 10 pixels (100 μm x 100 μm x 100 μm)

B. Aile de lecture mobile (Pixel2) (technologie 0.13 μm)

C. enc à dos :

- électronique simple 600 n m
- avec code 600 n m
- qualité de pixel en fonction de la position du pixel
- réduction de la consommation de l'axe de lecture

Résultats :

- corros 50 μm/voix
- corros 300 μm/voix
- Indicateur (Bite - 200 μm) test.
- électronique simple 600 n m
- avec code 600 n m
- qualité de pixel en fonction de la position du pixel
- réduction de la consommation de l'axe de lecture

Appareil de calibration 3D

#### Rétines artificielles

Technologie : XIM 0.13 μm

Le chip est découpé colonne par colonne. Chaque colonne possède 42 x 12 = 504 pixels dans ses propres verres-bonds.

Particularité des pixels : Auto-adaptation à la luminosité ambiante (gates/capteur de type feedback)

EVA : 12 pixels de type Deltacell + 12 pixels de type Naka-Rushion

La fonction de Naka-Rushion permet également de modéliser la vision des insectes.

# Column ADC for HR imaging applications

- LPSC Grenoble – Gravit
- Massive Array ADC
- Interlocuteur  
– Fatah RARBI

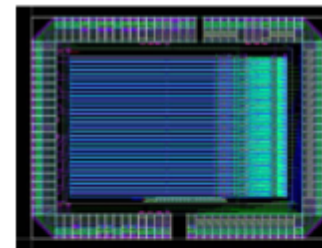


## Architecture



- 14 bit, .5MSPS ADC
- $< 500\mu\text{W}/\text{ch}$
- $30\mu\text{m}$  pitch, (length  $< 1.9\text{mm}$ )

## 1<sup>st</sup> prototype

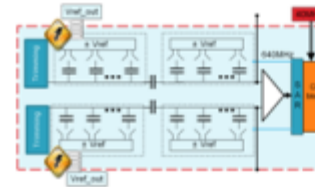


- CMOS 130nm
  - Analog power supply: 1.5V
  - Digital power supply: 1.2V
- Converter array based on SAR architecture
- 14 bit resolution
- Speed of .5MSPS/column
- $C_{in} \approx 3\text{pF}$
- Power Consumption:  $< 500\mu\text{W}/\text{column}$
- Pitch:  $30\mu\text{m}$  (length  $< 2\text{mm}$ )

# PEALL 12-b, 40-MSPS SAR ADC: A Power Efficient and Low Latency SAR ADC

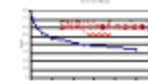
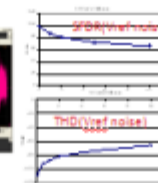
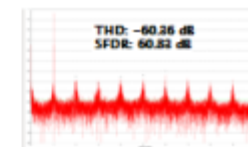
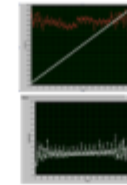
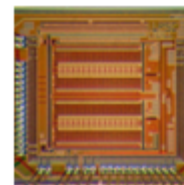
- LPSC Grenoble
  - ATLAS
- High-speed and low power ADC
- Interlocuteur
  - Fatah RARBI

#### Architecture

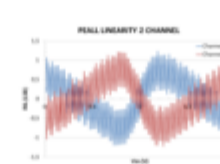
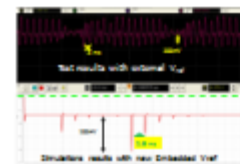


- 12 bit, 40 MSPS SAR ADC
- Differential Architecture
- 2 segmented capacitor Array
- No PLL needed: 640MHz clock

#### 1<sup>st</sup> prototype test results



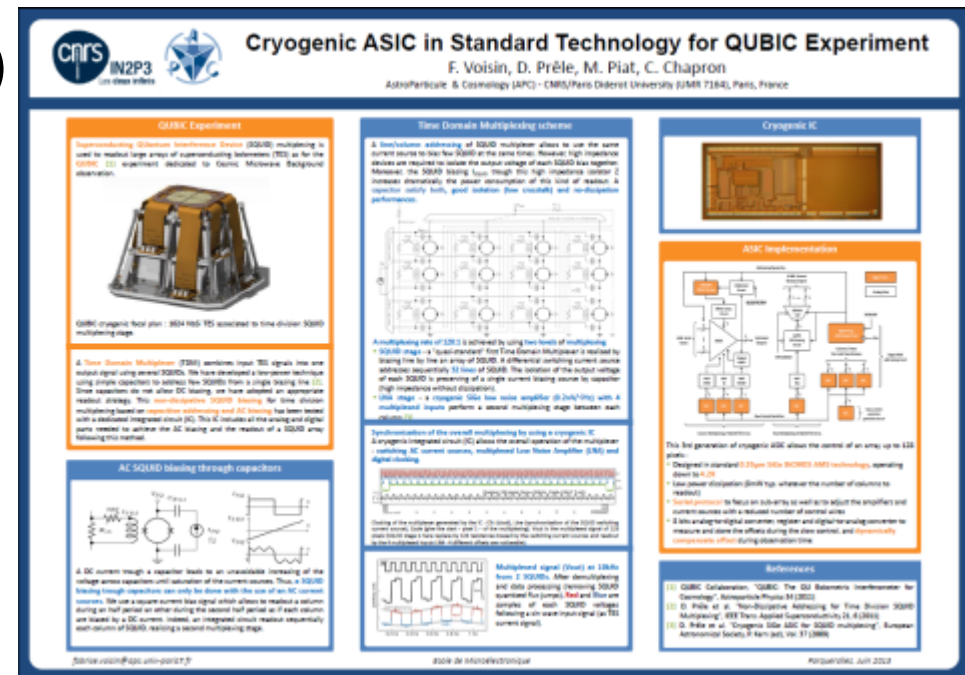
#### 2<sup>nd</sup> prototype simulation results



- 4 Channels, 12 bit, 40MSPS SAR ADC
- Differential Architecture
- Embedded Reference voltage
- No PLL needed: 640MHz clock
- LVDS output
- Low power: **30mW/ch.**

# Cryogenic ASIC in Standard Technology for QUBIC Experiment

- AstroParticule & Cosmologie (APC)  
F. Voisin, D. Prêle
- Description de l'ASIC réalisé pour l'instrument QUBIC dédié à l'observation du fond diffus cosmologique



**Cryogenic ASIC in Standard Technology for QUBIC Experiment**  
F. Voisin, D. Prêle, M. Piat, C. Chapron  
AstroParticule & Cosmologie (APC) - CNRS/Paris Diderot University (JURR 7184), Paris, France

**QUBIC Experiment**  
Superconducting Quantum Interference Device (SQUID) multiplexing is used to readout large arrays of superconducting qubits (SQDs) as for the QUBIC [1] experiment dedicated to Cosmic Microwave Background observation.

**Time Domain Multiplexing scheme**  
A time-domain multiplexing of SQUID multiplexers allows to use the same current source to bias the SQUID at the same time. However, high impedance devices are required to isolate the output voltage of each SQUID bias register. Moreover, the SQUID biasing loop, through the high impedance, causes a decrease dramatically the power consumption of this kind of system. A major priority is to find a good solution (from circuit) and multiplexing performance.

**Cryogenic IC**

**ASIC Implementations**

**AC-SQUID biasing through capacitors**

**References**

3009-26 MICROELECTRONIQUE  
Riquier-Virel, Juin 2013