Built-in references for ADC

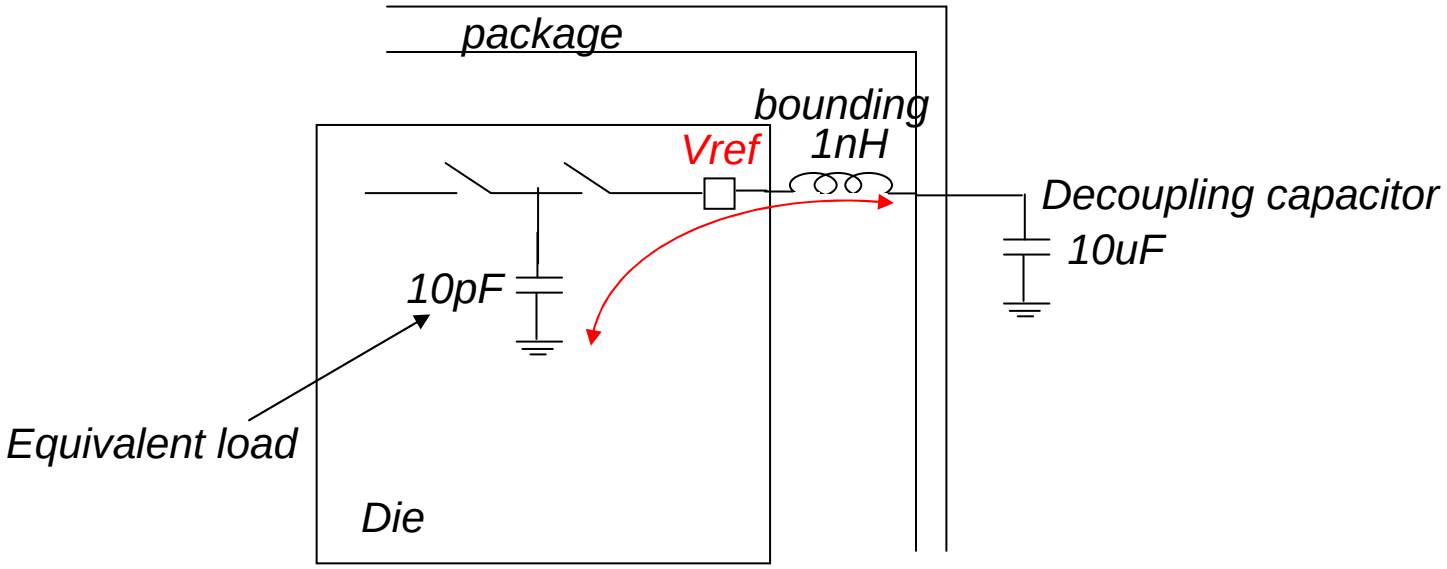
1. Reference using an external decoupling capacitor (limitations)
2. References based upon an opamp
3. References based upon an OTA
4. References using local feedback loops
5. References based on replica
6. References without any external decoupling capacitor (summary)
7. Annexes (bandgap under low supply voltage)

Built-in references for ADC

1. Reference using an external decoupling capacitor (limitations)

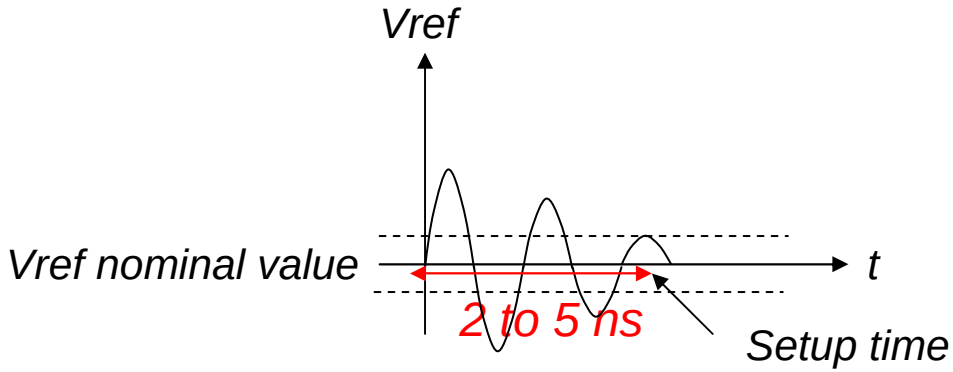
Reference using an external decoupling capacitor

The decoupling capacitor is much higher than the equivalent load, acting then as an ideal generator (i.e. virtual ground). During switch capacitor process, some charges are provided by the external decoupling capacitor in a very short time. This leads to a rapid variation of the current inside the inductor which directly translates into a voltage across it. As a result of this energy exchange between the decoupling capacitor and the internal load, oscillations appears on node Vref.



Reference using an external decoupling capacitor

Vref deviation from the nominal value should be less than an LSB within a fraction of the sampling clock to allow the ADC to perform normally.



$$\omega_{osc} = \frac{1}{\sqrt{LC}} \Leftrightarrow f_{osc} = \frac{1}{2\pi\sqrt{10^{-9}.10.10^{-12}}} = 1 \, or \, 2 \, Ghz$$

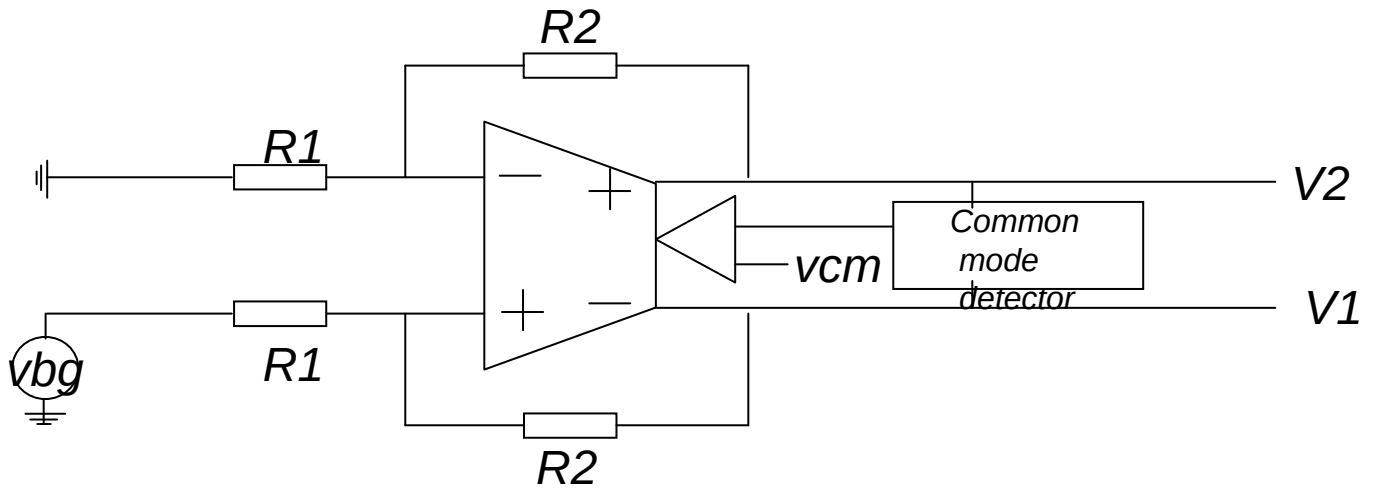
Since usual setup time is some nanoseconds, references using external decoupling capacitors are not suitable for ADC clocked at a frequency ***higher than 200Mhz***. Therefore, only references ***without any external decoupling capacitor*** will be addressed in this course.

Built-in references for ADC

1. Reference using an external decoupling capacitor (limitations)
2. References based upon an opamp

References based upon an OPAMP

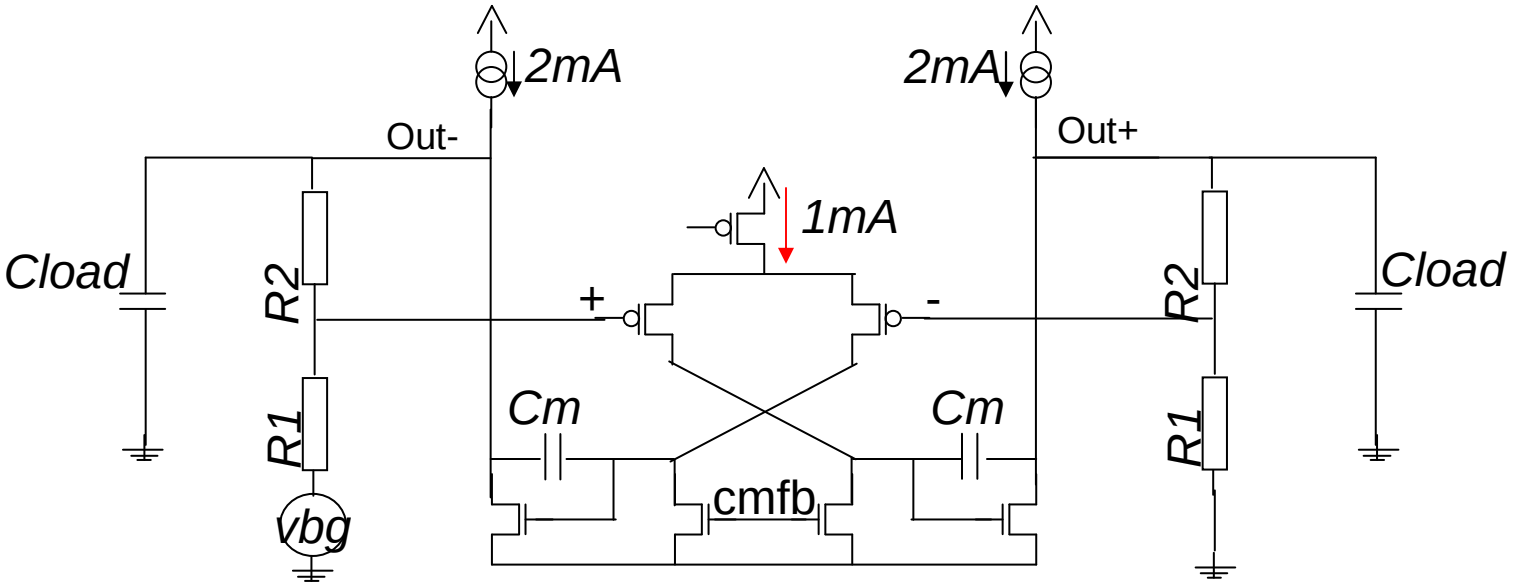
An example:



$$\begin{cases} V2 - V1 = \frac{R2}{R1} Vbg \\ V2 + V1 = 2.VCM \end{cases} \Leftrightarrow \begin{cases} V1 = VCM - \frac{1}{2} Vbg \frac{R2}{R1} \\ V2 = VCM + \frac{1}{2} Vbg \frac{R2}{R1} \end{cases}$$

References based upon an OPAMP

In the following example, ***no external decoupling capacitor*** is necessary since both the ***bandwidth*** is compatible with the available settling time of 2ns and the ***gain*** of 50db is sufficient for the required accuracy.



Miller compensated two gain stages amplifier

References based upon an OPAMP

Here below, you will find some indications to set main design parameters.

- ADC specifications: 2Vppdiff 200Mhz 8bits SAR (2.5v - 90nm technology).

- Required bandwidth:
  The time required to settle to n=8 bits accuracy must be lower than half a clock period (i.e. 5ns). Here, 2ns is targeted leading to a closed loop bandwidth of 440 Mhz as explained below:

$$ts = n\tau \ln 2 \Leftrightarrow \tau = \frac{ts}{n \ln 2} = \frac{2.10^{-9}}{8 \ln 2} \approx 0.36ns \Leftrightarrow BW_{CLOSED} = {}^{1}\!\!\diagup\!\!{}_{2\pi.\tau} \approx 440Mhz$$

  Since R2 is very closed to R1 (V2-V1=1volt), the closed loop gain approaches a value of 2. Thus, the open loop bandwidth should be :

$$BW_{OPEN} = 2 * BW_{CLOSED} \approx 880Mhz$$

References based upon an OPAMP

Let us calculate the amount of current needed to drive a miller capacitor of 2pf(value dictated by noise constraints) :

$$BW_{OPEN} = \frac{Gm}{2\pi Cmiller} \Leftrightarrow Gm = 880.10^{6}.2\pi.2.10^{-12} = 11.mA/V$$

- Needed current:

$$Gm = \frac{2.I}{(Vgs - Vt)} = \frac{I}{0.050} \Leftrightarrow I = 0.55mA$$

in each branch of the differential pair.

- Current in output stage is much higher to guarantee the overall stability. It can be shown that if the output load is in the order of 4pF, an output current of ***2mA*** is required in each branch .

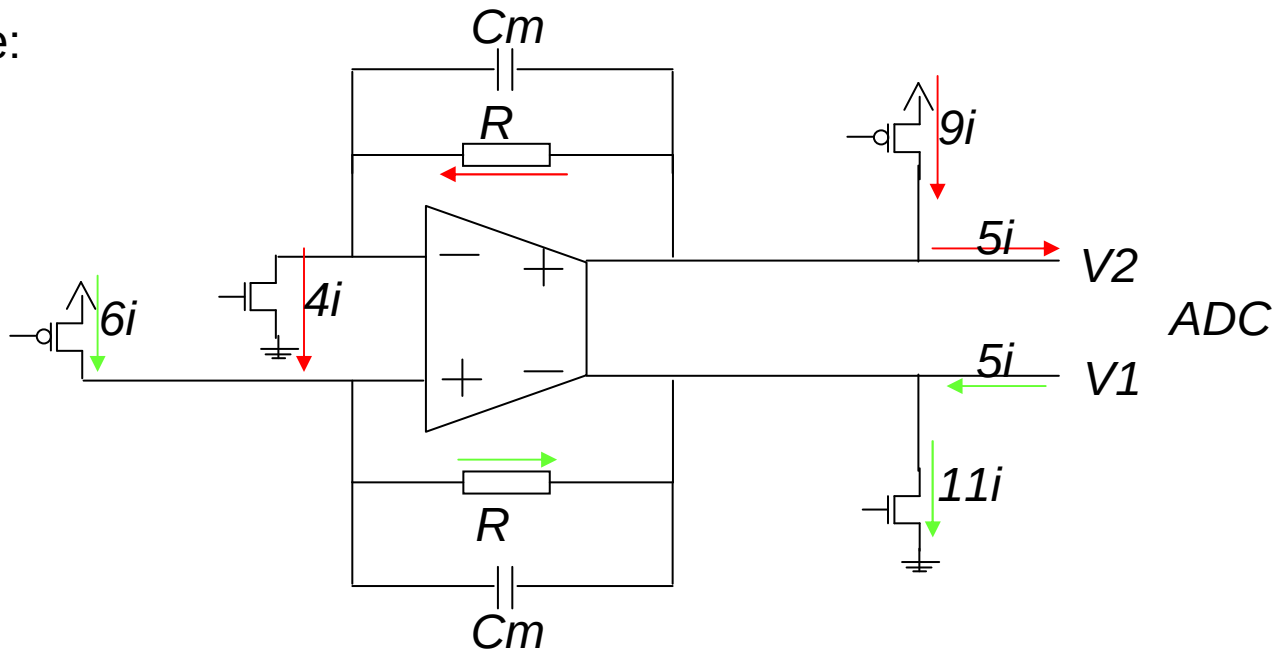
This type of references is only suitable for ***low resolution*** ADC (8 to 9 bits).

Built-in references for ADC

1. Reference using an external decoupling capacitor (limitations)
2. References based upon an opamp
3. References based upon an OTA

References based upon an OTA

An example:



$$\begin{cases} V2 - V1 = 10R.I \\ V2 + V1 = 2.VCM \end{cases} \Leftrightarrow \begin{cases} V1 = VCM - 5R.I \\ V2 = VCM + 5R.I \end{cases}$$

References based upon an OTA

Note that current sources (4i,6i) have been chosen instead of symmetrical current sources (5i,5i) to show the possibility of setting the input common mode voltage of the amplifier at a different value than the output common mode voltage (i.e. vcm). This allows to use either Nmos differential pair (if maximum transconductance is required) or Pmos differential pair (if low noise is preferable).

If these currents are generated via a bandgap, we have i=Vbg/Rbg where Rbg is the resistance used inside the bandgap.

If the resistance R is a replica of Rbg :

$$\begin{cases} V1 = VCM - 5\dfrac{R}{Rbg}.Vbg \\ V2 = VCM + 5\dfrac{R}{Rbg}.Vbg \end{cases}$$

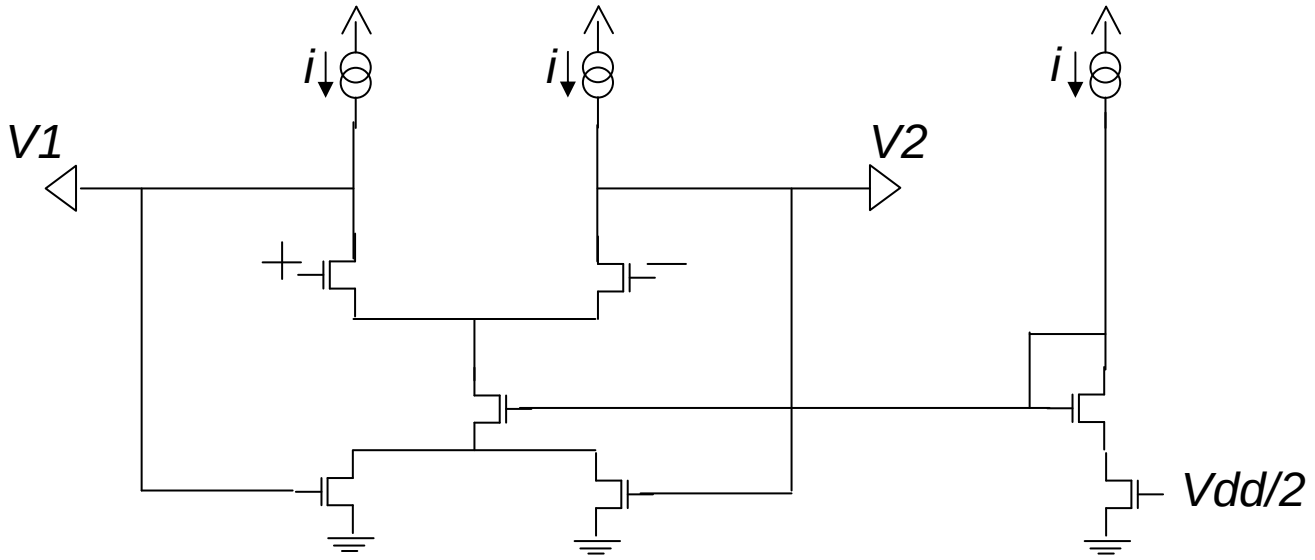
References based upon an OTA

At a first order, the differential reference (V1-V2) is proportional to a ***bandgap voltage***. In fact, the global accuracy is not so good since many imperfections affect its behavior (resistance mismatches, amplifier offset, low open loop gain, current sources mismatches). This limitation can be overcome by using a ***calibration*** at startup for example.

On the other hand, this reference provides a ***low output impedance*** even at high frequency. Thus, as we will see later, only ***one gain stage*** amplifier is used providing both maximum ***bandwidth*** and ***stability***. Of course, consumption is quite high (some milliamps) to ensure low impedance at the frequency of current spikes (i.e. when capacitors are switched towards this reference).

Notice that at very high frequency, output impedance is kept low due to feedback capacitors (named Cm) which connect the input differential pair in a diode configuration. Then, output impedance is 1/Gm if Gm is the transconductance of the amplifier. That’s why the current inside the differential pair is so high.

References based upon an OTA



Example of a single stage OTA

References based upon an OTA

Transconductance of the amplifier:

$$Gm = \frac{2.I}{(Vgs - Vt)} = \frac{I}{0.050}$$

Where I is the current in each branch of the differential pair. Transistors operate in their saturation region close to ***subthreshold***.

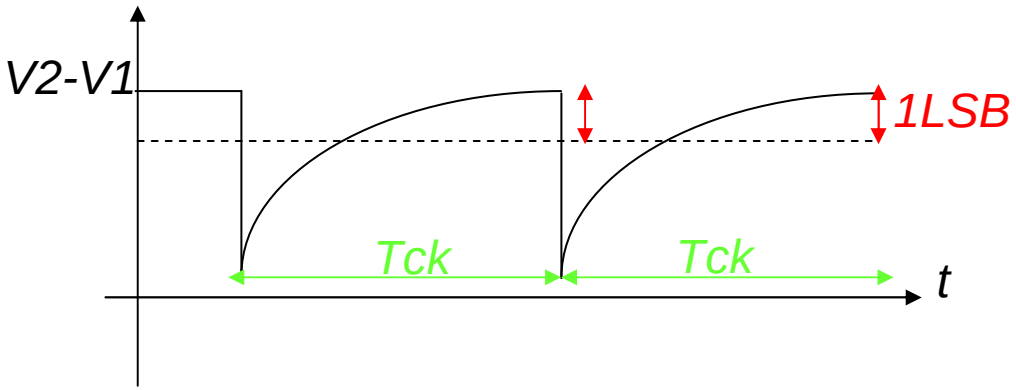
For I=2mA, we have Gm=40mA/V.

Output impedance is then around 25 ohms (1/Gm).

Now, let us evaluate if this Gm is sufficient to drive 10pF load at high clock frequency in case of a 12 bits ADC (10pF is a value close to the total capacitor of a 12 bits ADC).

References based upon an OTA

When the capacitive load is connected to the transconductance, a drop first appears during the instantaneous charge sharing between this load and the overall capacitor formed by transistors.

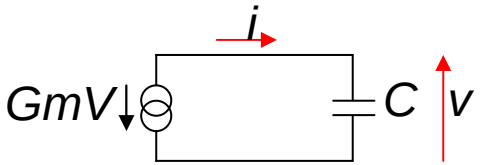


Then, transconductance has to provide some charges to the load in order to restore the quantity V2-V1 to its quiescent value. This should occurred within a certain amount of time, (i.e. one third of the clock period).

References based upon an OTA

The small signal equivalent circuit can be represented as below:

(V=V2-V1)



So:

$$-GmV = C\frac{dV}{dt} \Leftrightarrow \frac{dV}{dt} + \frac{Gm}{C}V = 0 \Leftrightarrow V(t) = K.e^{-\frac{Gm}{C}t}$$

Then the time constant and the corresponding bandwidth are:

$$\tau = {}^{C}\!/_{Gm} \Leftrightarrow BW = {}^{Gm}\!/_{C}$$

The time required to settle to n bits accuracy is:

$$ts = n\tau \ln 2 = n\frac{C}{Gm}\ln 2 = 12\frac{10.10^{-12}}{40.10^{-3}}0.69 \approx 2ns$$

References based upon an OTA

In fact, this time doesn't take into account the slew rate behavior of the transconductance during the very first phase.

This kind of references appears only compatible with clock frequency less than ***400 Mhz***. This latter may be increased up to ***5*** or ***600 Mhz*** using a high performance technology (65nm,40nm or bicmos) and at the cost of an increased consumption.

These schematics have been used in a 200Mhz 12bits pipeline ADC (2.5v - 90nm technology).

Built-in references for ADC

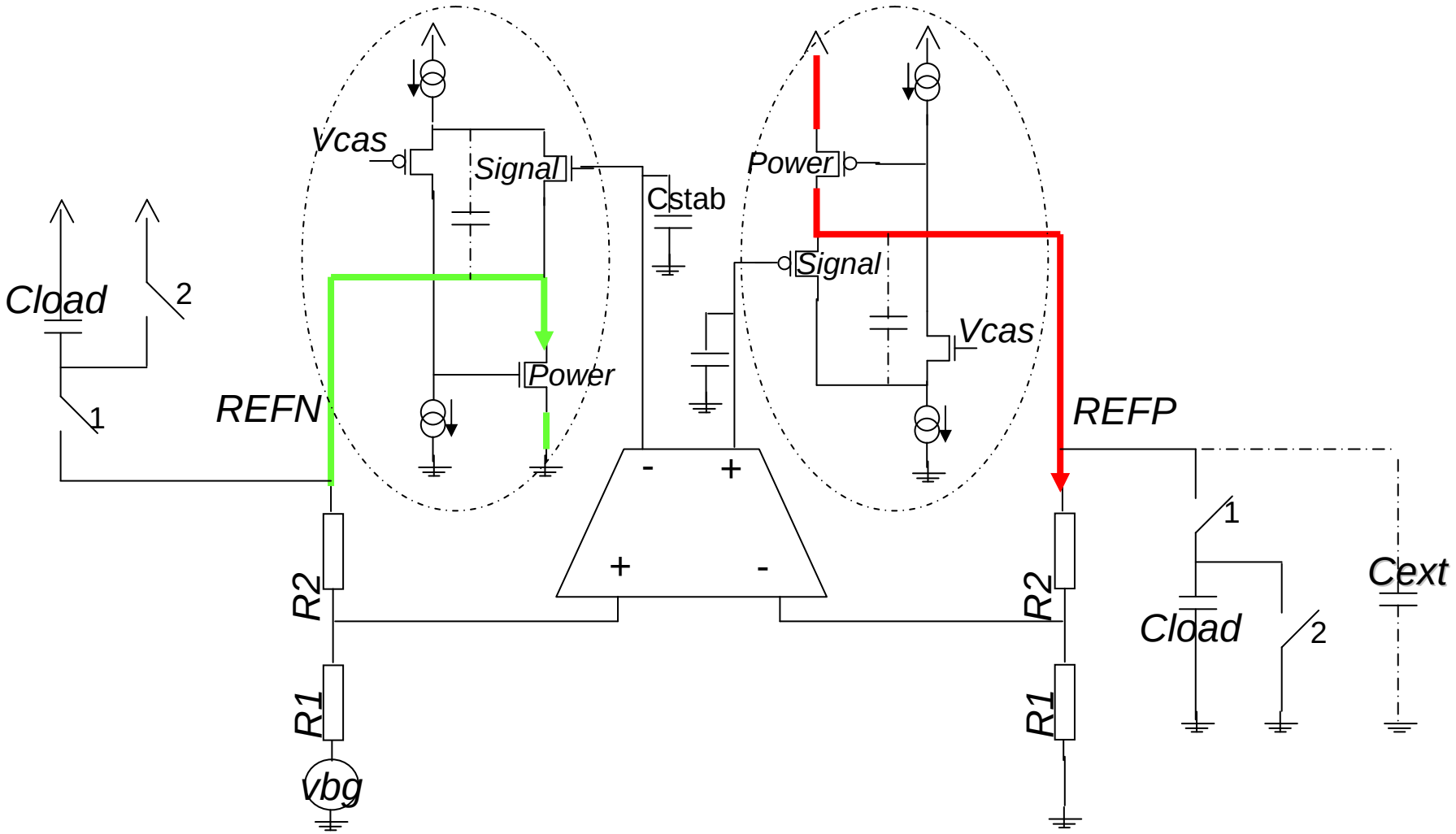
1. Reference using an external decoupling capacitor (limitations)
2. References based upon an opamp
3. References based upon an OTA
4. References using local feedback loops

References using local feedback loops

From an architectural standpoint, this approach differs from the first one where a high impedance opamp relies on negative feedback to ensure driving capability. Here, a local feedback loop is inserted in place of a classical follower to drive the output load. Hence, ***accuracy*** is guarantee by the ***global*** loop whereas ***speed*** is ensured by the ***local*** loop. Consequently, the main amplifier can be very simple and with a limited bandwidth.

One important thing to note is that we need to ***source*** some current into node REFP whereas we need to ***sink*** some current from node REFN. Classically, REFP would be driven by an Nmos source follower, but since REFP is close to the supply voltage, such a follower is not suitable (the same applies to REFN). This schematic acts as a follower but with the right polarity.

References using local feedback loops



References using local feedback loops

The way it works is the following. When the ADC sinks some current on node REFP, the main amplifier reacts by increasing the voltage on the gate of the signal transistor which has the effect of cutting it off. Since the current inside the loop is constant, the voltage on the gate of the power transistor decreases and its current increases. Hence, the ***global loop*** tracks the ***average current*** on node REFP. On the other hand, a switched capacitor ADC frequently requires some charges in a very short time. This rapid voltage drop on REFP tends to cut off the signal transistor and consequently the current inside the power transistor increases. Hence, the ***peak current*** is taken in charge by the ***local loop***.

It is worth adding a small bypass ***capacitor*** between the node REF and the source of the cascode in order to ***speed up*** the loop. By doing this, the latter behaves like a signal transistor.

References using local feedback loops

For test purpose, this approach also differs from the first one, since stability can be ensured ***with or without*** external decoupling capacitors (Cext). This comes from the fact that the dominant pole is now created by Cstab whereas the output pole due to Cext remains a secondary pole even if value as high as some ***nanofarads*** is used for Cext.

In fact, this structure is a GM-enhanced cell. The overall Gm is given by:

$$Gm_{equi} = (Gm_{signal} \times Zg) \times Gm_{power} = M \times Gm_{power}$$

Where Zg is the impedance on the grid of the power transistor. The multiplier M can be as high as ***many hundreds*** pushing the associated pole (Gm_{equi}/Cext) well beyond the dominant pole for value of Cstab of only few ***picofarads***. Note that an electrical serial resistance (esr) is always present on Cext increases again the secondary pole.

These schematics have been used in a 200Mhz 12bits pipeline ADC (2.5v - 65nm technology).

Built-in references for ADC

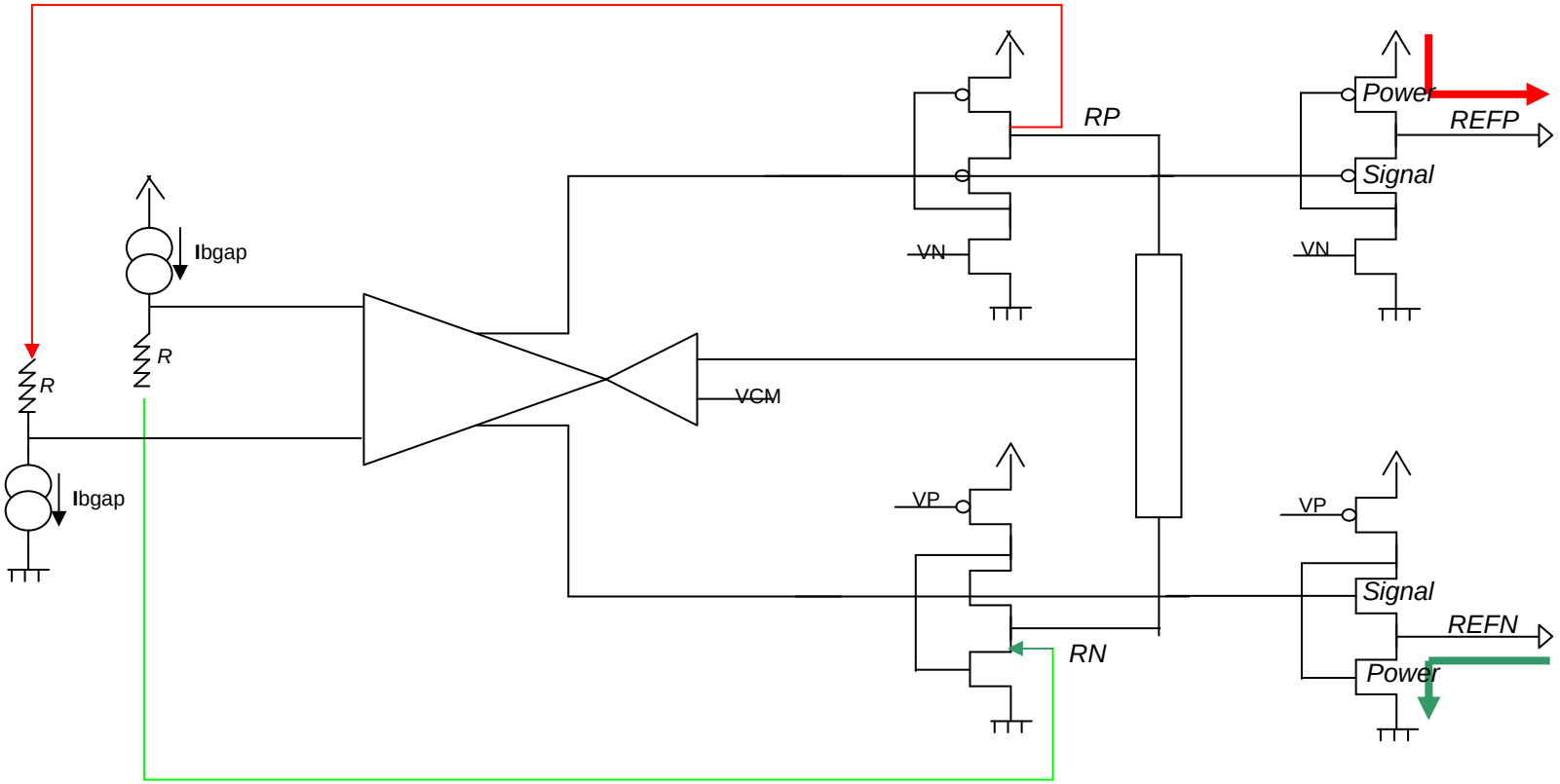
1. Reference using an external decoupling capacitor (limitations)
2. References based upon an opamp
3. References based upon an OTA
4. References using local feedback loops
5. References based on replica

References based on replica

This architecture is suitable at ***low supply voltage*** (i.e. lower than 1.5v) and when using thin oxyde MOS with ***multiple threshold voltages*** (high Vt, standard Vt, low Vt …) which is often the case in modern technologies.

The ***power*** transistors are classically ***high Vt*** Mosfet whereas ***signal*** transistors are ***standard Vt*** Mosfet (or even low Vt). This allows to make sufficient drop from the supply voltage so as to saturate the signal transistors. By doing this, references can be very close to the supply voltages (i.e. 100mV) which is highly preferable in low voltage environment. Taking a supply voltage of 1.1v as an example, we can reach REFP=0.9v and REFN=0.2v. As a consequence, the differential reference is equal to 0.7v leading to a dynamic of 1.4Vppdiff for the ADC.

References based on replica



*REF = REFP – REFN = RP – RN = 2*R*Ibgap*

References based on replica

The differential amplifier tries to make its both entries equal and as node RP is shifted upwards by the quantity R*Ibgap and node RN is shifted downwards by the same quantity, we obtain:

$$\begin{cases} RP - RN = 2.R.Ibgap \\ RP + RN = 2.VCM \end{cases} \Leftrightarrow \begin{cases} RN = VCM - R.Ibgap \\ RP = VCM + R.Ibgap \end{cases}$$

Then, as the replica is connected in parallel of the output follower (via the gate of the signal transistor) and as its current is a homothetic version of the current inside the output follower, voltage on node REFP is ***equal*** to voltage on node RP (the same applied to REFN/RN).

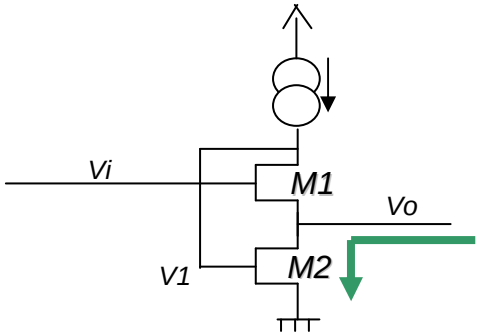
If the output (source or sink) current ***differs*** from its nominal value, it will translate into a ***Vgs*** change for the ***powe***r transistor. Thus, it will only modulate the ***Vds*** of the ***signal*** transistor (early effect) which will have few impact on nodes REFP/REFN.

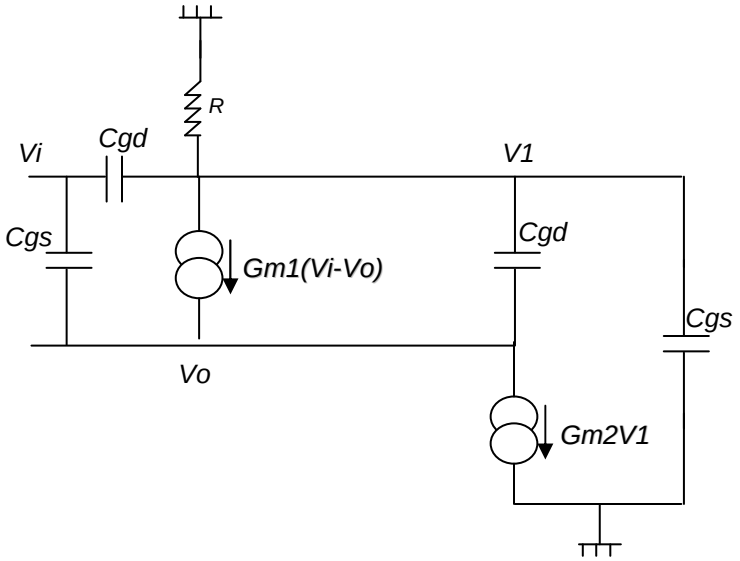
References based on replica

Note that only the ***replica part*** consumes a significant amount of ***power*** , mainly for speed reason. The other part is a slow one with few requirements in terms of speed and can be biased with some microamps.

It is worth using the same kind of resistance for this reference generator (shift resistances, common mode detector,…) and for the bandgap cell. By doing this, a perfect tracking will operate between both cells.

References based on replica





$$\begin{cases} I_{out} = gm_1(V_i - V_o) - gm_2 V_1 \\ V_1 = -gm_1(V_i - V_o) r_d \end{cases} \Rightarrow I_{out} = gm_1(V_i - V_o) + gm_2 gm_1 (V_i - V_o) r_d$$

$$\Rightarrow \frac{I_{out}}{V_i - V_o} = gm_1(1 + gm_2 r_d)$$

$$\Rightarrow Zout = \left(\frac{V_i}{I_{out}}\right)_{V_o=0} \approx \frac{1}{gm_2 gm_1 r_d}$$

References based on replica

In fact, this approach is very similar to the previous one which was a ***folded version*** of this replica. Due to the relatively large supply voltage (2.5v) and to the limited value of the differential reference REF (1v), it was not possible to use this replica technique in the previous case since the voltage drop across power Mosfets is not sufficient to saturate signal Mosfets. That's why a folded version has been chosen with its drawbacks in terms of ***speed*** and ***noise***.

Notice that replicas are made using ***Flip Voltage Follower*** (***FVF***) cells as denoted in the literature.

These schematics have been used in a 200Mhz 14bits sigma delta ADC operating on a 4Mhz bandwidth (1.2v - 65nm technology).

Built-in references for ADC

1. Reference using an external decoupling capacitor (limitations)
2. References based upon an opamp
3. References based upon an OTA
4. References using local feedback loops
5. References based on replica
6. References without any external decoupling capacitor (summary)

References without any external decoupling capacitor (summary)

	Converter type	Technology (CMOS)	Supply Voltage	Clock frequency	Resolution	Calibration
OPAMP based	SAR	90 nm	2.5v	200 MHz	8-9 bits	No
OTA based	Pipeline	90 nm	2.5v	400-600 MHz	10-12 bits	Yes
Local LOOP	Pipeline	65 nm	2.5v	200 MHz	10-12 bits	No
REPLICA	Sigma-Delta	65 nm	1.2v	200-600 MHz	12-14 bits	No

Built-in references for ADC

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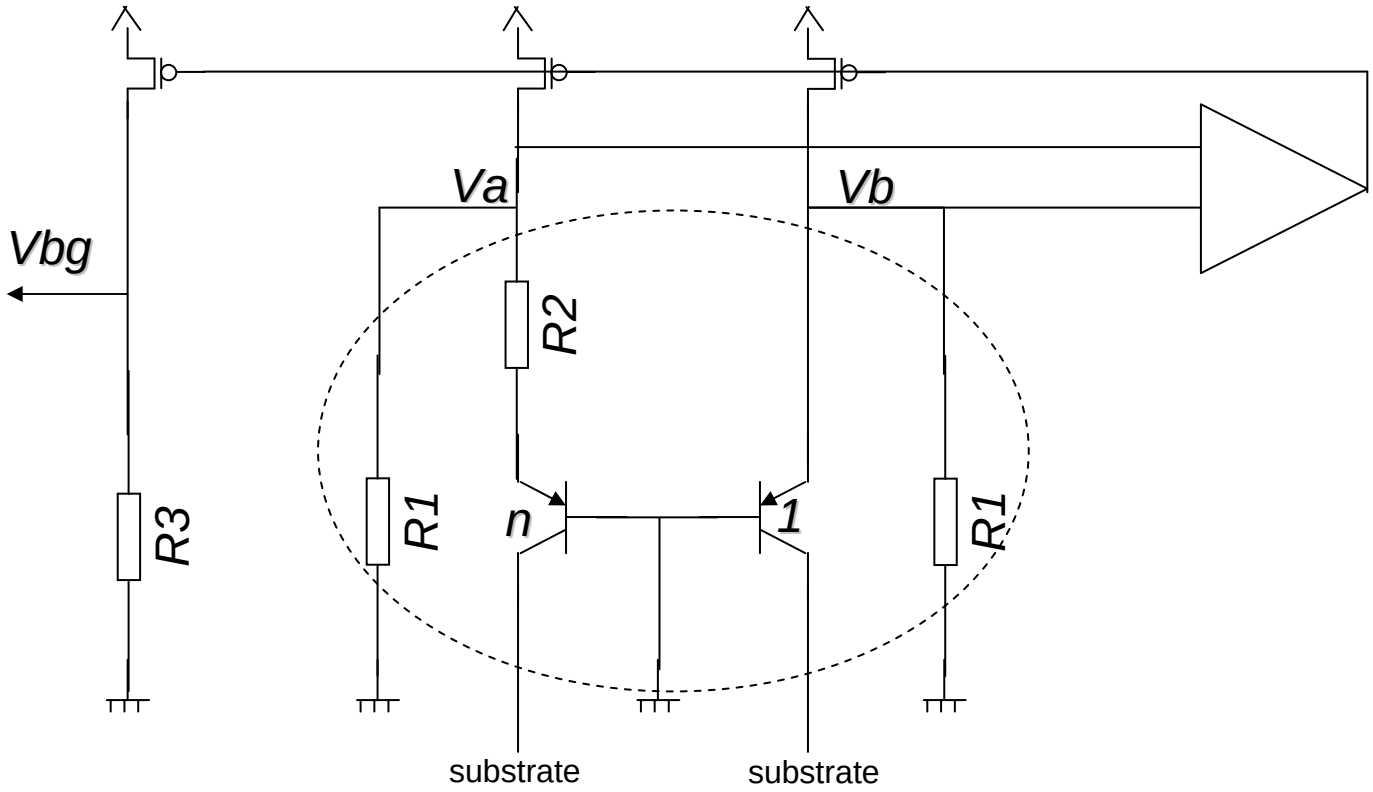
7. Annexes (bandgap under low supply voltage)

bandgap under low supply voltage



$$Vbg = \frac{R3}{R1} Vbe + \frac{R3}{R2} Vt \ln n$$