User Guide

1-Clock duty cycle

2-Clock jitter

3-Voltage references

4-Input bandwidth

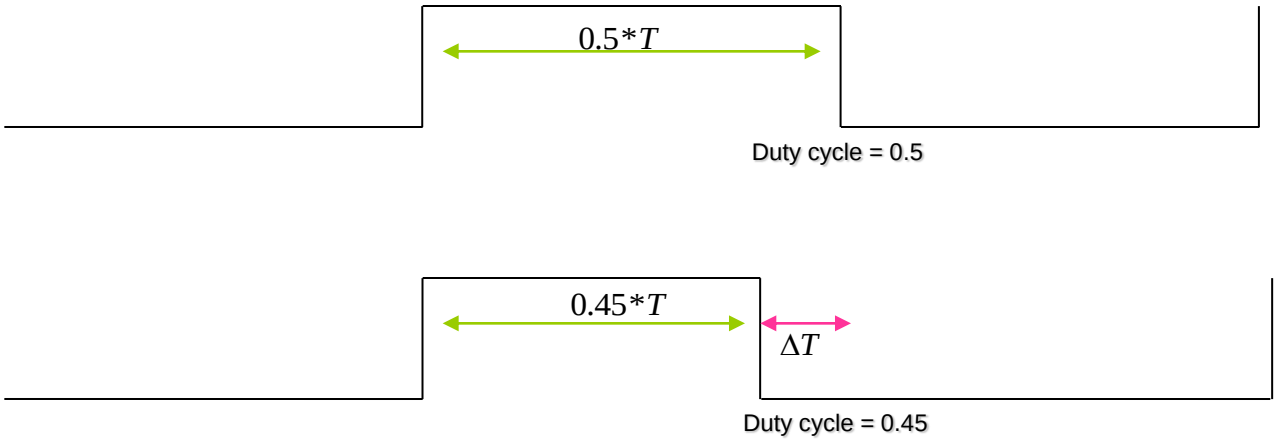
5-Differential approach

User Guide

1-Clock duty cycle

Clock duty cycle

Since this presentation is about switched capacitor ADC, clock duty cycle is of main importance. As illustrated below, a ***duty cycle different from 0.5*** directly translates into less time for the electronic to settle. Thus, the effect is similar to an ***increase of the clock frequency***.



In this illustration, the apparent clock frequency for a duty cycle of 0.45 is now:

$$Fappck = \frac{1}{2*0.45*T} = 1.11*Fck$$

User Guide

1-Clock duty cycle

2-Clock jitter

Clock jitter

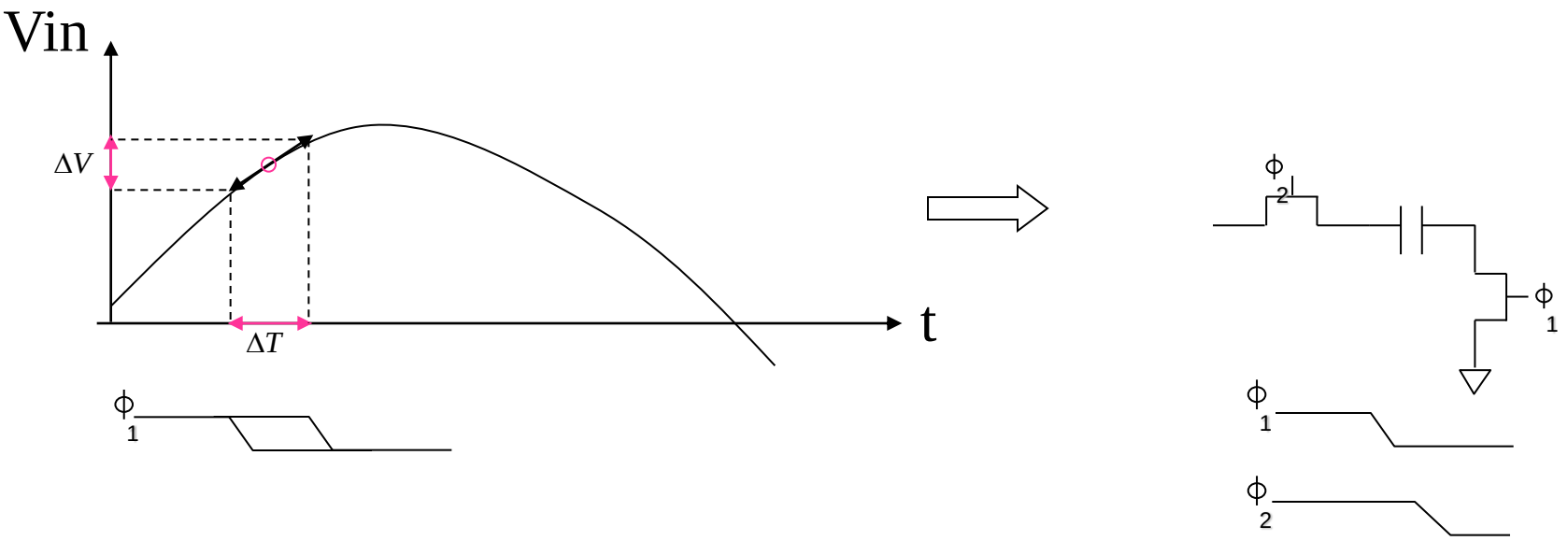
Only ***Random Jitter***, also called Gaussian jitter, is treated here. ***Deterministic jitter***, like ISI (inter symbol interference) jitter, comes from system consideration and are not part of this presentation.

Since most jitter in a electrical circuit is caused by ***thermal noise***, which has a Gaussian distribution, random jitter also follows a ***Gaussian distribution*** (Normal distribution).

Jitter can be quantified in the same terms as all time-varying signals, e.g., ***RMS***. Also like other time-varying signals, jitter can be expressed in terms of spectral density, e.g. ,***phase noise***.

Sampling frequency is normally assumed to be constant. Samples should be taken at regular intervals. If some jitter is present on the clock signal, then it will produce an error proportional to the ***slew rate*** of the input signal and to the ***absolute value*** of the clock error.

Clock jitter



Clock jitter originates from noise inside ***clock generator*** and from noise inherent to the ***PLL***. Clock jitter directly translates into ***sampling noise*** and adds to the overall sampling noise.

Clock jitter

In case of a sinusoidal input signal and in presence of a clock jitter with an RMS value σ_j, sampling noise due to this jitter can be calculated as below:

$$v = A\sin\omega t \Rightarrow \frac{dv}{dt} = A\omega\cos\omega t$$

$$ElementarySamplingNoise = \frac{dv}{dt}\cdot\sigma_j$$

The overall sampling noise, named here Jitternoise, is then:

$$Jitternois\,e_{rms} = \sqrt{\frac{1}{T}\int_0^T\left(\frac{dv}{dt}\cdot\sigma_j\right)^2 dt} = \sigma_j\cdot\sqrt{\frac{1}{T}\int_0^T\left(\frac{dv}{dt}\right)^2 dt} = \sigma_j\cdot\sqrt{\frac{1}{T}\int_0^T\left(A\omega\cos\omega t\right)^2 dt}$$

$$Jitternois\,e_{rms} = \sigma_j\frac{A\omega}{\sqrt{2}}$$

Clock jitter

Signal to noise degradation due to clock jitter can be expressed as:

$$SNR = 20\log(Vin_{rms} / Jitnoise_{rms}) = 20\log\left(\frac{A/\sqrt{2}}{\sigma_j A\omega/\sqrt{2}}\right)$$

$$SNR = -20\log(\sigma_j \omega)$$

Note that ***input frequency***, not clock frequency, is the determining factor with respect to jitter performance.

Let us calculate the SNR for a input sine wave of frequency 100Mhz and a clock jitter of $1ps_{rms}$:

$$SNR = -20\log(2\pi.100e06.1e-12) \approx 64db$$

$$\Rightarrow ENOB \approx 10.4bits$$

(State of the art jitter for PLL with an LC oscillator is around 150fs).

User Guide

1-Clock duty cycle

2-Clock jitter

3-Voltage references

Voltage references

In case of external decoupling references, some cautions have to be taken.

First, ***access resistance*** to the pad should be lower than ***few ohms*** (5 ohms for a 12 bits ADC under 2.5v supply voltage is common).

Secondly, decoupling should be done as close as possible to the pins. Differential decoupling is always better and must include both chemical (high value) and ceramic (low value but low esr) capacitors.

User Guide

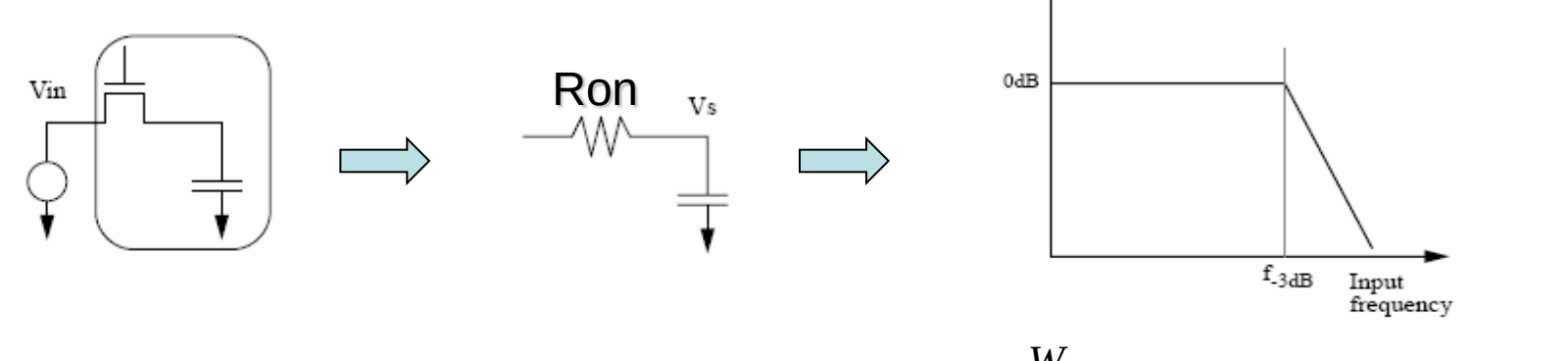
1-Clock duty cycle

2-Clock jitter

3-Voltage references

4-Input bandwidth

Input bandwidth



$$Ron = 1 \Big/ \left(K.\frac{W}{L}.(Vgs\_Vt) \right)$$

So

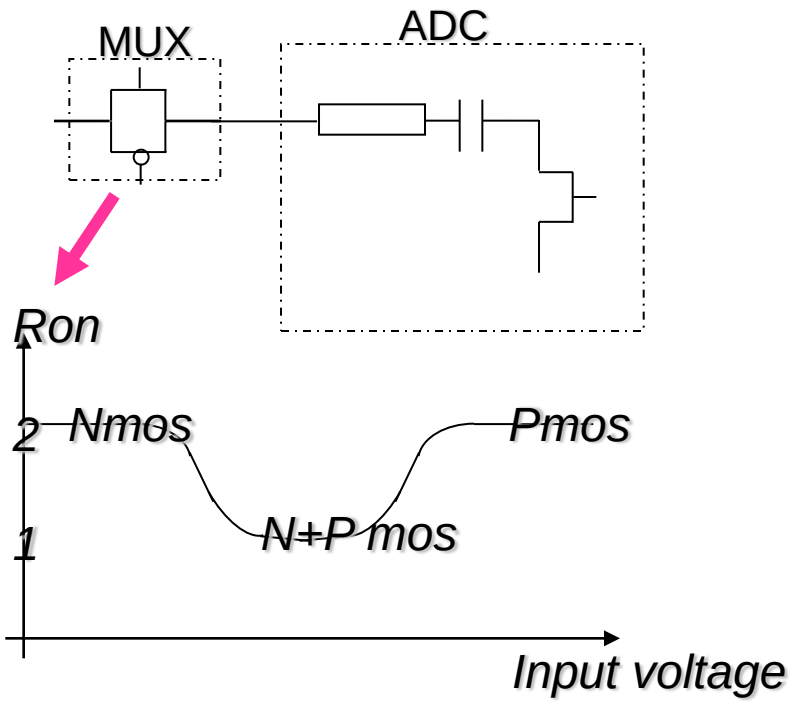
$$f_{-3db} = \frac{1}{2\pi} \cdot \frac{k \cdot \frac{W}{L} \cdot (Vgs - Vt)}{Cs}$$

Example: Vgs-Vt=1v W/L=10 k=70µA/V Cs=1pF => f_{-3db}=100Mhz

Since Vgs (hence Ron) is modulated by the input signal, low-pass filter bandwidth is also modulated. This directly leads to distortion since the ***gain depends on the input signal amplitude***. To avoid this phenomena, *Ron constant switch is usually used.*

Input bandwidth

In case of multiplexer in front of the ADC, the equivalent input resistance is no more constant.



Therefore, the ***Ron*** of the multiplexer must be compatible with the ***resolution*** of the converter and the equivalent ***input capacitance***.

User Guide

1-Clock duty cycle

2-Clock jitter

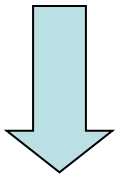
3-Voltage references

4-Input bandwidth

5-Differential approach

Differential approach

1. Low deterministic sampling error (Charge injection, Clock feed through)
2. High power supply rejection (PSRR)
3. Low distortion (THD)
4. High signal to noise ratio (SNR)



Use ***Differential structures*** in the reception chain as soon as possible