Short course on preamplifiers

Porquerolles 2013

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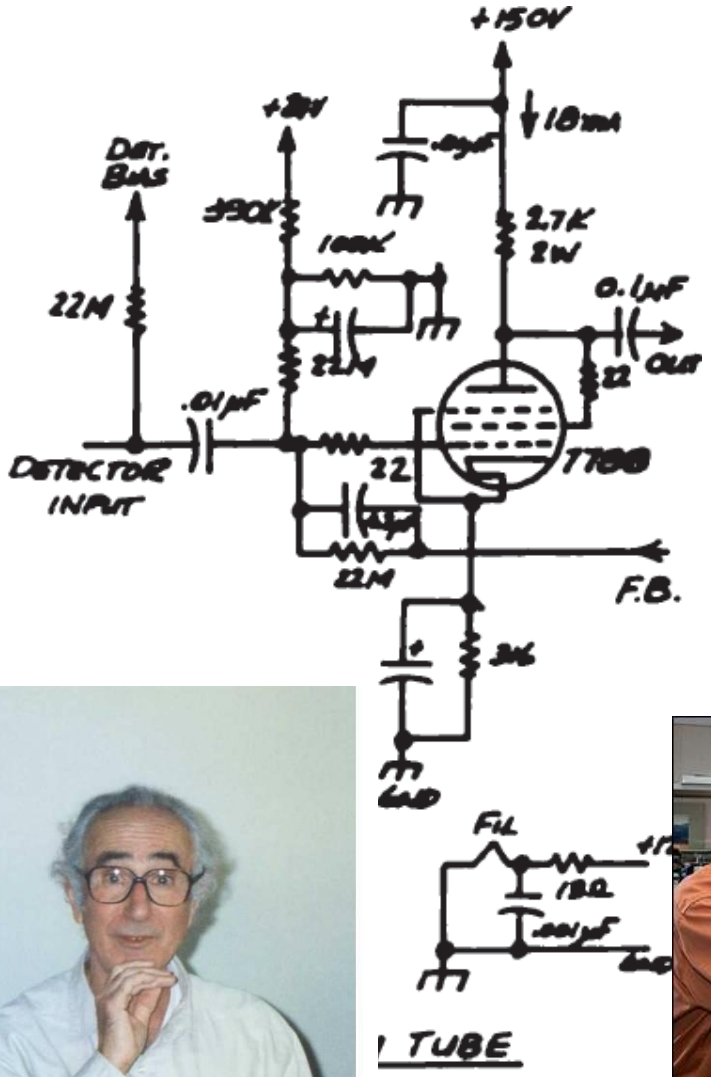
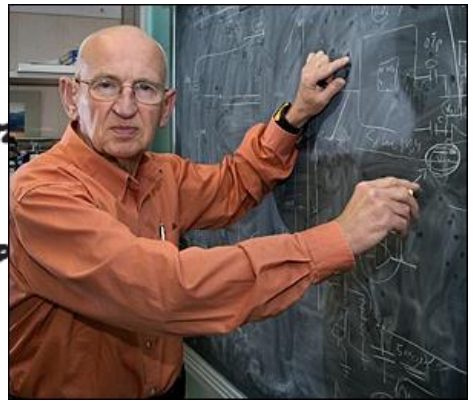
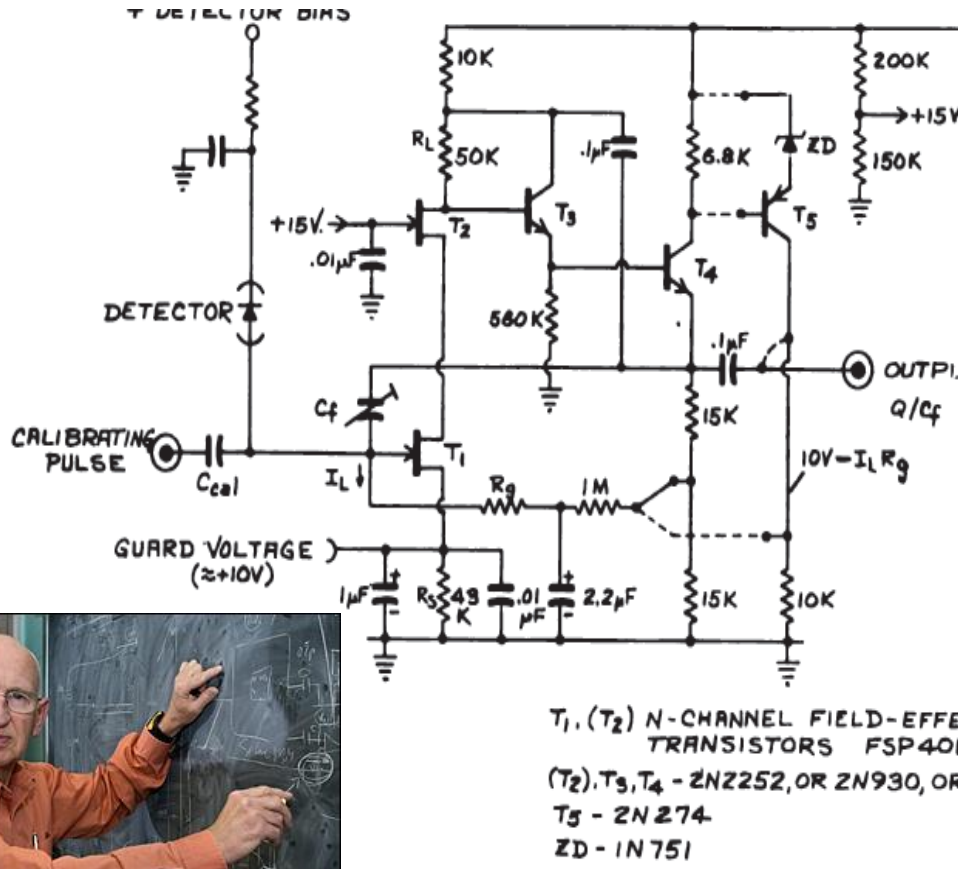
New developments in charge preamps (1963)







Radeka's preamp (Monterrey 63)

Electronically cooled resistors [TNS 73]

SIGNAL, NOISE AND RESOLUTION IN POSITION-SENSITIVE DETECTORS*

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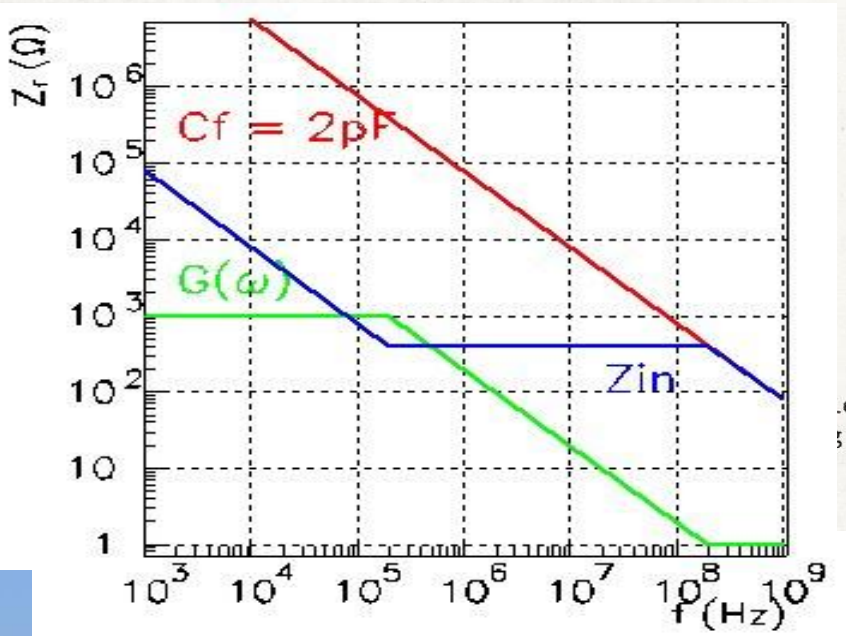
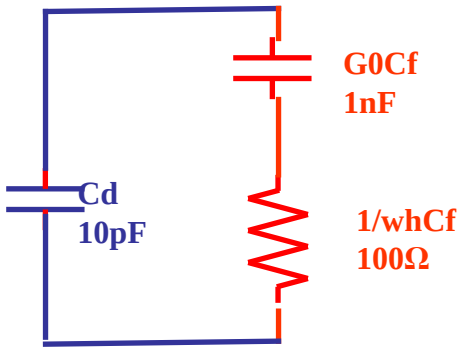
ABSTRACT

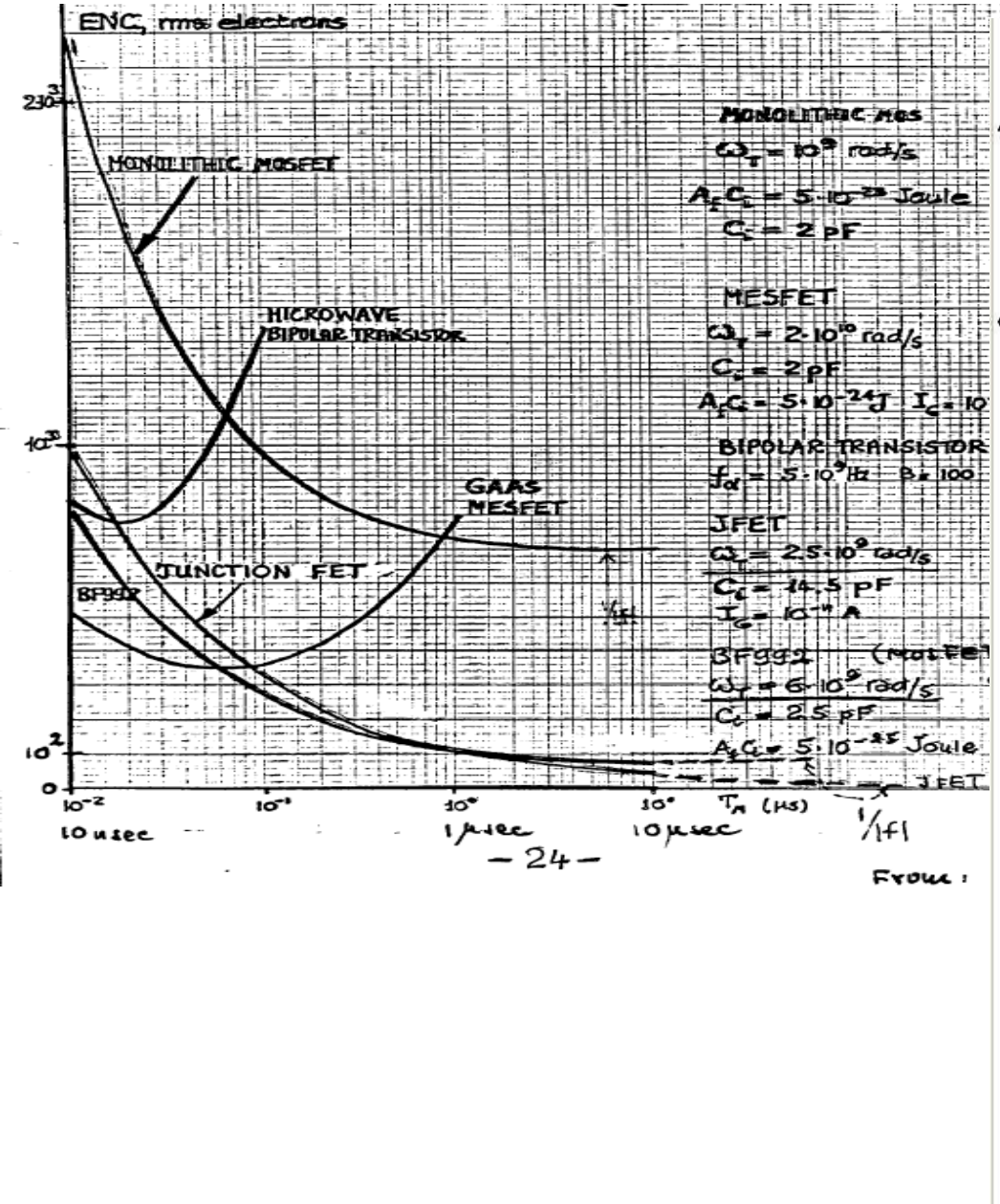
An analysis is presented of signal, noise and position resolution relations for some of the most interesting position-sensing methods. "Electronic cooling" of delay line terminations is introduced in order to reduce noise in the position-sensing with delay lines. A new method for terminating transmission lines and for "noiseless" damping which employs a capacitance in feedback is presented. It is shown that the position resolution for the charge division method with resistive electrodes is determined only by the electrode capacitance and not by the electrode resistance, if optimum filtering is used.

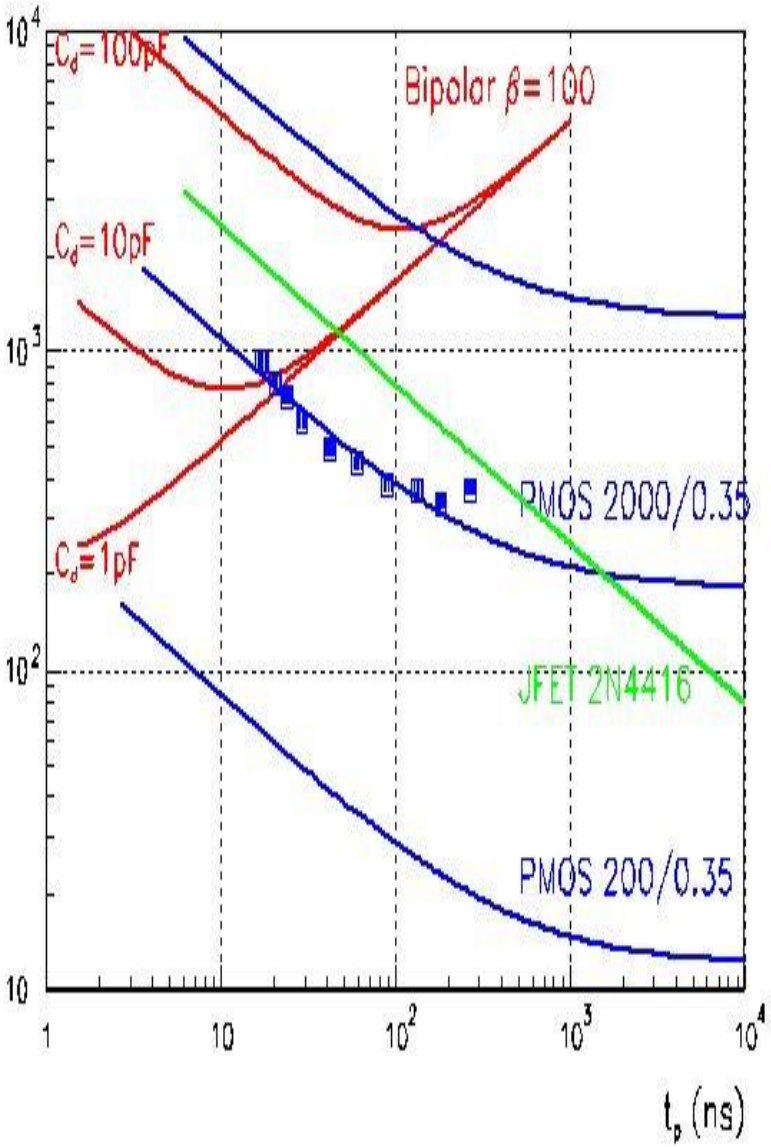


$$Zin = 1/j\omega\, G_0 C_F + 1/\, G_0 \omega_0\, C_F$$



ENC for various technologies

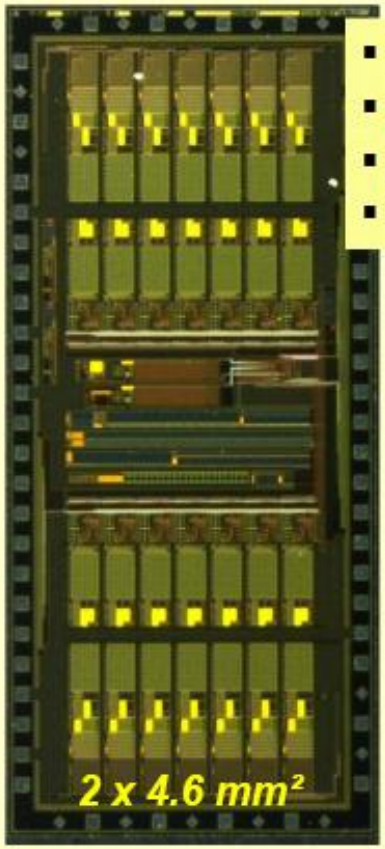




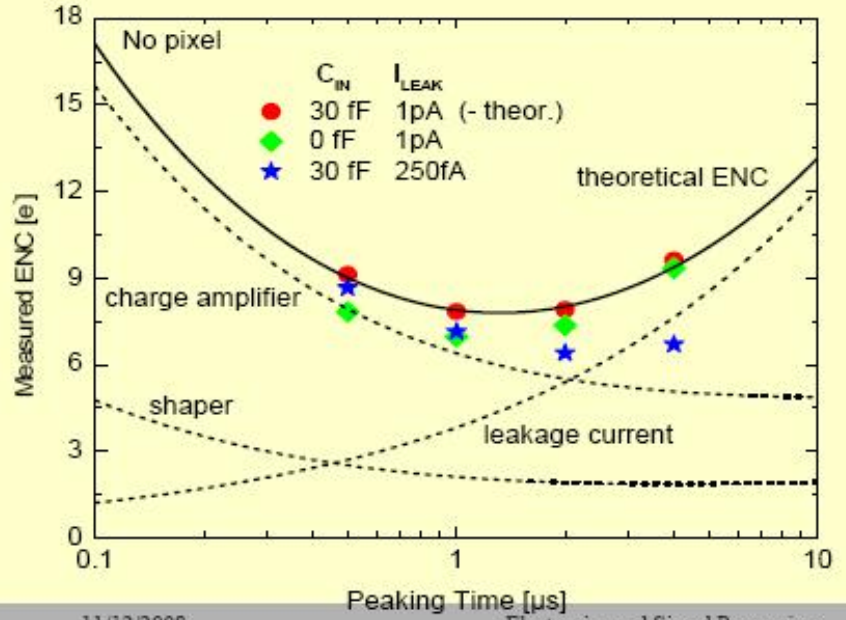
Ultra-Low Noise ASIC High Resolution X-Ray Spectroscopy

Collaboration with NASA at Moon Elemental Mapping

16 mm² Semiconductor Drift Pixels, 500 cm²



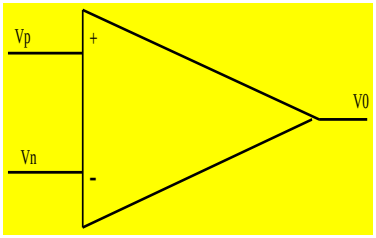
- 14 channels, 1.2 mW/channel
- sub-10 electrons resolution
- peak detection and sparse readout
- 30,000 transistors, dev. time: 15 months



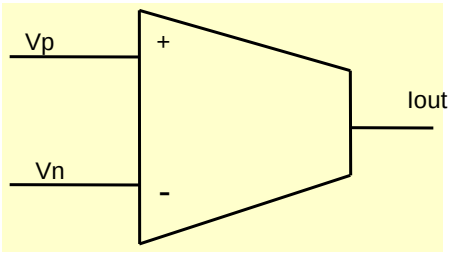
G. De Geronimo et al., NSS (2007)

Amplifiers : a large zoo

- Voltage feedback operationnal amplifier (VFOA)
- Voltage amplifiers, RF amplifiers (VA,LNA)
- Current feedback operationnal amplifiers (CFOA)
- Current conveyors (CCI, CCII +/-)
- Current (pre)amplifiers (ISA,PAI)
- Charge (pre)amplifiers (CPA,CSA,PAC)
- Transconductance amplifiers (OTA)
- Transimpedance amplifiers (TZA,OTZ)

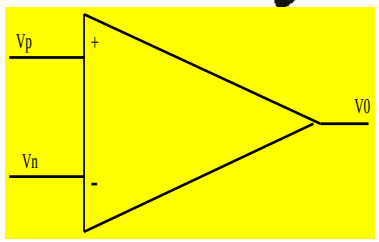


- Mixing up open loop (OL) and closed loop (CL) configurations !

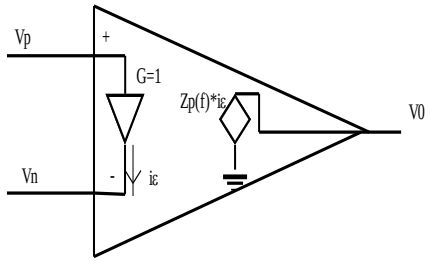


Only 4 open-loop configurations

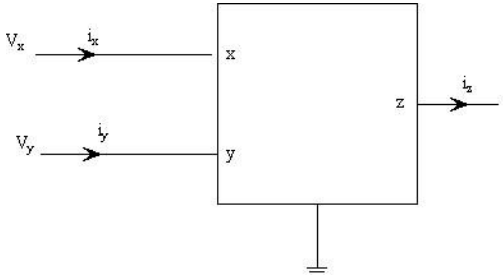
- Voltage operationnal amplifiers (OA, VFOA)
  - Vout = G(ω) Vin diff
  - Zin+ = Zin- = ∞ Zout = 0



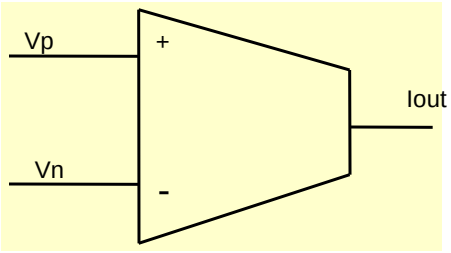
- Transimpedance operationnal amplifier (CFOA !)
  - Vout = Z(ω) iin
  - Zin- = 0 Zout = 0



- Current conveyor (CCI,CCII)
  - Iout = G(ω) Iin
  - Zin = 0 Zout = ∞

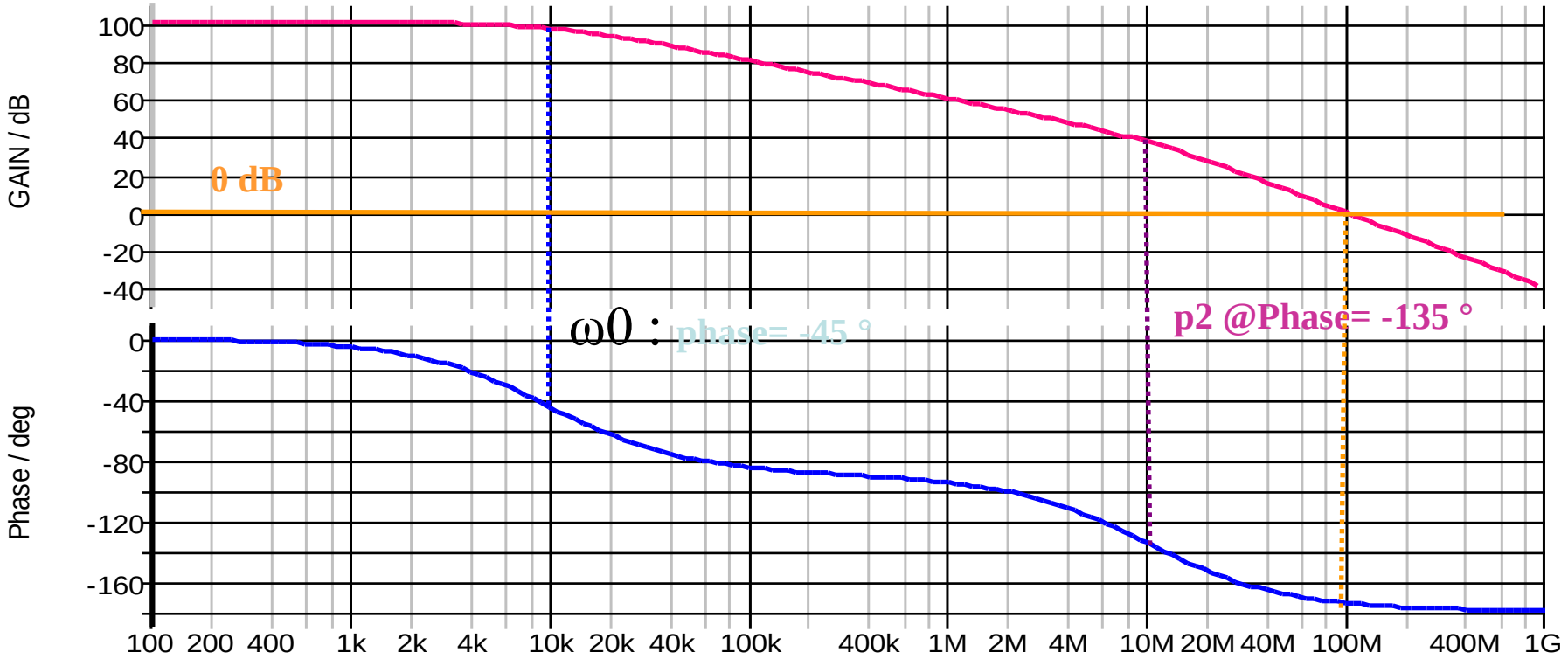


- Transconductance amplifier (OTA)
  - Iout = Gm(ω) Vin diff
  - Zin+ = Zin- = ∞ Zout = ∞



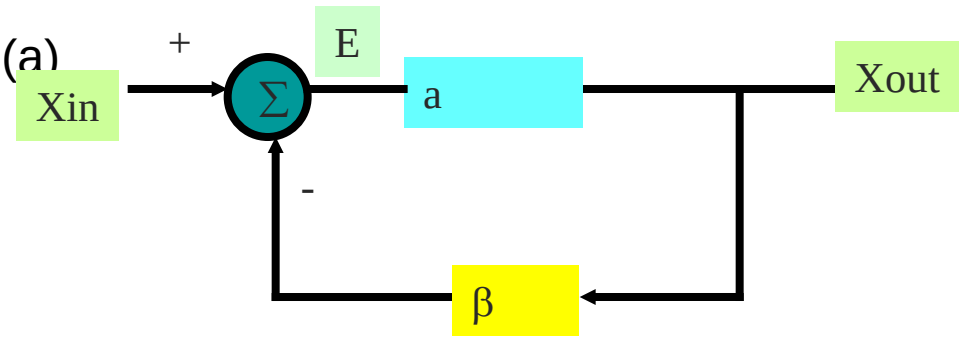
Open loop gain variation with frequency

- Define exactly what is « gain » vout/vin, vout/iin…
- « Gain » varies with frequency : $G(j\omega) = G_0/(1 + j\ \omega/\omega_0)$
  - **G_0** low frequency gain
  - **ω_0** dominant pole
  - **$\omega_C = G_0\ \omega_0$** Gain-Bandwidth product (sometimes referred to as unity gain frequency)

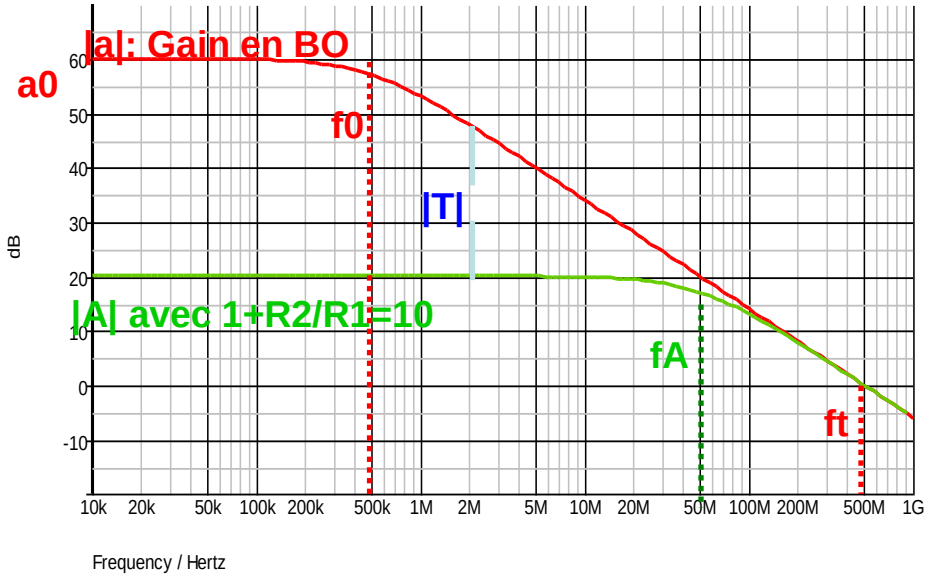


Feedback : an essential tool

- Improves gain performance
  - Less sensitivity to open loop gain (a)
  - Better linearity
- Essential in low power design
- Potentially unstable
- Feedback constant : β = E/Xout
- Open loop gain : a = Xout/E
- Closed loop gain : Xout/Xin -> 1/β
- Loop gain : T = 1/aβ

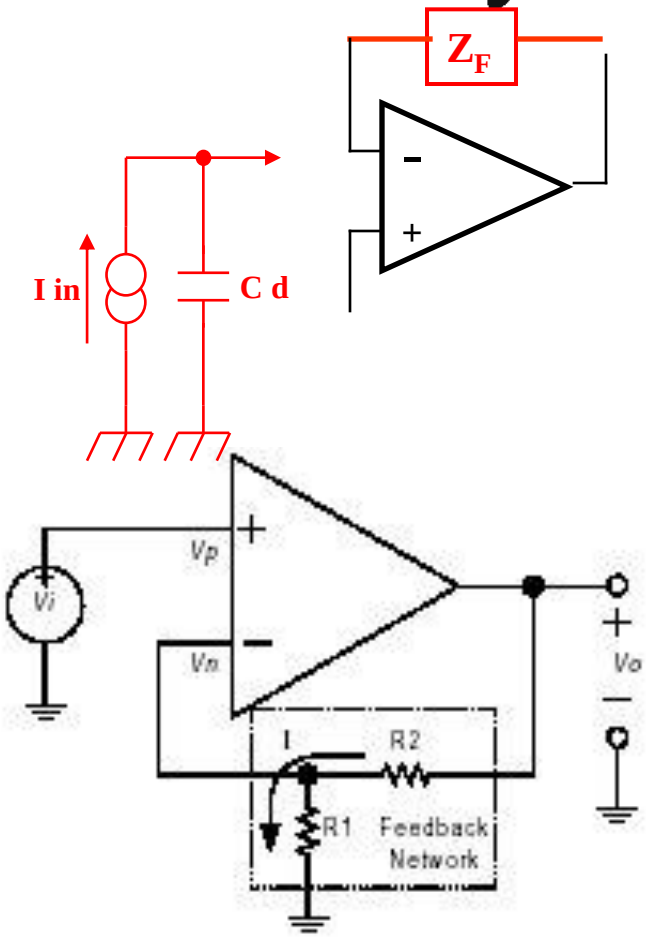


$$\frac{Xout}{Xin} = \frac{a}{1 + a\beta} = \frac{1/\beta}{1 + 1/a\beta}$$



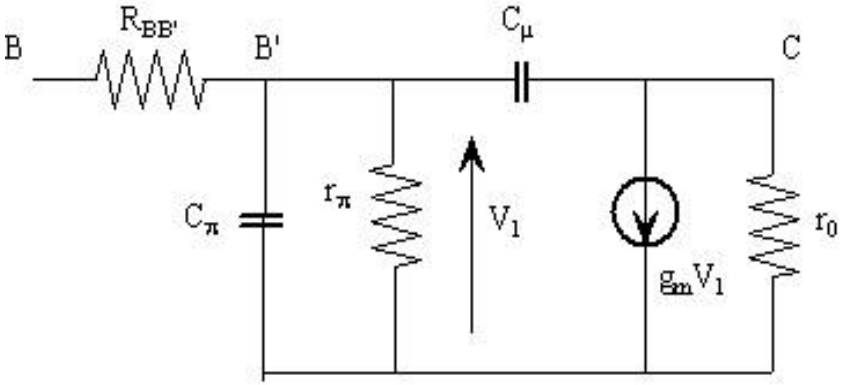
Only 4 feedback configurations

- Shunt-shunt = transimpedance
  - Small Zin (= Zin(OL)/T) -> current input
  - small Zout (= Zout(OL)/T) -> voltage output
  - De-sensitizes transimpedance = 1/β = Zf
- Series-shunt
  - Large Zin (= Zin(OL)*T) -> voltage input
  - Small Zout (= Zout(OL)/T) -> voltage output
  - Optimizes voltage gain (= 1/β)
- Shunt series
  - Small Zin (= Zin(OL)/T) -> current input
  - Large Zout (= Zout(OL)*T) -> current output
  - Current conveyor
- Series-series
  - Large Zin (= Zin(OL)*T) -> voltage input
  - Large Zout (= Zout(OL)*T) -> current output
  - Transconductance
  - Ex : common emitter with emitter degeneration



Summary of transistor level design

- Performant design is at transistor level

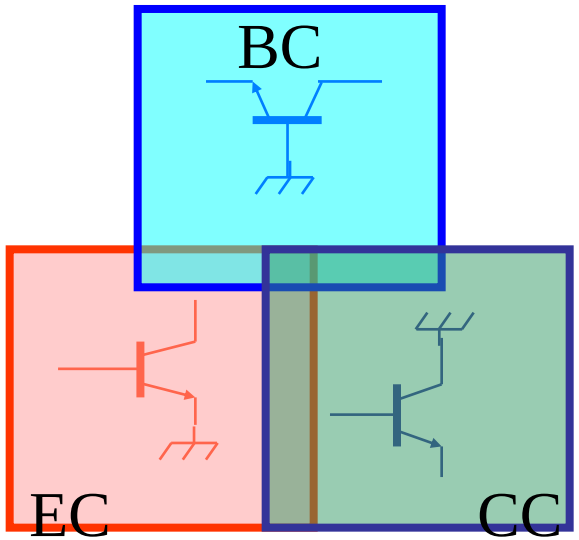


High frequency hybrid model of bipolar

- Simple models
  - hybrid π model
  - Similar for bipolar and MOS
  - Essential for design

- **Three basic configurations**
  - Common emitter (CE) = V to I (transconductance)
  - Common collector (CC) = V to V (voltage buffer)
  - Common base (BC) = I to I (current conveyor)

- Numerous « composites »
  - Darlington, Paraphase, Cascode, Mirrors…



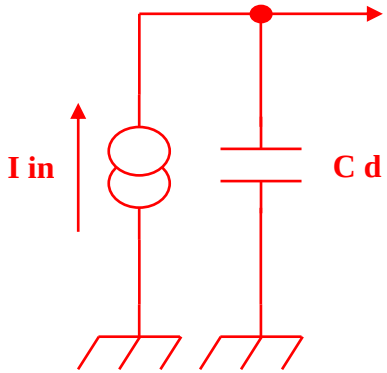
The *Art* of electronics design

Detector modelization

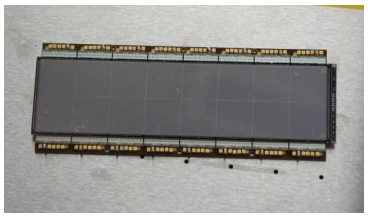
- Detector = capacitance Cd
  - Pixels : 0.1-10 pF
  - PMs : 3-30pF
  - Ionization chambers 10-1000 pF
  - Sometimes effect of transmission line

- Signal : current source
  - Pixels : ~100e-/µm
  - PMs : 1 photoelectron -> 10^5-10^7 e-
  - Modelized as an impulse (Dirac) : $i(t)=Q_0\delta(t)$

- Missing :
  - High Voltage bias
  - Connections, grounding
  - Neighbours
  - Calibration…



Detector modeilization



CMS pixel module

ATLAS LAr calorimeter

Signal & Source modelization

Vacuum Photomultipliers

G = 10^5 – 10^7

Cd ~ 10 pF

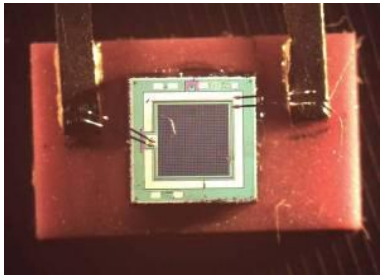
L ~ 10 nH

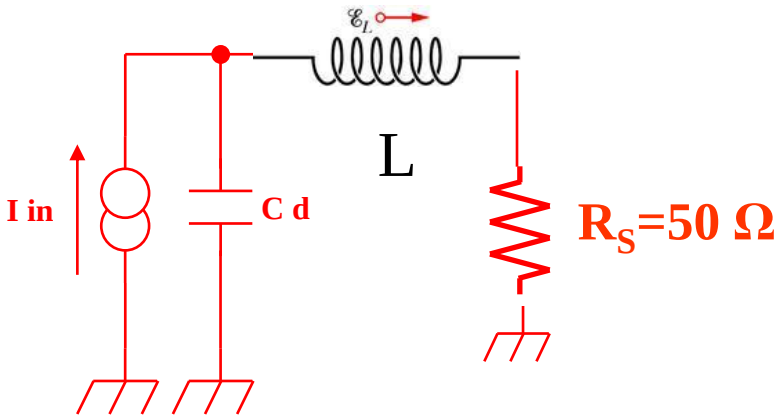
Silicon Photomultipliers

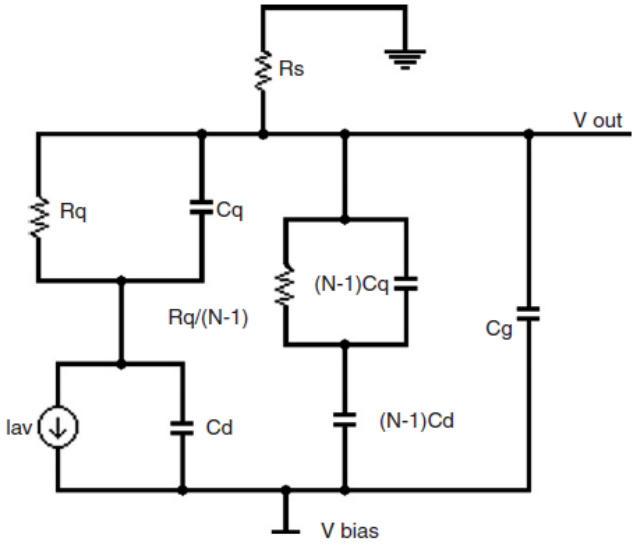
G = 10^5 – 10^7

C = 10 - 400 pF

L = 1 – 10 nH

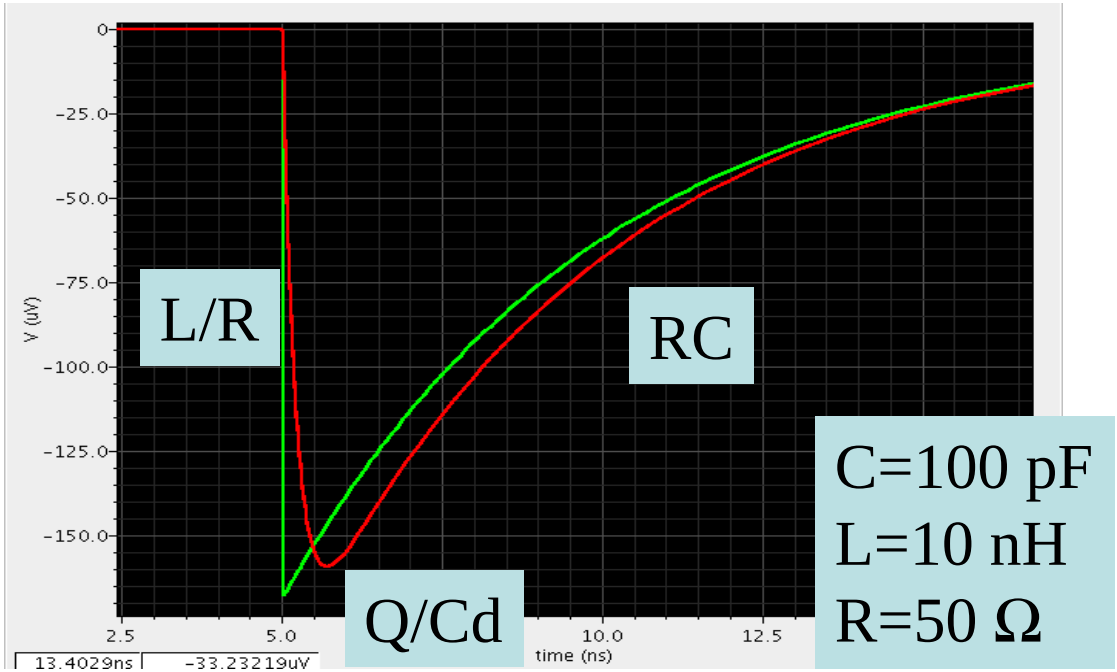


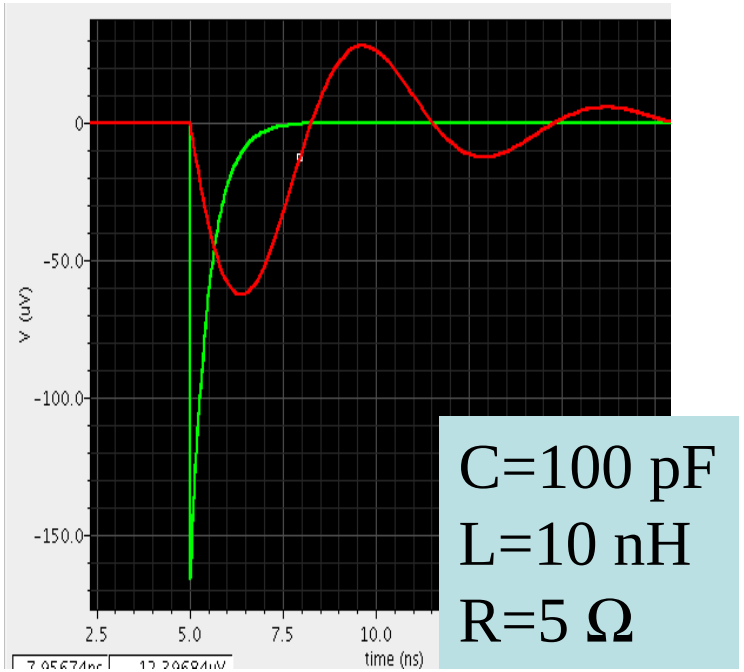




Examples of pulse shapes

- Short pulse : Q=16 fC, Cd=100 pF, L=0-10 nH, RL=5-50 Ω
- Smaller signals with SiPM (large Cd) ~ mV/p.e.
- Sensitivity to parasitic inductance
- Choice of RL : decay time, stability
- Convolve with current shape… (here delta impulse)





Optimizing signal shape for timing

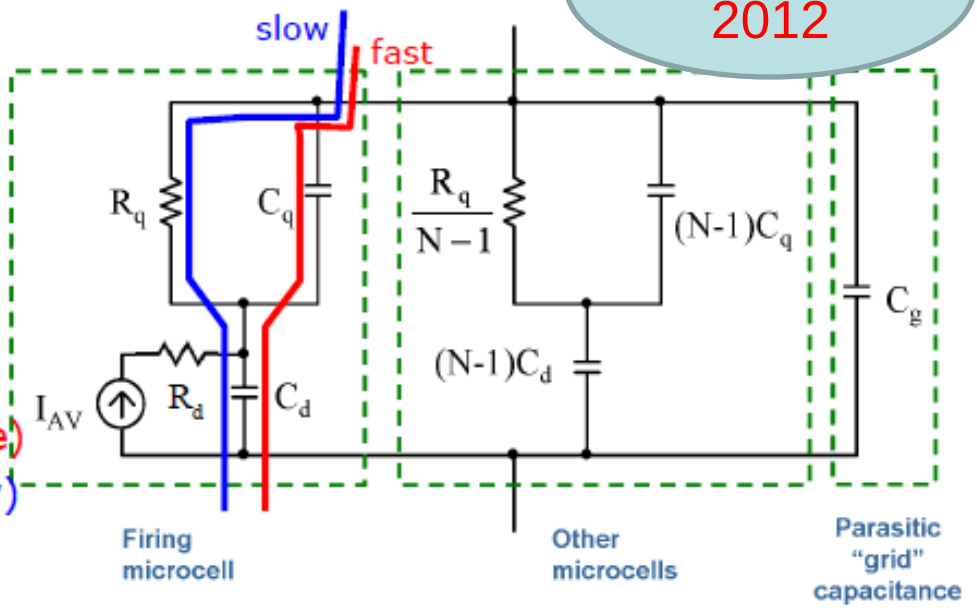
Collazuol 2012

Single cell model → $(R_d||C_d)+(R_q||C_q)$

SiPM + load → $(||Z_{cell})||C_{grid} + Z_{load}$

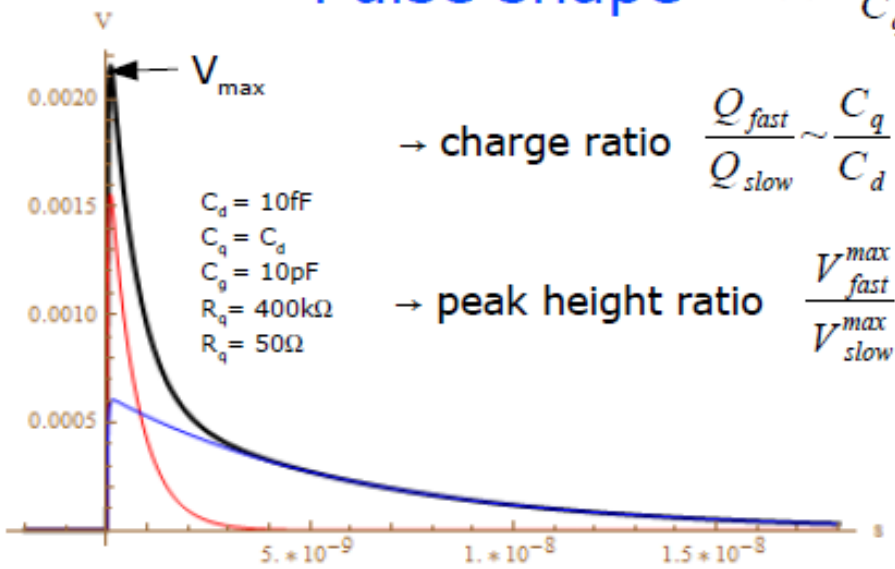
Signal = slow pulse ($\tau_{d\ (rise)}$, $\tau_{q\text{-}slow\ (fall)}$) +
+ fast pulse ($\tau_{d\ (rise)}$, $\tau_{q\text{-}fast\ (fall)}$)

- $\tau_{d\ (rise)} \sim R_d(C_q+C_d)$
- $\tau_{q\text{-}fast\ (fall)} = R_{load}\ C_{tot}$ (fast; parasitic spike)
- $\tau_{q\text{-}slow\ (fall)} = R_q\ (C_q+C_d)$ (slow; cell recovery)



Pulse shape

$$V(t) \simeq \frac{Q}{C_q+C_d}\left(\frac{C_q}{C_{tot}} e^{\frac{-t}{\tau_{FAST}}} + \frac{R_{load}}{R_q}\frac{C_d}{C_q+C_d} e^{\frac{-t}{\tau_{SLOW}}}\right)$$



→ charge ratio $\frac{Q_{fast}}{Q_{slow}} \sim \frac{C_q}{C_d}$

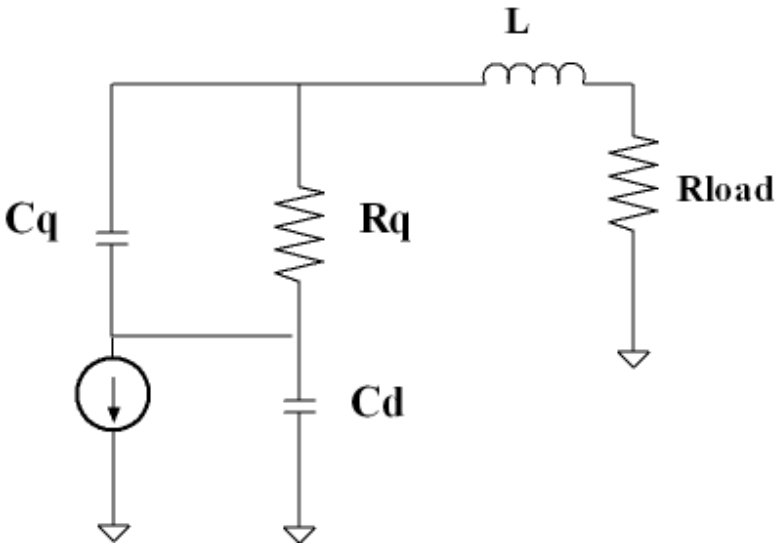
→ peak height ratio $\frac{V^{max}_{fast}}{V^{max}_{slow}} \sim \frac{C_q^2 R_q}{C_d C_{tot} R_{load}}$

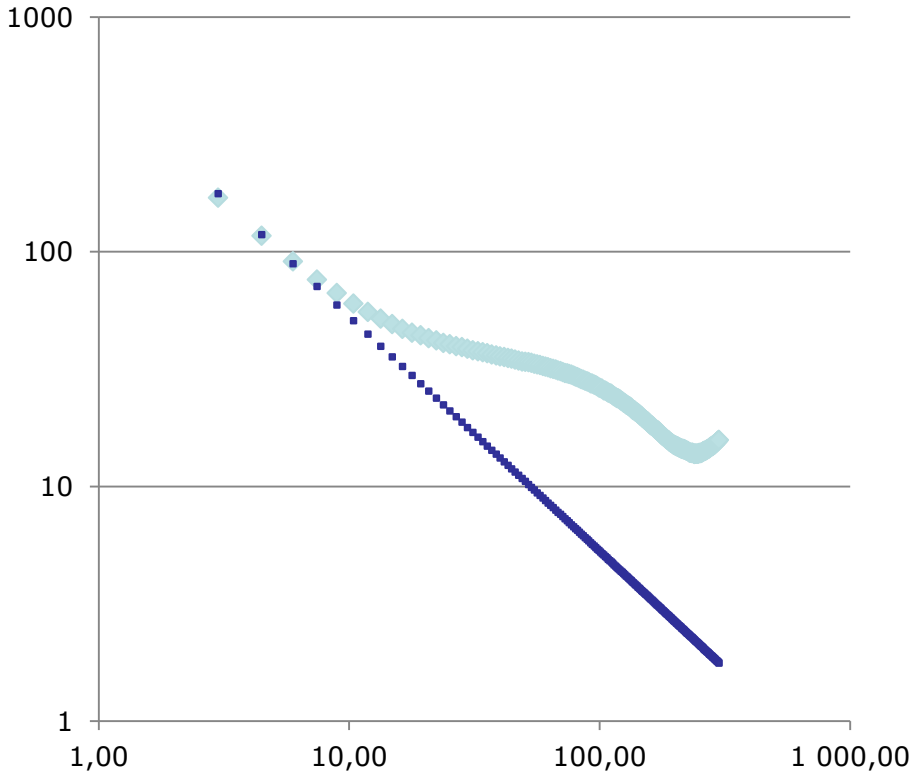
increasing with Rq and $1/R_{load}$ (and Cq of course)

Increasing C_q/C_d or/and R_q/R_{load}
→ spike enhancement
→ better timing

SiPM impedance and model

- RLC too simple, inaccurate at high frequency
- CdRqCqLR OK
  - May better explain HF noise behaviour





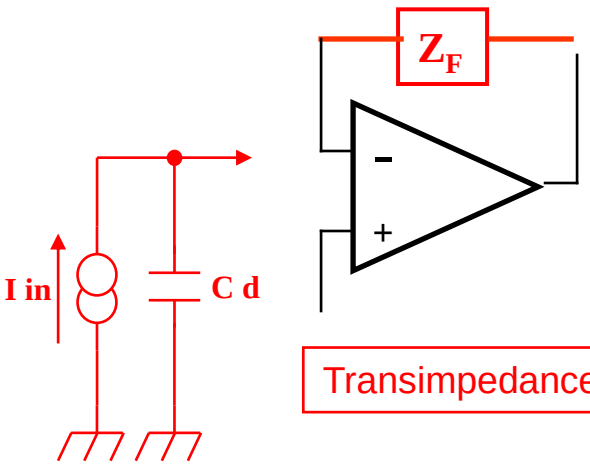
Measured impedance
MPPC HPK 3x3 mm
Line : C = 320 pF

Transimpedance configuration

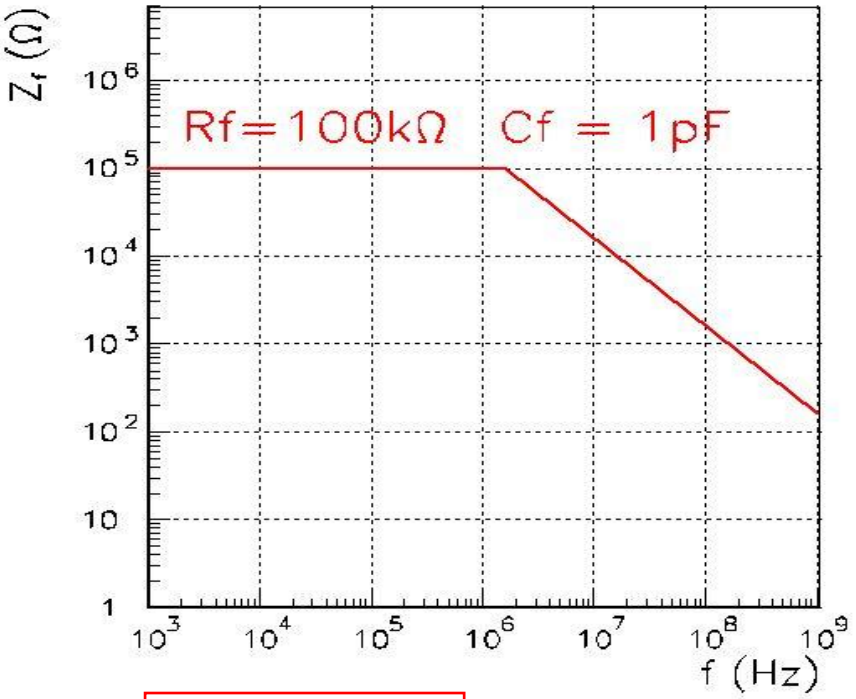
- Transfer function
  - Using a VFOA with gain G
    - $V_{out} - v_{in} = - Z_f\, i_f$
    - $V_{in} = Z_d\,(i_{in} - i_f) = - v_{out}/G$
  - $V_{out}(\omega)/i_{in}(\omega) = - Z_f / (1 + Z_f /GZ_d)$

- $Zf = Rf / (1 + j\omega\, RfCf)$
  - At $f << 1/2\pi RfCf$:
    $V_{out}(\omega)/i_{in}(\omega) = - R_f$
    current preamp
  - At $f << 1/2\pi RfCf$:
    $V_{out}(\omega)/i_{in}(\omega) = - 1/j\omega C_f$
    charge preamp

- Ballistic defict with charge preamp
  - Effect of finite gain : G_0
  - Output voltage «only» Q C_d/G_0C_f



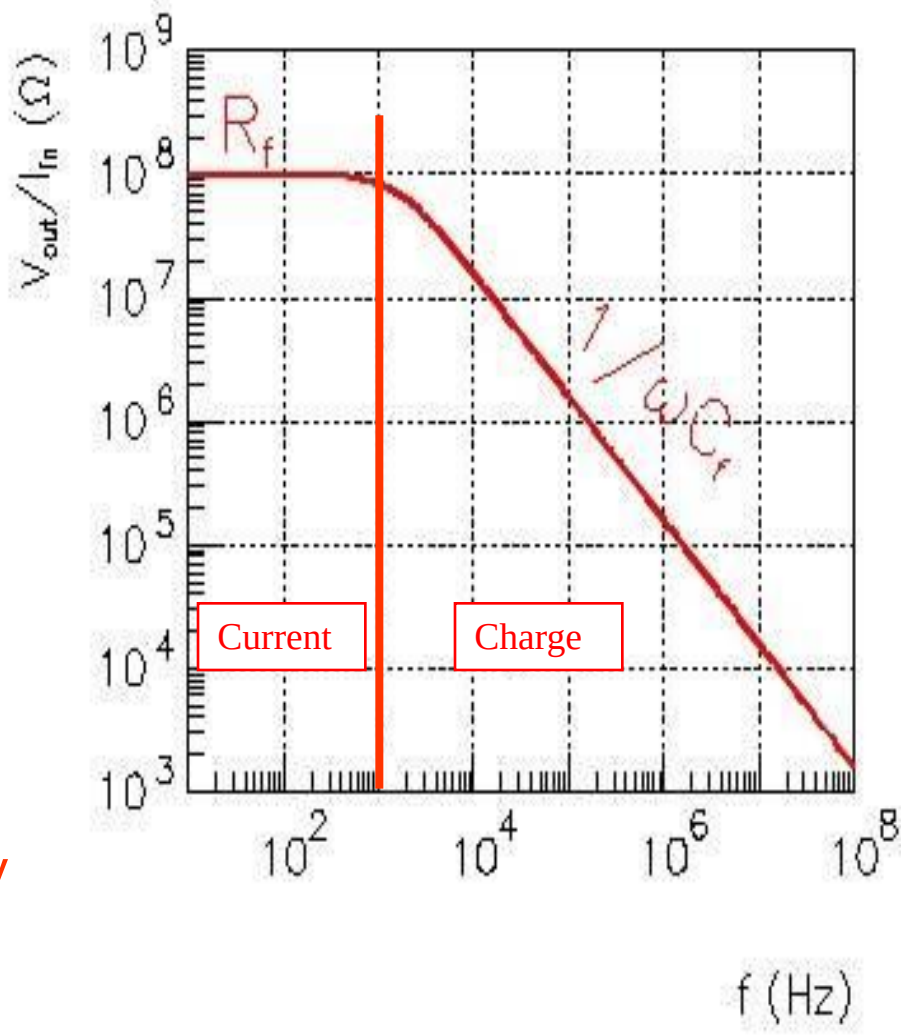
Transimpedance amplifier



Transfer function

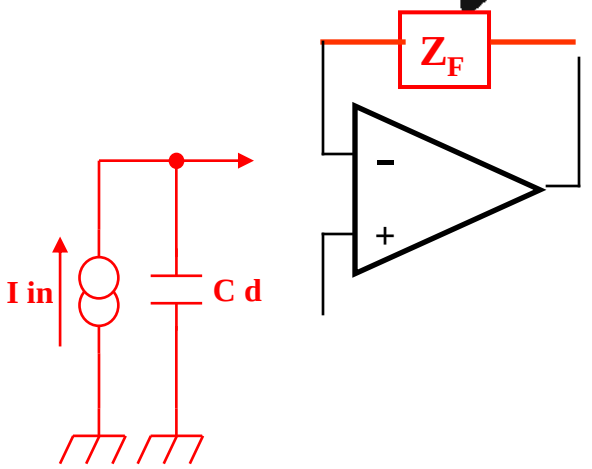
Charge vs Current preamps

- Charge preamps
  - Best noise performance
  - Best with short signals
  - Best with small capacitance
- Current preamps
  - Best for long signals
  - Best for high counting rate
  - Significant parallel noise
- Charge preamps are not slow, they are long
- Current preamps are not faster, they are shorter (but easily unstable)



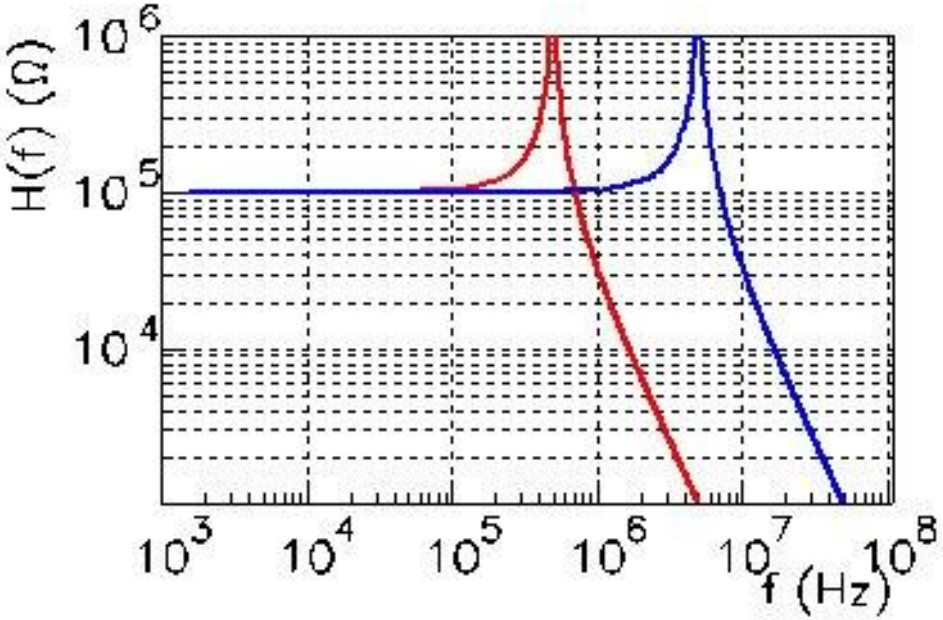
Transimpedance amplifier (ctd)

- Transimpedance :
  - $V_{out}(\omega)/i_{in}(\omega) = - Z_f / (1 + Z_f / G\ Z_d)$
  - $Z_f = R_f / (1 + j\omega\ R_f C_f)$
  - $G(\omega) = G_0/(1 + j\ \omega/\omega_0)$
  - $H \sim - R_f / (1 + j\omega\ R_f C_f/G_0 - \omega^2\ R_f C_d\ /G_0\omega_0)$



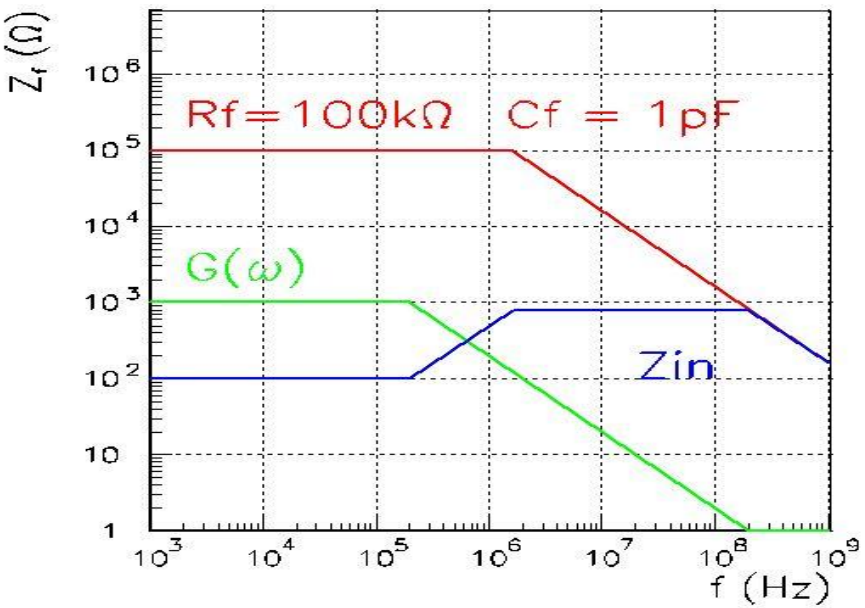
- 2^{nd} order system, easily oscillatory
  - Quality factor : $Q = 1/Cf\ \sqrt{(C_d/R_f\ G_0\omega_0)}$
  - $Q > 1/2$ -> ringing
  - **Damping : Q=1/2**

    => $C_f=2\ \sqrt{(C_d/R_f\ G_0\omega_0)}$
  - BW limitation at RfCf

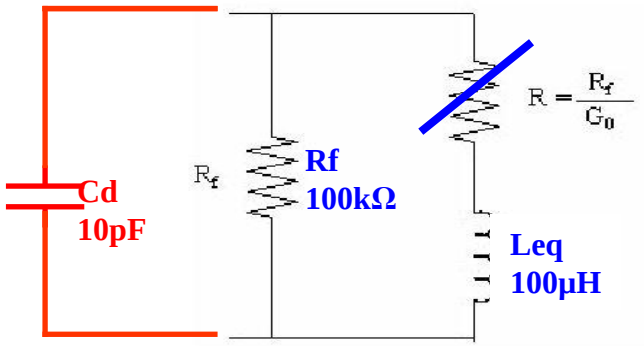


Input impedance

- Input impedance
  - Zin = Zf / G+1
  - Zin->0 virtual ground
  - Minimizes sensitivity to detector impedance
  - Minimizes crosstalk
- Equivalent model
  - $G(\omega) = G_0/(1 + j\ \omega/\omega_0)$
- Terms due to Cf
  - $Zin = 1/j\omega\ G_0C_f + 1/\ G_0\omega_0\ C_f$
  - Virtual resistance : $Req = 1/\ G_0\omega_0\ C_f$
- Terms due to Rf
  - $Zin = R_f/\ G_0 + j\ \omega\ R_f/\ G_0\omega_0$
  - Virtual inductance : $Leq = R_f/\ G_0\omega_0$
- Possible oscillatory behaviour with capacitive source



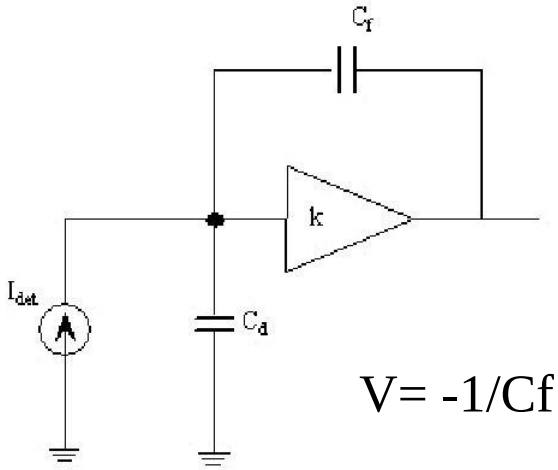
Input impedance or TZA



Equivalent circuit at the input

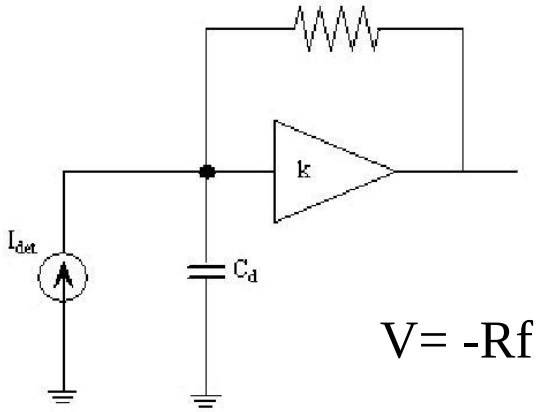
Charge and Current preamps

- Charge preamp
- Capacitive feedback Cf
- Vout/Iin = - 1/jωCf
- Perfect integrator : vout=-Q/Cf∫
- Difficult to accomodate large SiPM signals (200 pC)
- Lowest noise configuration
- Need Rf to empty Cf



$$V = -1/Cf \int i(t)dt$$

- Current preamp
- Resistive feedback Rf
- Vout/Iin = - Rf
- Keeps signal shape
- Need Cf for stability



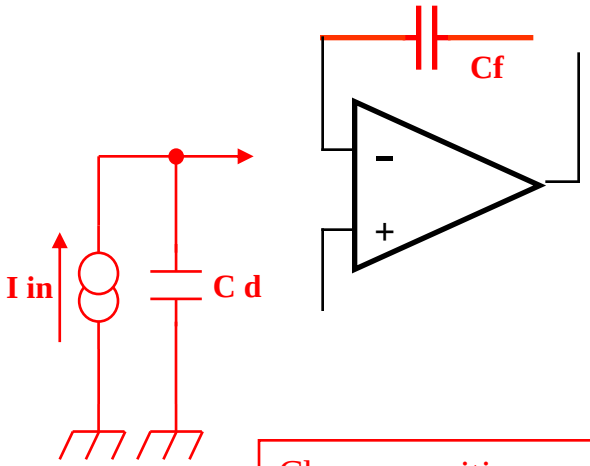
$$V = -Rf\ i(t)$$

Ideal charge preamplifier

- ideal opamp in transimpedance
  - Shunt-shunt feedback
  - transimpedance : v_{out}/i_{in}
  - Vin-=0 =>$V_{out}(\omega)/i_{in}(\omega) = - Z_f = - 1/j\omega C_f$
  - Integrator : $v_{out}(t) = -1/C_f \int i_{in}(t)dt$

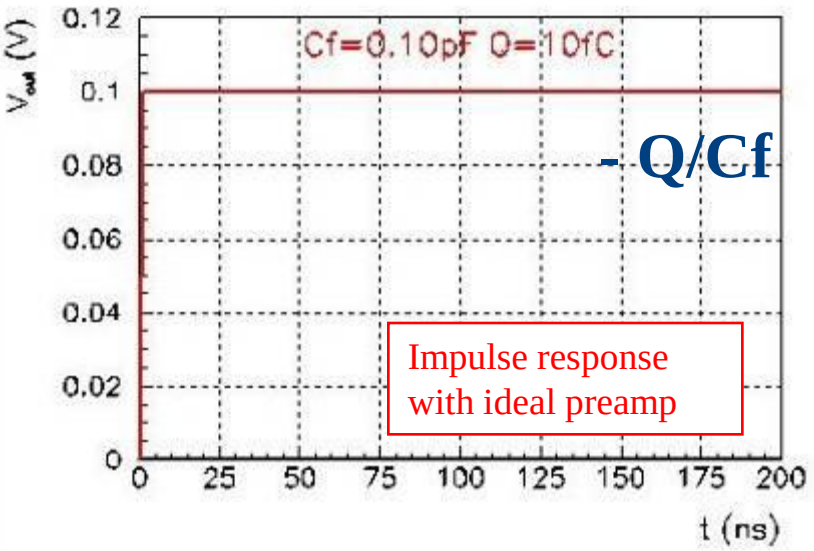
$$v_{out}(t) = - Q/C_f$$

  - « Gain » : $1/C_f$: 0.1 pF -> 10 mV/fC
  - C_f determined by maximum signal



Charge sensitive preamp

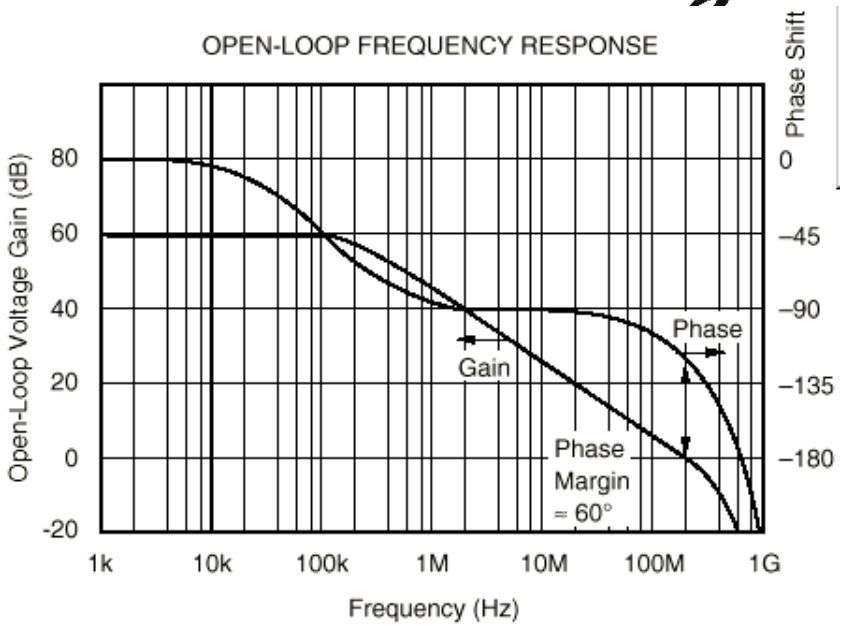
- Integration on Cf
  - Simple : V = - Q/C_f
  - Unsensitive to preamp capacitance C_{PA}
  - Turns a short signal into a long one
  - The front-end of 90% of particle physics
  - But always built with custom circuits…

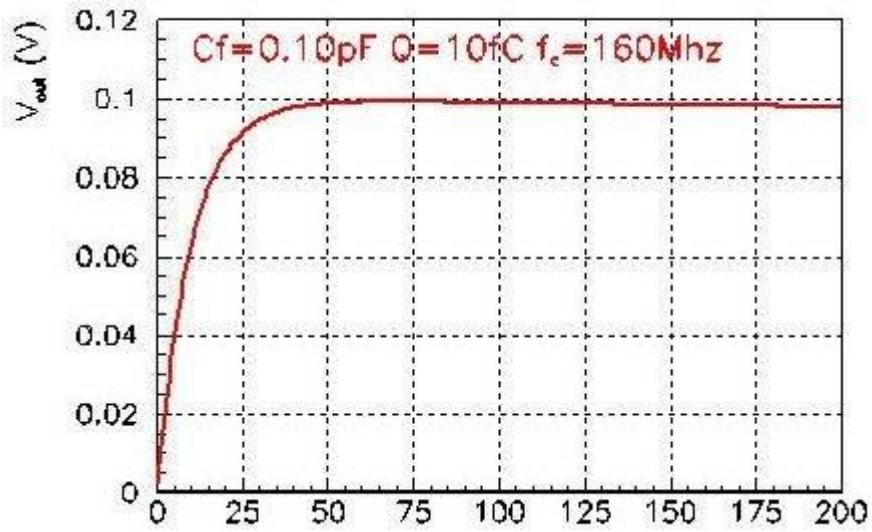


Impulse response with ideal preamp

Preamp speed

- Finite opamp gain
  - $V_{out}(\omega)/i_{in}(\omega) = - Z_f / (1 + C_d / G_0 C_f)$
  - Small signal loss in $C_d/G_0C_f << 1$ (ballis
- Finite opamp bandwidth
  - First order open-loop gain
  - $G(\omega) = G_0/(1 + j\ \omega/\omega_0)$
    - G_0 : low frequency gain
    - $G_0\omega_0$: gain bandwidth product
- Preamp risetime
  - Due to gain variation with ω
  - Time constant : τ *(tau)*
  - $\tau = C_d/G_0\omega_0C_f$
  - Rise-time : $t_{10\text{-}90\%} = 2.2\ \tau$
  - Rise-time optimised with $w_{C\ or}\ C_f$

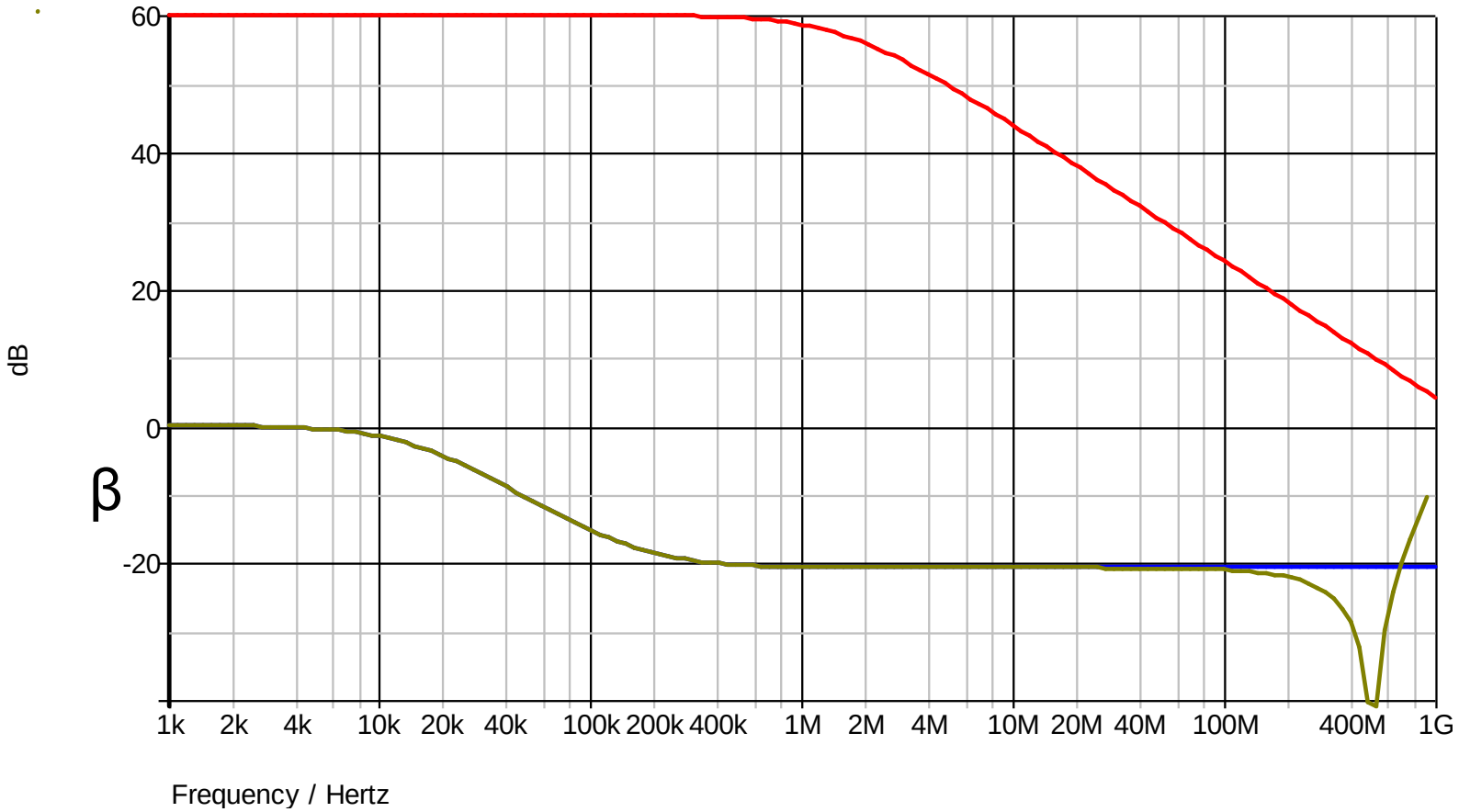




Impulse response with non-ideal preamp

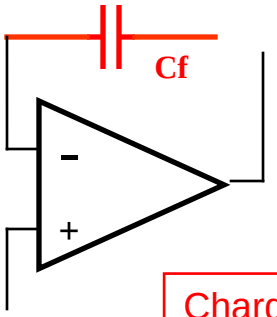
Preamp stability

- Calculating β = E/Xout = Zd/(Zd+Zf)

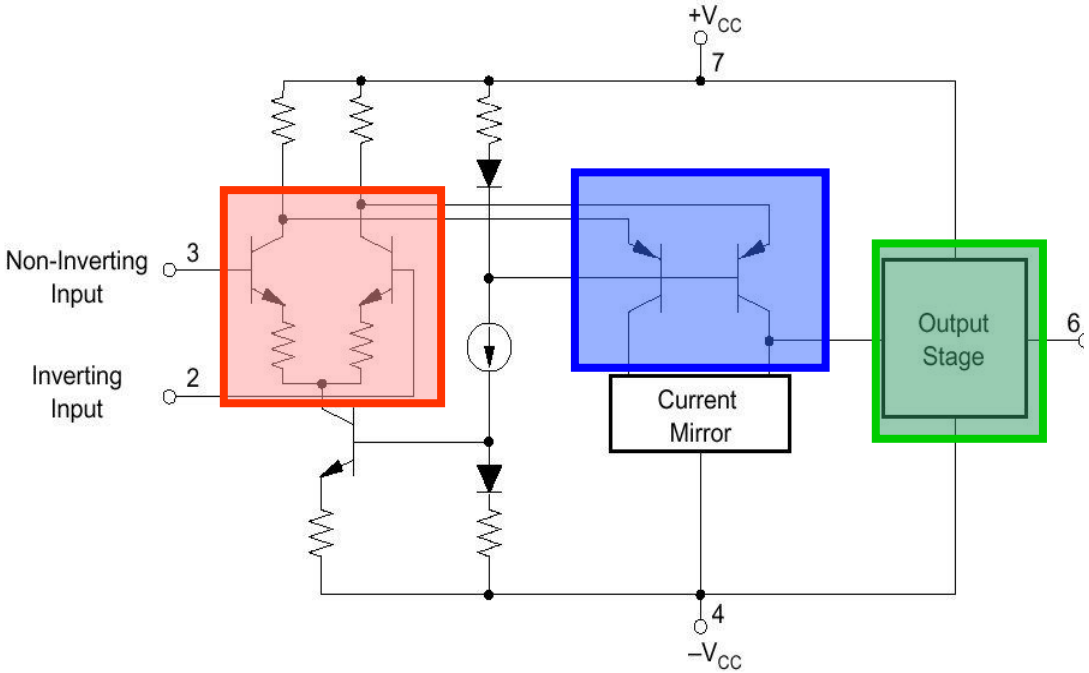


Designing a charge preamp…

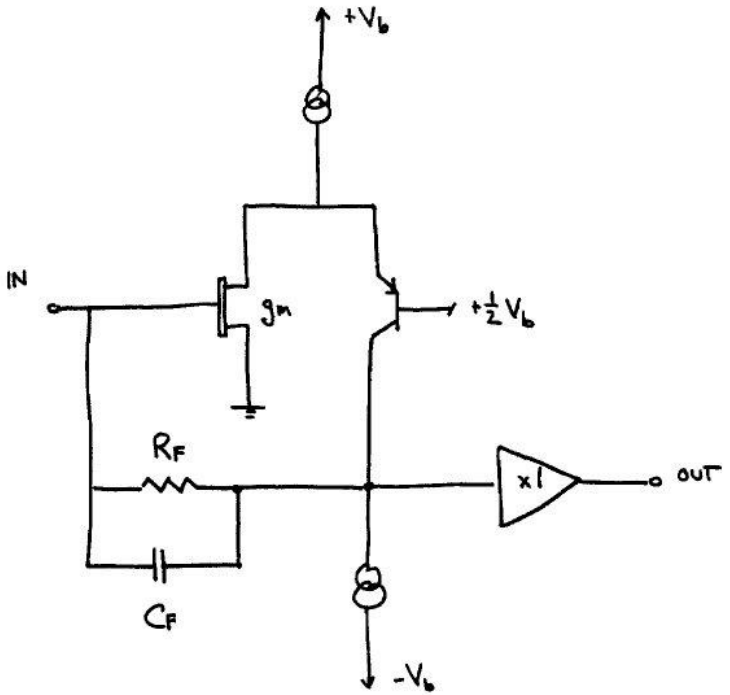
- From the schematic of principle
  - Using of a fast opamp (OP620)
  - Removing unnecessary components…
  - Similar to the traditionnal schematic «Radeka 68 »
  - Optimising transistors and currents



Charge preamp



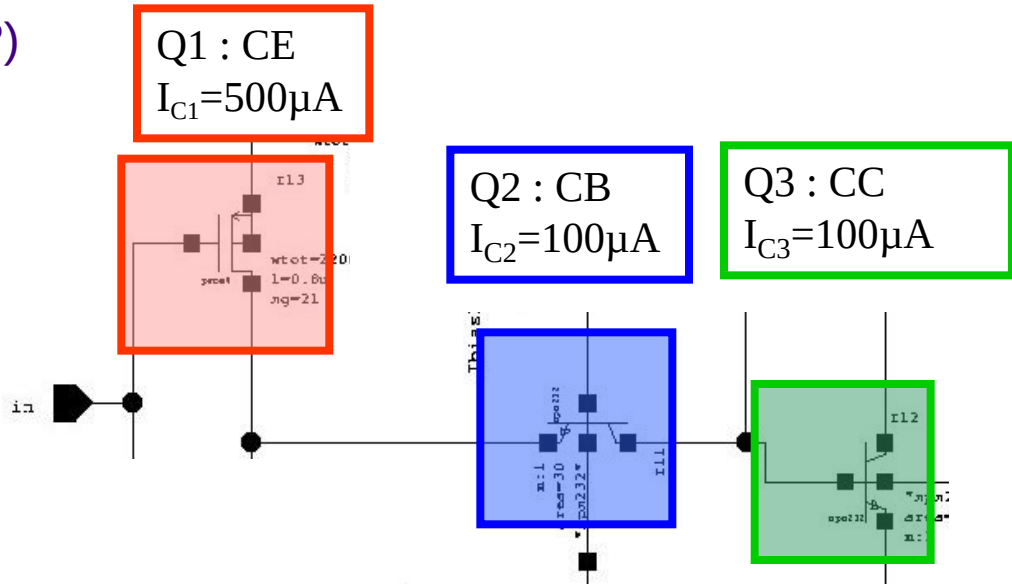
Schematic of a OP620 opamp ©BurrBrown



Charge preamp ©Radeka 68

Example : designing a charge preamp (2)

- Simplified schematic
- Optimising components
  - What transistors (PMOS, NPN ?)
  - What bias current ?
  - What transistor size ?
  - What is the noise contribution of each component ?
  - how to minimize it ?
  - What parameters determine the stability ?
  - Waht is the saturation behaviour
  - How vary signal and noise with input capacitance ?
  - How to maximise the output voltage swing ?
  - What is the sensitivity to power supplies, temperature…



Simplified schematic of charge preamp

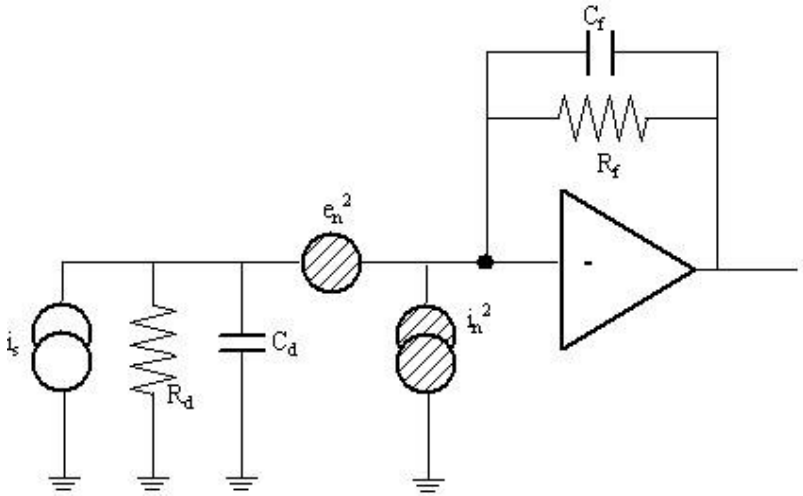
Noise in transimpedance amplifiers

- 2 noise generators at the input
  - Parallel noise : (i_n^2) (leakage)
  - Series nosie : (e_n^2) (preamp)

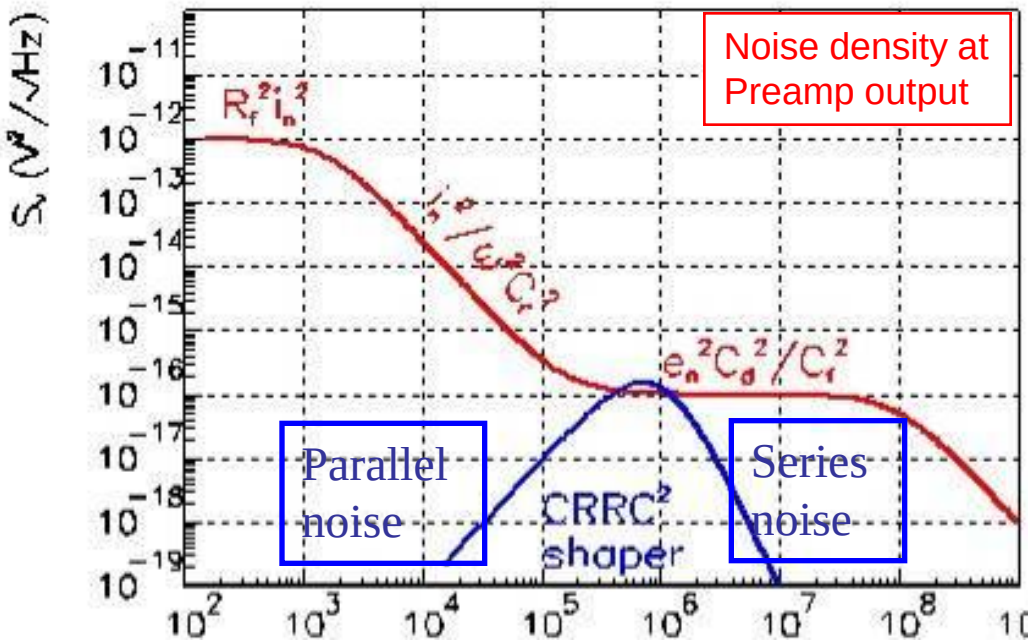
- Output noise spectral density :
  - $Sv(\omega) = (i_n^2 + e_n^2/|Z_d|^2) * |Z_f|^2$

- For charge preamps
  - $Sv(\omega) = i_n^2 /\omega^2 C_f^2 + e_n^2 C_d^2/C_f^2$
  - Parallel noise in $1/\omega^2$
  - Series noise is flat, with a « noise gain » of C_d/C_f

- *rms* noise V_n
  - $V_n^2 = \int Sv(\omega)\, d\omega/2\pi \rightarrow \infty$
  - Benefit of shaping…



Noise generators in charge preamp



Equivalent Noise Charge (ENC) after CRRC^n

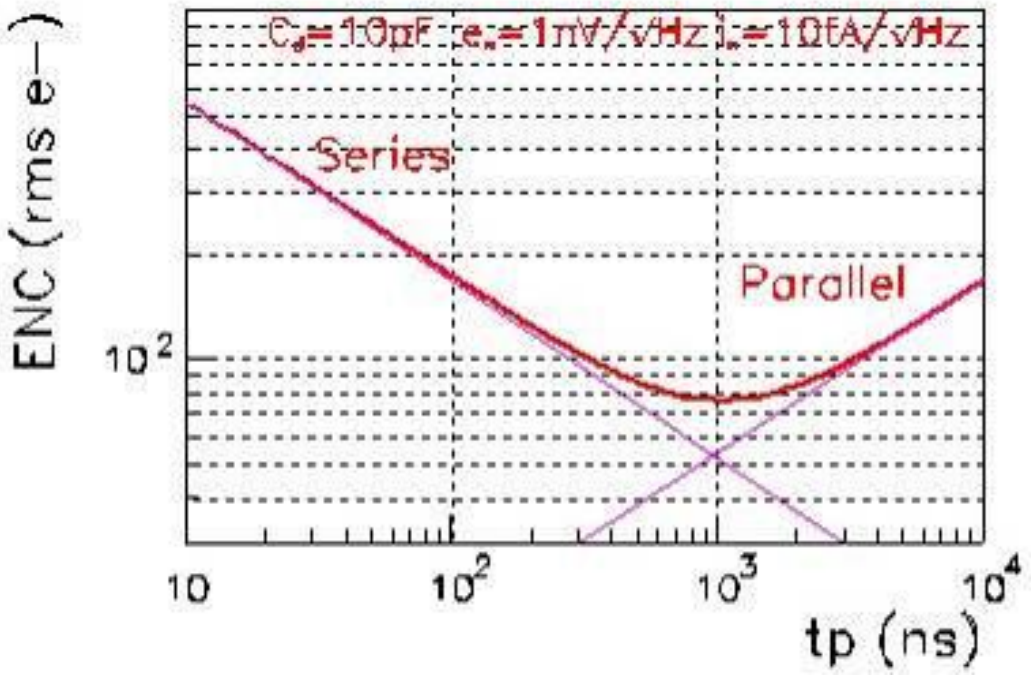
- A useful formula : **ENC (e- rms) after a CRRC^2 shaper :**

$$ENC = 174\ e_n C_{tot}/\sqrt{t_p}\ (\delta) \oplus 166\ i_n \sqrt{t_p}\ (\delta)$$

  - e_n in nV/ √Hz, i_n in pA/ √Hz are the preamp noise spectral densities
  - C_{tot} (in pF) is dominated by the detector (C_d) + input preamp capacitance (C_{PA})
  - t_p (in ns) is the shaper peaking time (5-100%)

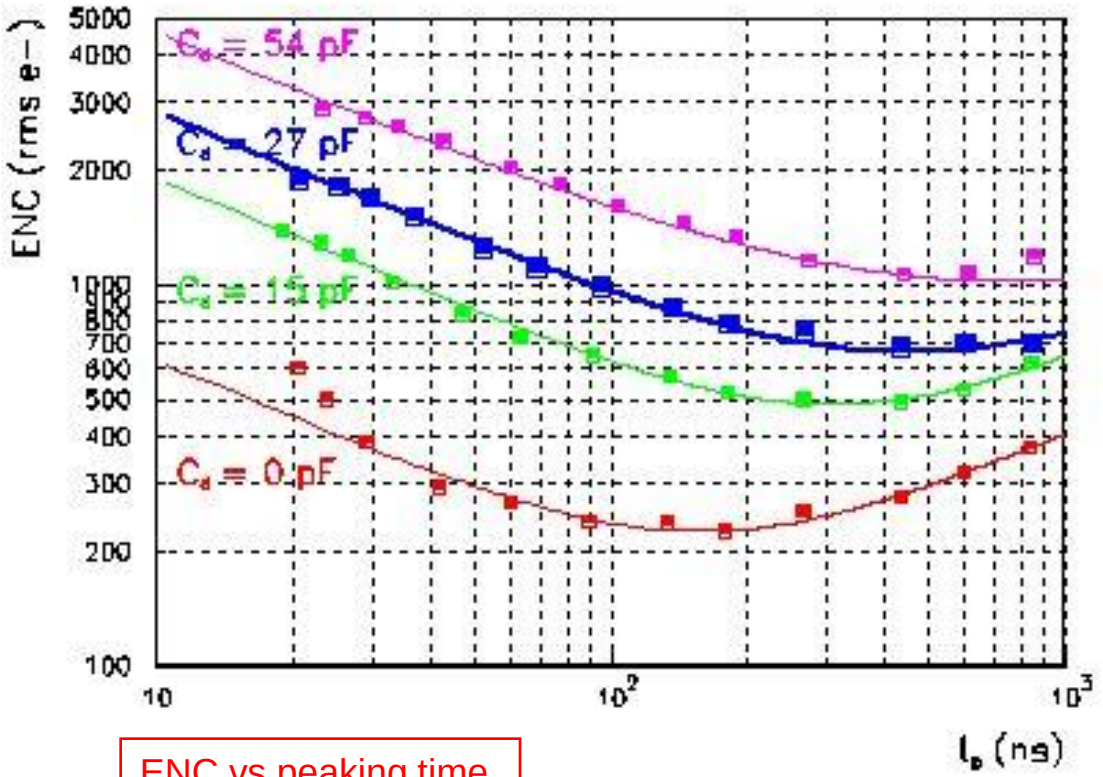
- **Noise minimization**
  - Minimize source capacitance
  - Operate at optimum shaping time
  - Preamp series noise (en) best with high trans-conductance (g_m) in input transistor

    => large current, optimal size

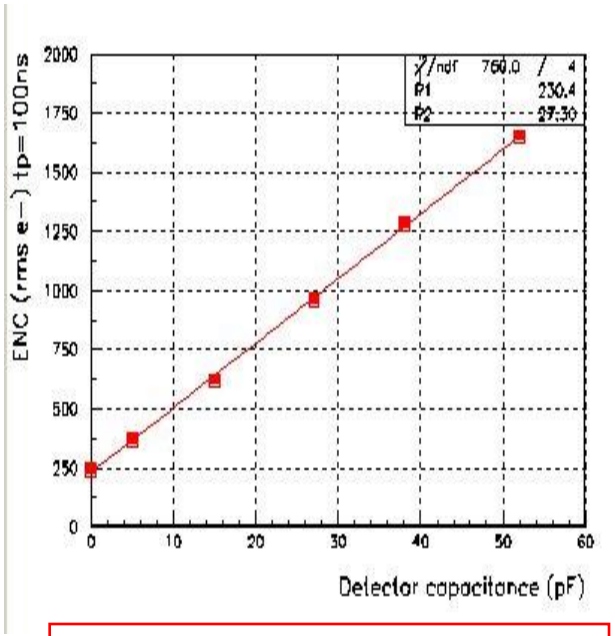


Example of ENC measurement

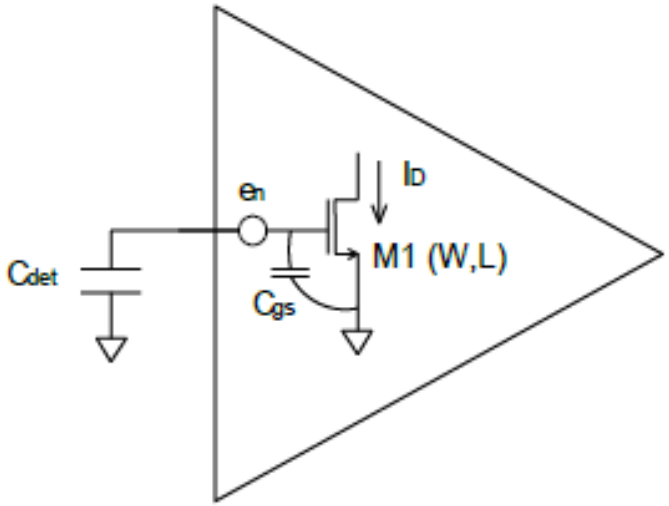
- 2000/0.35 PMOS 0.35µm SiGe Id=500 µA
  - Series : en = 1.4 nV/√Hz, C_{PA} = 7 pF
  - 1/f noise : 12 e-/pF
  - Parallel : in = 40 fA/√Hz



ENC vs peaking time



ENC vs Capacitance tp=100ns



$$ENC^2 = \left(C_{det} + C_{gs}\right)^2 \cdot \left(\frac{4kT\gamma}{g_m t_m} + \frac{K_F}{C_{gs}}\right)$$

white 1/f

Choose minimum L for best g_m/C_{gs} ratio

Increasing M1 width makes e_n smaller while C_{gs} gets larger

⇒ ***optimum width for M1 must exist***

1/f noise:

$$C_{gs,opt} = C_{det}$$

White -- two cases :

I. Fixed V_{gs} (fixed current density, fixed f_T)

$$g_m \propto C_{gs}$$

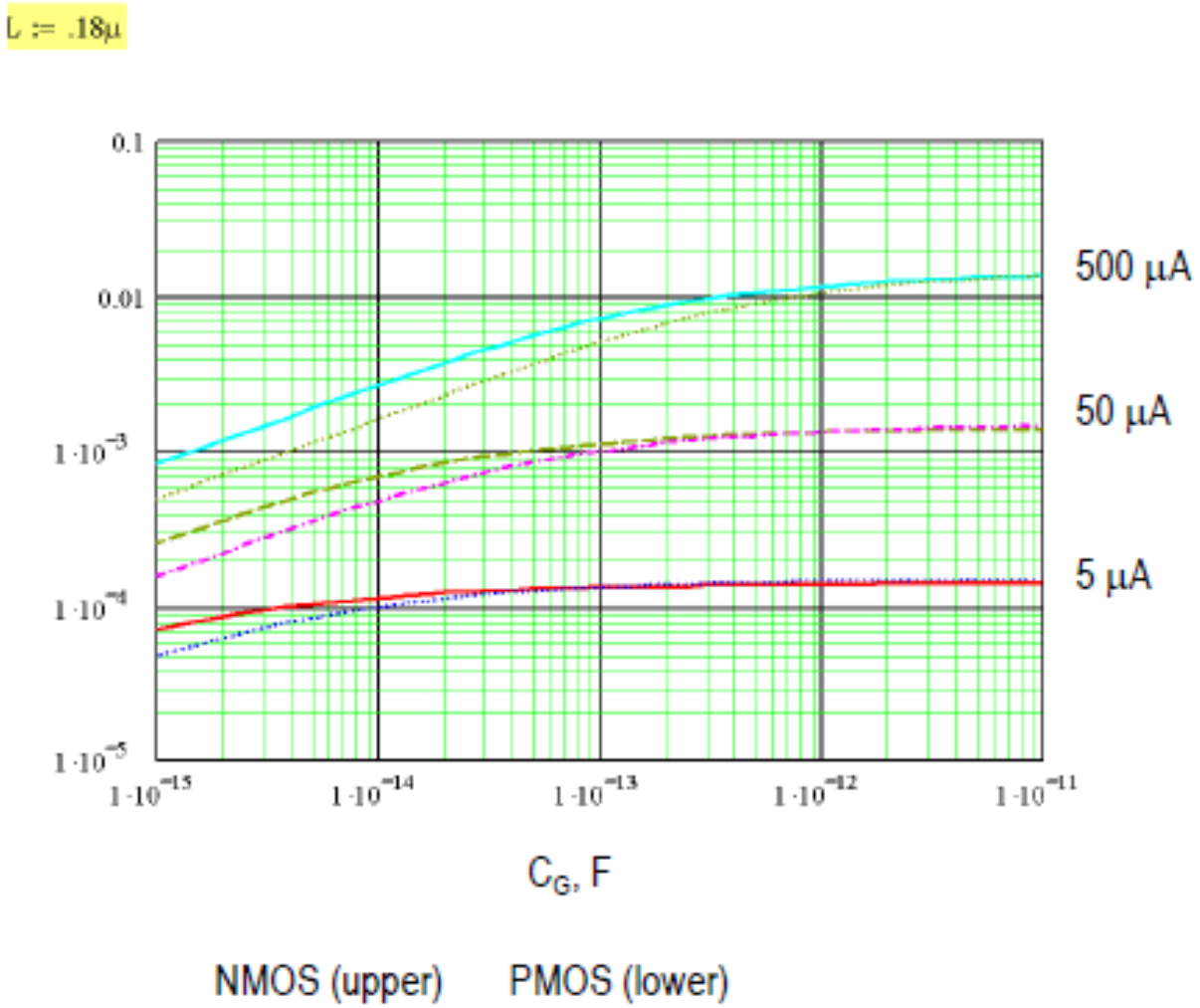
$$C_{gs,opt} = C_{det}$$

II. Fixed I_D (practical case)

$$g_m \propto C_{gs}^{1/2} \text{ [strong inversion]}$$

$C_{gs,opt} = C_{det}/3$

Optimising MOS size [Paul O'Connor BNL]



Strong inversion:

$g_m \sim \sqrt{C_G}$

$g_{m,n} \sim 3 g_{m,p}$

Weak inversion:

$g_m \sim const.$

$g_{m,n} = g_{m,p}$

Gate resistance [Paul O'Connor BNL]

- Polysilicon gate is resistive:
  - ρ_{poly} 25 Ω/sq.
  - $\rho_{silicided\ poly}$ 4 Ω/sq.

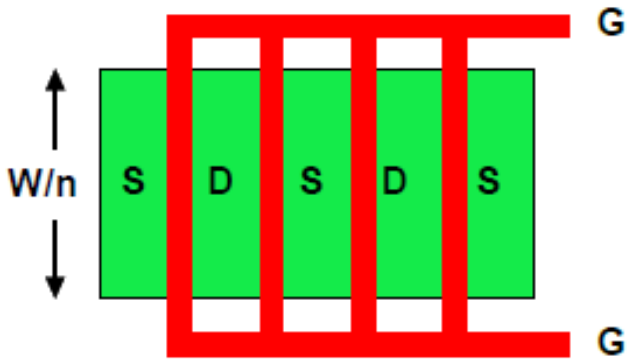
resistance of non-interdigitated gate:

$$R_g = \rho_{poly} \cdot \frac{W}{L}$$

series noise due to gate resistance:

$$e_{ng}^2 = 4kT \cdot R_{eq}$$

FET with interdigitated layout



n gate fingers
n = 4

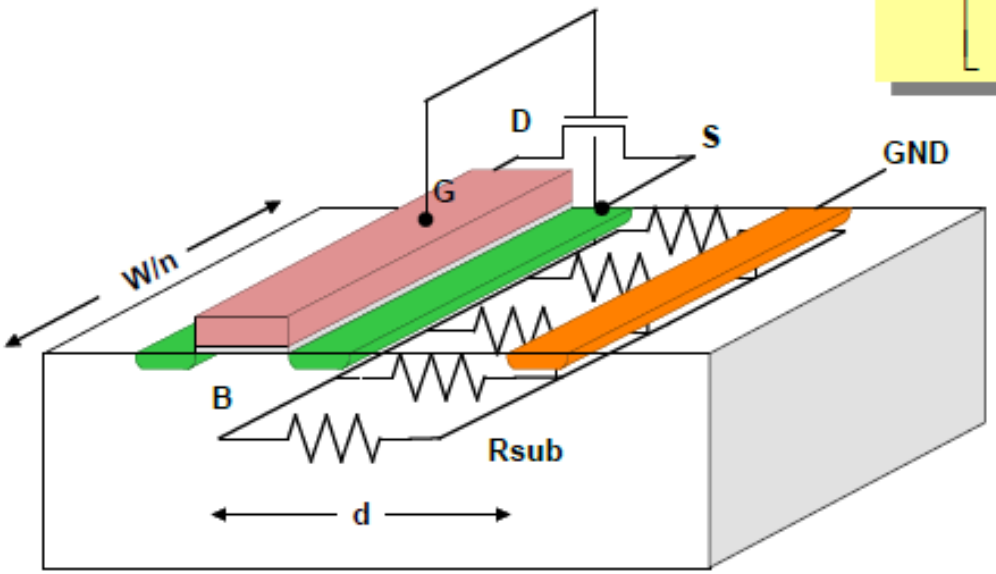
Layout	Req driven one end	Req driven both ends
Single finger	Rg/3	Rg/12
Interdigitated n fingers	$Rg/3n^2$	$Rg/12n^2$

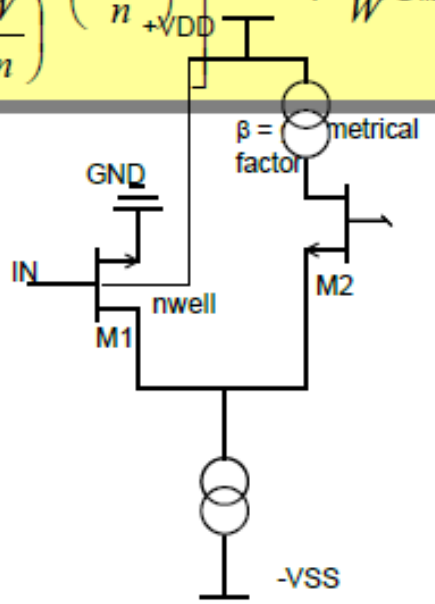
Bulk noise[Paul O'Connor BNL]

- Resistive substrate couples to the channel via the back transconductance g_{mb}.
- Substrate resistance is distributed.

leads to noise in the channel:

$$i_{db}^2 = \left[4kT \cdot n \cdot \beta \frac{d}{\left(\frac{W}{n}\right)} \cdot \left(\frac{g_{mb}}{n} \right)^2 \right] = 4kT\beta \frac{d}{W} g_{mb}^2$$

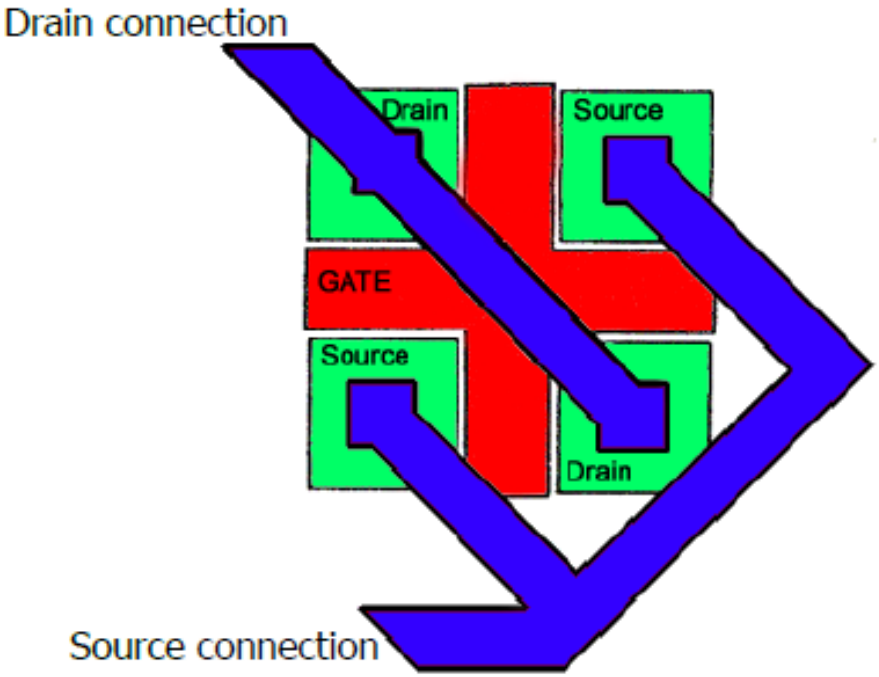




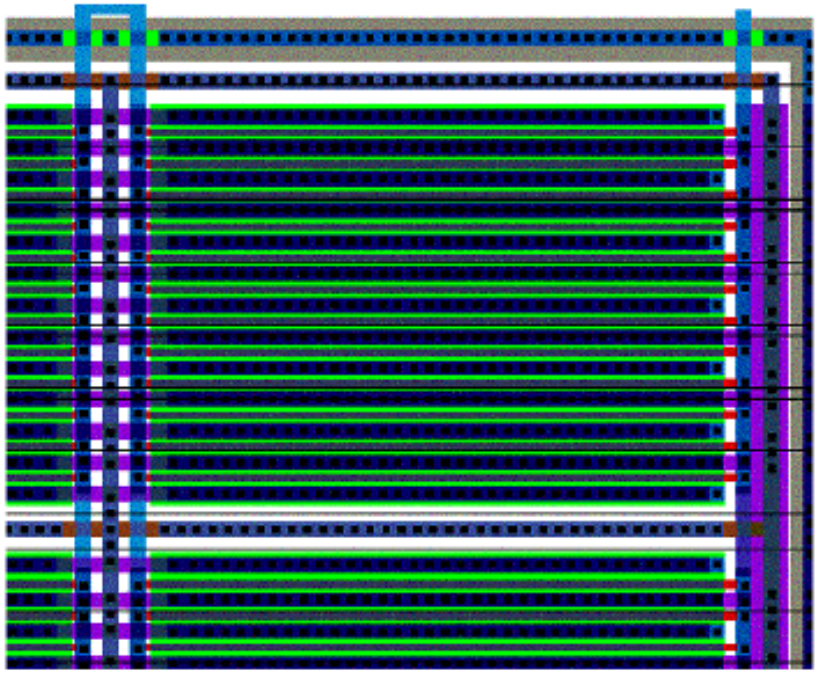
- Minimize by reverse biasing the source-substrate junction.

Layout techniques [Paul O'Connor BNL]

Waffle iron layout

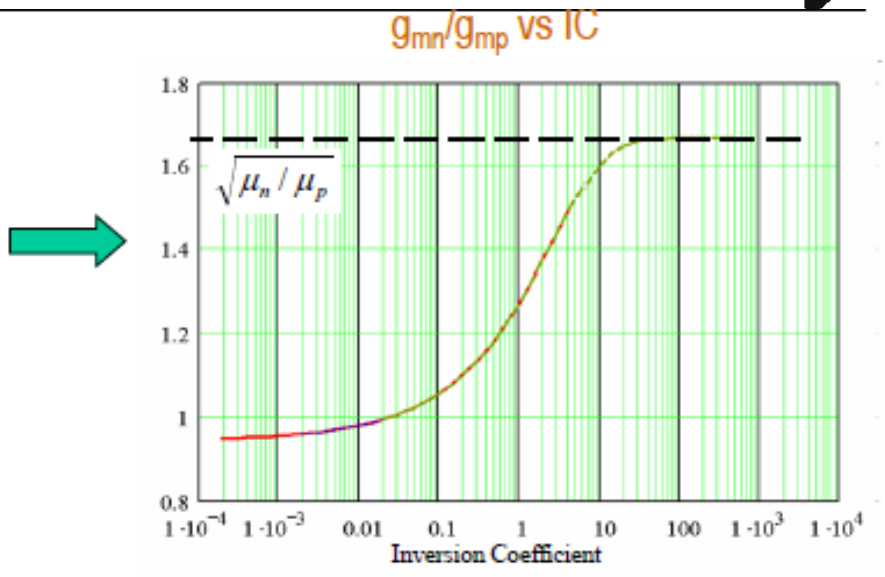


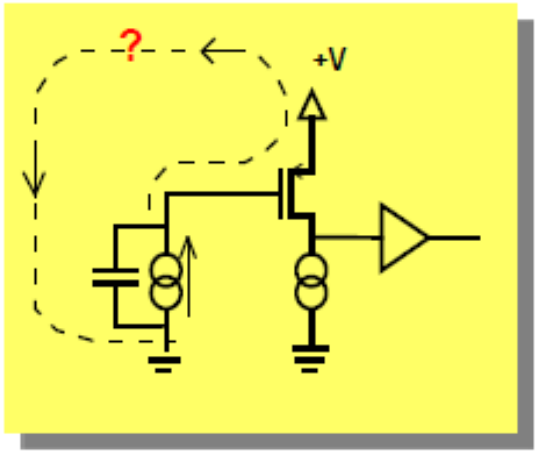
Substrate contacts, guard ring, multiple gate fingers contacted both ends

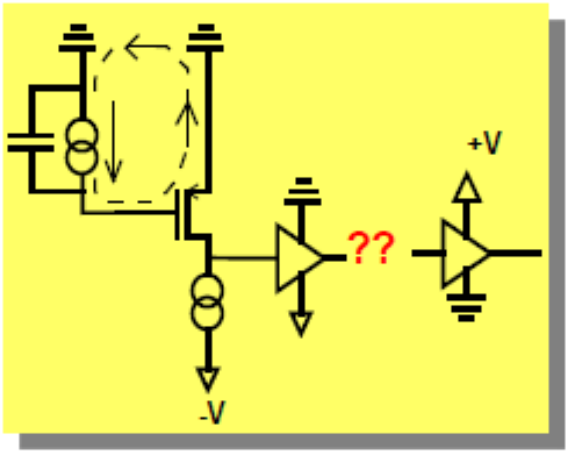


PMOS vs NMOS [Paul O'Connor BNL]

- *PMOS lower 1/f noise*
- *NMOS white series noise advantage over PMOS diminishes each generation*
- *PMOS can be operated at reverse V_{BS} to reduce bulk resistance noise*
- *PMOS lower tunneling current at ultra-thin t_{ox}*
- *Single-supply operation of PMOS-input preamp awkward:*

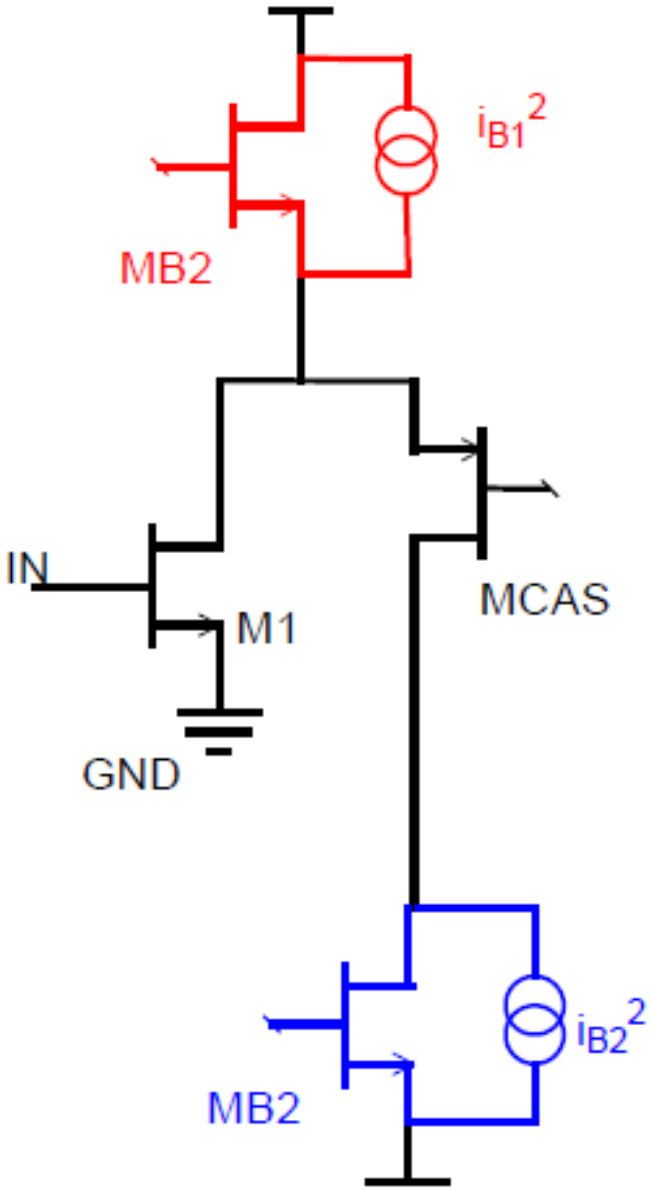






Secondary noise sources [Paul O'Connor BNL]

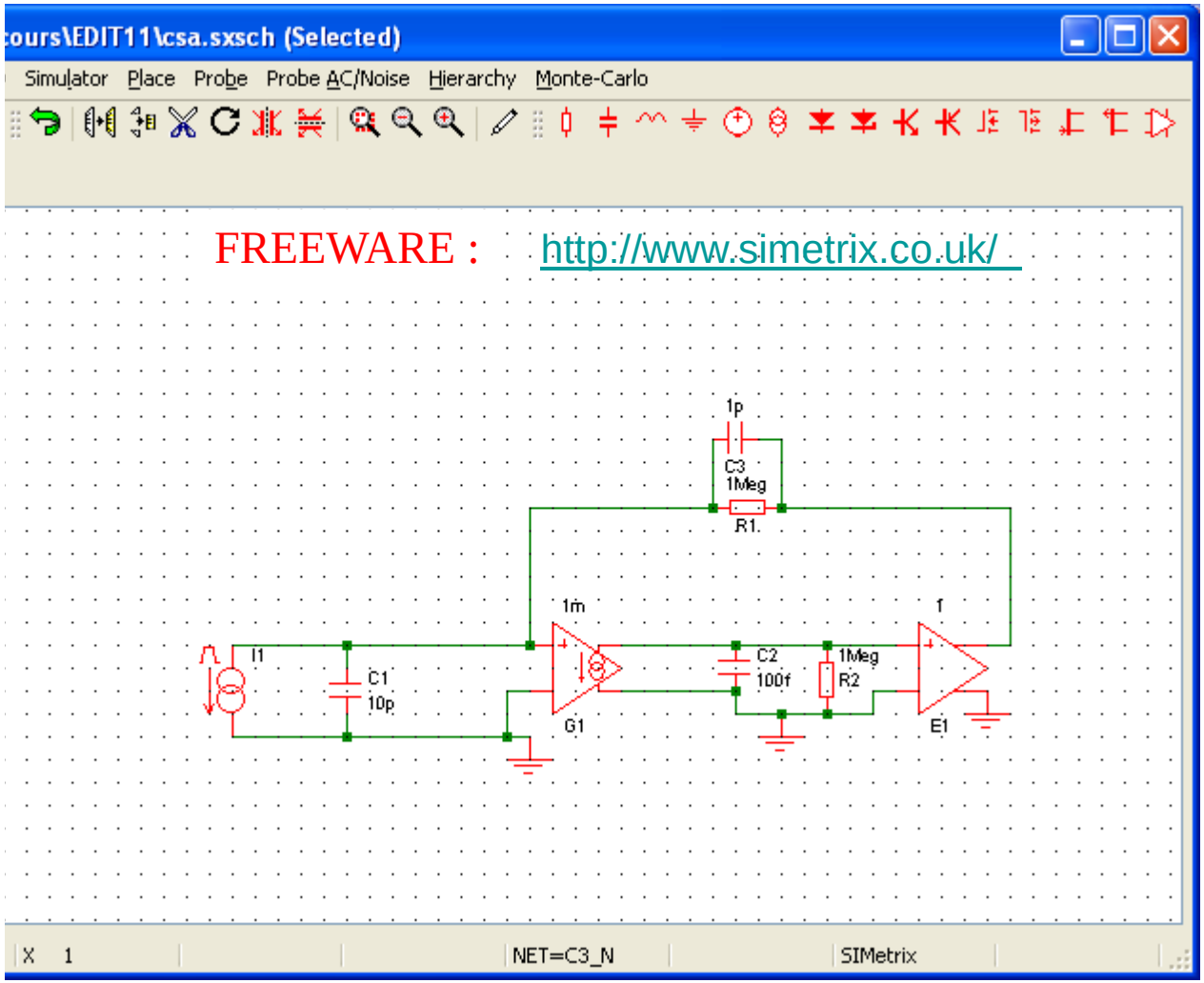
- i_{B1}^2 and i_{B2}^2 are effectively in parallel with the input transistor
- Their contribution to input (white) thermal series noise is $(g_{mB1,2}/g_{m1})^2$.
- We minimize their g_m w.r.t. that of M1
- $g_{mB1,2} = \sqrt{2\mu C_{ox} W I_D / L}$
- use low W/L (i.e. long-gate) devices with large or degenerate with source resistor.
- Keep W/L as small as possible (thus V_{gs}-V_T large) while keeping $V_{DS} > V_{gs}$-V_T.
- Various ways to optimize.



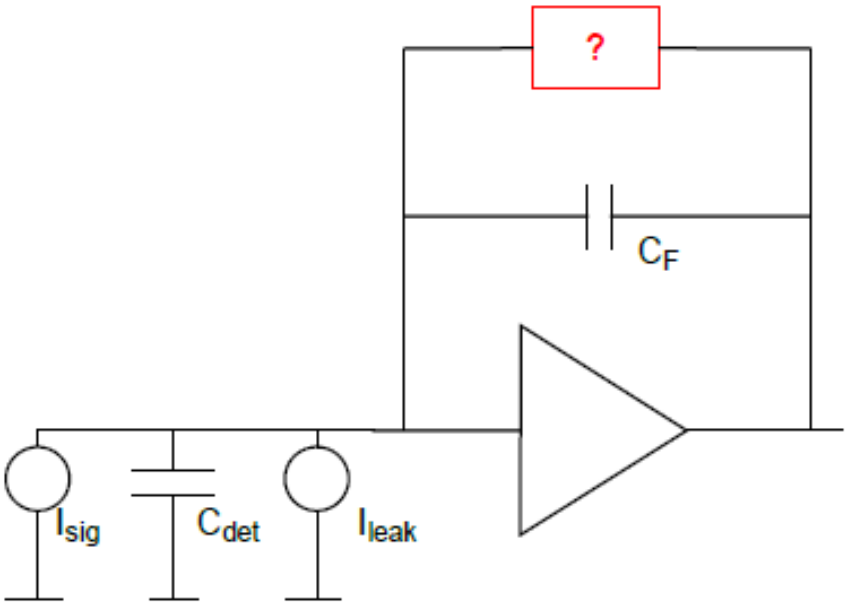
Simple simulations : Simetrix freeware

Example : bandwidth and EMC of simple charge preamp

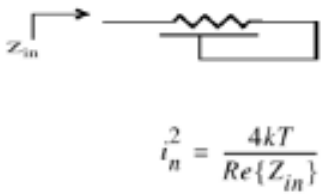
- Simulate impulse response
- Frequency response
- Input impedance
- Ballistic deficit
- Effect of amplifier gain
- Effect of resistive feedback
- Test pulse injection
- Effect of input capacitance
- Parasitic inductance
- Capacitive crosstalk
- Resistive/Inductive ground return



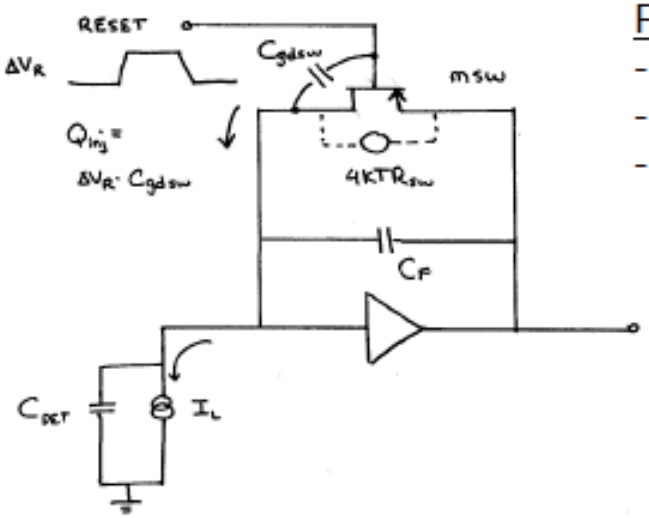
Preamp reset [Paul O'Connor BNL]



- all charge preamplifiers need DC feedback element to discharge the input node and stabilize the bias point
- usually, a resistor in the MΩ – GΩ range is used
- monolithic processes don't have high value resistors
- we need a circuit that behaves like a high resistor and is also
  - *insensitive to process, temperature, and supply variation*
  - *low capacitance*
  - *lowest possible noise*
  - *linear*



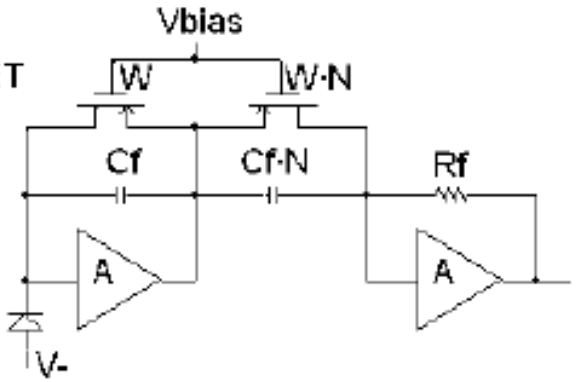
Physical resistor
- always accompanied by parasitic capacitance
- de-stabilizes circuit and increases noise
- noise higher than 4kT/R by factor ~ RC/t_m



Pulsed reset by MOS switch
- sampled noise $\sqrt{kTC_F}$
- Q_{inj} noise from switch control voltage
- leakage current integrates on output node $dV_{out}/dt = I_L/C_F$

Reset techniques [Paul O'Connor BNL]

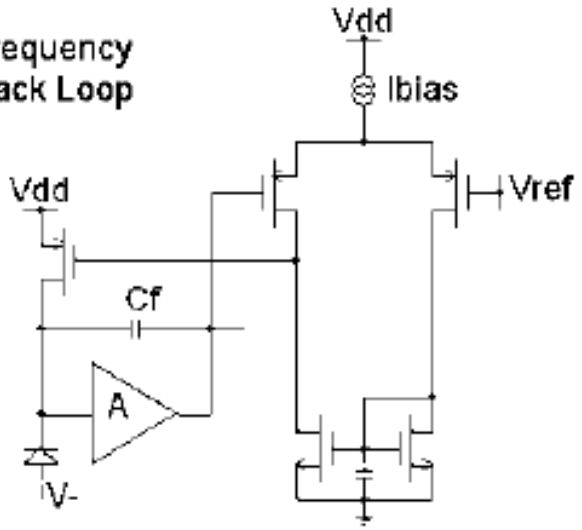
Single MOSFET



O'Connor et al., TNS v44 n3 (1997)
De Geronimo et al., NIM A421 (1999)
De Geronimo et al., TNS v47 n4 (2000)

- provides effective current gain -N
- full compensation (high linearity)
- minimum noise (thermal)
- requires baseline stabilization
- can be realized in multiple stages

Low Frequency Feedback Loop

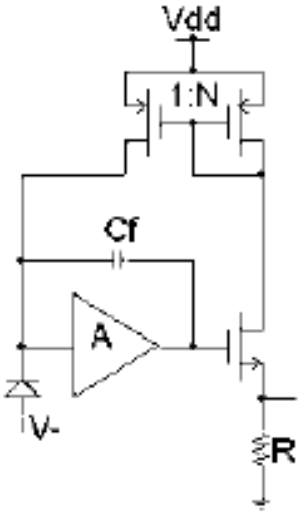


Krummenacher, NIM A350 (1991)
Ludewigt et al., TNS v41 n4, (1994)
Vandenbussche et al., TNS v45, n4 (1998)
Manfredi et al., Nucl.Phys.B 61B, Proc.Suppl. (1998)

- noise can be high
- requires baseline stabilization at high rates
- compensation an issue

Reset techniques [Paul O'Connor BNL]

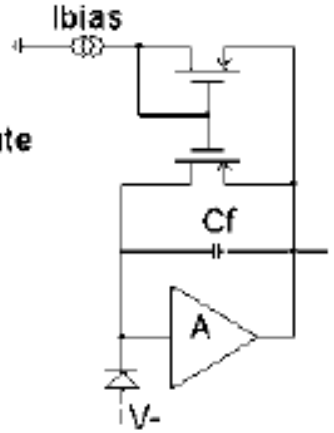
R-Scaling



Santiard et al., CERN-ECP/94-17 (1994)
Chase et al., NIM A409 (1998)
Sampietro et al., Elec.Lett. v34 n19 (1998)

- noise can be high (large values of R and N required)
- linearity an issue
- parasitic capacitor an issue
- compensation available in some configuraitions
- requires baseline stabilization

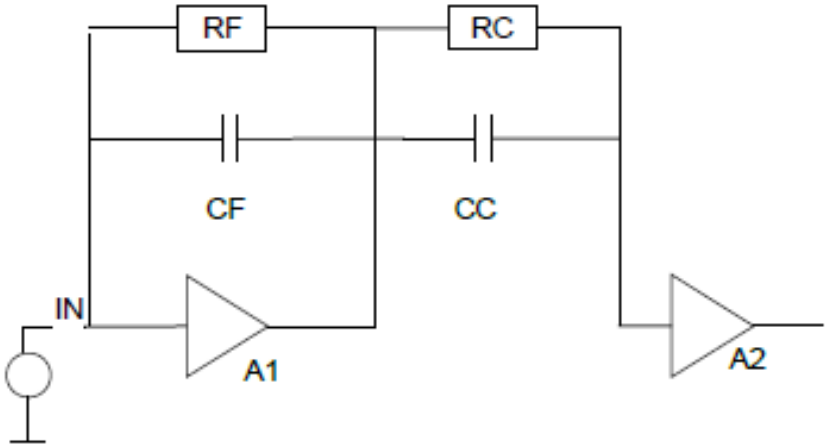
Slew-rate Limited



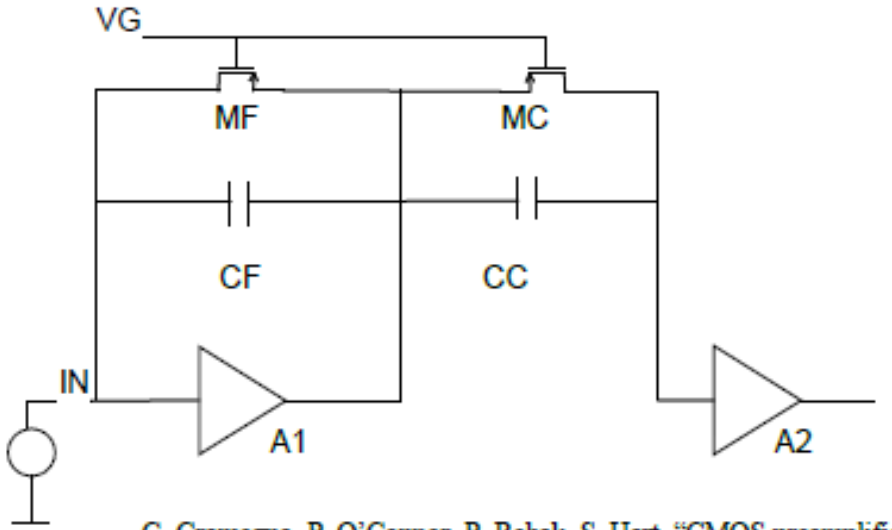
Blanquart et al., NIM A395 (1997)
Blanquart et al., NIM A439 (2000)

- MOSFET operates in saturation only when there is signal activity
- noise can be high (it requires Ibias > Idet)
- parasitic capacitor an issue
- suitable for Time-Over-Threshold processing techniques
- requires baseline stabilization at high rates
- linearity an issue
- compensation an issue

Automatic pole zero [Paul O'Connor BNL]



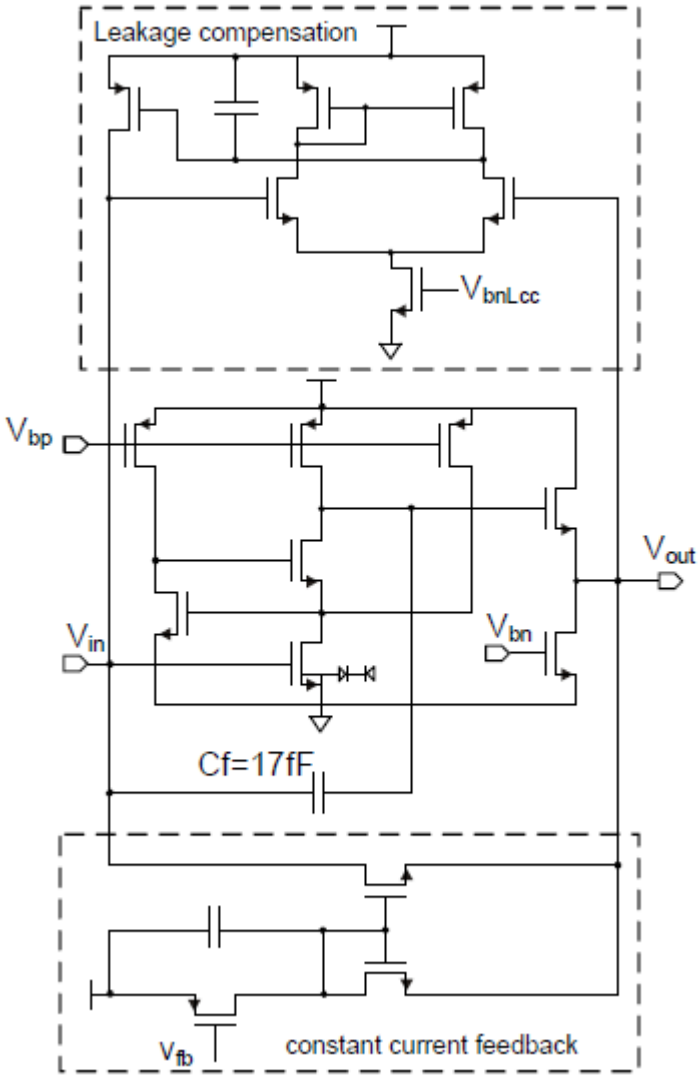
- Classical
  - *RF · CF = RC ·CC*
  - *Zero created by RC,CC cancels pole formed by RF, CF*



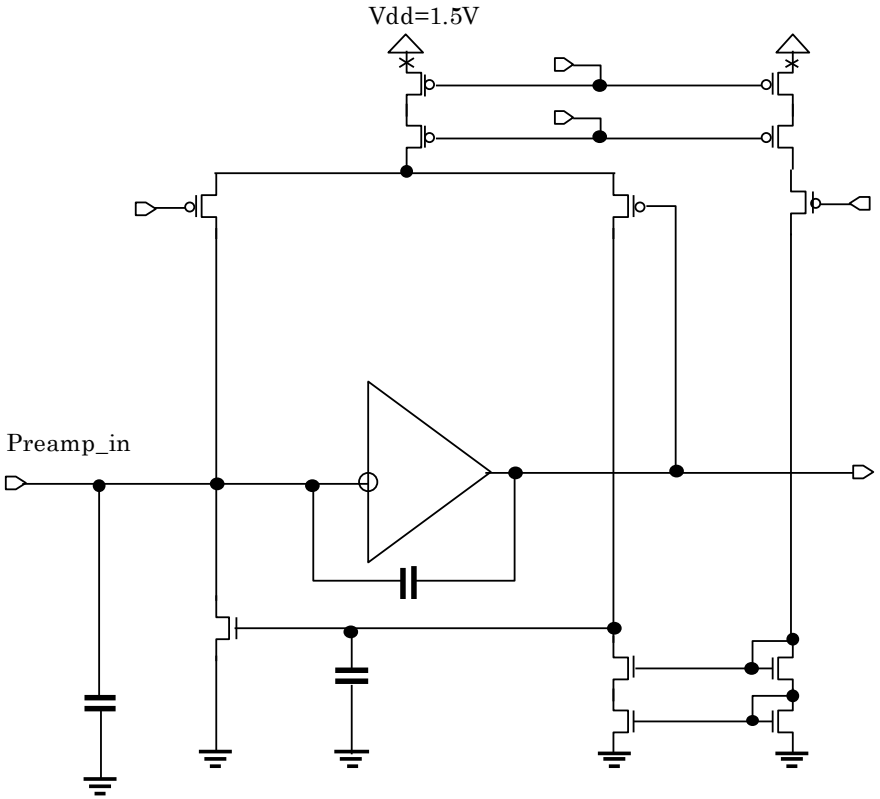
G. Gramegna, P. O'Connor, P. Rehak, S. Hart, "CMOS preamplifier for low-capacitance detectors", NIM-A 390, May 1997, 241 – 250.

- IC Version
  - *CC = N · CF*
  - *$(W/L)_{MC} = N \cdot (W/L)_{MF}$*
  - *Zero created by MC, CC cancels pole formed by MF, CF*
  - *Rely on good matching characteristics of CMOS FETs and capacitors*

Examples : pixels

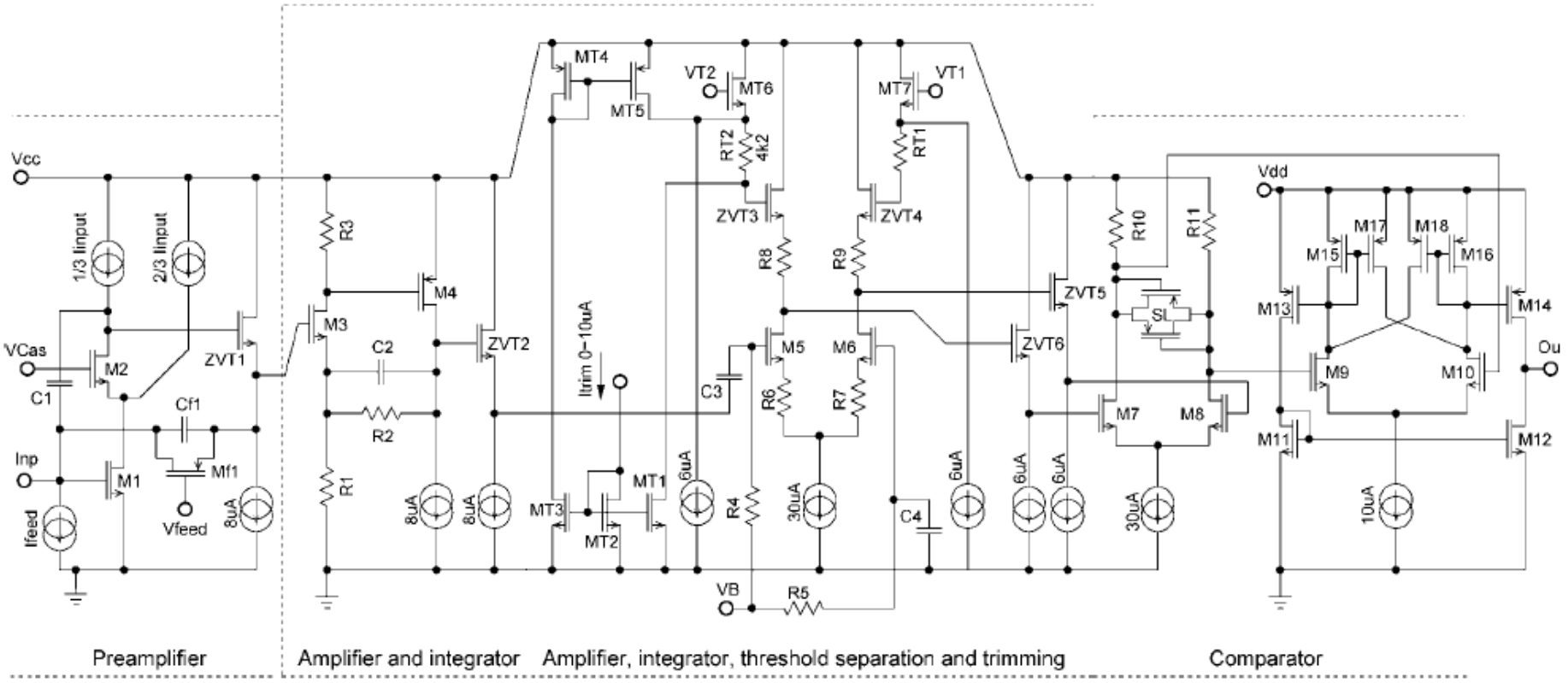


ATLAS FEI4



TIMEPIX

Examples : Si strips



ATLAS ABCN

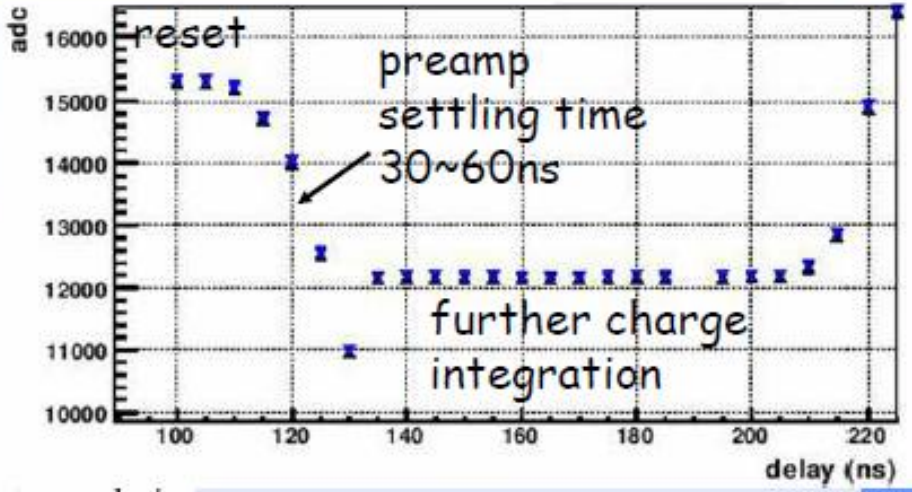
Examples : switching preamp

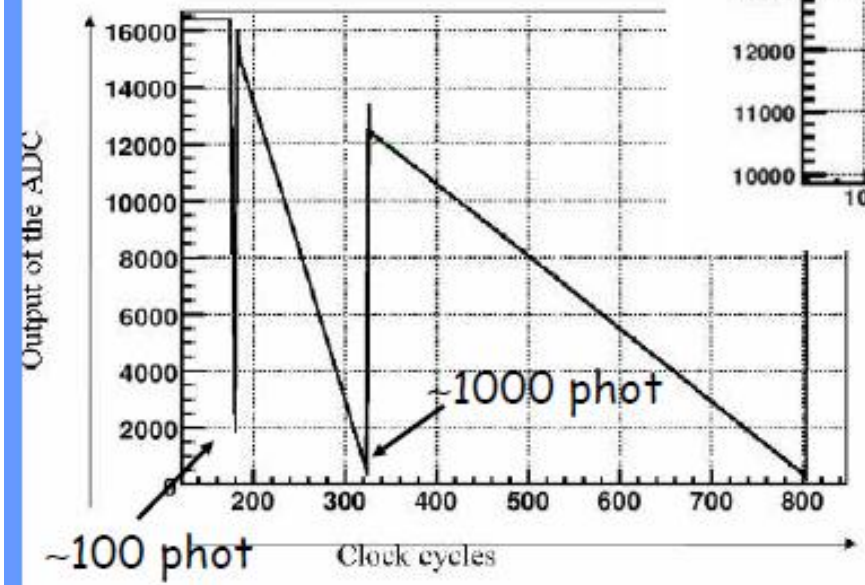
Adaptive Gain

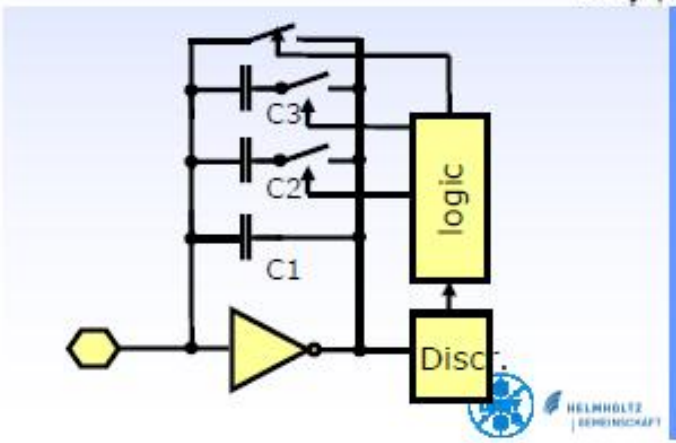
XFEL AGPID

AGIPD

- multiple (3) scaled feedback cap (60fF/3pF/10pF)
- 1:35:4 gain reduction(s)







Alessandro Marras
PIXEL 2012. 02-07.09.2012

Chosen Technology: AMS CMOS 0.35µm

Noise Minimization of MOSFET Input Charge Amplifiers Based on $\Delta\mu$ and ΔN $1/f$ Models

Giuseppe Bertuccio and Stefano Caccia

***Abstract*—The optimization of the noise performance of integrated complementary metal–oxide semiconductor (CMOS) charge amplifiers is studied in detail considering accurate $1/f$ noise modeling for the input metal–oxide semiconductor field-effect transistor (MOSFET) biased in a strong inversion-saturation region. This paper aims to generalize and correct previously published analyses which have been based on two limiting and sometimes not applicable assumptions: a fixed MOSFETs bias current and the general validity of the McWhorter $1/f$ noise model. This study considers the two main $1/f$ noise models: 1) the mobility fluctuation, known as $\Delta\mu$ or Hooge model, which is followed by p-channel MOSFETs and 2) the carriers number fluctuation, also known as ΔN or McWhorter model, which is applicable only for n-channel MOSFETs. The front-end noise optimization is made with the $1/f$ component alone, thus determining the ultimate performance, and also considering the presence of series and parallel white noise sources. It is shown that different design criteria are valid of p- or n-channel MOSFETs: the $\Delta\mu$ model results in an optimum bias current and a different optimum gate width with respect to ΔN model. Two-dimensions suboptimum noise minimization criteria are derived when power or area constraints are imposed to the circuit design. Starting from experimental data on CMOS 1/f noise, examples of application of the presented analysis are shown to predict the lower limits of the $1/f$ noise contribution for the currently available CMOS technologies.**

***Index Terms*—Charge amplifier, complementary metal–oxide semiconductor (CMOS) integrated circuit (IC), integrated circuits (ICs), low-noise circuit, 1/f noise.**

amplifier concept for radiation detector readout [3], a large variety of implementations have been studied and developed involving all types of front-end devices and technologies (junction field-effect transistor (JFET), metal semiconducor field-effect transistor (MESFET), high-electron mobility transistor (HEMT) , bipolar junction transistor (BJT), metal-oxide semiconductor field-effect transistor (MOSFET)) in order to maximize performance in terms of speed, noise, power consumption, or chip area. In the last five years, intense attention has been given to the design of charge amplifiers implemented in CMOS technologies because of their advantages in terms of high integration density, low power consumption, wide bandwidth and digital logic integration, as required in many applications.

The most common objective in CSA design is the minimiz tion of the equivalent noise charge (ENC), which requires careful design of the input stage. In particular, the $1/f$ noi associated with the drain current of the input device plays major role in ultra low-noise design, as recently demonstrat with CSA with noise levels of a few electrons root mean squa (rms) [4].

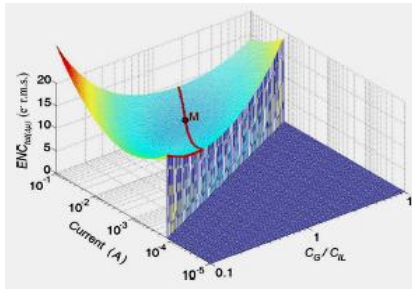
Previous works have studied the noise optimization of CMC CSA but with two restrictive and sometimes not applicable a sumptions: 1) a fixed bias current of the input MOSFET, main determined by power consumption or bandwidth constraints a 2) the general validity of the McWhorter $1/f$ model (see ne section) [5]–[10]. In our analysis, we remove both of these a

$$ENC^2_{1/f(\Delta\mu)} = 2\pi A_2\left(\frac{n\alpha_H L}{q\sqrt{2\mu}}\right)\left[\frac{(C_{IL}+C_G)^2}{\sqrt{C_G^3}}\right]\sqrt{I}$$

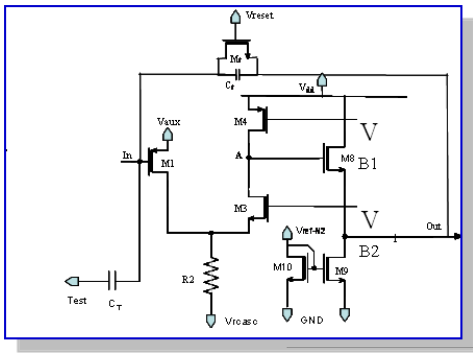
$$ENC^2_{1/f(\Delta N)} = 2\pi A_2\left(\frac{nkTN_T}{2\gamma C'_{ox}}\right)\left[\frac{(C_{IL}+C_G)^2}{C_G}\right]$$

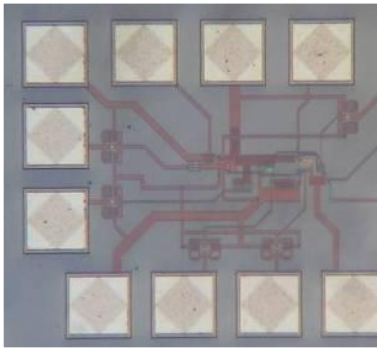
$$I \geq I_{\min} = R_{\min} I_S,$$

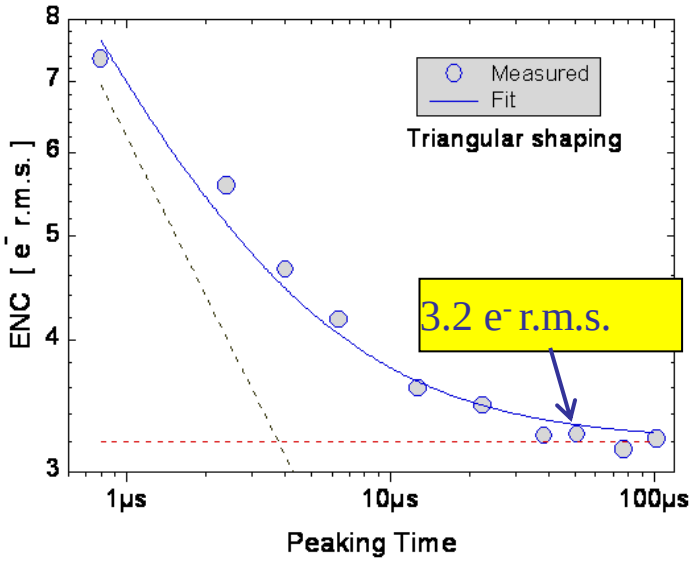
$$\begin{cases} ENC^2_{tot(\Delta\mu)} = k_{WS}\dfrac{(C_{IL}+C_G)^2}{\sqrt{C_G}}\dfrac{1}{\sqrt{I}}\dfrac{1}{\tau} \\ \quad +k_{\Delta\mu}\dfrac{(C_{IL}+C_G)^2}{\sqrt{C_G^3}}\sqrt{I} + k_{WP}\tau \\ I \geq R_{\min} I_S \end{cases}$$



G. Bertuccio , S. Caccia
IEEE Trans. Nucl Sci. 56, 2009, pp. 1511



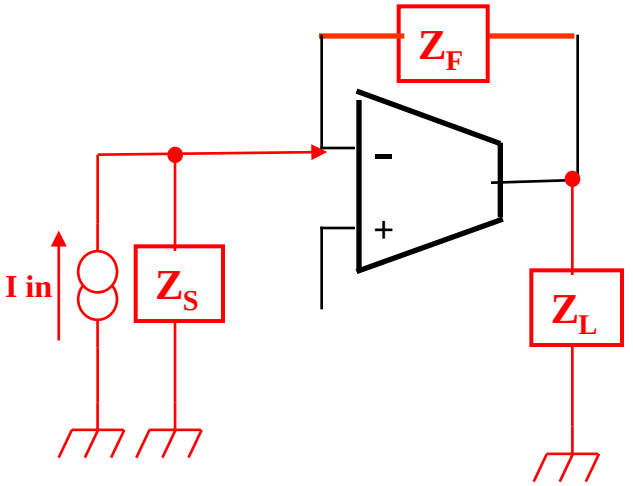


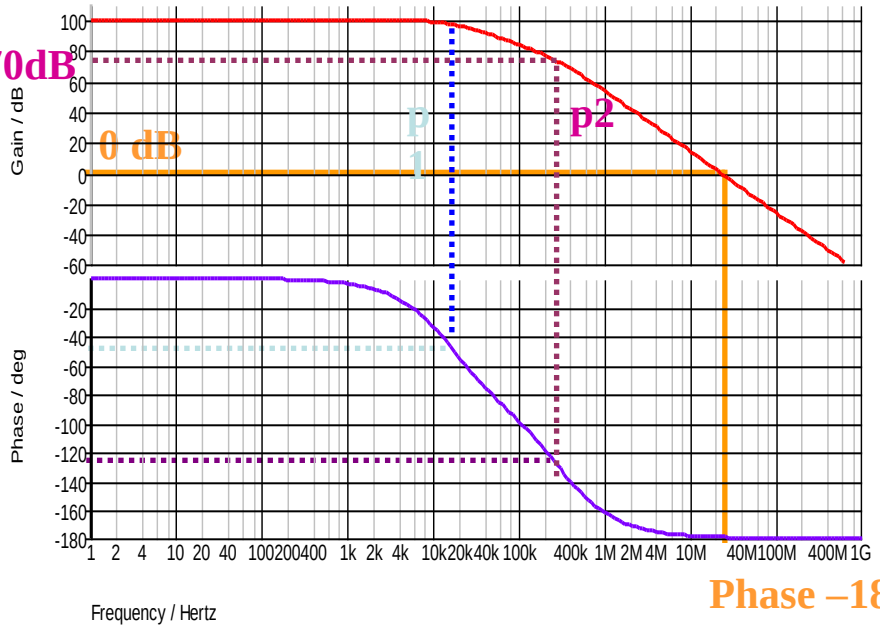


G. Bertuccio et al., NIM, A 579, 2007, pp. 243

Transimpedance amplifier with OTA

- Transfer function
  - Using an OTA with gain Gm
    - $I_{OUT} = V_{OUT} / Z_L + (V_{OUT} - V_{IN}) / Z_F$
    - $I_{IN} = V_{IN} / Z_S - (V_{OUT} - V_{IN}) / Z_F$
    - $I_{OUT} = GmV_{IN}$
  - $V_{out}(\omega)/i_{in}(\omega) = - Z_F / (1 + (1 + Z_F/Z_S)(1+Z_F/Z_L)/(Gm-1/Z_F))$
    $\sim - Zf$
  - Input impedance : $\sim Zf/GmZ_L$
  - Output impedance : $\sim 1/Gm$
- Effect of pole splitting ($Z_F=C_F$)
  - $ZS=RS/(1+sR_SC_S)$, $Z_F=1/sC_F$
  - Dominant pole : $1/GmR_SR_LC_F$
  - Second pole : $GmC_F/(C_SC_F+C_LC_F+C_SC_L)$

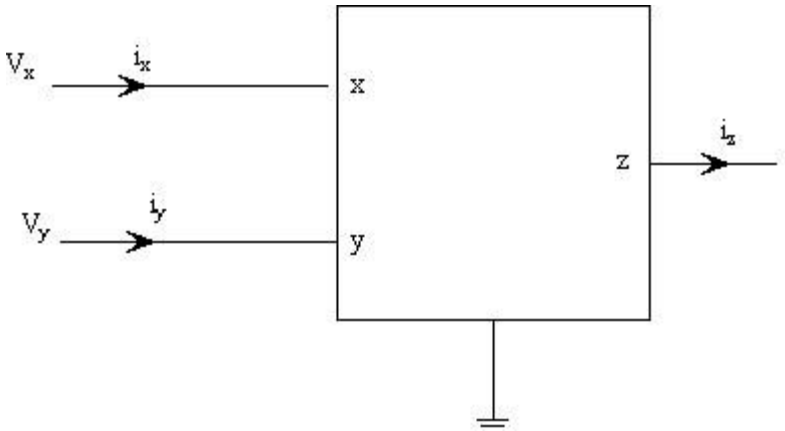




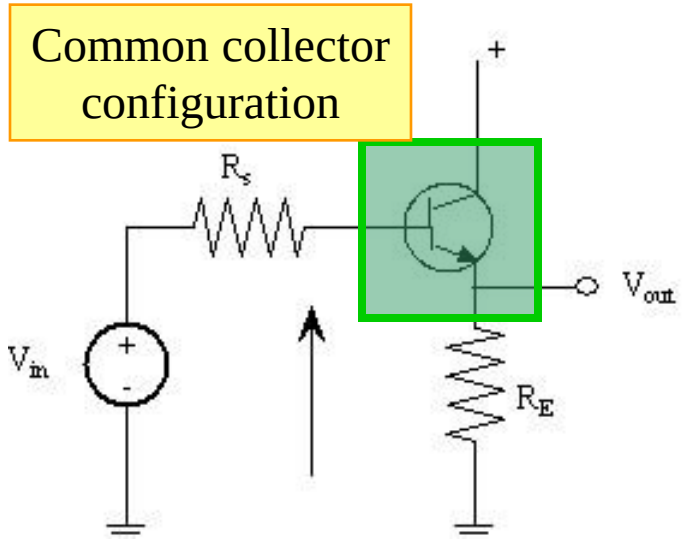
Current conveyors

- Formal description as CCI, CCII

$$\begin{pmatrix} Iy \\ Vx \\ Iz \end{pmatrix} = \begin{pmatrix} 0 & 1/0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \begin{pmatrix} Vy \\ Ix \\ Vz \end{pmatrix}$$

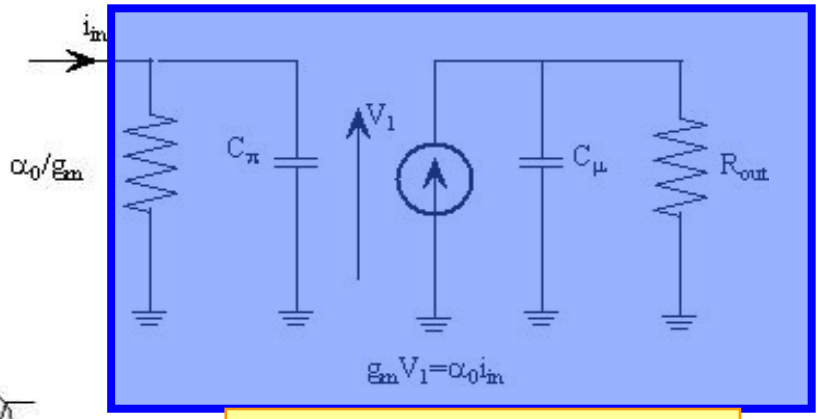


- View it as an ideal transistor
  - Vout = Vin
  - Iout = Iin



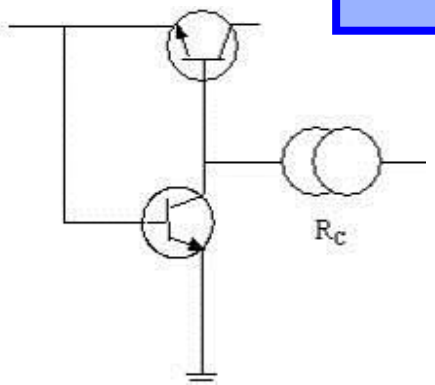
Simple current conveyors

- Common base
  - Input impedance Rin = $1/g_m$
  - Output impedance: Rout = $(1+g_mR_S)r_0$
  - Current gain : $A_i \sim 1$
  - Very fast : Frequency response : $\sim F_T$

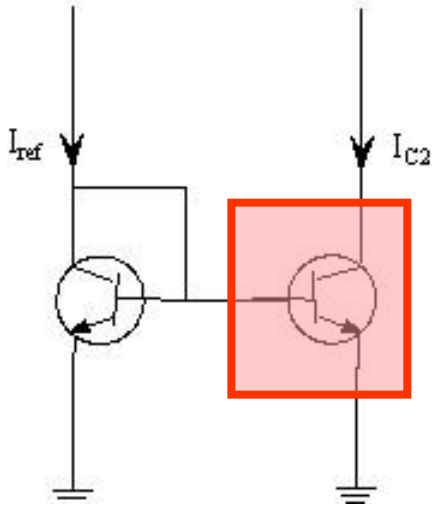


Equivalent circuit of CB

- Super common base



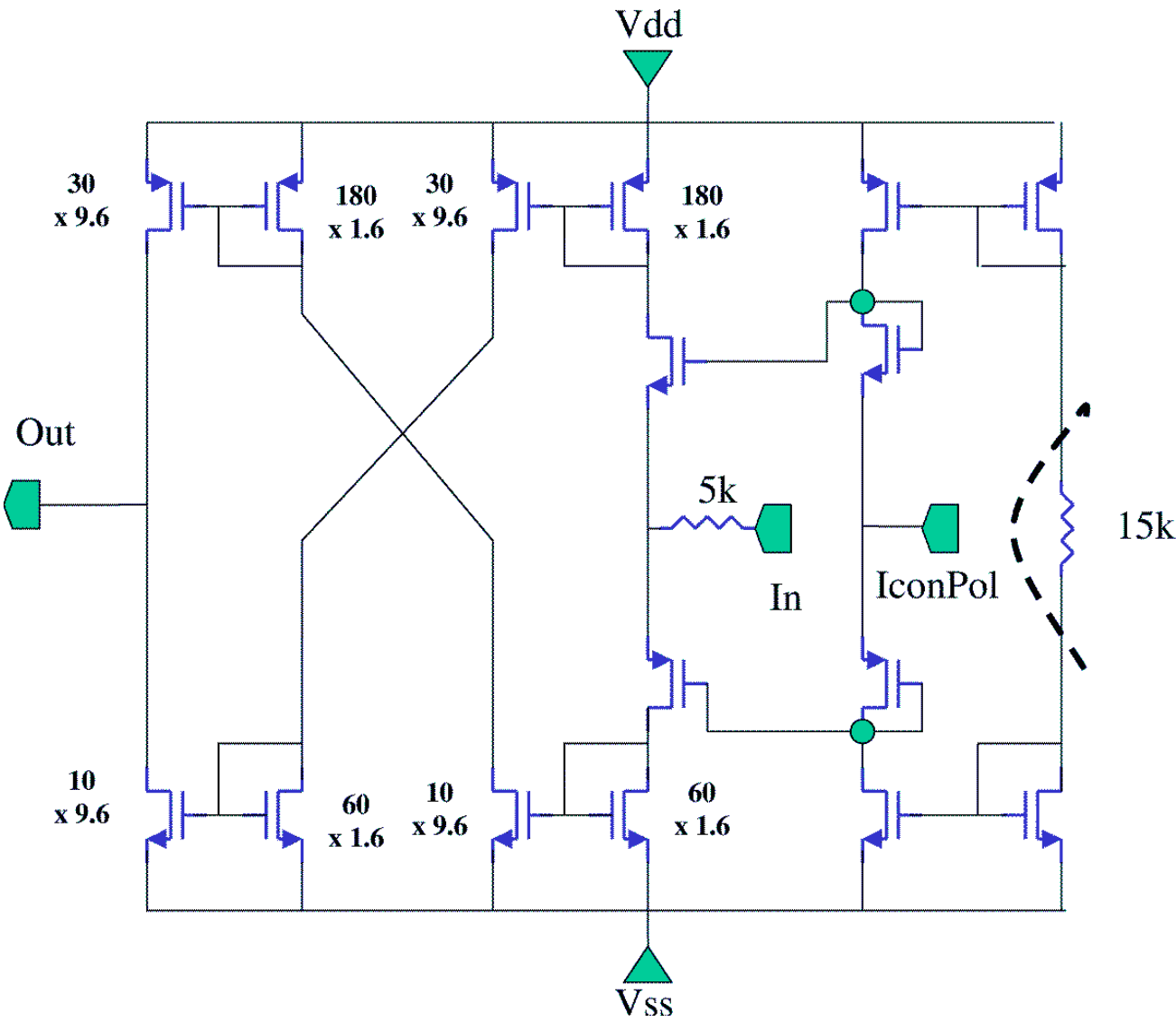
- Current mirror :
  - Same V_{BE} => same current
  - Input impedance : $R_{in} = 1/g_{m1}$
  - Output impedance : Rout = $1/r_{02}$
    - Can be increased with composites
  - Current ratio : $I_{C2}/I_{C1} = 1$
    - Can be increased by changing the area



Current mirror

Current conveyors

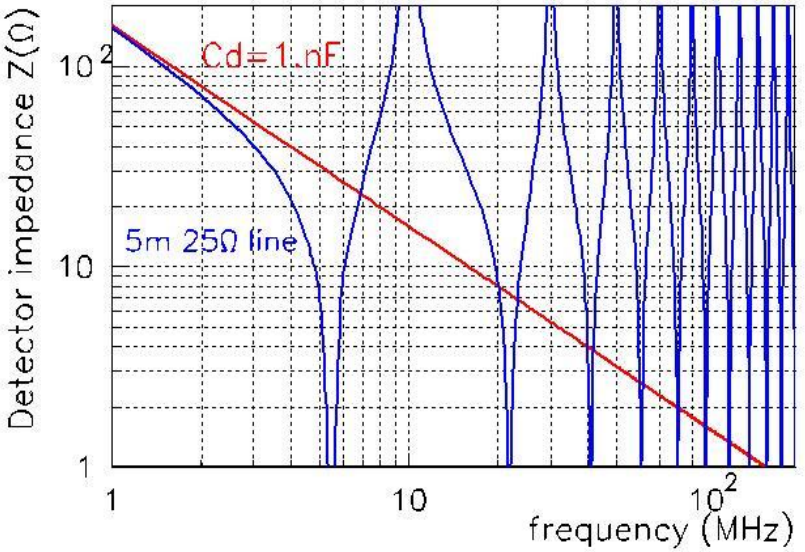
- ICON : symetrical current conveyor
  - CB + mirror
- Input impedance : 1/gm
- Output impedance : $1/g_{DS}$



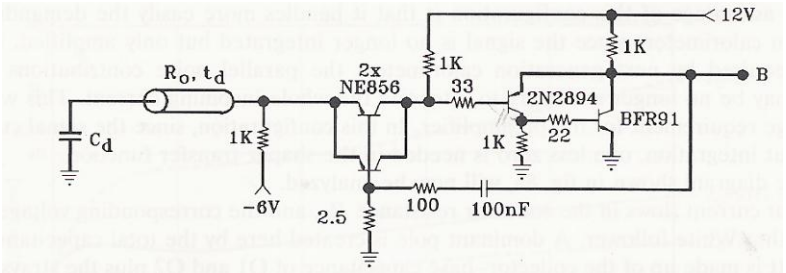
Example ATLAS ØT preamps

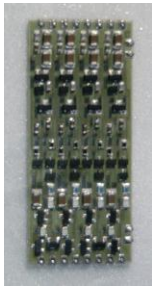
- Line terminating preamplifiers
  - No noise penalty at fast shaping
  - ENC ~ en/Z*tp

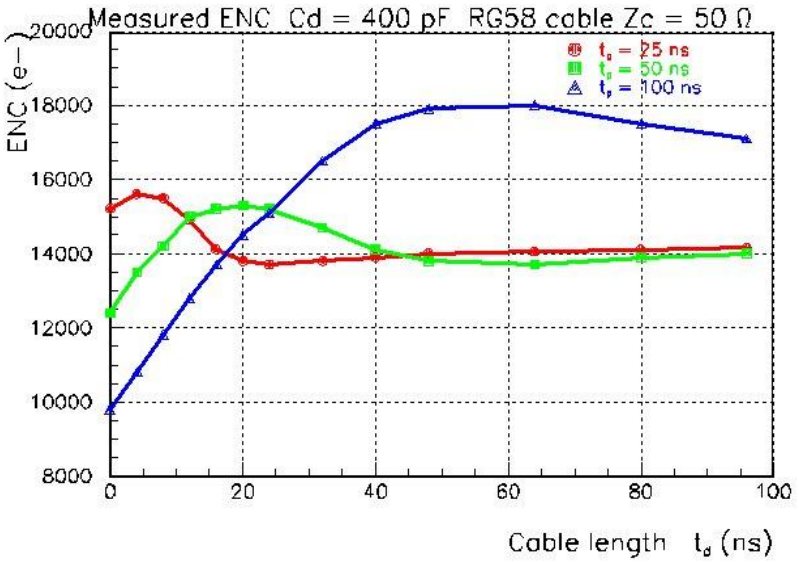
$$Z = \frac{1 - \omega.R_C C_d \tan \omega.t_d}{j\omega.C_d + j \tan \omega.t_d / R_C}$$



- Current sensitive configuration
  - Avoids saturation with large and long LAr pu
  - Parallel noise negligible with fast shaping
  - Bipolar transistors, exhibit superior series n

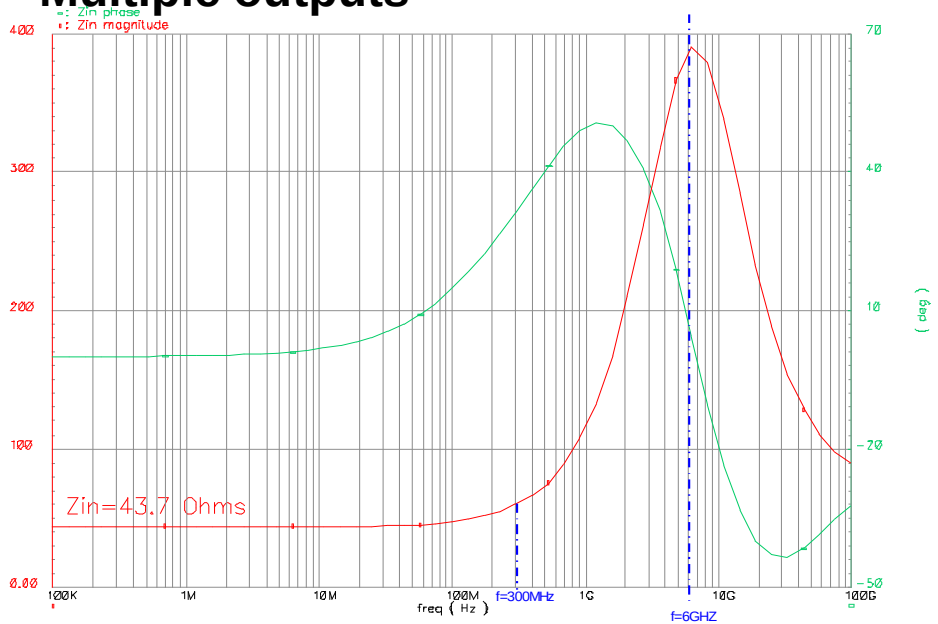


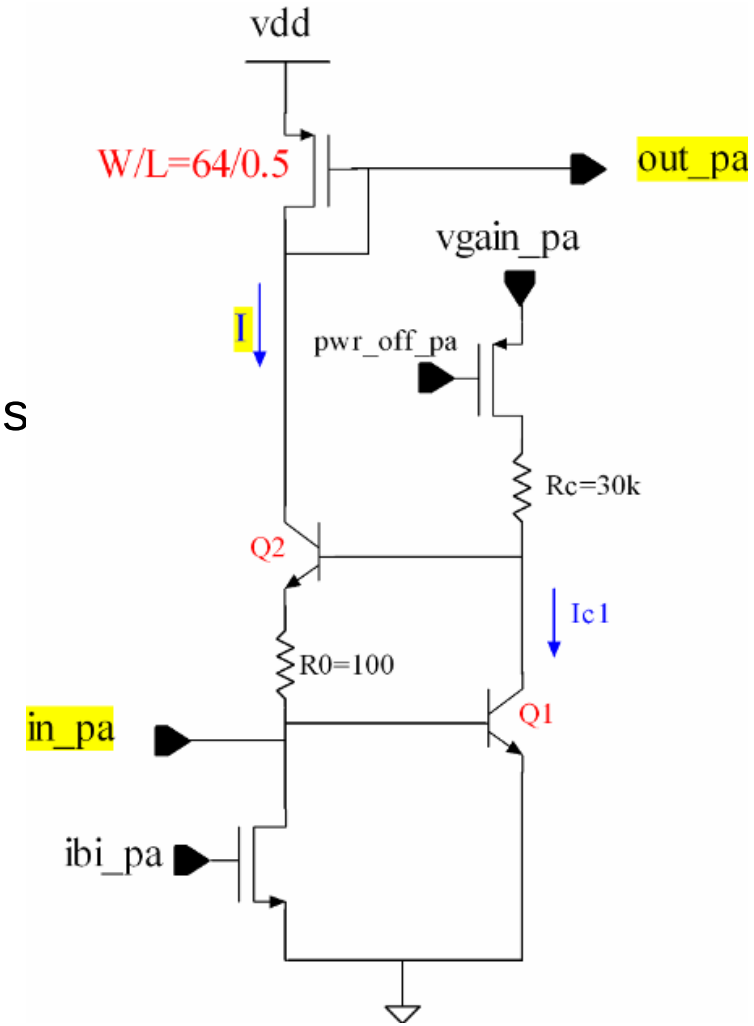




SCB conveyor

- Current conveyor
  - « Super common base » configuration
  - low input impedance, small « equivalent inductance » (<20 nH)
  - Zin = $1/g_{m1}g_{m2}R_c$ = 10-100Ω
  - good performance of SiGe
- Variable output mirrors : 8 bits = gain adjus
  - **Multiple outputs**

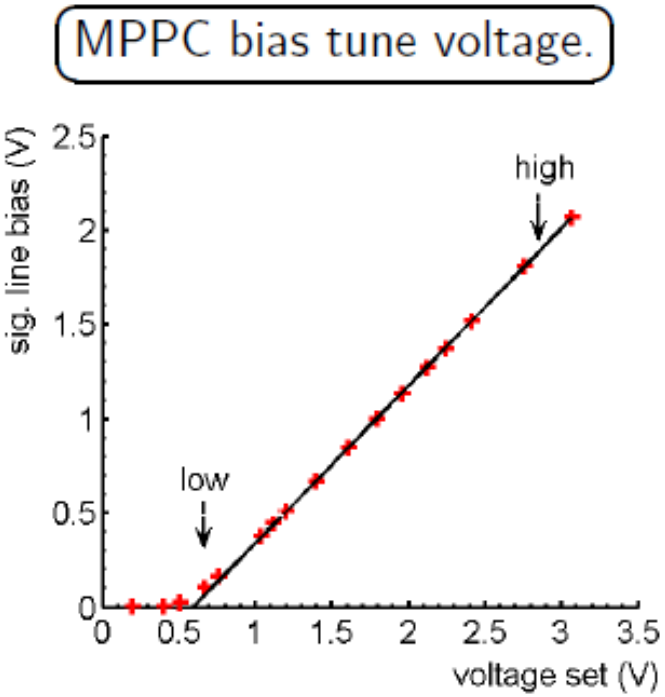


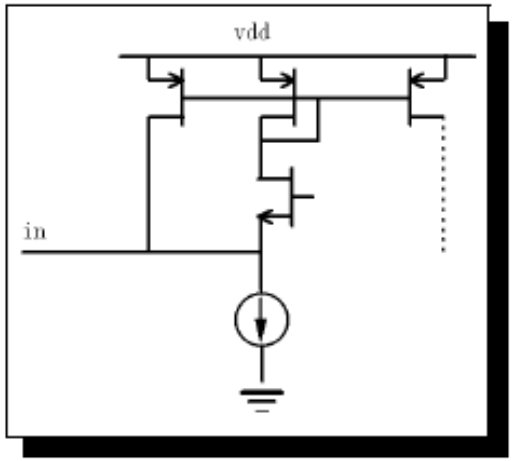


ATLAS note : ATL-LARG-95-010 (1995)

Nucl Instr and Meth ***A521*** (2004) 378-392

Examples : Klaus (U. Heidelberg)





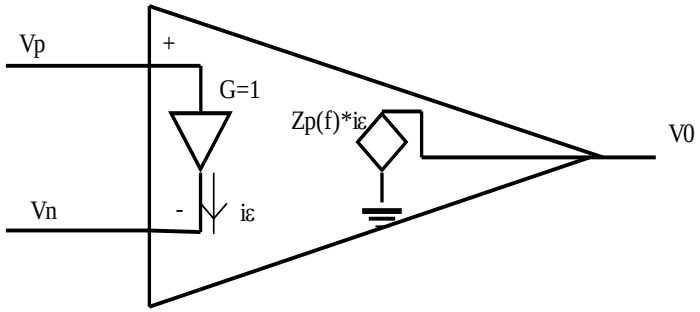
- residual $\leq \pm 1\%$ @ [0.7V 3V]
- $V_{tune} \sim V_{set} - V_{th}$
- output tune range [0.3V 1.9V] > 1.5V

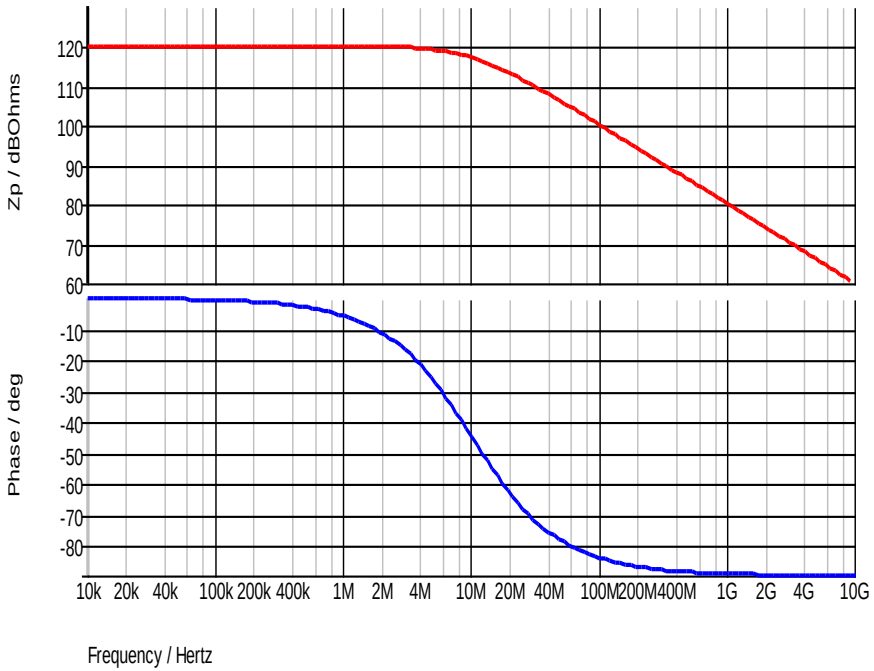
Current feedback opamp

- Transimpedance open loop amplifier
  - Vout = Zt(f) Iin- or iε
- Low impedance inverting input
  - Current error signal (iε)
- Dissymetric inputs
  - High impedance non-inverting input
  - Low impedance inverting input
  - Buffer that ensures Vin- = vin+
- State Equation :

$$Vin- = Vin+$$
$$Vout = Zt(\omega)\ Iin -$$

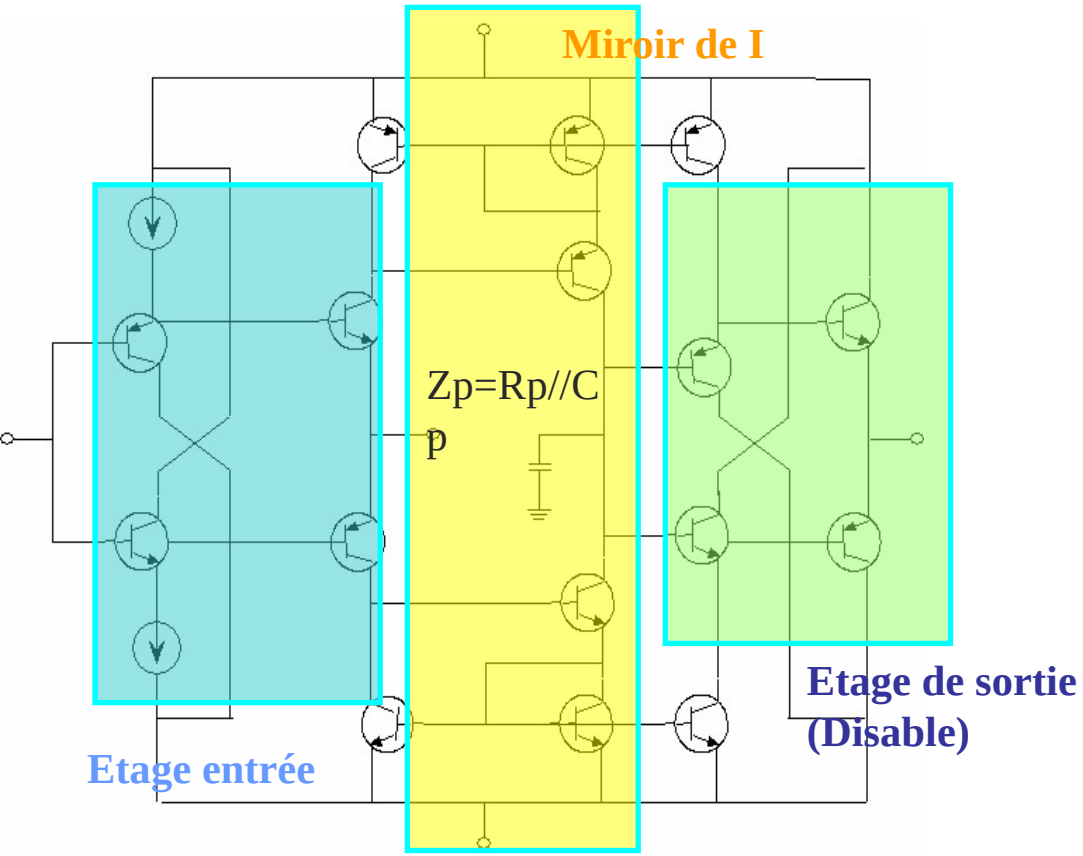
- Transimpedance varies with frequency
  - $Zt(\omega) = Rt/(1 + j\omega/RtCt)$
  - Typ : Rt=1MΩ, Ct=100 fF => f_0 ~ 1.6 MHz

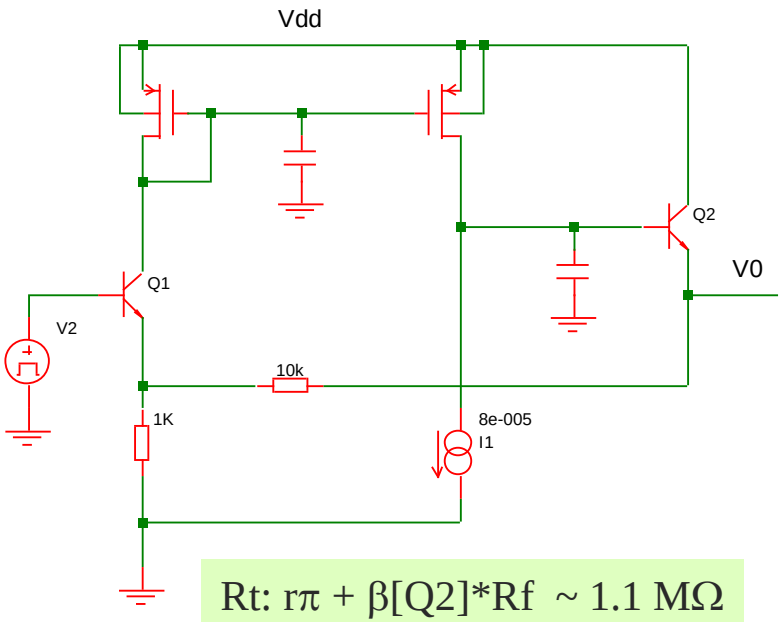




Practical realization

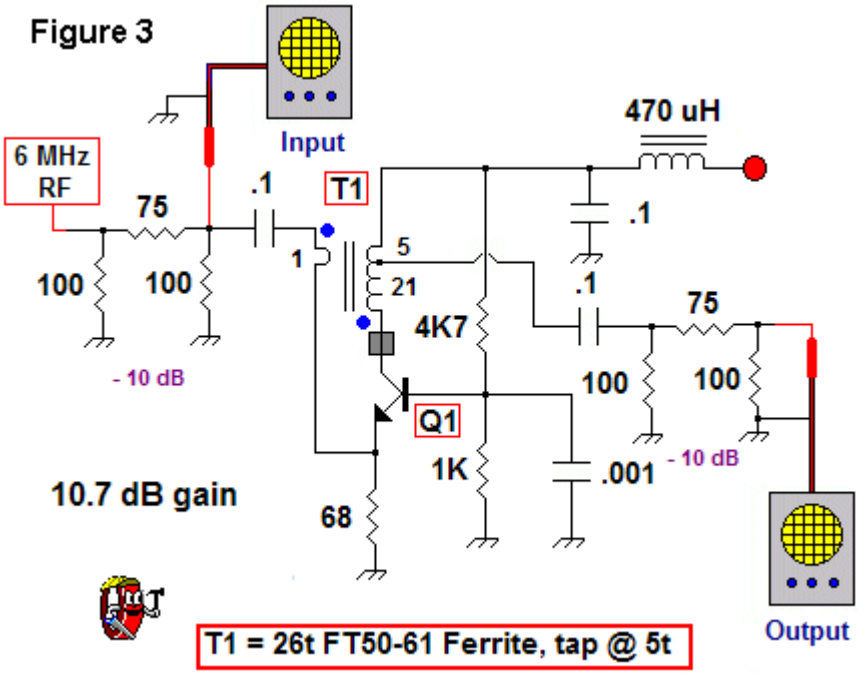
- CCII + buffer : “diamond”
- Commercial products : CLC400 (90’s)
- Custom design in 0.35µ

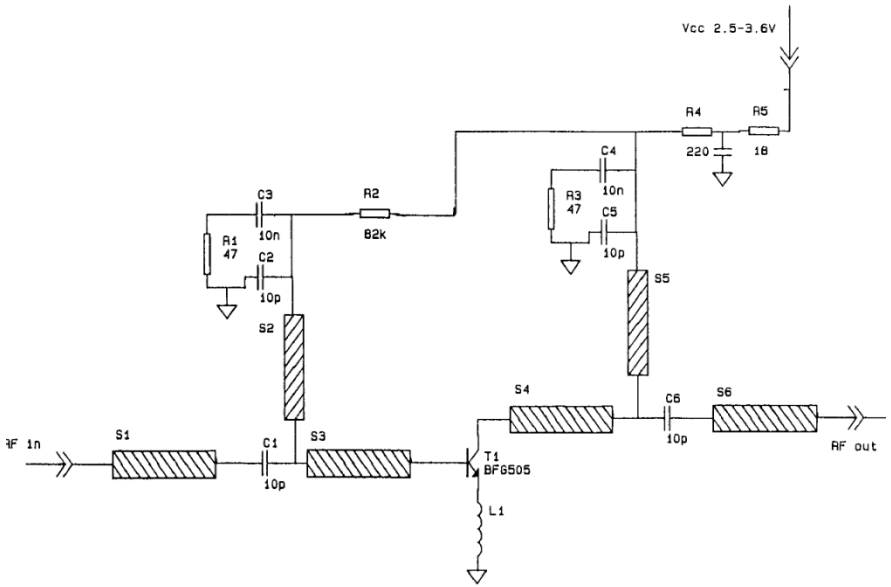




Rt: rπ + β[Q2]*Rf ~ 1.1 MΩ
Ct ~ 0.2 pF

High speed preamps…

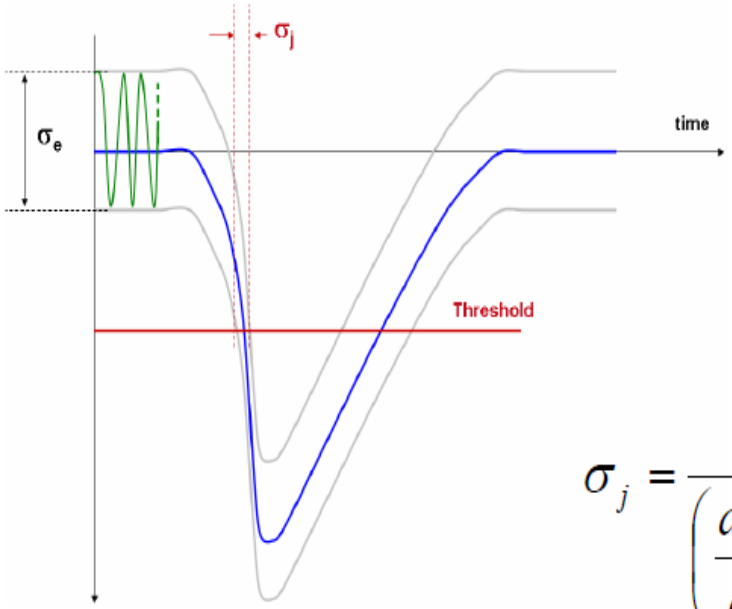




Noise and jitter

- Electronics noise dominated by series noise en
  - Large detector capacitance
  - For voltage preamp and load resistor RL,
  - Output rms noise $Vn^2=(en^2+4kTRs)\ G^2\ \pi/2*BW_{-3dB}$
  - Typical values : Rs=50 Ω, en=1 nV/√Hz Vn=1 mV for G=10, BW=1GHz
  - For current sensitive preamps, possible noise peaking due to Cd

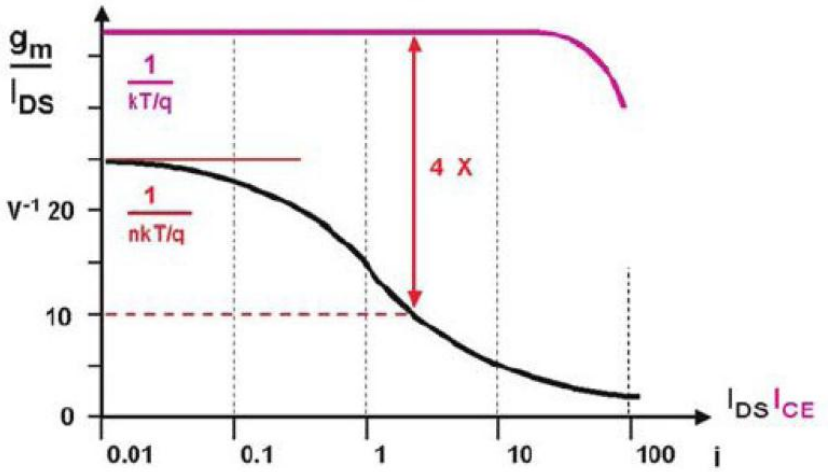
- Jitter
  - Part due to electronics noise :
  - σt = σv / (dV/dt)
  - Minimized by increasing BW

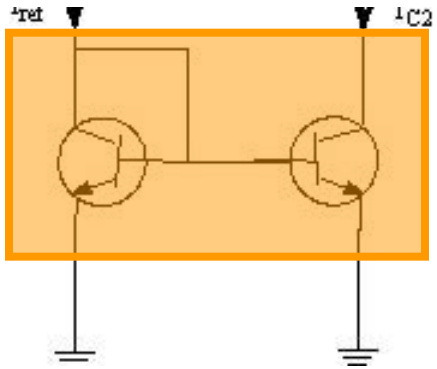


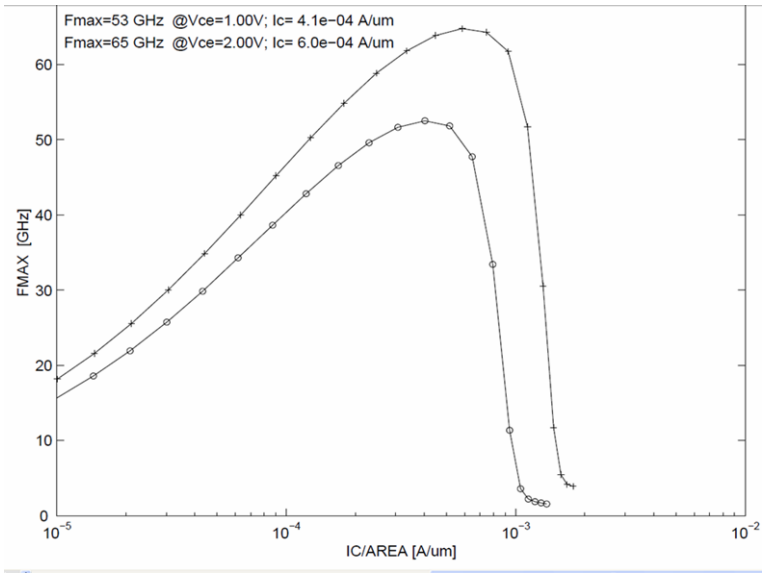
$$\sigma_j = \frac{\sigma_e}{\left(\frac{dV}{dt}\right)_{threshold}}$$

Power and speed with SiGe

- BJT : best g_m /I ratio $(1/U_T)$
  - Large transconductance with small d
- Speed goes as $F_T = g_m / 2\pi C$
  - C~10 fF g_m typ mA/V
  - F_T ~60 GHz for SiGe 0.35µm
  - Interesting for fast preamps
- Not forgetting 100V Early voltage and (A~mV*µm)
- $V_{BE}=V_T Ln(I_C/I_S)$
- Large swing : V_{CEsat} ~3 U_T



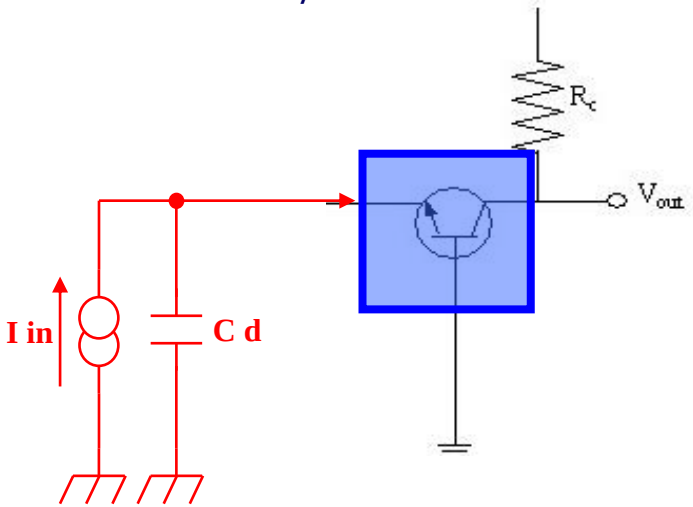




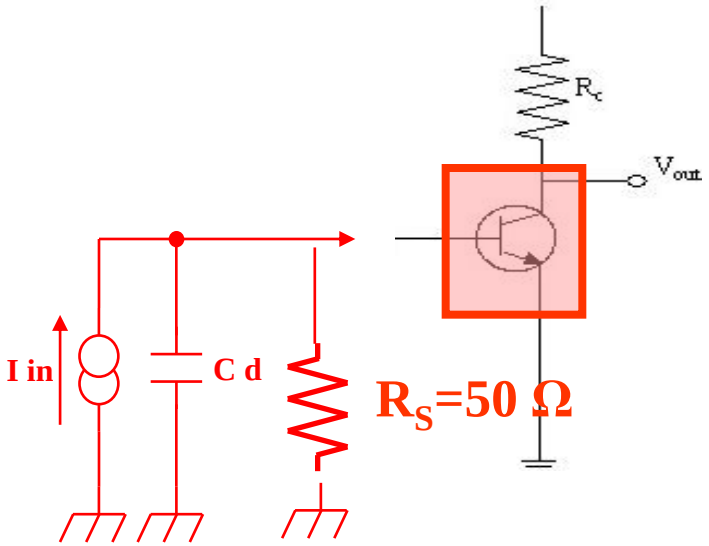
High speed configurations

- Open loop configurations : current conveyors, RF amplifiers
- Usually designed at transistor level MOS or SiGe

- **Current conveyors**
- Small Zin : current sensitive input
- Large Zout : current driven output
- Unity gain current conveyor
- E.g. : (super) common-base configuration
- Low input impedance : Rin=1/gm
- Transimpedance : Rc
- Bandwitdth : 1/2πRcCu > 1 GHz



- **RF amplifiers**
- Large Zin : voltage sensitive input
- Large Zout : current driven output
- Current conversion with resistor R_S
- E.g. common-emitter configuration
- Transimpedance : -gmRcRs
- Bandwitdth : 1/2πRsCt



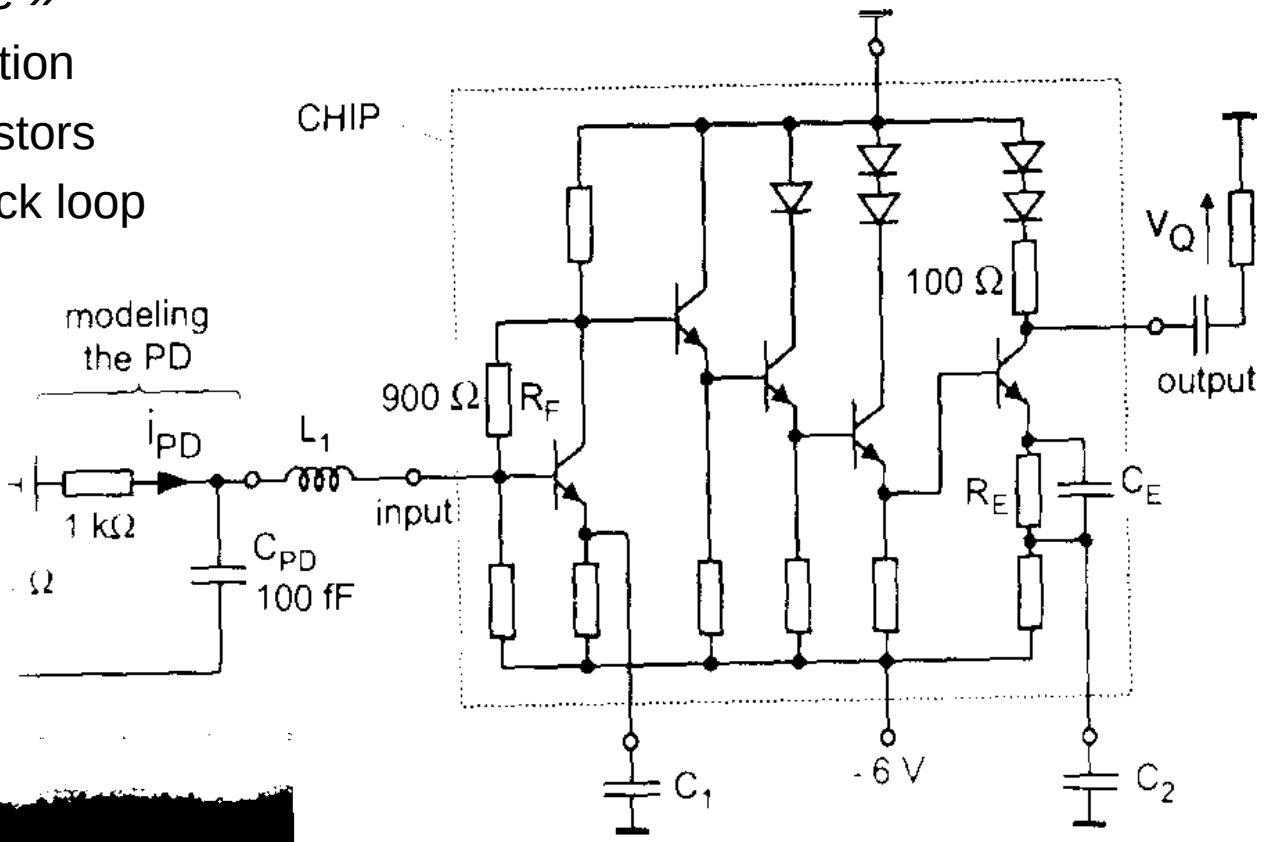
Experimental results

Testboard #3	RF (Common Emitter)	Common Base	Super Common Base
With 100pf/50 Ohm injector (SiPM emulation)		Vb_cb : 400 #DAC	Vb_scb : 1023 #DAC
Noise floor (pedestal)	185-187 #DAC / 1.196V	216-224 #DAC / 1.259V	340-342 #DAC / 1.514V
Signal value @ 10pe	235 #DAC / 1.300V	137 #DAC / 1.085V	115 #DAC / 1.038V
Signal amplitude @ 10pe (signal minus pedestal)	50 #DAC / 110mV	83 #DAC / 174mV	226 #DAC / 476mV
Gain (mV/pe)	**10.4mV/pe (5 #DAC/pe)**	**17.4mV (8.3 #DAC)**	**47.6mV/pe (22.6 #DAC/pe)**
Jitter - threshold 1 pe @10pe	**13ps RMS**	**6ps RMS**	**8ps RMS**
Jitter - threshold 3 pe @10pe	**8ps RMS**	**6ps RMS**	**8ps RMS**
With 100nF DC block (for voltage gain & BW meas.)	**18mV injection**	**18mV injection**	**7mV injection**
Signal Value	267 #DAC / 1.371V	41 #DAC / 0.884V	192 #DAC / 1.2V
Signal amplitude (signal minus pedestal)	81 #DAC / 175mV	179 #DAC / 375mV	150 #DAC / 320mV
Voltage gain (before 50 ohm bridge => factor of 0 .5)	**4.86 V/V**	**10.4 V/V**	**22.5 V/V**
Bandwidth, after discriminator (Δt 10% T50% meas.)	**Δt : 150ps / 660MHz**	**Δt : 360ps / 280MHz**	**Δt : 400ps / 250MHz**

With 1pe-=160 fC

40 Gb/s transimpedance amplifier

- « Simple architecture »
  - CE + CC configuration
  - SiGe bipolar transistors
  - CC outside feedback loop
  - « pole splitting »



Conclusion

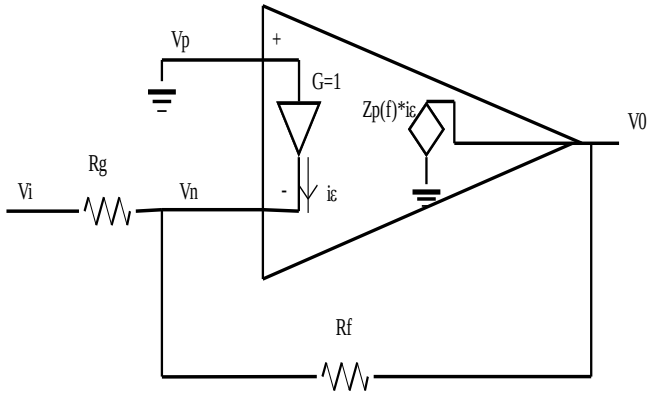
- A good preamp is necessary but not enough to make a good chip….

Backup

Closed loop gain

- Inverting voltage gain
  - Iin- = -Vin/Rg - Vout/Rf
  - Vout = Zt Iin-

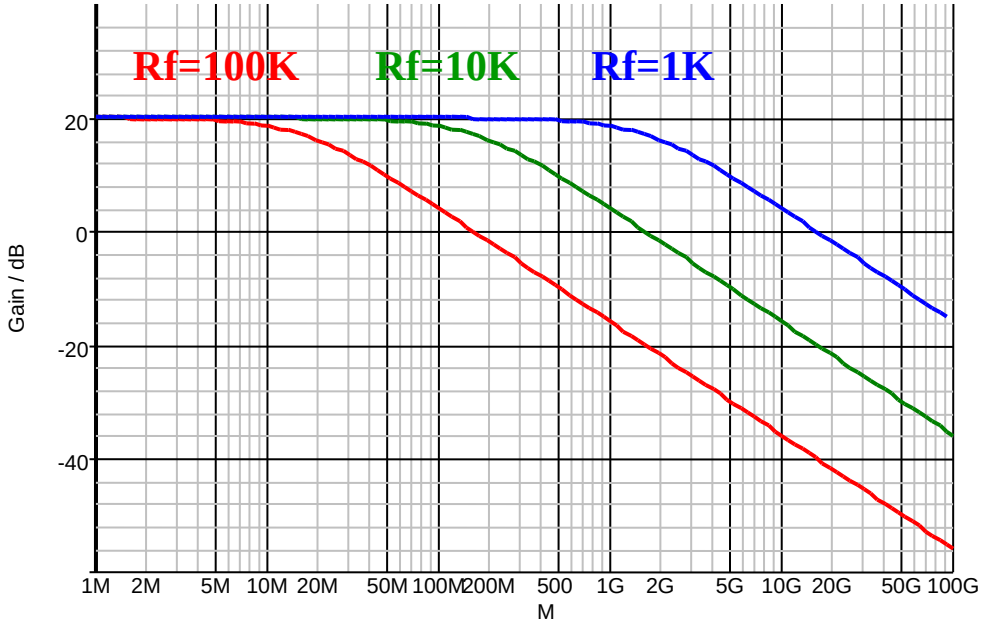
$$\frac{V_0}{V_i} = -\frac{R_f}{R_g}\frac{1}{1+\frac{R_f}{Z_T}}$$



- Bandwidth
  - Replacing Zt= Rt/(1 + jω/RtCt)

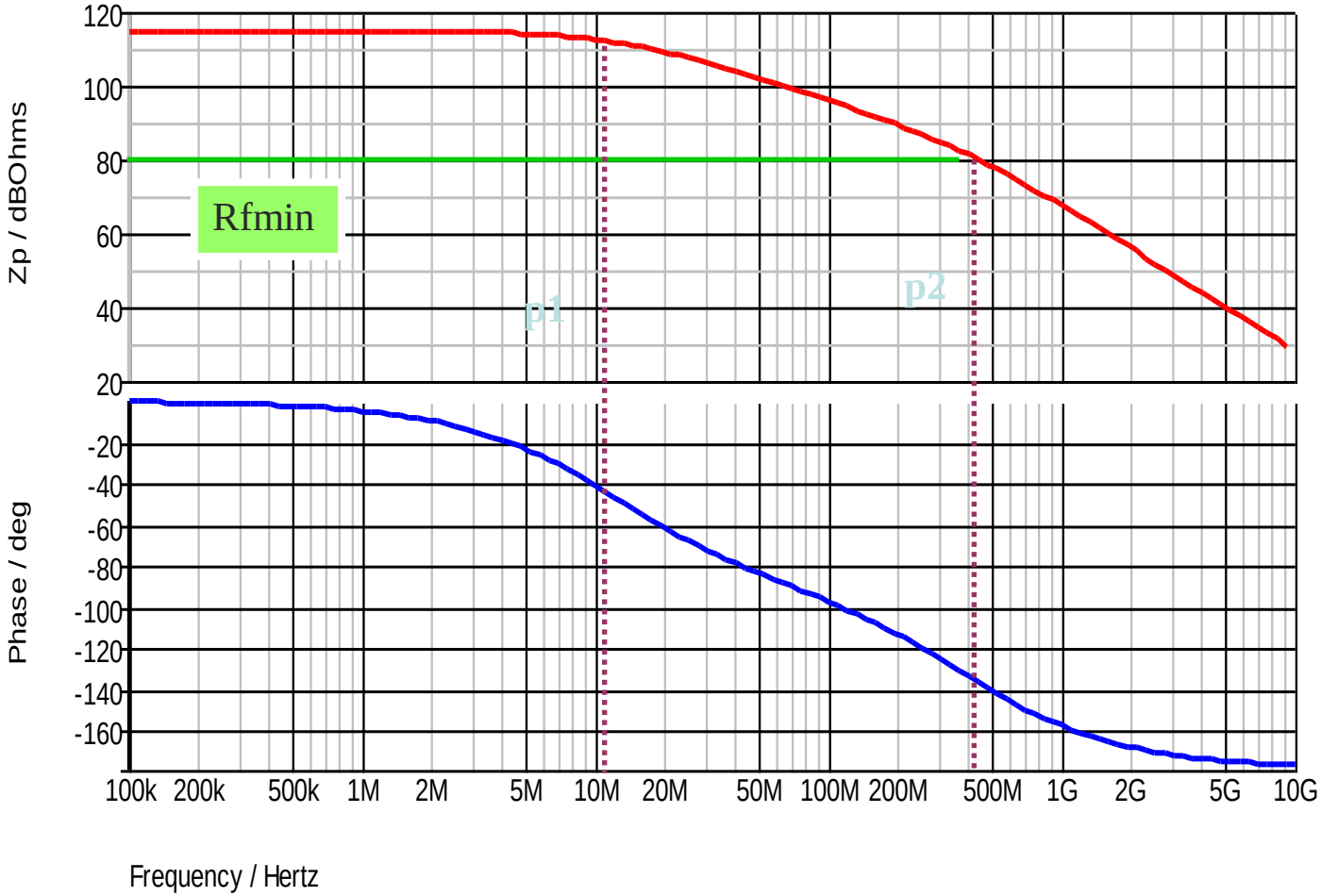
$$\frac{V_0}{V_i} = -\frac{R_f}{R_g}\frac{1}{1+\mathrm{j}\,\omega R_f C_T}$$

  - Bandwidth depends only on Rf (not Rg)
- Bandwidth independent of closed loop gain !



Stability analysis

- Evaluation of feedback ratio : β = Iin-/Vout = 1/Rf
- Stability if |1/aβ| > 1
- Gives a Rfmin such that a(p2) = Rfmin (phase margin 45°)

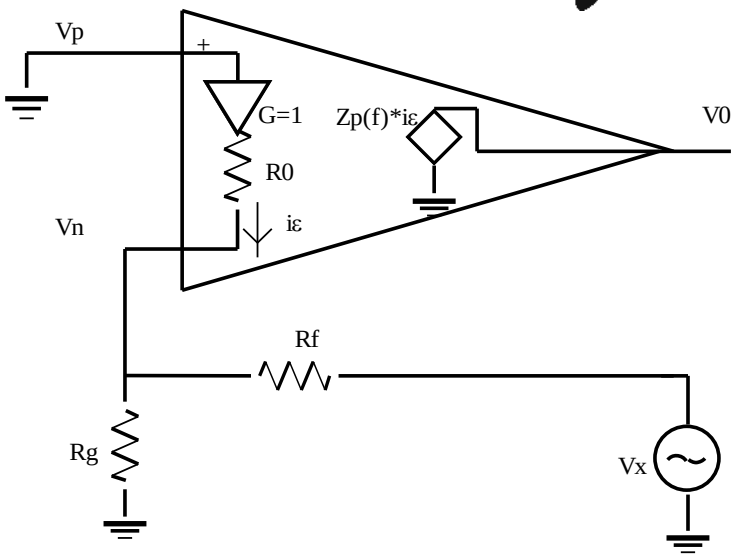


2nd order effects

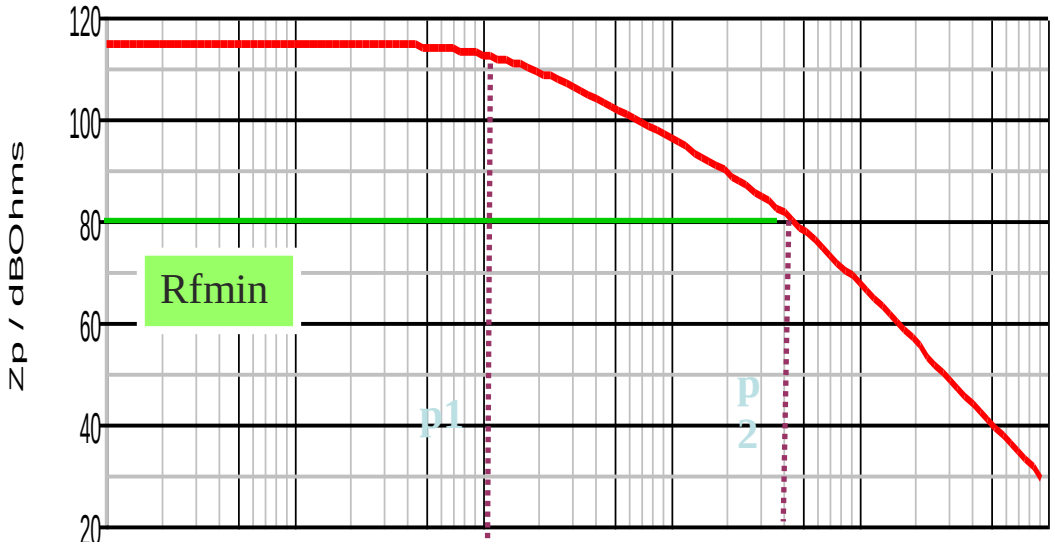
- Input buffer has finite impedance : R0 (typ 50Ω)
- Calculating feedback β :

$$i_\varepsilon = \frac{V_x}{R_f + R_g // R_0} \frac{R_g}{R_g + R_0}$$

$$\frac{1}{\beta} = R_f . \left(1 + \frac{R_0}{R_g // R_f}\right)$$

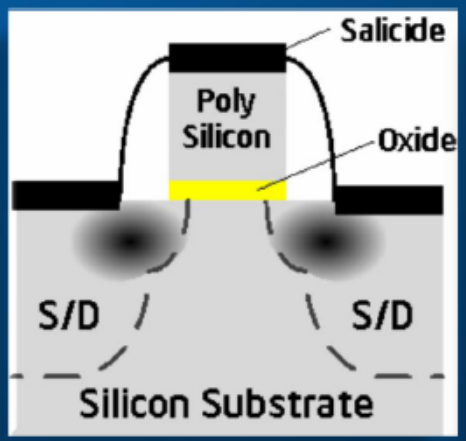


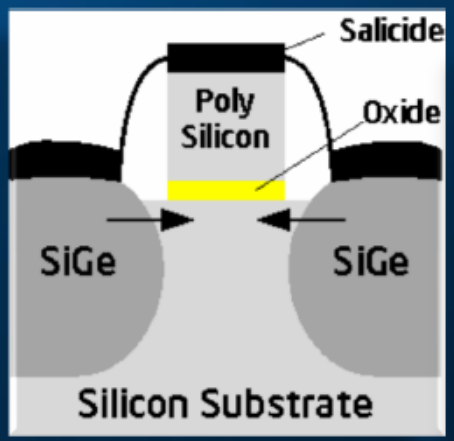
- Bandwidth changes with closed loop gain $A_0=1+R_f/R_g$
  - f-3dB = $f_0 Z_0/(1+R_0 A_0)$
  - Rf can often be decreased to keep 1/B = Rfmin

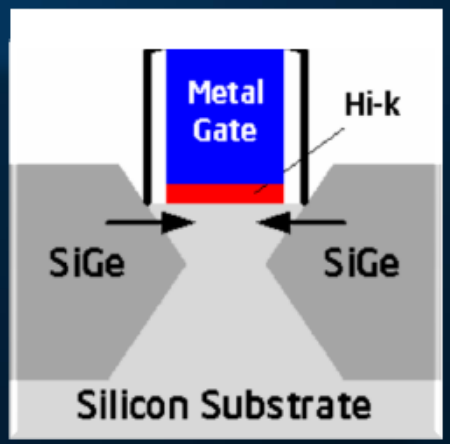


Intel CMOS Transistor Architecture Evolution in the Last Decade

.13 um and before	90nm/65 nm	45 nm/32 nm
Traditional	Strained Silicon	High k/Metal Gate + Strained Silicon



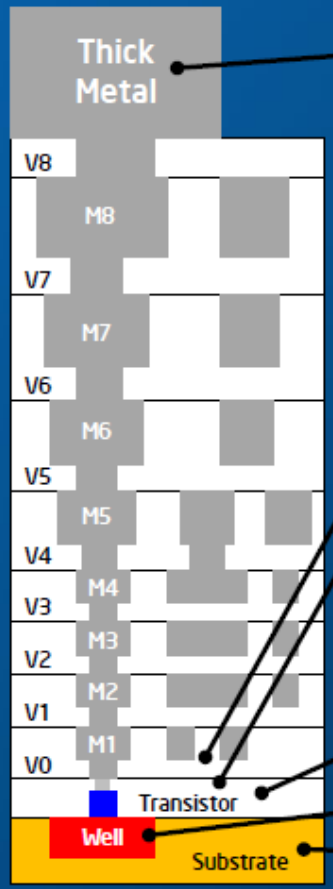




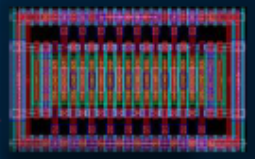
CMOS scaling has evolved from classical dimensional scaling to modern scaling with innovations in structures and materials

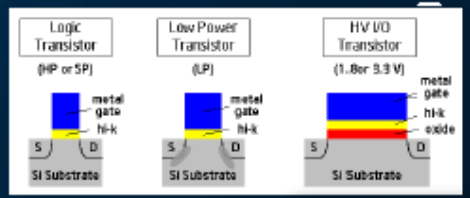
C.-H. Jan, Dec/10 IEDM '10, San Francisco 7

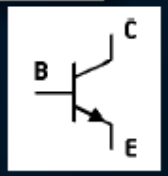
32 nm RF CMOS Technology

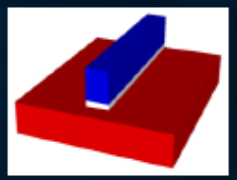


- TM1 Inductor: high Q and density
- Passives:
  - Precision Resistor
  - High Q Inductor
  - High Density Decap
- HV PA Transistor
- RF Transistor: Templates/Modeling
- Transistor:
  - Logic, low power, I/O
  - JFET, BJT
- Well: Triple Well/Deep Nwell
- Substrate: High Resistivity

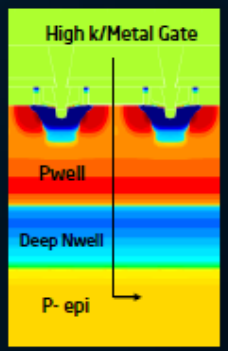






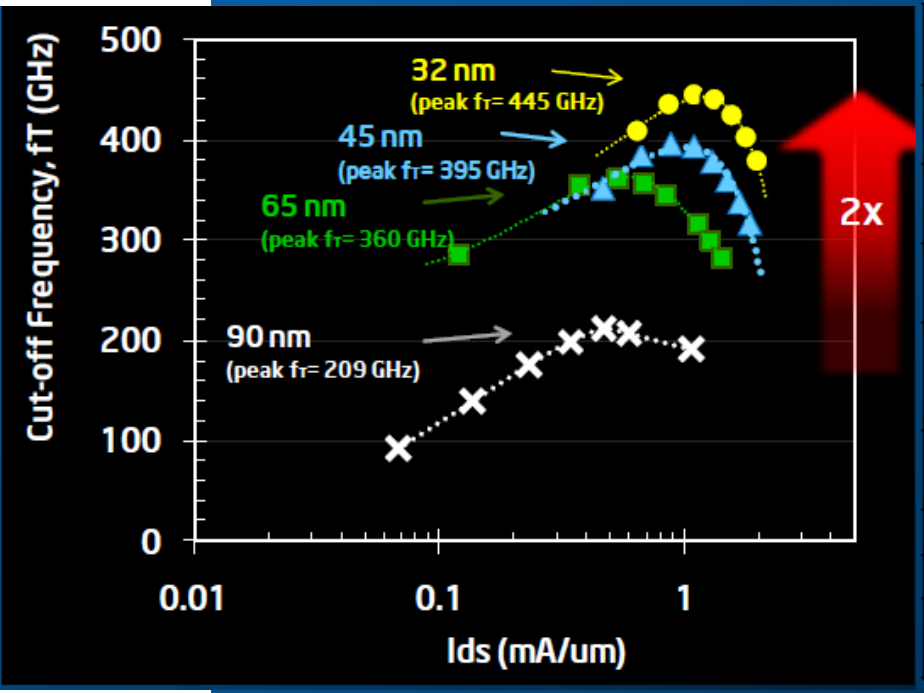


RF Models



Basic 32 nm CMOS technology is expanded with many more mixed signals/RF features to meet RF SoC requirements

RF CMOS Technology Performance Metrics



RF Devices	RF Circuits	Key Device Characteristics
Logic Transistor	MAC/BB, ADC, DAC	Idsat, Idlin, Vt, Ioff
Analog Transistor	ADC, DAC, MAC/BB	Gm, Rout, Matching, Linearity, Noise, NF_{min}
RF Transistor	PA, Mixer, T/R Switch	f_T, f_{max}, 1/f Noise, NF_{min}
PA Transistors	PA	Ron, Linearity, f_T, f_{MAX}, Efficiency, Breakdwn V,
Precision Resistors	ADC, DAC, BB Filter, others	R, σR/R, Matching
Linear Capacitors	PLL, VCO	C, Q, Matching
Varactors	PLL, VCO	Tuning Ratio, Q, Kv_{CO},
Inductor/ Transformer/Balun	PA, LNA, Mixer	L, Q

What are the impacts of CMOS scaling on these metrics ?

C.-H. Jan, Dec/10 IEDM '10, San Francisco 11

Generic MOSFET scaling trends

Novel materials and architectures

http://www.sematech.org/meetings/archives/symposia/9027/pres/Session%202/Jammy_Raj.pdf

New Mat'l/Structure

High-K
MG

planar

45nm
2007

32nm
2009

22nm
2011+

16nm (?)
2013+

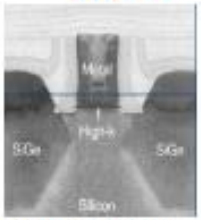
12 nm + (2015+)

III-V Device

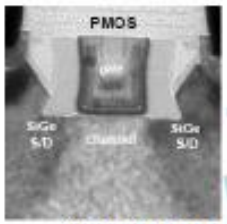
Si-Ge Device

Intel,
IEDM 2007,9

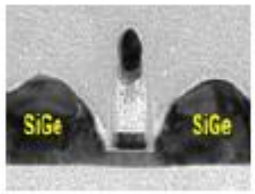
T-FET



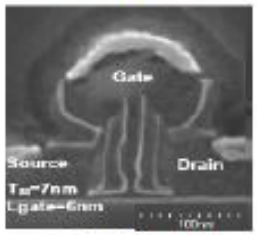
(Production)
Intel IEDM 2007



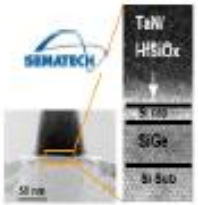
(Production)
Intel IEDM 2009

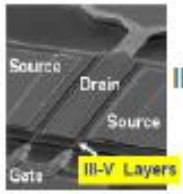


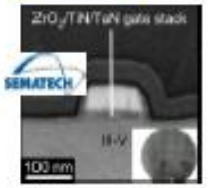
IBM, IEDM 2009



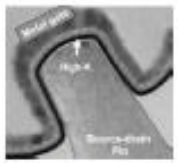
6nm Length
B. Doris IEDM 2002





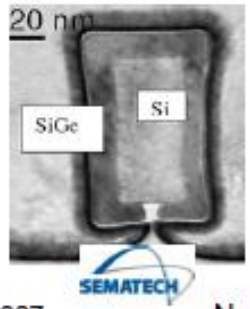


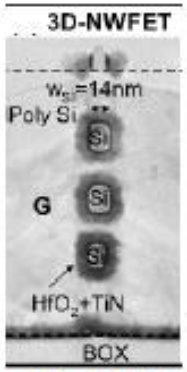
Non-planar



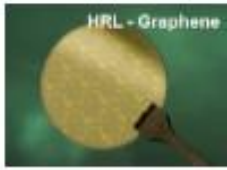
Intel Tri-Gate,
VLSI 2006

NXP FINFET, VLSI 2007





Nano-wire (LETI IEDM'08)



Signal & Source modelization

Vacuum Photomultipliers

G = 10^5 – 10^7

Cd ~ 10 pF

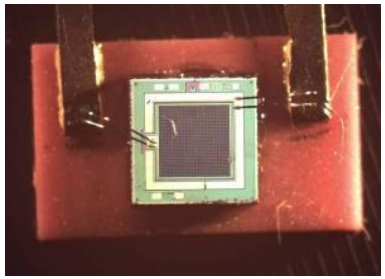
L ~ 10 nH

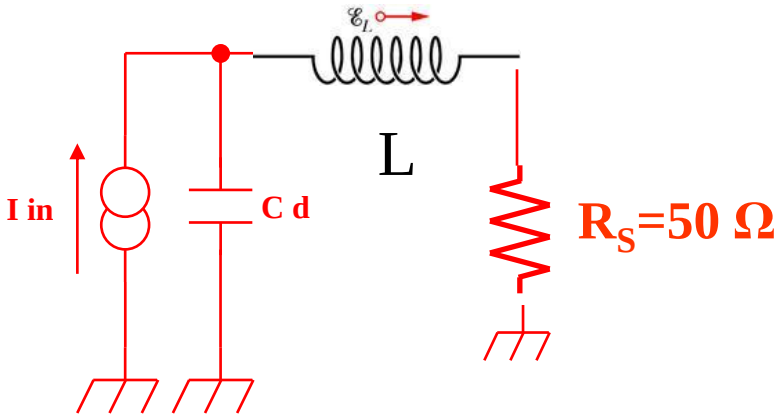
Silicon Photomultipliers

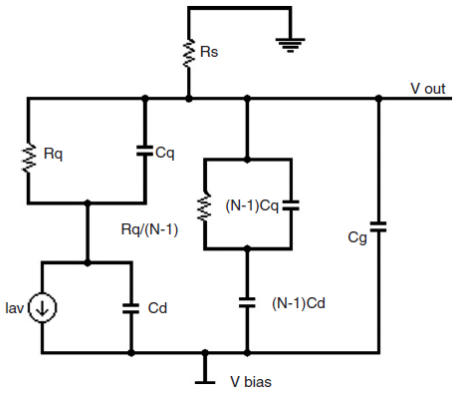
G = 10^5 – 10^7

C = 10 - 400 pF

L = 1 – 10 nH

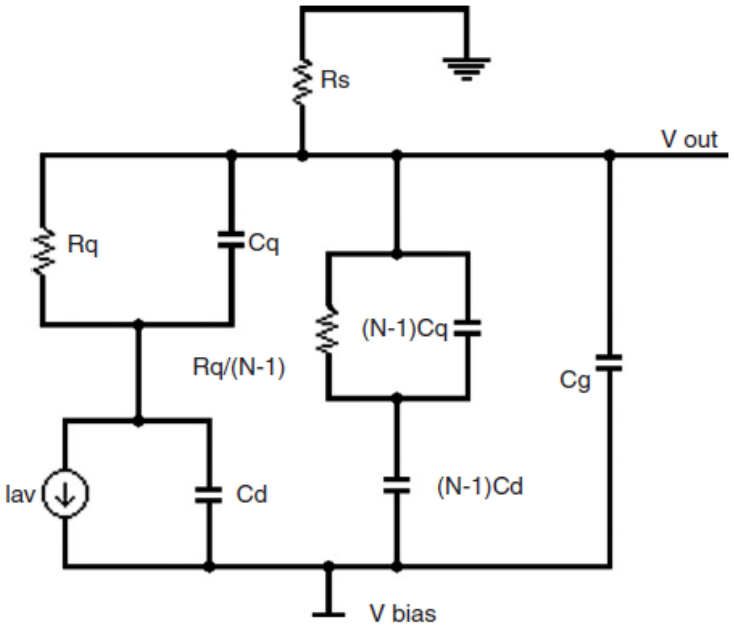






SiPM modelization

- Modelization by Corsi et al [NIM A572 2007]



[F. Corsi et al. NIM A572]

SiPM IRST, $N = 625$, $V_{bias} = 35$ V	
R_q (kΩ)	393.75
V_{br} (V)	31.2
Q (fC)	148.5
C_d (fF)	34.13
C_s (fF)	4.95
C_g (pF)	27.34

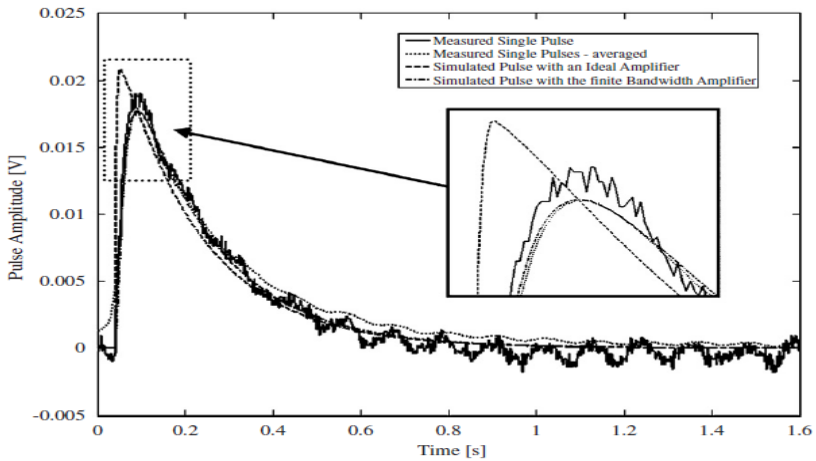


Fig. 2. Fitting of real data with the simulation results on the device model.

Electrical model of a SiPM

Collazuol 2008

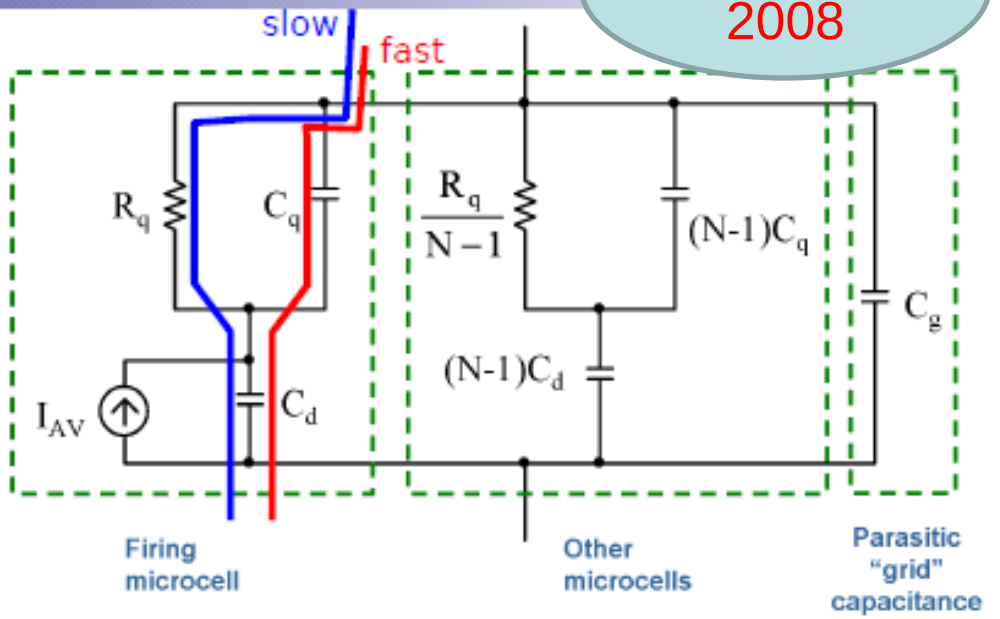
R_q: quenching resistor (hundreds of kΩ)

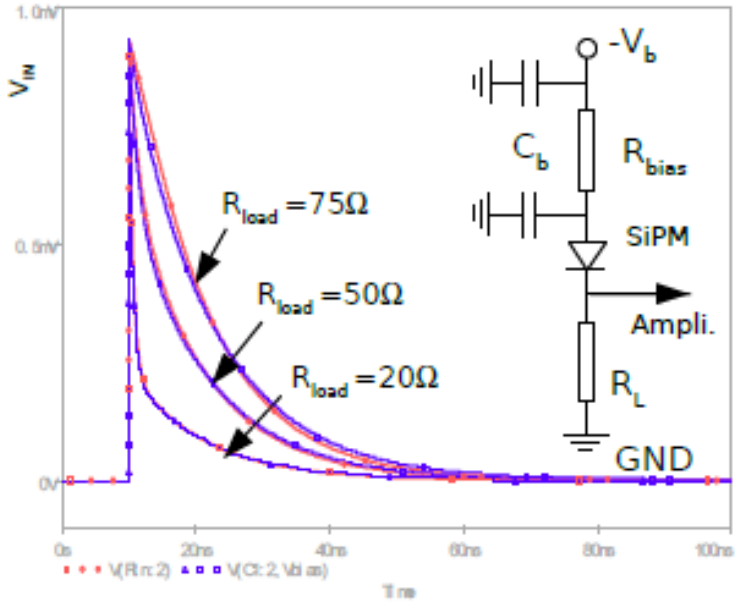
C_d: junction capacitance (few tens of fF)

C_q: parasitic capacitance in parallel to R_q (few tens of fF, $C_q < C_d$)

I_{AV}: SiPM ~ ideal current source current source modeling the total charge delivered by a cell during the avalanche $Q=\Delta V(C_d+C_q)$

C_g: parasitic capacitance due to the routing of Vbias to the cells (metal grid, few tens of pF)





1) the peak of V_{IN} is independent of R_s

A constant fraction Q_{IN} of the charge Q delivered during the avalanche is instantly collected on $C_{tot}=C_q+C_{eq}$.

2) The circuit has two time constants:

- $\tau_{IN} = R_L\, C_{tot}$ (fast)
- $\tau_r = R_q\,(C_d+C_q)$ (slow)

Decreasing R_s, the time constant τ_{IN} decreases, the current on R_s increases and the collection of Q is faster

F. Corsi, C. Mazzocca et al.

SiPM equivalent circuit

Collazuol 2010

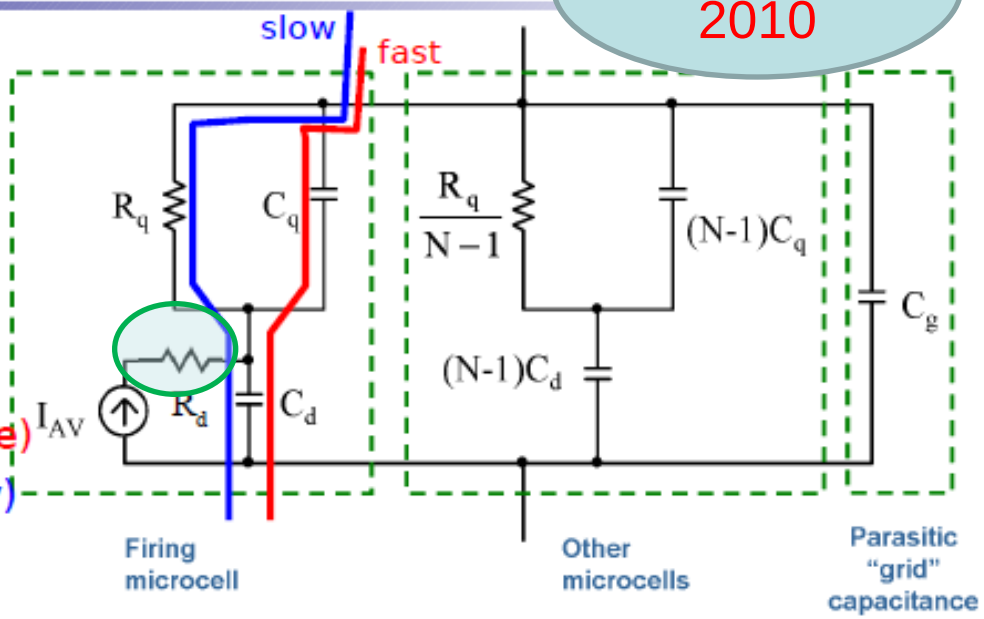
Single cell model → $(R_d||C_d)+(R_q||C_q)$

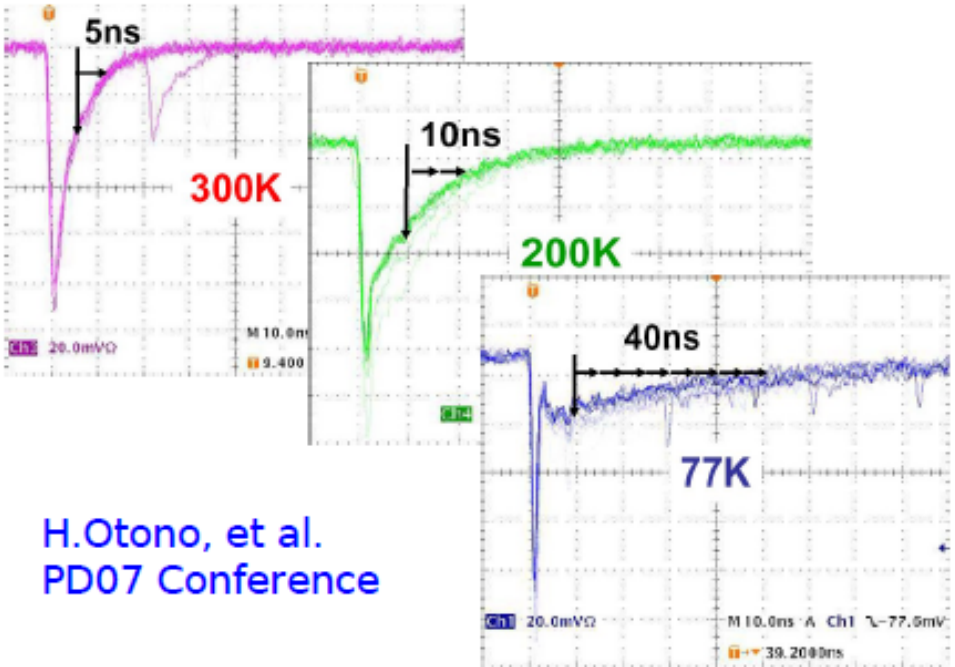
SiPM + load → $(||Z_{cell})||C_{grid} + Z_{load}$

Signal = slow pulse ($\tau_{d\ (rise)}$, $\tau_{q\text{-}slow\ (fall)}$) +
+ fast pulse ($\tau_{d\ (rise)}$, $\tau_{q\text{-}fast\ (fall)}$)

- $\tau_{d\ (rise)} \sim R_d(C_q+C_d)$
- $\tau_{q\text{-}fast\ (fall)} = R_{load}\ C_{tot}$ (fast; parasitic spike)
- $\tau_{q\text{-}slow\ (fall)} = R_q\ (C_q+C_d)$ (slow; cell recovery)

F. Corsi, et al. NIMA 572(2007)





H.Otono, et al.
PD07 Conference

Pulse shape:

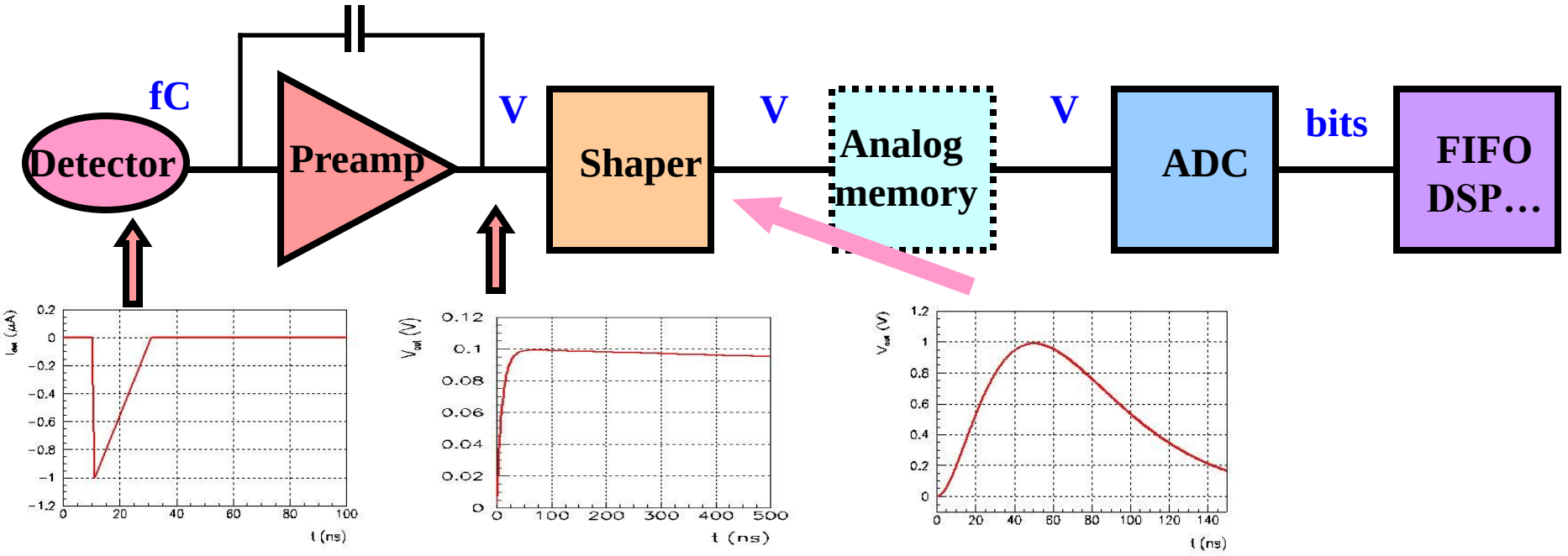
The two current components show different behavior with Temperature

→ fast component is independent of T because stray C_q couple with external R_{load} (no dependence on T) while R_q is strongly dependent on T

(we used low light level, BW filters against noise and AC coupling → difficult to disentangle the two components)

Overview of readout electronics

- Most front-ends follow a similar architecture



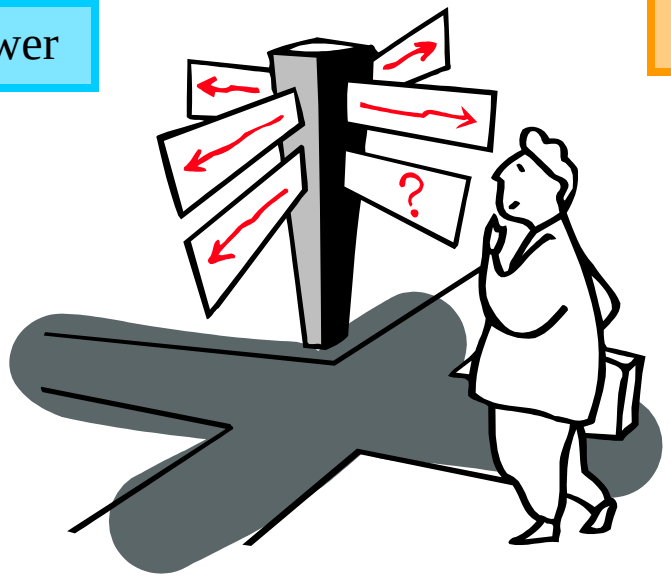
- Very small signals (fC) -> need amplification
- Measurement of amplitude and/or time (ADCs, discris, TDCs)
- Several thousands to millions of channels
- Trends : high speed, low power

Readout electronics : requirements

Low noise

Low power

High speed



High reliability

Large dynamic range

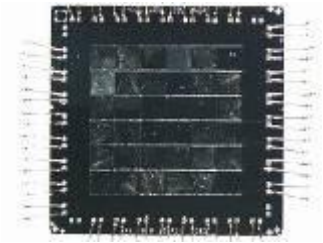
Radiation hardness

Low cost !
(and even less)

Low material

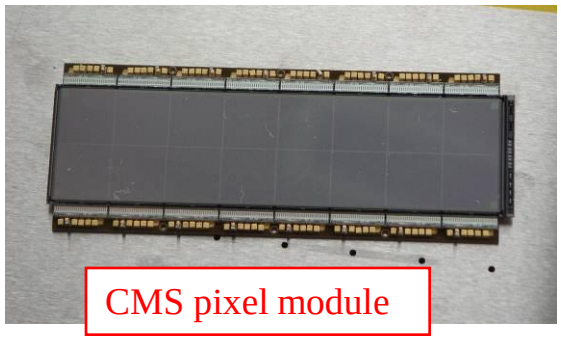
Detector(s)

- A large variety
- A similar modelization



6x6 pixels,4x4 mm^2
HgTe absorbers, 65 mK
12 eV @ 6 keV

PMT in ANTARES



CMS pixel module

ATLAS LAr calorimeter

A few (personal) comments

- Strong push for high speed front-end > GHz
  - Essential for timing measurements
  - Several configurations to get GBW > 10 GHz
  - Optimum use of SiGe bipolar transiistors

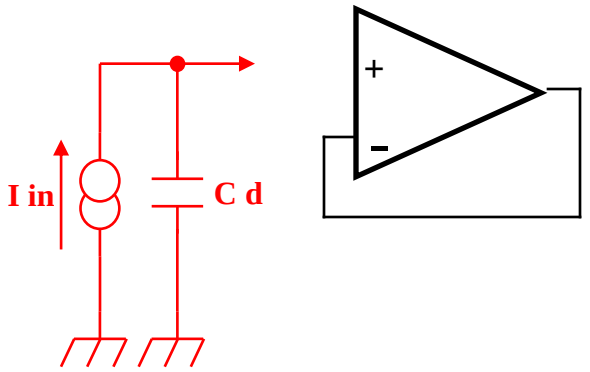
- Voltage sensitive front-end
  - Easiest : 50Ω termination, many commercial amplifiers (mini circuit…)
  - Beware of power dissipation
  - Easy multi-gain (time and charge)

- Current sensitive front-end
  - Potentially lower noise, lower input impdance
  - Largest GBW product

- In all cases, importance of reducing stray inductance

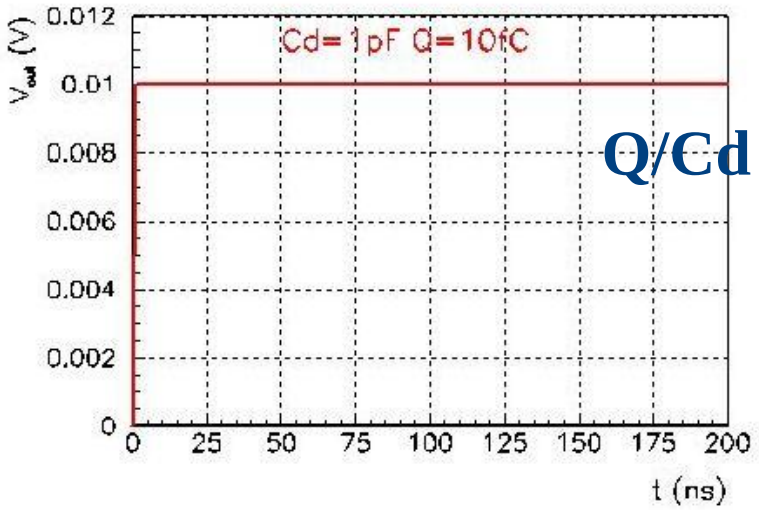
Reading the signal

- Signal
  - Signal = current source
  - Detector = capacitance C_d
  - Quantity to measure
    - Charge => integrator needed
    - Time => discriminator + TDC



Voltage readout

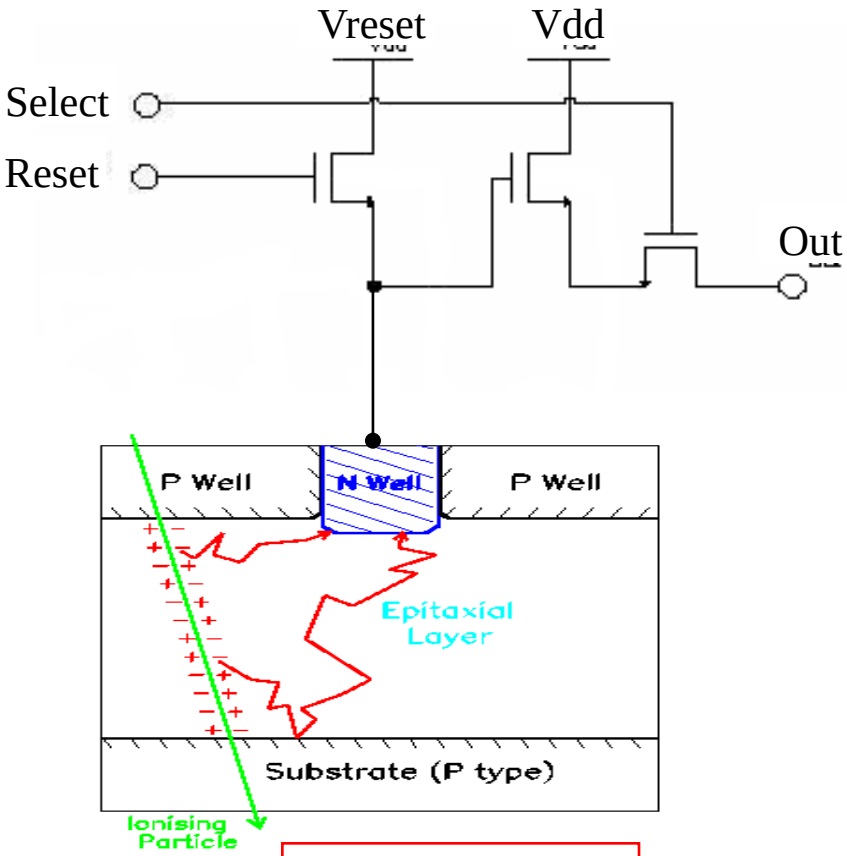
- Integrating on Cd
  - Simple : $V = Q/C_d$
  - « Gain » : $1/C_d$: 1 pF -> 1 mV/fC
  - Need a follower to buffer the voltage… => parasitic capacitance
  - Fast : speed of buffer
  - Gain loss, possible non-linearities
  - crosstalk
  - Need to empty Cd…



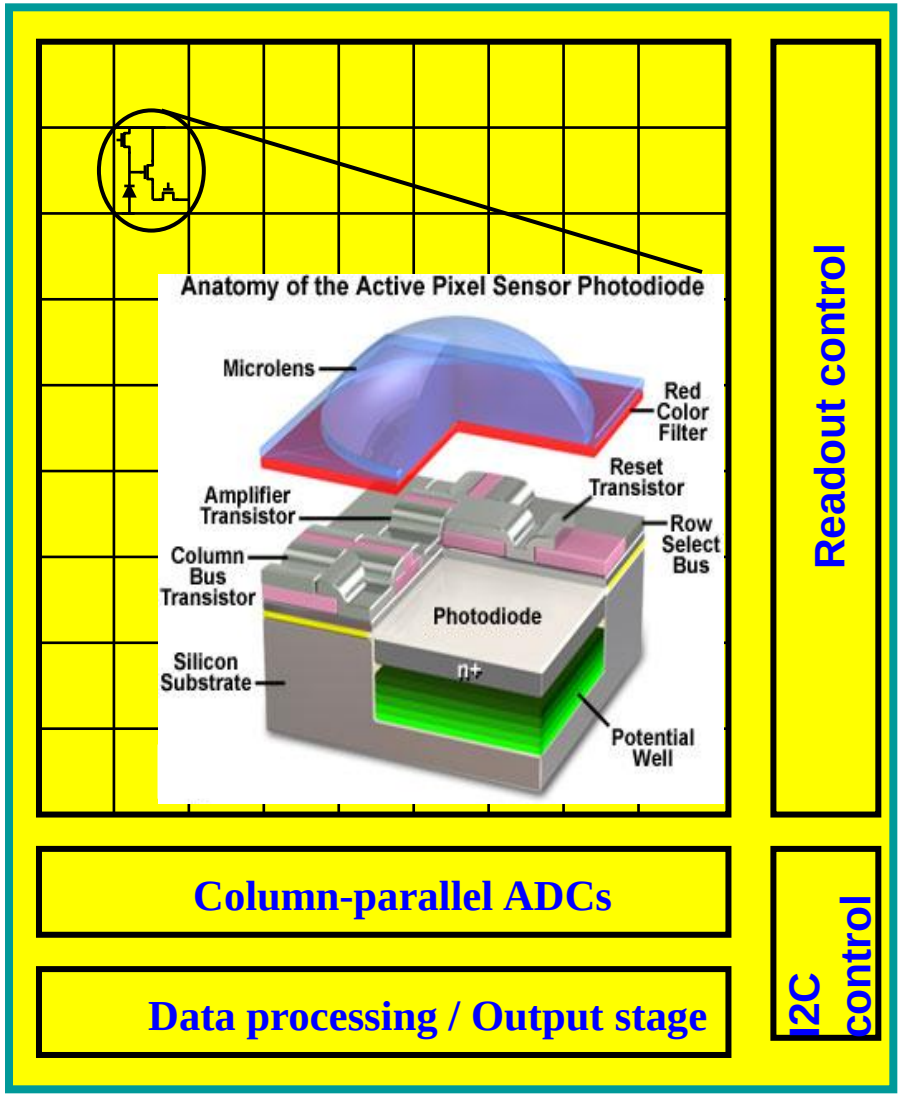
Impulse response

Monolithic active pixels

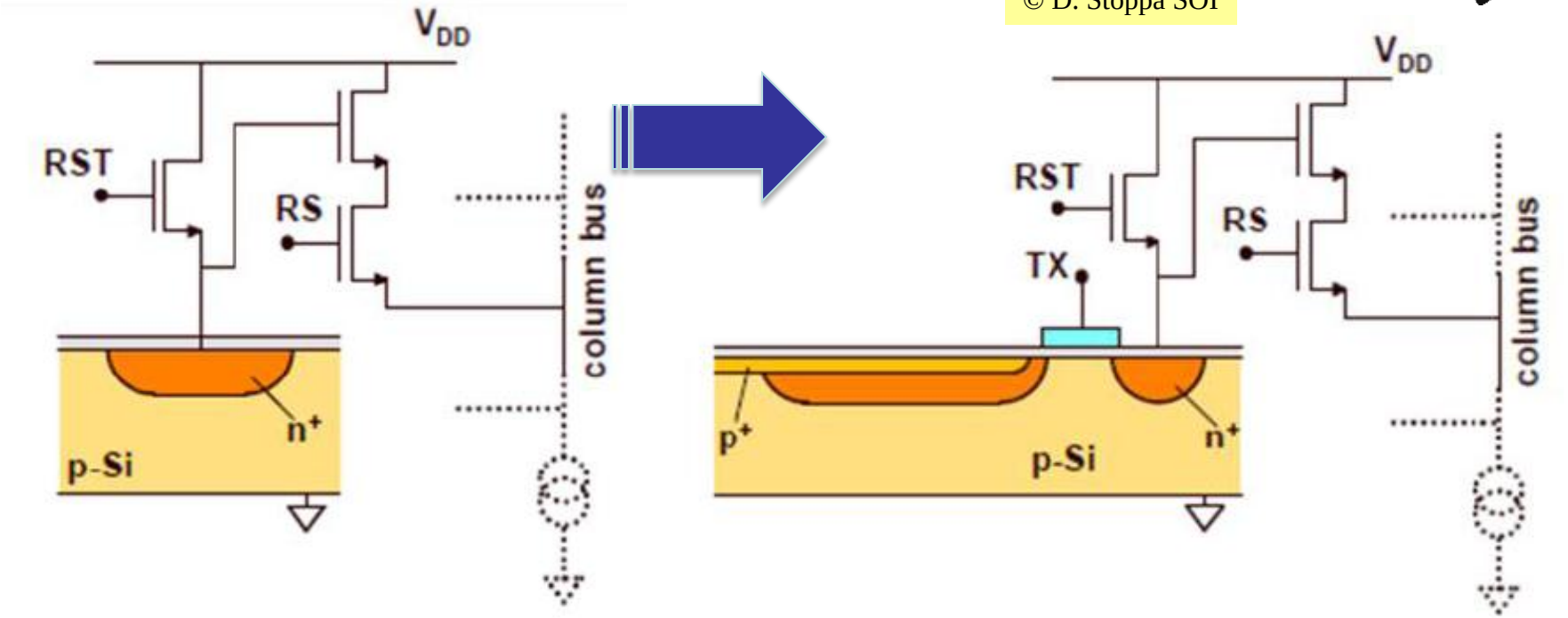
- Collect charge by diffusion
- Read ~100 e- on Cd~10fF = few mV



MAPS readout



CMOS Image Sensor Technology

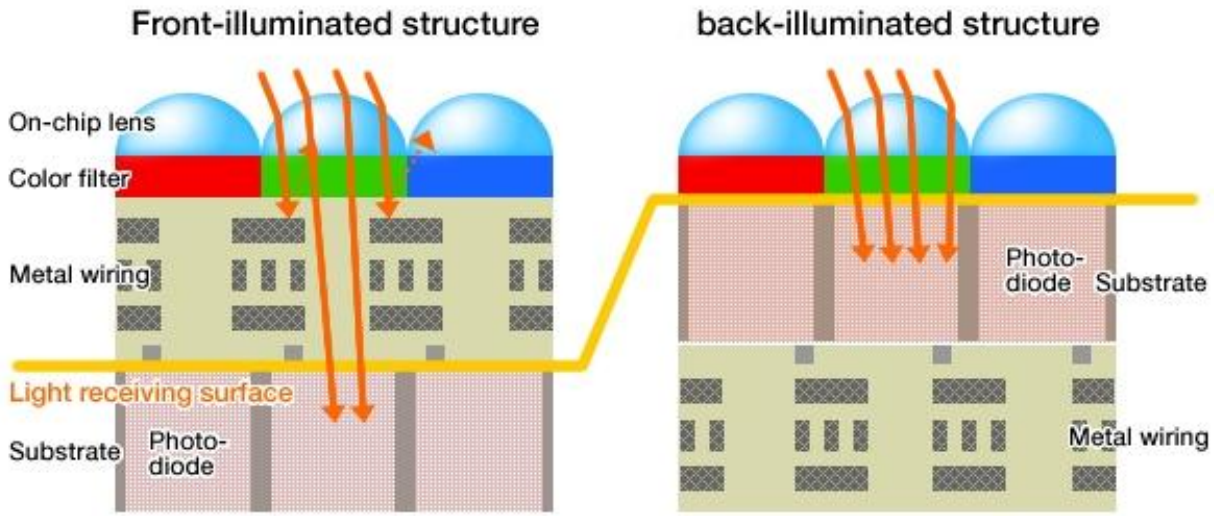


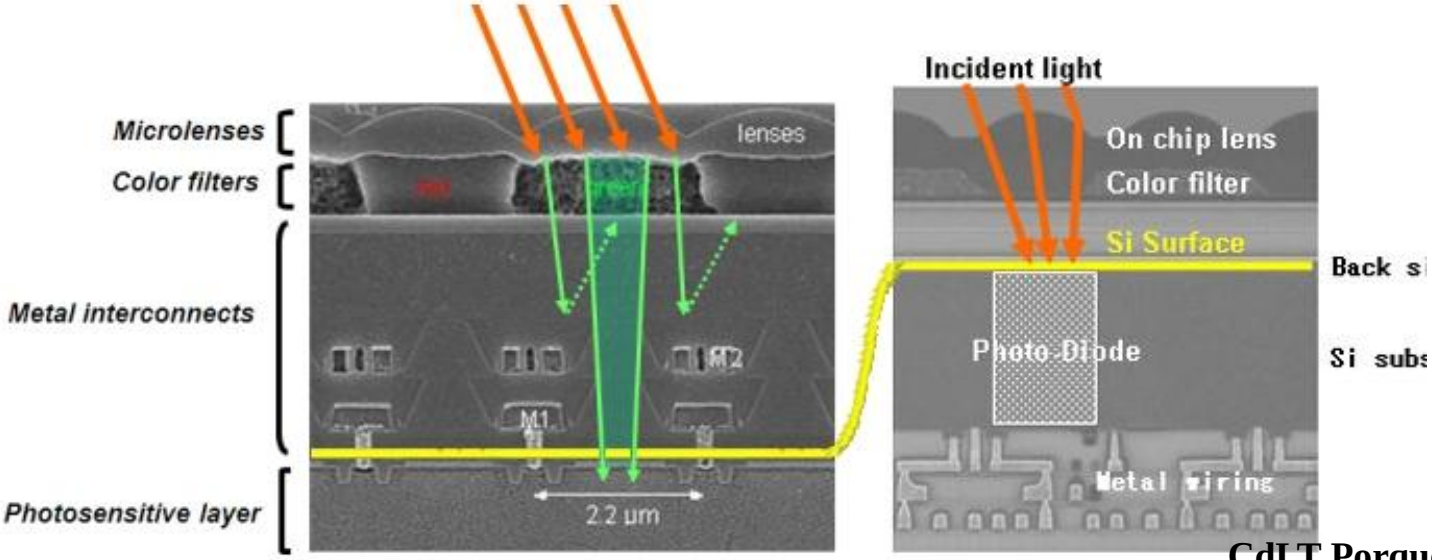
http://indico.cern.ch/conferenceTimeTable.py?confId=170595#20120

Pinned photodiode:

- 1/10 dark current
- Integration capacitance is small (floating diffusion)
- Correlated-Double-Sampling -> no more kT/C
- Sharing of in-pixel electronics

CMOS Image Sensor Technology

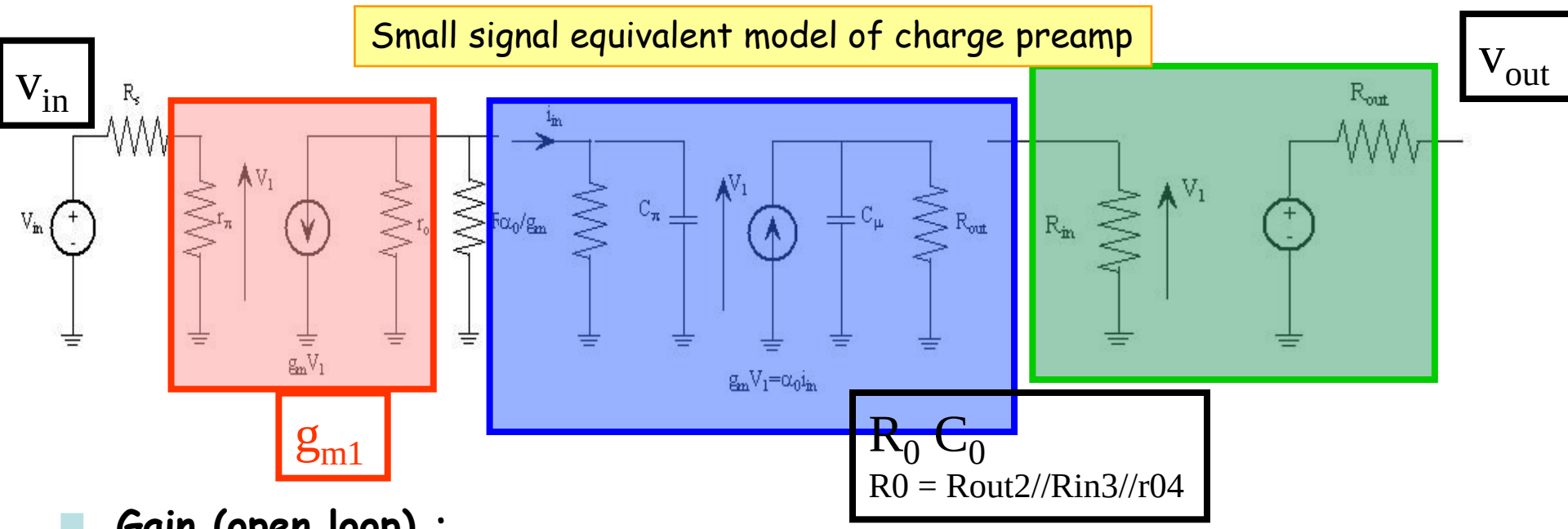




- 65nm CMOS-CIS, Pinned photodiode:
- Pixel pitch <**1.1um**
- Global shutter, **DR>80dB**
- Extra pixel-level circuitry (8um pitch)
- Rolling shutter, **DR>140dB**
- In-pixel Buried SF, High-Gain Column Amplifier and CMS:
- **PN<0.7e**
- Special Column-level ADCs:UHDTV,
- 3**3Mpixel@120fps**

Example : designing a charge preamp (3)

- Small signal equivalent model
  - Transistors are replaced by hybrid π model
  - Allows to calculate open loop gain



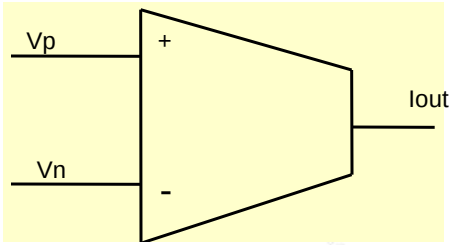
- **Gain (open loop) :**

$$v_{out}/v_{in} = - g_{m1} R_0 /(1 + j\omega R_0 C_0)$$

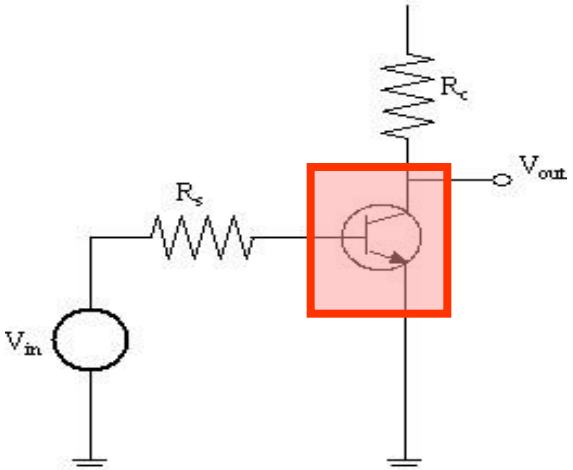
- *Ex : g_{m1}=20mA/V , R_0=500kΩ, C_0=1pF => G_0=10^4 ω_0=210^6 $G_0\omega_0$=2 10^{10} = 3 GHz !*

Transconductance amplifier (OTA)

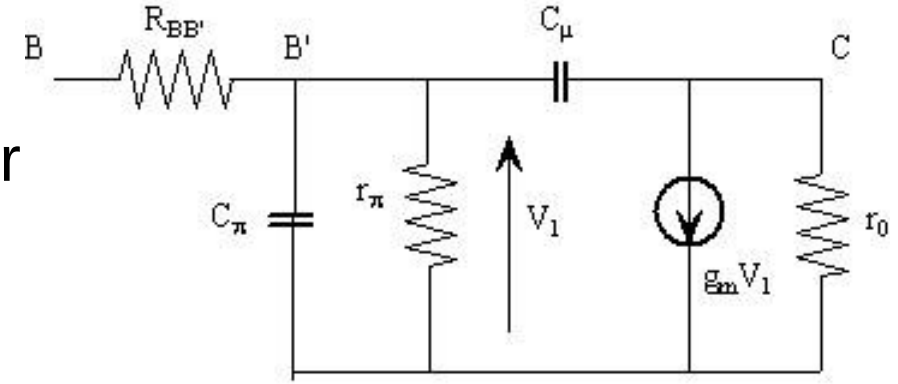
- Voltage input : large Zin
- Current output : large Zout
- V2I conversion : Iout= Gm(ω) Vin diff



- Simplest form : transistor Common Emitter
  - Voltage controlled current source $g_m v_{BE}$
  - Transconductance : $\mathbf{g_m} = \partial I_C / \partial V_{BE} = I_C / U_T$
  - Can be varied by changing I_C
  - Large input resistance $r_\pi = \beta_0 / g_m$
  - Large output resistance $r_0 = V_A / I_C$



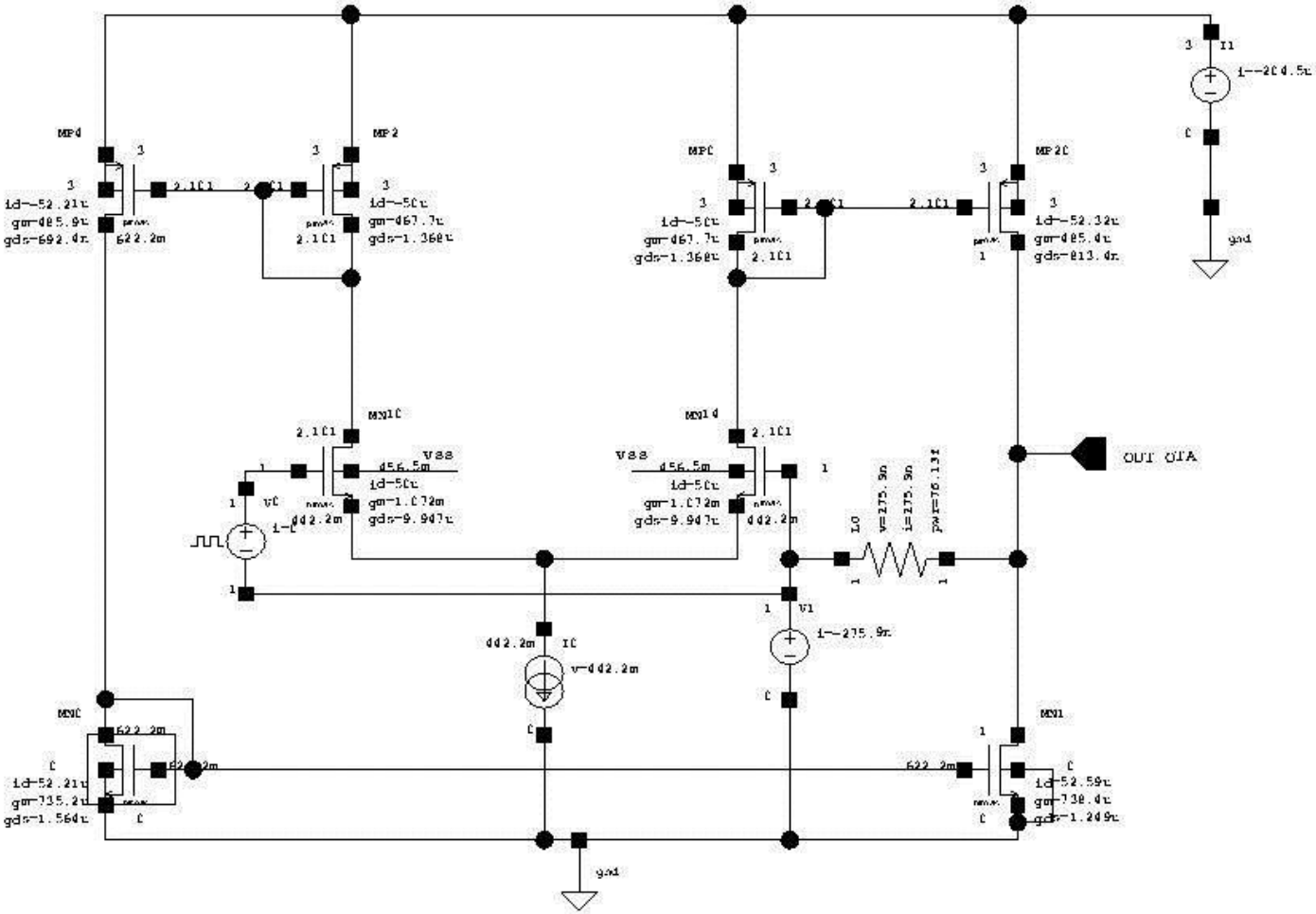
- Add current mirror to get iout to GND
- Add differential pair for differential pair



High frequency hybrid model of bipolar

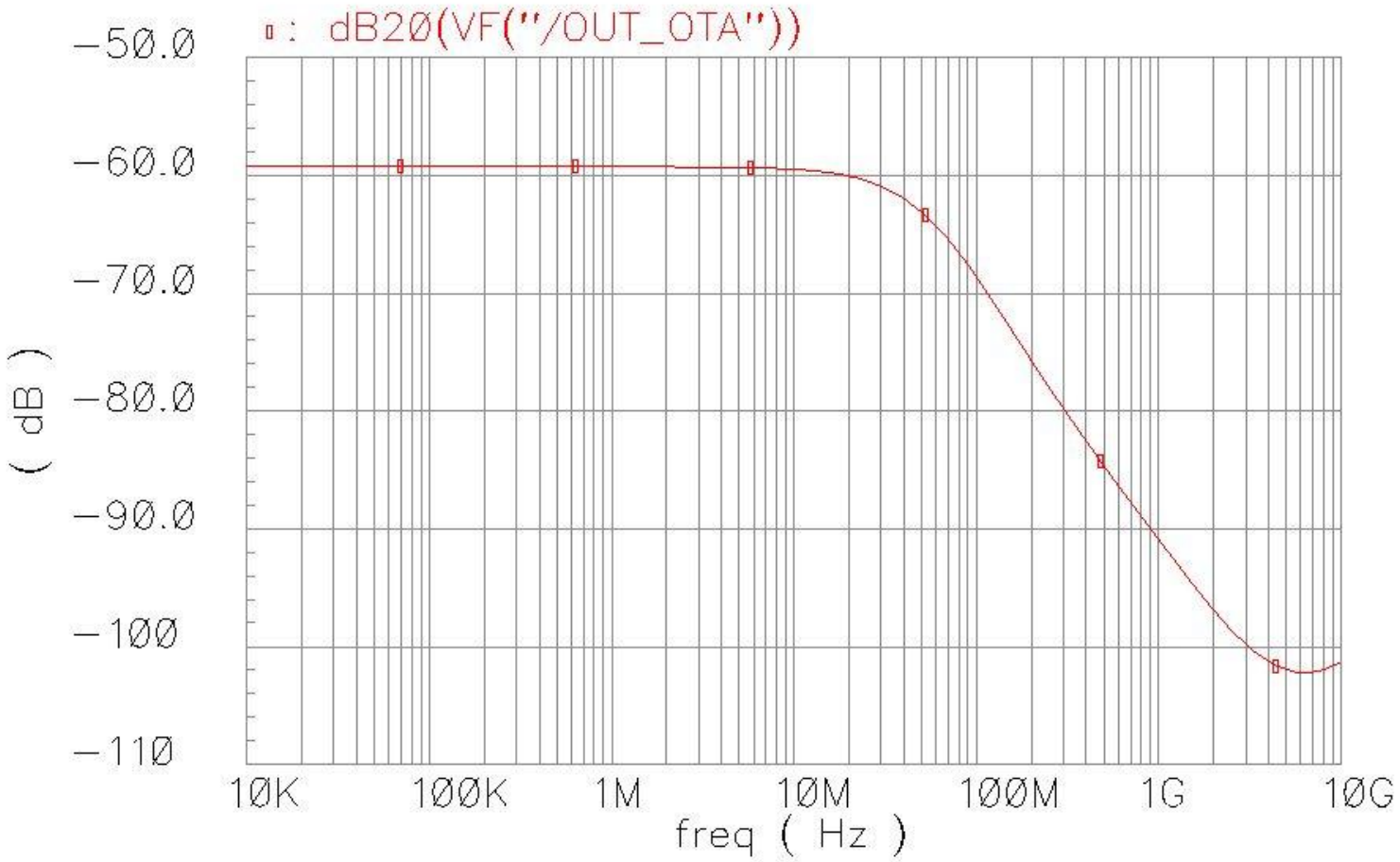
OTA open loop gain simulation

- Differential input voltage, 1 Ω output load



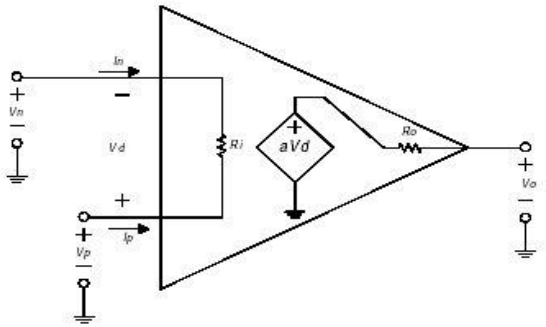
OTA frequency response

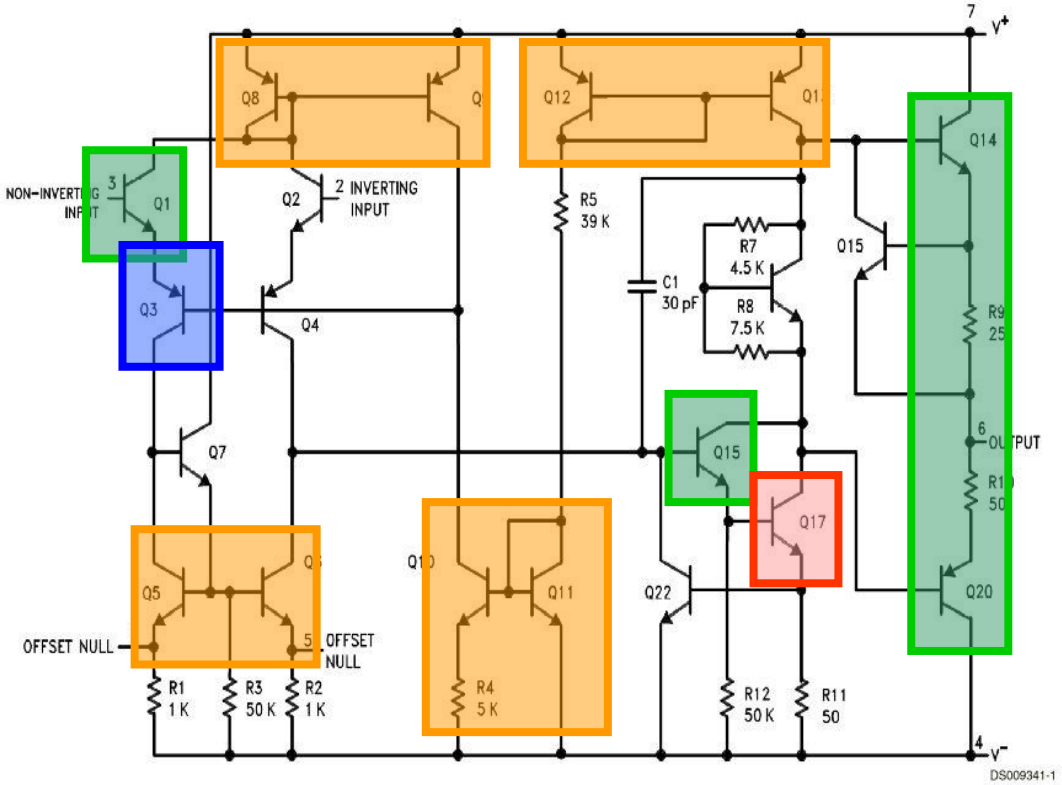
- Dominant pole : $Z_{OUT}C_{LOAD}$
- Second pole : mirrors C/gm

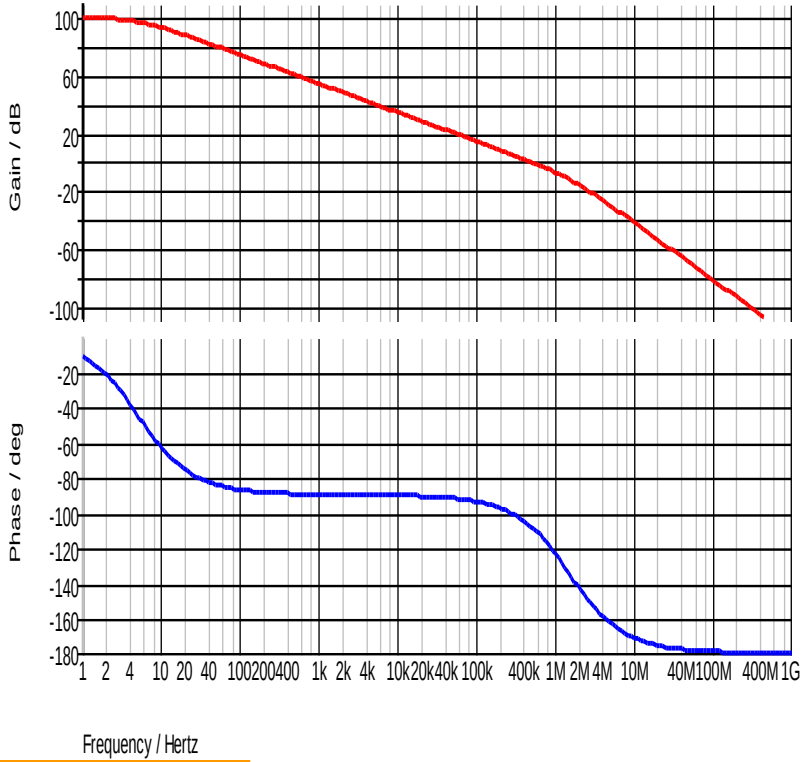


Voltage Feedback Operationnal Amplifiers

- Back to the 70's : LM741
  - 3 stages : Paraphase=CE, Darlington=CE
  - G0 = 200 000, f0 = 5Hz, GBW = 1 MHz, F



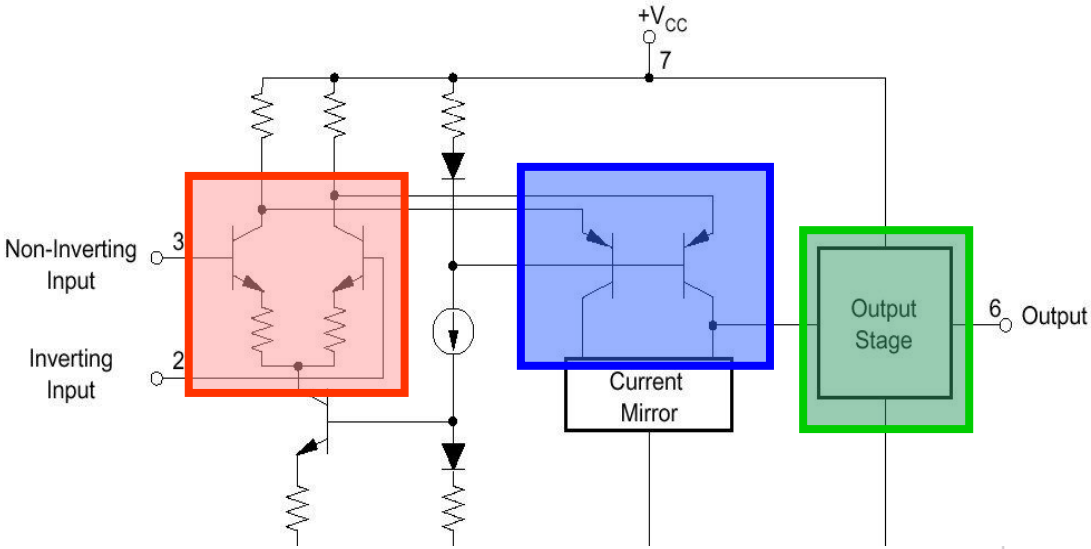


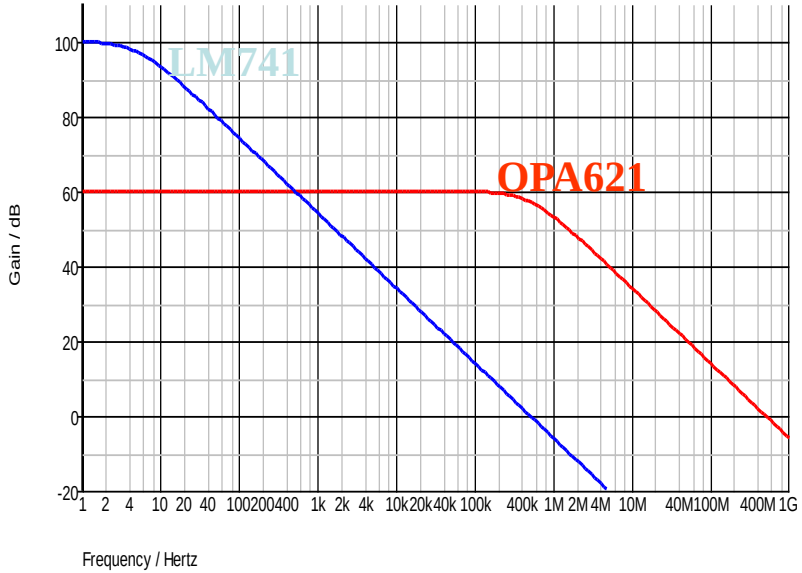


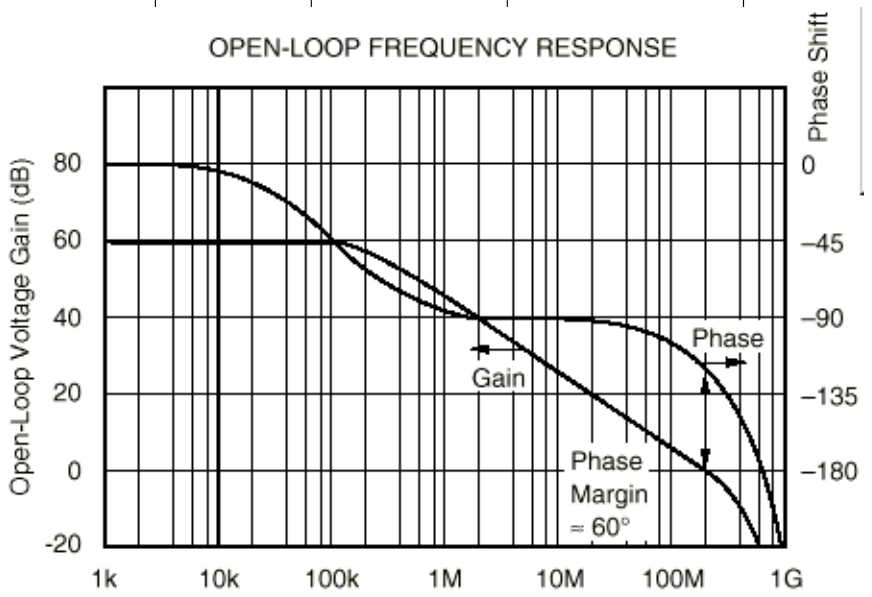
Schematic diagramm of a LM741 (1970) ©National Semiconductors

Voltage Feedback Operationnal Amplifiers

- Breakthrough in the 90's
  - 2 stages : Cascode =CE,
  - Pd = 250 mW
  - G0 = 1 000
  - f0 = 500kHz
  - GBW = 500 MHz







Open loop frequency response of OP620

Charge preamp seen from the input

- Input impedance with ideal opamp
  - Zin = Zf / G+1
  - Zin->0 for ideal opmap
  - « Virtual ground » : Vin = 0
  - Minimizes sensitivity to detector impedance
  - Minimizes crostalk

- Input impedance with real opamp
  - Zin = $1/j\omega\ G_0C_f + 1/\ G_0\omega_0\ C_f$
  - Resistive term : Rin = $1/\ G_0\omega_0\ C_f$
    - Exemple : $w_C = 10^{10}$ rad/s C_f= 1 pF => Ri… – 100 Ω
  - Determines the input time constant : $t = R_{eq}C_d$
  - Good stability= (…!)
  - Equivalent circuit :

Input impedance or charge preamp