IN2P3
Institut national de **physique nucléaire**
et de **physique des particules**

Electronics Developments at IN2P3

- IN2P3 Profile
- Instrumentation Network
- Microelectronics for Instrumentation

Ecole de microélectronique IN2P3 2015 – Fréjus
Claude Colledani

Intro

Présentation faite à Topical Workshop on Electronics for Particle Physics

- Constat
  - IN2P3 et IRFU conçoivent de l'électronique pour les expériences au CERN
    - Les manips au LHC ont un effet moteur
  - Et pour BEAUCOUP d'autres
- Motivation externe
  - Donner une vision plus complète de nos instituts à la communauté internationale HEP centrée au CERN
- Motivation interne
  - Une diversité qui gagne être connue de tous
  - Y voir les avantages
    - Réutilisation des circuits sur plusieurs expériences, gain en ressource et en temps
  - Y voir les risques
    - Emiettement , compétition interne stérile, perte de masse critique

Intro

Fil conducteur de la présentation

- Vision synthétique de la µE à IN2P3 et IRFU passant par
  - Présentation des domaines d'intervention de l'IN2P3 et de l'IRFU
  - Présentation du réseau d'instrumentation
  - Positionnement de la µE dans le réseau

- Illustrations de la µE via les thématiques réseaux
  - Pour l'ensemble des domaines de physique

- Avancées le long d'axes de développements
  - Plateformes, familles d'ASIC
- Qui produisent
  - Réalisations placées sur des expériences
  - Circuits dérivés/modifiés pour d'autres applications

Pas de labos mentionnés
Seuls apparaissent
In2p3 et Irfu

Intro

Version µE 2015

- Ne déroge pas aux buts premiers mais avec plus d'interactivité
  - Les spécialistes des circuits sont dans la salle ➔ L'occasion pour rendre cette présentation interactive en faisant
- MAJ sur les circuits mentionnés
  - Bilan de réalisation du cahier des charges
  - Bilan de Production, de Mise en service (Durée de vie / Fiabilité)
  - Impact du circuit dans la communauté Nat/Internationale
- Evolution du circuit / du savoir-faire accumulé
  - Question: Aujourd'hui feriez-vous les mêmes choix?
  - Contraintes pour Evolution et **Breakthrough**
    - Architecture, Blocs fonctionnels / Building blocks
    - Moyens RH / Techno (process)
- Au niveau de chaque équipe
  - Collaboration sur ces thématiques
  - Les échanges entre labos du réseau µE / Autres

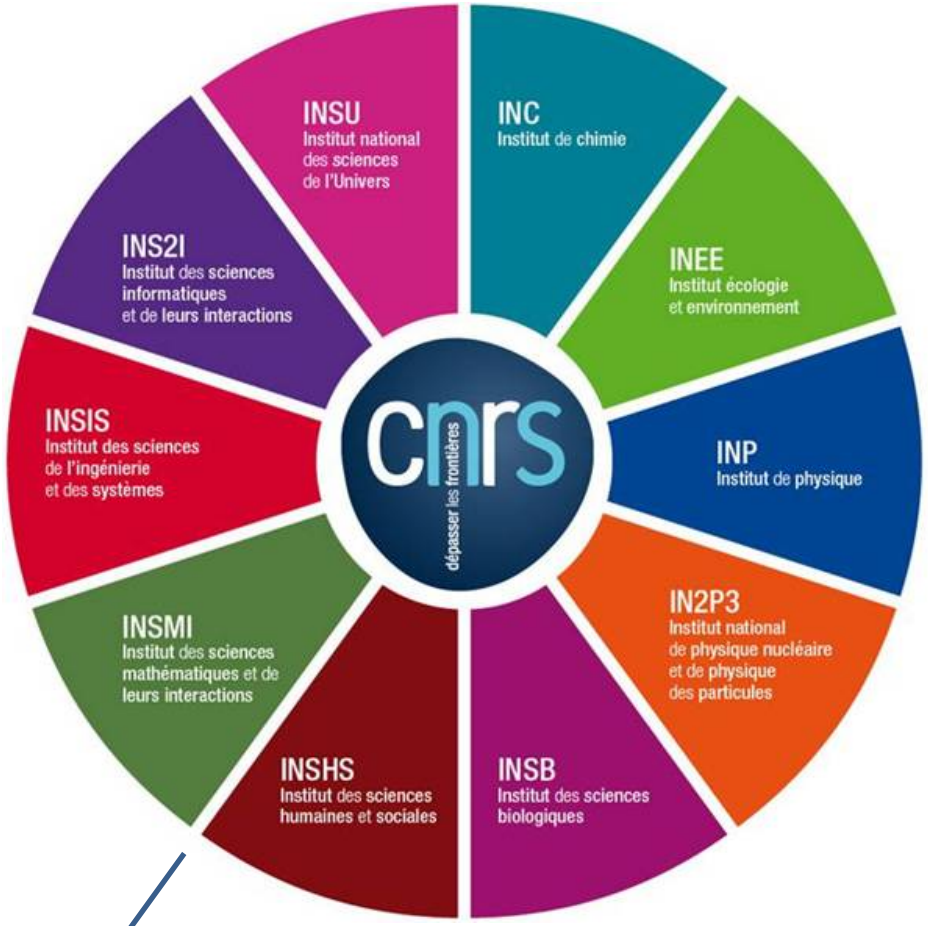
IN2P3, one Institute of CNRS

CNRS

10 institutes
1,100 research units
(95% in partnership)

34,000 *researchers, engineers, technicians*

€3.3 billion
budget

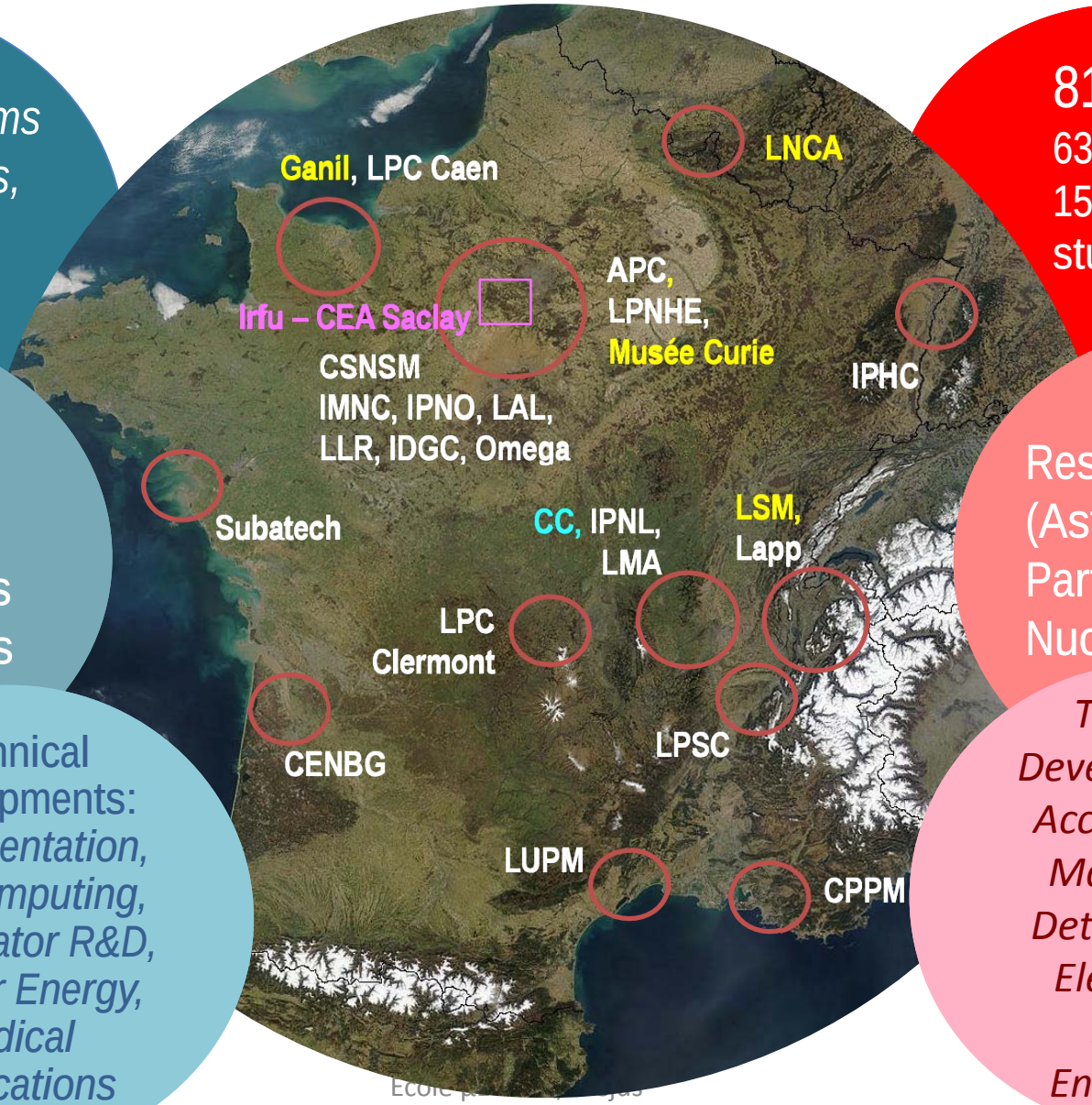


Où fait-on de la µE ?
INP, INSU, INSIS ?

IN2P3 in partnership with IRFU

25 *labs & platforms*
2500 *researchers, engineers and technicians*

815 FTE
630 staff
150 postdocs-students



Research in Astroparticles, Particle Physics Nuclear Physics

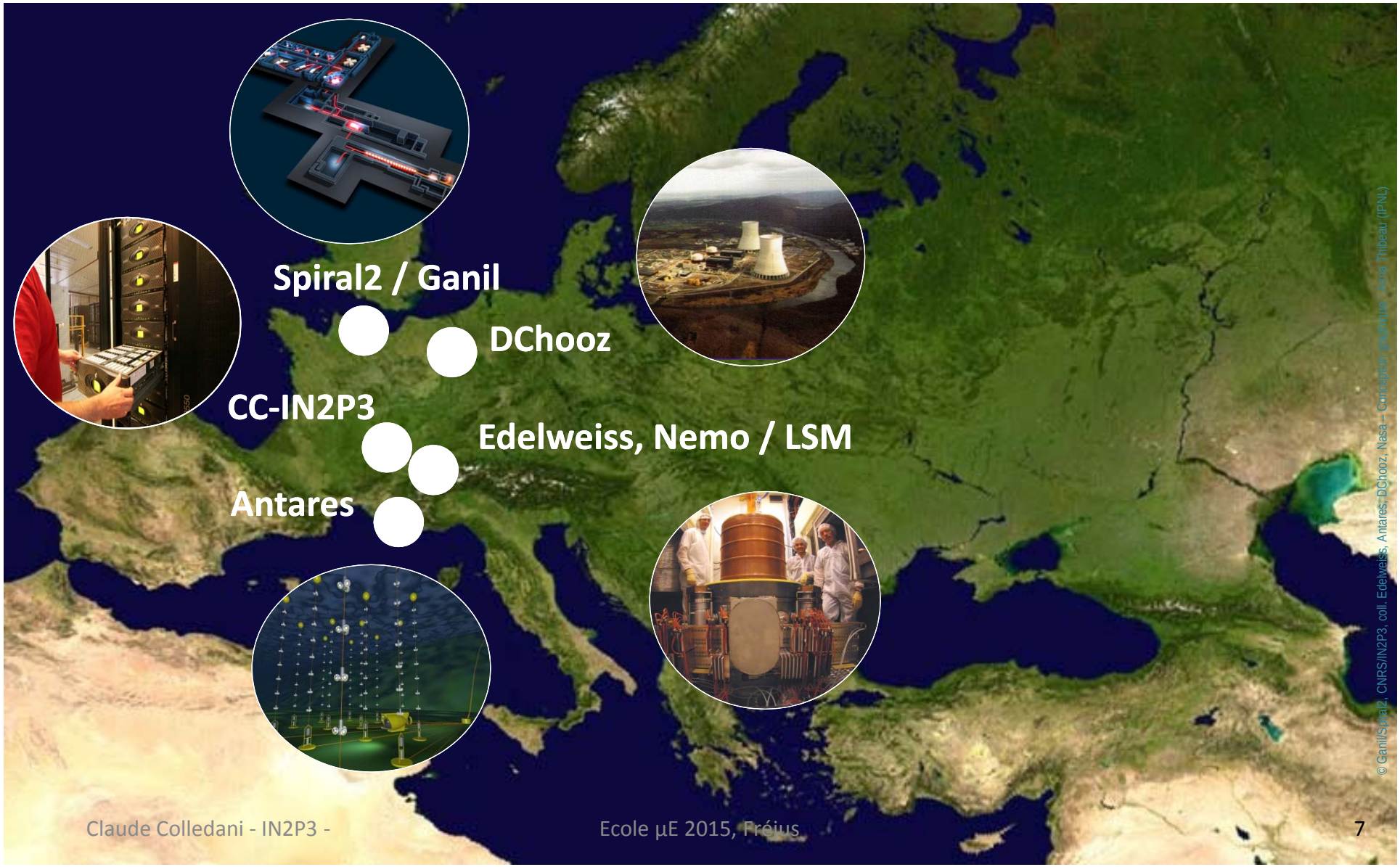
Research fields: (Astrophysics) Particles and Nuclear physics

Technical Developments: *Instrumentation, Grid computing, Accelerator R&D, Nuclear Energy, Medical Applications*

Technical Developments : Accelerator & Magnetism, Detectors and Electronics, System Engineering

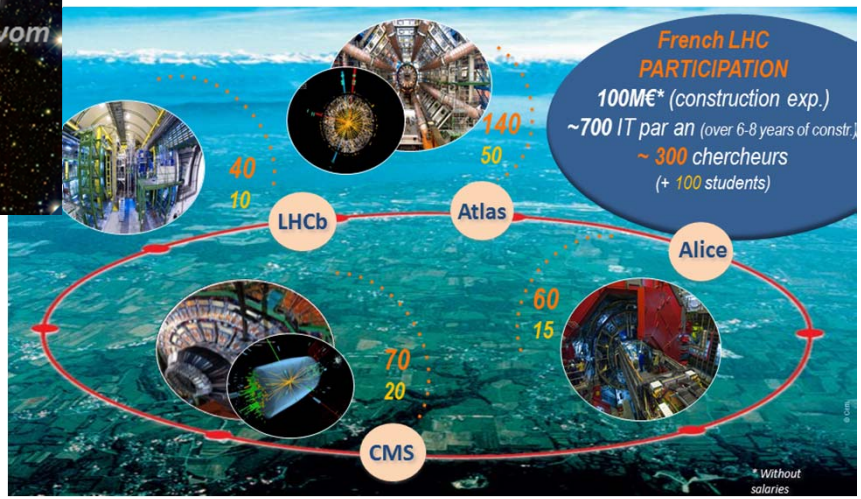
Ref: U. Bassler- FCPPL 2014

Research Infrastructures



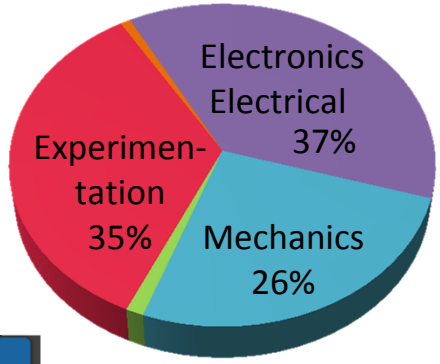
International Collaborations

- 40 Major International Projects



Instrumentation

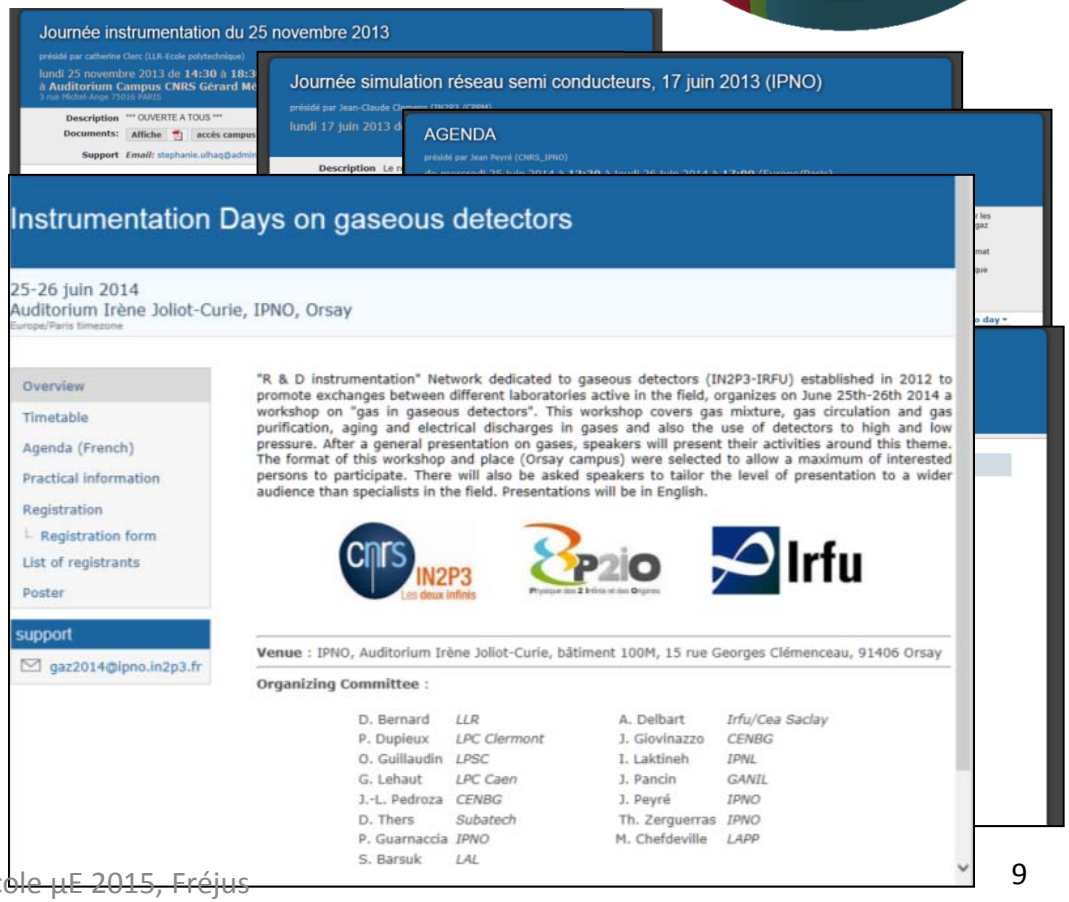
- **Supporting Instrumentation R&D**
  - **730 Engineers & Technicians**



- **Instrumentation Network setup in 2012**
  - To improve exchanges between experts
  - To promote common actions

- **5 Topics**
  - Radio-detection
  - Cryogenic Detectors
  - Photo-detectors
  - Gaseous Detectors
  - Semiconductor Detectors

- **3 Transversal Topics**
  - R&D for Mechanics
  - DAQ
  - Microelectronics
  - + 07/2014: Command & Control

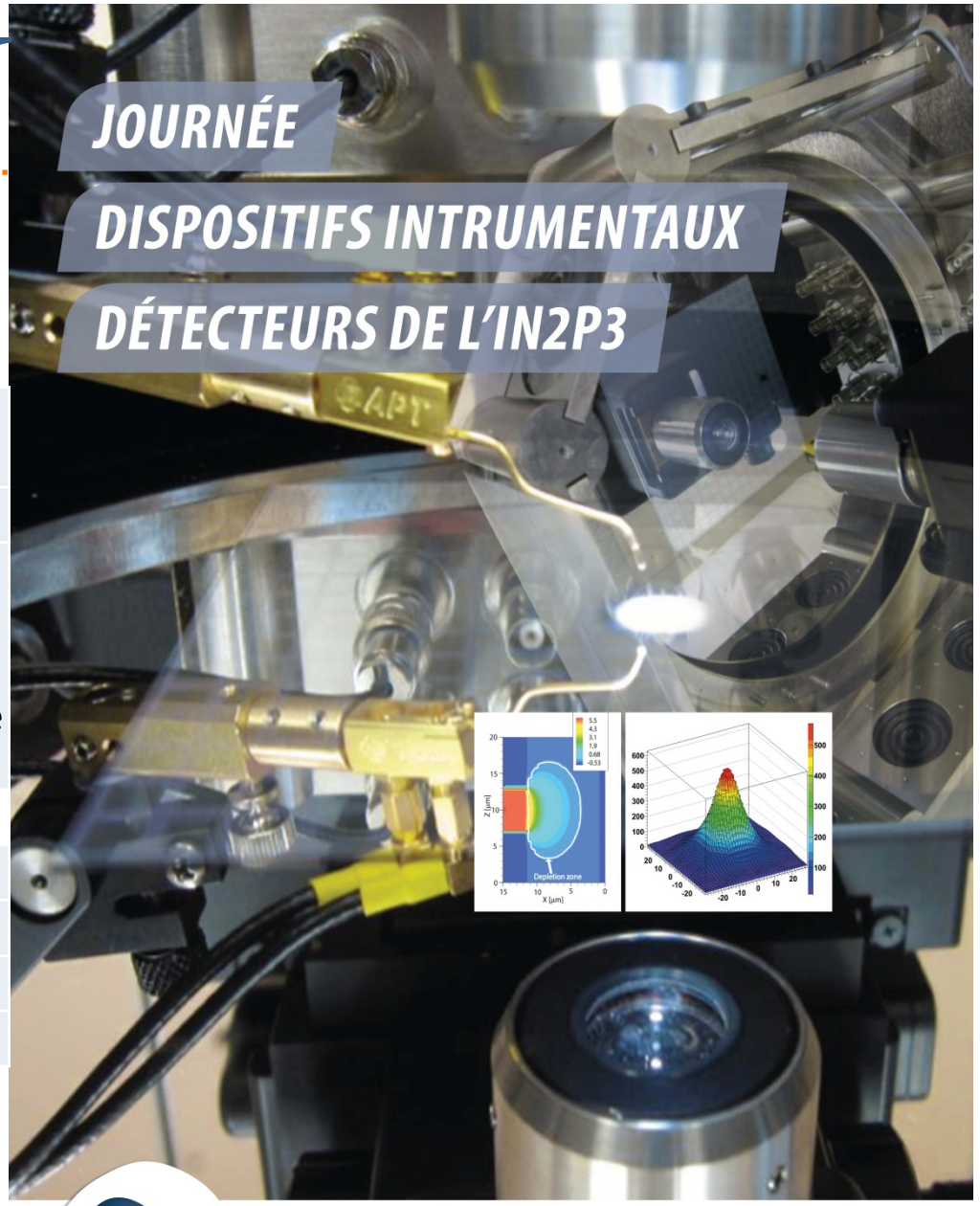


MAJ

Présentations encore possibles

Présentation Orale	Sujet
Pôle MicRhAu	Activités du pôle
APC	Instrument QUBIC dédié à la détection des modes B du fond diffus cosmologique Intégration et mise en œuvre d'¼ de plan focal

Poster	Sujet
LPC-CAEN	Système de PAC
OMEGA	Réalisations ASIC
IPHC	Télescope de faisceau



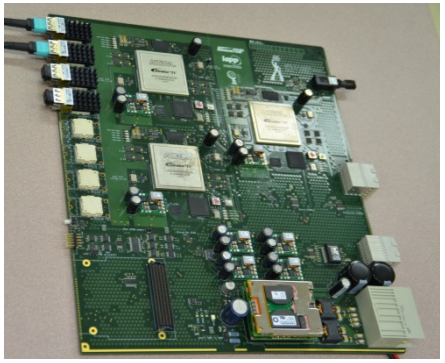
www.cnrs.fr

Jeudi 18 juin 2015
Amphi Charpak, LPNHE, 75005 Paris
Programme et inscription : https://indico.in2p3.fr/event/11589/

DAQ Network

- **Existing since 2011**
  → 30 people
- **Promoting**
  - Common standards
  - Design reuse, shared FPGA IPs
  - Common developments centered on
    - LHC upgrades
    - GANIL experiments
- **Strong interest in xTCA**
  - Member of PICMG
    - *PCI Industrial Computer Manufacturers Group*
  - Working Group of xTCA for Physics
    - Clocks, Gates and Trigger distribution

***LHCb** : Prototype Board*



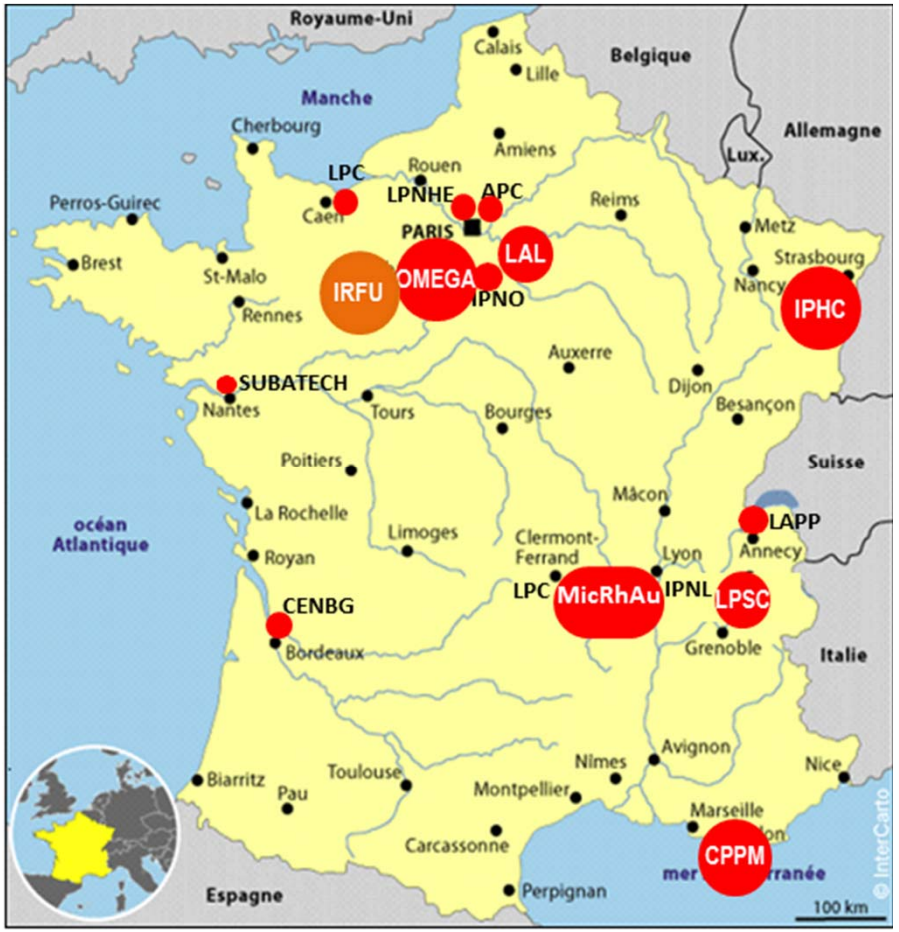
***ATLAS LArg Cal**: ATCA ABBA*

***BAORADIO- PAON:** Digitizer Frequency Separator*

***SPIRAL2/FAIR :** MUTANT*

Microelectronics Network

- **Since 2005**
- **14 Teams (+ Irfu)**
  - ➔7 teams ≥ 4 designers
    - ➔ 3 teams ~ 10 people
- **Internal meetings**
  - School (1 week), alternating with
  - Workshop (2 days)
- **Collaborations**
- **Knowhow / IP exchanges**
- **CAD tools**
  - Unified management
    - License server @ IT Center
  - Training program
    - 100 days / year for Cadence ASIC and PCB, ~35 Engineers/Technicians



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Membres du réseau µE

LABO	Permanents	PostDoc/CDD	PhD	Masters	Autres	Permanents + CDD + PhD
APC	2	1	0			
CENBG						
CPPM	6	1	1	3		
GANIL	0	0	0			
IPHC	18	2	1	2		
IPNO	4	0	0			
LAL	5	0	0			
LAPP	2	0	1			
LPC_Caen	3	0	0			
LPNHE	2	0	0	1		
LPSC	4	0	3			
MicRhAu	12	0	1	5		
OMEGA	9	1	0			
SUBATECH	2	0	0			
IRFU	7	0	0	1	1 DUT	
TOTAL IN2P3	69	5	7	11		81
Gd Total	76	5	7	12	1	88

Grande diversité mais Confusion

Pas des ETP

67	2012	88
76		99

Profils annoncés
Analog
Analog /mixte /test
Analog et digital
Analog FE
Analog/Digital
Analog/digital et test
Analog/FE/BE/Mixte
Analog/Mixte
Analog/mixte /test
Analogique
Analogique FE CAD
Digital
CAO & Cad support
Mixte FE
Numerique
NumériqueBE, Support
TCAD simulation and test
Test
TCAD/Analog/Mixte/Test

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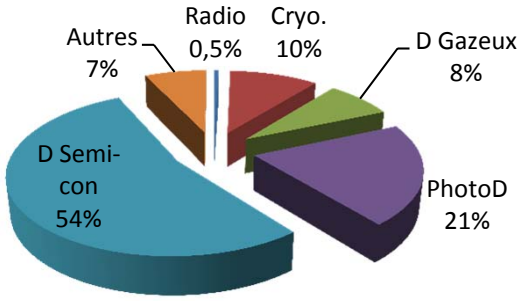
Nomenclature réajustée

TCAD	Etude du semi-conducteur
Analog	Conception analogique FE+BE
Analog/Mixte	Conception analogique et sous-ensemble numérique "full custom". Conception schéma + Simulation mixte + Routage manuel et semi-automatique sous Virtuoso
Numérique	Conception HDL. Simulation sur test bench HDL. Synthèse, Placement-Routage automatique sous Encounter
FE	Conception, Simulation
BE	Réalisation Layout: Virtuoso ou Encounter
Support	Installation, Support outils et kits
CAO	Réalisation cartes PCB pour test
Test	Réalisation banc de tests. Participation à la définition de la testabilité et de la caractérisation des circuits. Mise en œuvre
Intégration System	Implantation de l'architecture du SoC

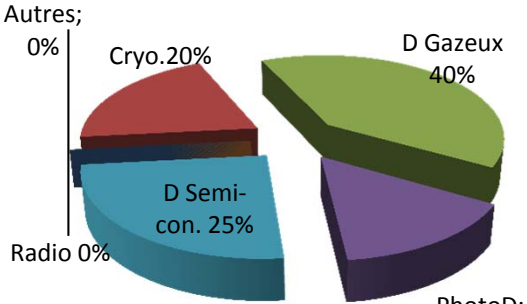
Profils selon nomenclature	
TCAD/Analog/Test	2
Analog/FE	4
Analog	12
Analog/Mixte	30
Analog/Mixte/Test	11
Analog/Numériquel/Test	5
Numérique	9
Numérique/Support	3
CAO & Cad support	2
BE	2
Test	8
Total	88



IN2P3 RH %

Pour les réseaux

Réseau	IN2P3 RH %	IRFU %
Radiodétection	0,5%	0%
Cryogénie	10,3%	20%
Détecteurs gazeux	7,8%	40%
Photodétecteurs	20,7%	15%
Détecteurs semi-conducteurs	54,1%	25%
Autres	7,1%	0%



MAJ

Enseignement

LABO	Matière/ Observation	Niveau
CPPM	Cours de conception de circuits numériques	Electronique, MASTER II
IPHC	Cours de µE, 1 E-C	Master
LAPP	Electronique de base	IUT 1ere année
LPSC	1 E-C	
	Electronique de base	Master
	Signal processing	ESIPAP
	Microélectronique	Cours d'initiation au Maghreb et Afrique de l'Ouest
MicRhAu	Microélectronique, 1 E-C	Master I & II (Clermont)
		DUT mesure phys (Clermont)
		Ecole Ingé CPE- TP (Lyon)
	Microélectronique	Master II - TP (Lyon)
OMEGA	Microélectronique	Ecole polytechnique, 3e annee
	TP	ENSTA
IRFU		Centrale-Supelec, Ingé. 1ère année
		ESIPE, Apprentis Ingénieur

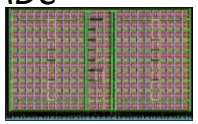
Expertise & Skill

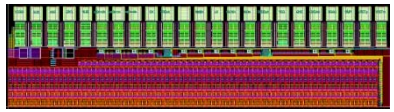
Building Blocks

Low noise, low power & radiation tolerant
Analog, Mixed, Digital

- FE amplifiers, shapers
- Band Gaps, Regulators, POR
- RO & Ctrl: Serializer, Tx , I2C, JTAG
- Memories: Analog / Digital
- DAC / ADC / SoC A-based, D-based

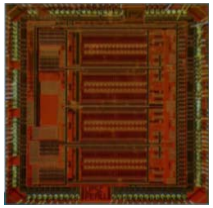
12-bits SAR ADC
100 kSPS
180 x 300 µm²
IBM 130 nm





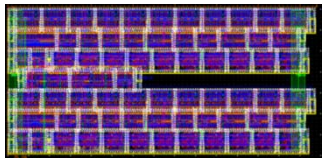
SEU Tolerant Memory
230 x 1820 µm² - *130 nm, FEI-4*

4 x 12-bits SAR ADC



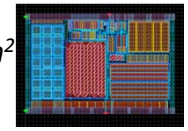
40 MSPS,
5mW/ch
10 mm²,
130 nm

10 ps TDC R&D

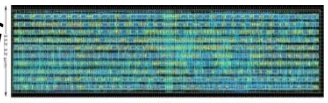


35 x 75 µm²
IBM 130 nm

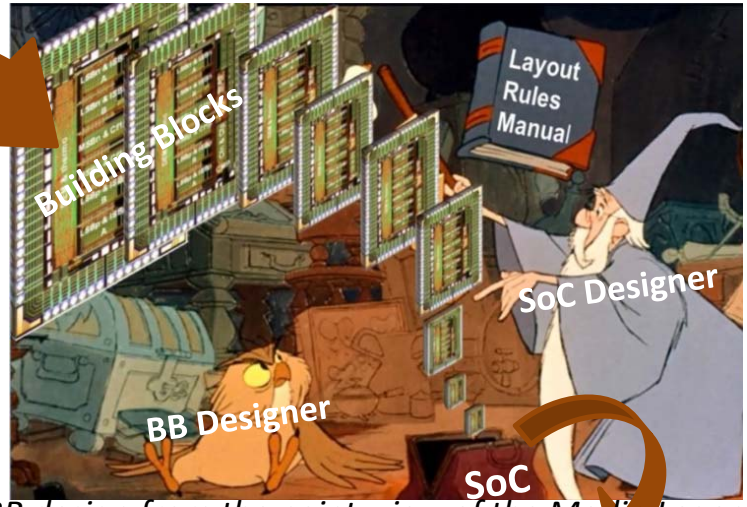
BAND GAP
196 x 133 µm²
TJ 180 nm



JTAG Ctlr



725 x 112 µm², TJ 180 nm



BB design from the point view of the Merlin Legend

System Level Design for SoC

Functional Block Assembly

- Multi-Channel FE + Massive A 2 D
- Data Reduction Processing
- Memory Buffers/ Management
- Embedded Regulation Systems

Distribution

- Power Distribution Grid / Domain
- Clock Distribution
- Data Flow

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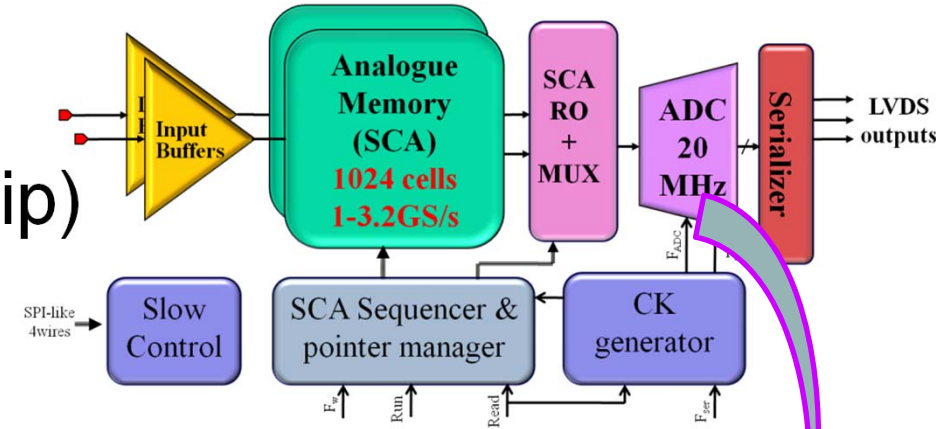
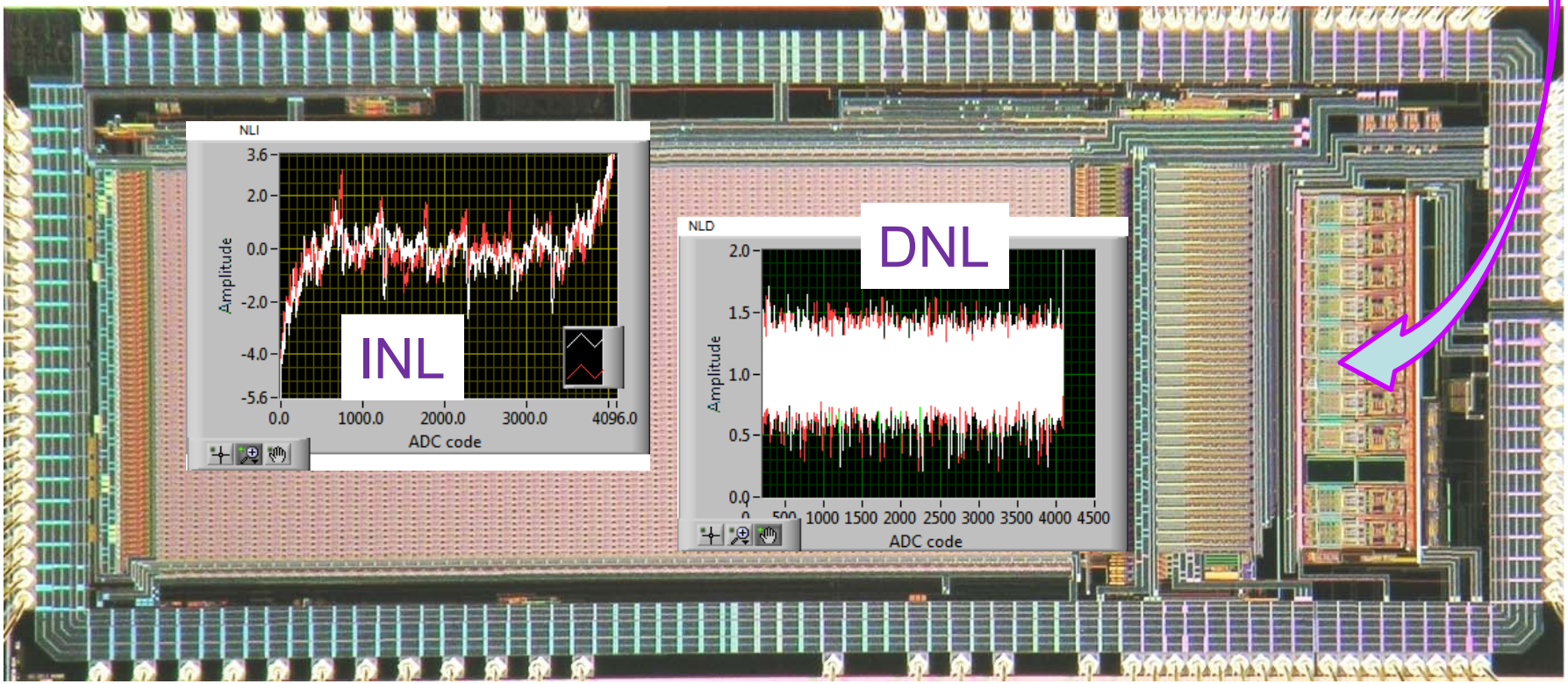
ADC_IP pour collaboration CTA: NECTAR

– 2 read-out channels

– CMOS 0,35µm: 3x7mm(chip)

– (premier circuit de ce type)





MAJ

Bilan de cette collaboration (IRFU/LPSC)

Condition de réussite d'IP

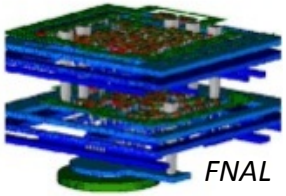
- ***Bilan de réalisation du cahier des charges***
- ***Bilan de Production, de Mise en service (Durée de vie / Fiabilité)***
- ***Impact du circuit dans la communauté Internationale***
- ***Question: Aujourd'hui feriez-vous les mêmes choix?***

Vrai partenariat , Respect mutuel et implication forte

- **Mieux que prévu, et meilleurs que nos propres résultats**
- **Production: OUI, Fiable, très reproductible=> design robuste**
- **Plusieurs publis communes; CTA/HESS**
- **Oui sans hésiter, mais avec une architecture SAR**

Looking for synergies

- **Participating to International R&D Programs**
  - RD53 (2013),
  - AIDA (2011) + H2020
  - EUDET (2006-2010)
  - 3DIC - TSV (2009)



FNAL

- **Sharing Process**
  - Successive CERN nodes (65 nm, 130 nm & 180 nm for MAPS)
    - 9 laboratories applying for 65 nm TSMC NDA
  - Specific & cheap processes
    - Large usage of CMOS / BiCMOS- SiGe .35 µm
    - Equivalent 180 / 130 nm nodes are considered
    - For the numerous non-CERN experiments
      - Few tens of channels to integrate , Limited ASIC production

MAJ

Process 2015

Technologie	Nœud	# Labos (C + N + P)	Labo
AMS	350 nm BiCMOS SiGe	5	APC, IPNO LAPP, OMEGA, IRFU
AMS	180 nm CMOS	4	CPPM, LPC-Caen, LPNHE,
AMS	350 nm CMOS	8	CPPM, LPC-Caen, LPNHE, LPSC, MicRhAu, Subatech, IRFU, IPHC
ESPROS	150 nm CMOS	1	IPHC
GF / Tezzaron	130 nm CMOS / 3D	1	CPPM, OMEGA(A), IPHC(A)
Global Foundry	130 nm CMOS	1	CPPM, IPHC(A)
IBM	130 nm CMOS	2	MicRhAu, LPSC, CPPM?
LFOUDRY	150 nm CMOS	2	CPPM, IRFU(N)
ST Micro	130 nm CMOS (?)	1	LPSC(N)
ST Micro	130 nm SIGE	1	OMEGA(N)
ST Micro	140 nm IMG	1	LPSC(N)
TOWER JAZZ	180 nm CIS	2	IPHC, IRFU
TOWER JAZZ	130 nm SiGe	1	OMEGA(N)
TSMC	65 nm CMOS	9	CPPM, IPHC, LAL, LAPP, LPNHE, LPSC, MicRhAu(2x), OMEGA,
TSMC	130 nm CMOS	2	MicRhAu, OMEGA
XFAB	350 nm CMOS	2	IPHC(A), IRFU(N)
XFAB	180 nm CMOS	2	IPHC(P), IRFU(N)

NDA

Total process 17

C /. = Courant; P = Ponctuel
N = Nouveau; A = Abandon

Looking for synergies

- **R&D covers all IN2P3 physics and detectors domains**
  - Large discrepancy in the projects size ➔ From small analog ASIC to full SoC
    - Impact Design teams profiles
    - Impact on process #

  - New designs always required ➔ Design Reuse has to be considered first
    - Impact on manpower, schedule, budget

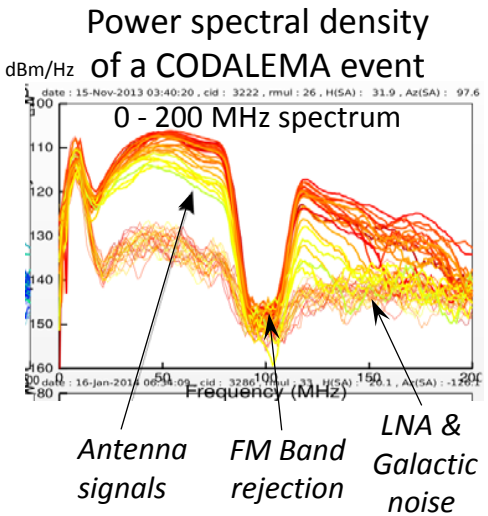
  - Pushing for coherent ASIC families development, which will provide flexible designs and staged performances

- **Detector Networks must help to converge**

  - Following of presentation is organized by detector categories
  - Focus on circuits <u>Designed</u> for specific projects,
    <u>Reused</u> for other applications

Radio-detection Network

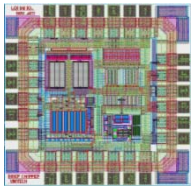
- **Full Custom Analog ASIC - LNA optimized for associated antennas**
  - Developed to detect Air Showers produced by Ultra-High-Energy cosmic rays
- **LONAMOS for Butterfly & LWA**
  - Optimized for 20-80 MHz
  - Efficient up to 200 MHz
- **Small but Successful**
  - 1rst generation, 0.8 µm CMOS
    - 2004, 400 chips
  - 2nd generation, 0.35 µm CMOS
    - 2011 700 chips
    - 2014 6000 chips



Butterfly Antenna, 2.2 x 1.5 m
Codalema @ Nancay - France

Long-Wavelength Antenna
NenuFAR @ Nancay - France

Experiment	Installed
CODALEMA@ Nançay-France	(60 Butterflies + 10 LWA) x 2
AERA @Auger-Argentina	(100+25 Butterflies) x2
TREND @ China	(54 Butterflies) x 2
HELYCON @ Greece	(12 Butterflies) x2
NenuFAR @ Nançay-France	(190 LWA x 2) + 5600



LONAMOS 1,4 x 1,4 mm²
CMOS 0.35 µm , 2011

Fully differential architecture
Zin digitally adjustable
OIP3=33dBm
NF<1dB
Gp=27dB
BW>200MHz

MAJ Radio NET
- Didier Charrier-

- Point sur les circuits mentionnés
  - Bilan de réalisation du cahier des charges
  - Bilan de Production, de Mise en service (Durée de vie / Fiabilité)
  - Impact du circuit dans la communauté Nat/Internationale
- Evolution du circuit / du savoir-faire accumulé
  - Question: Aujourd'hui feriez-vous les mêmes choix?
  - Contraintes pour Evolution et **Breakthrough**
    - Architecture, Blocs fonctionnels / Building blocks
    - Moyens RH / Techno (process)

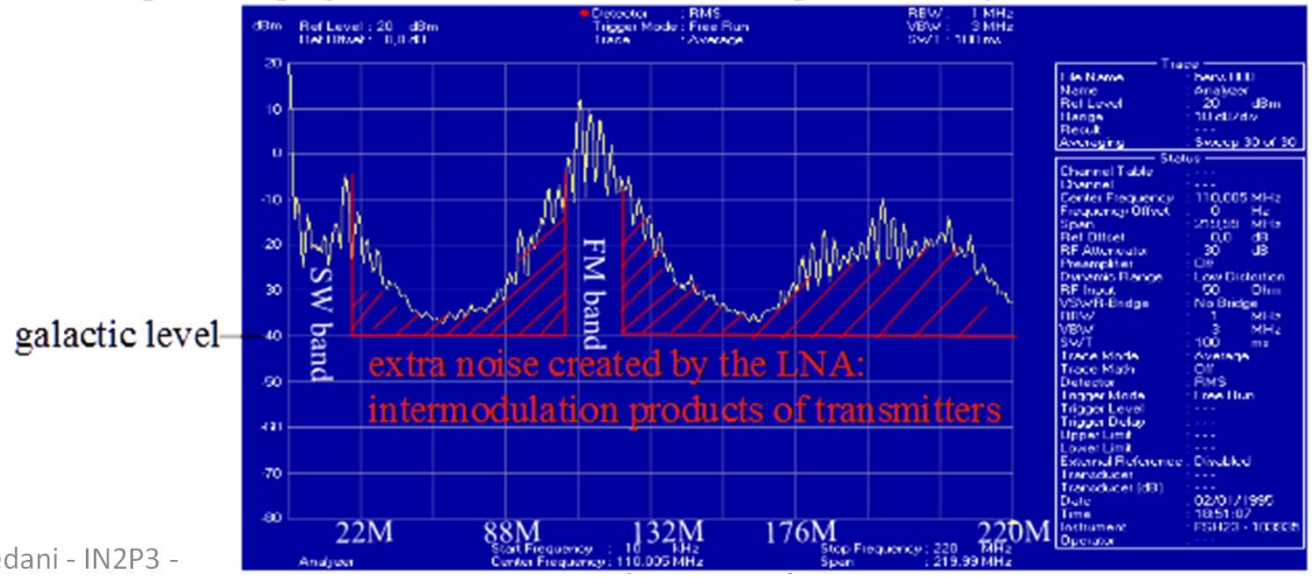
- Au niveau de chaque équipe
  - Collaboration sur ces thématiques
  - Les échanges entre labos du réseau µE / Autres
- AOB + Qui d'autre veut intervenir sur la µE pour ce réseau

MAJ

Wide bandwidth RF design

- **transient signal to be detected can be much weaker than parasitic signals**
  - for radio detection: signal amplitude can be ~70dB less than radio transmitters
  - Wide bandwidth needed (transient detection) ==> high input power Pin
  - May decrease Pin by low order input filtering but phase distortion (pulse spreading)
  - poor linearity ==> additional noise(intermodulation products) in the useful bandwidth
  - ==> **linearity**(IP2, IP3,...) is **not less important** as noise characteristics
- **Design of low noise AND high linearity amplifier**
  - require high IPn values in the **full** bandwidth at least up to FM band (88-108MHz)
  - difficulty to improve both linearity and noise
  - trade off between linearity, noise, bandwidth, phase distortion, consumption...

spectrum performed with an antenna and a poor linearity LNA(IIP3=63mV) at Nançay



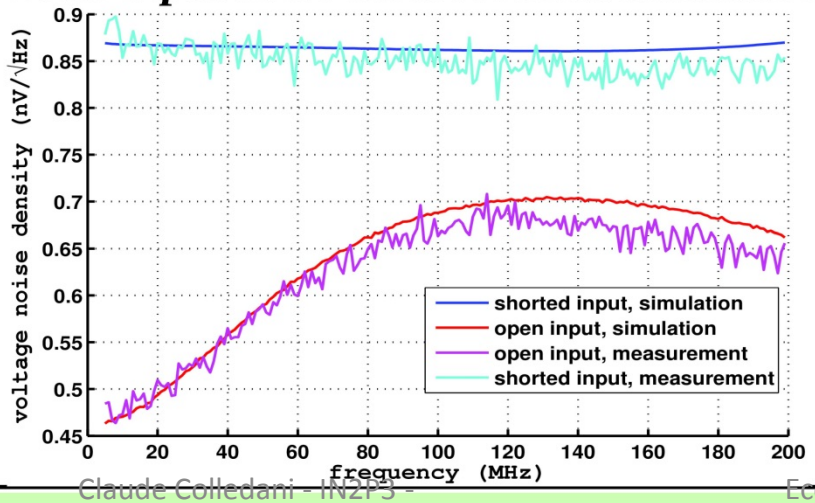
MAJ

LONAMOS measured characteristics

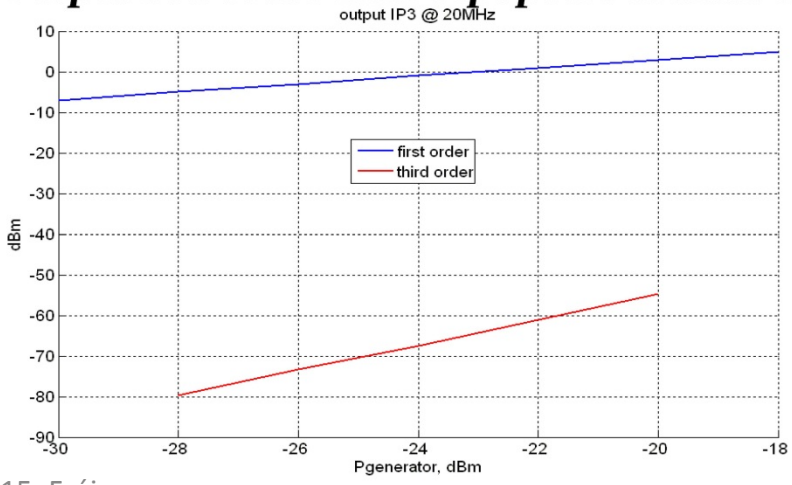
OIP3	33 dBm	bandwidth	>200 MHz
IIP3	1.1 V	|S12|	-63 dB
OCP(-1dB)	15 dBm	|S22|	-18 dB
NF(matched)	0.8 dB	input impedance	adjustable
NFopt	0.7 dB	gain drift	-0.004 dB/K
Gp	27 dB	consumption	310 mW
σ(Gp)	0.07 dB	production yield *	98.5 %
$-d\varphi(S_{21})/d\omega$	2 ns	package*	QFN20

- Fully differential architecture
  - input differential pair
  - output common source push-pull
  - reject even order harmonics
  - reject common noises
  - no input BALUN required
- Feedback
  - with linear component
  - high open loop gain up to FM band
- no external lightening clamp required
- unexpensive AMS CMOS 0.35µ technology

Total input noise measurement/simulation



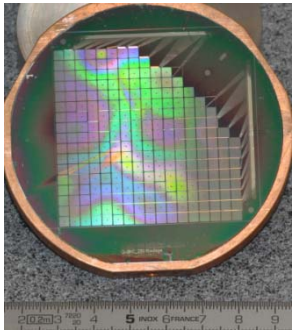
Output 3rd order intercept point measurement



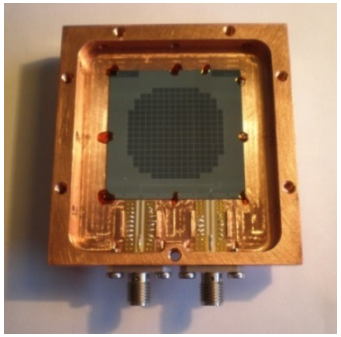
Beyond LONAMOS

- **Need for an antenna-LNA with extended bandwidth up to 500MHz**
  - radio detection: EXTASIS project: explore deeply low and high frequencies
  - radio astronomy: Square Kilometer Array (SKA) project ???
- **Technology choice**
  - need higher gm/I and higher Ft transistors
  - but need low cost technology
  - ==> SiGe AMS 0.35u or IHP 0.25u(Europractice)
- **required characteristics**
  - Gp ~ 20dB
  - bandwidth 500MHz
  - IIP3 >13dBm up to 500MHz
  - antenna + LNA equivalent input noise temperature
    - < 150 K @ 50MHz
    - < 100 K @ 100 MHz
    - < 45 K @ 200 MHz
    - 30K from 300 MHz to 500MHz (AsGa may be required)

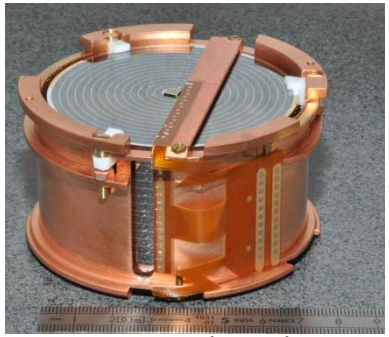
Cryogenics Network



*250 pixels **TES** matrix (Transition Edge Sensors)*
QUBIC @ South Pole



***K**inetic **I**nductance **D**etector*
NIKA @ Pico Veleta, Spain



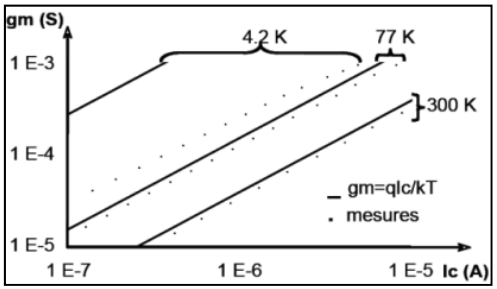
HP-Ge ionizing-heat detector
EDELWEISS @ LSM, France

Scintillating Bolometer ZnMo4 and its 2 light detectors
LUMINEU @ LSM, France

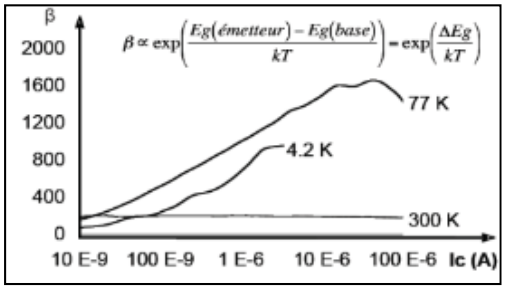
- **Electronics main constraints @ ~2 - ~110 K (LAr)**
  - No valid transistor models ➔ Characterization
    - Bipolar: gm ↗, β ↗ …
    - MOS: Substrate becomes Insulated ➔ Kink Effect

      → $T_{parasitic}$, $I_{leakage}$, V_{th} history effect

- **Thermal & Electric effects of Interconnects**

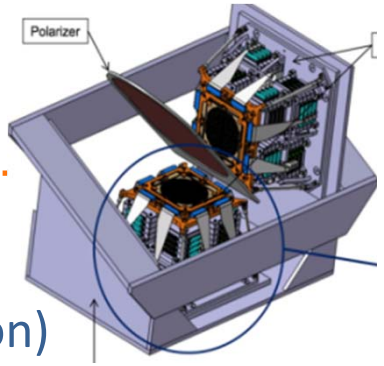


Gm of *SiGe bipolar 0.35µm*



β of *SiGe bipolar 0.35µm*

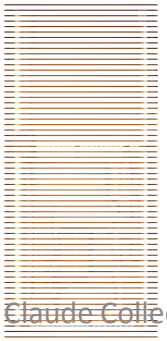
Cryogenic electronics for QUBIC



Focal plan (@100mK)

- **QUBIC Cryostat, 2016 @ Dome C - Antarctica**
  - To measure Cosmic Microwave Background (B-mode polarization)
- **SQMUX128 @ 40 K**
  - 16 chips for the cryogenic focal plan
    - 2048 TES (NbSi Transition Edge Sensor)
    - 2048 SQUID multiplexed stage
      - 100 KHz readout , Input LNA (0.2 nV/√Hz)
  - Cryogenic effects correction
    - Digital lib. redesigned (Kink effect)
  - ~100 chips to produce
    - 6 cryostats
- **Variant for collaboration @ PMO**
  - Purple Mountain Observatory (Dome-A / China)

SQUID implementation

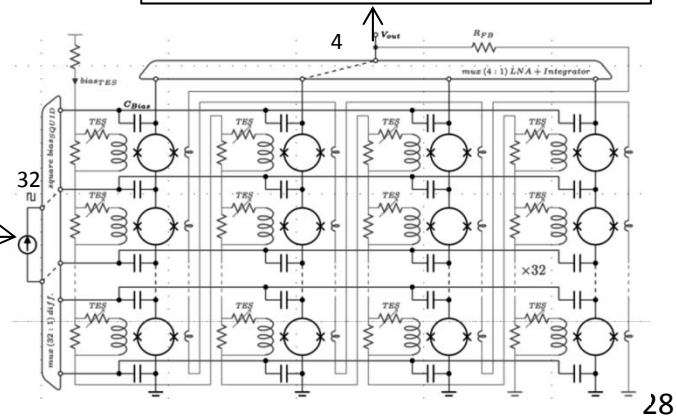


Matrix RO: configurable up to 128 SQUIDS
32 Biasing Current Sources with Diff Outputs
4 Differential Multiplexed Analog Inputs
100 kHz multiplexed Input LNA (0.2nV/√Hz)
Individual automatic Squid offset compensation (8 bits ADC & DAC, FSM, 128 x 8 memory block)
8 mW Power Dissipation

SQUMUX128, 20mm² , 0.35 µm SiGe

Successive bias of 32 Rows
AC Multiplexed Current Sources

4 Column Analog outputs
multiplexed toward input LNA



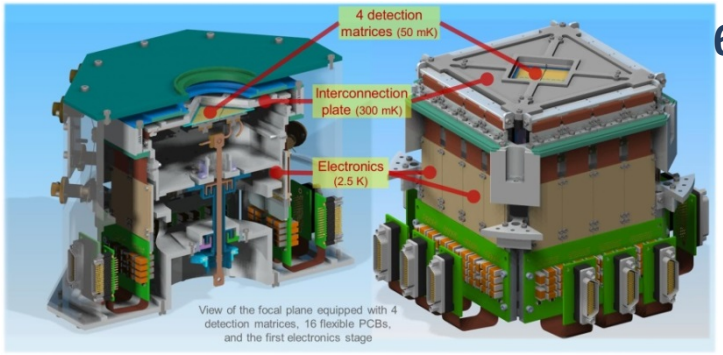
SQUID matrix Read Out

From Compact & Extreme Cold to Huge & Cold

X-ray micro-calorimeter for IXO/ATHENA satellites

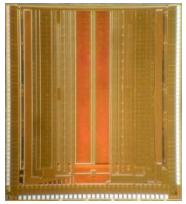
4096 channels

6 dm³



- **2 stages of T: 2.5 K and 15 K**
  - Cryocooler with very-low power budget
- **3 circuits, 2 process** (CNRS/LPN - CEA/Irfu col.)
  - HEMT Input Stage @ 2.5 K (High Zin)
  - Mxp & Pwr Commuting, SiGe ASIC @ 2.5K
  - Amplifying SiGe ASIC @15 K

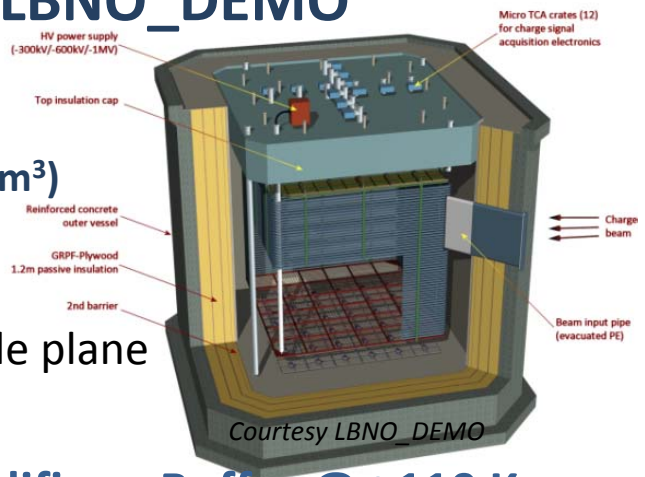
Stage 3 chip - Irfu-CryoCanal1 24,1 mm²



Stage 2 chip -Irfu-CryoCom1 9,4 mm²

LAr TPC demonstrator, for WA105, LBNO_DEMO

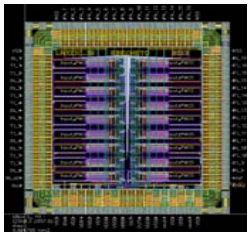
300 tons
6x6x6 m³ (216 m³) active volume
7680 channels
for 36 m² anode plane



Courtesy LBNO_DEMO

- **16 ch. Amplifier + Buffer @ ~110 K**
  - To profit from minimal noise conditions
- **Schedule**
  - MPW submission : 22 September 2014
  - Production: Q3 2015
  - 8 000 channel ~ 500 chips

LARZIC chip CMOS ~6 mm²



MAJ CRYO NET
- Damien - Edouard - Olivier -

- Point sur les circuits mentionnés
  - Bilan de réalisation du cahier des charges
  - Bilan de Production, de Mise en service (Durée de vie / Fiabilité)
  - Impact du circuit dans la communauté Nat/Internationale
- Evolution du circuit / du savoir-faire accumulé
  - Question: Aujourd'hui feriez-vous les mêmes choix?
  - Contraintes pour Evolution et **Breakthrough**
    - Architecture, Blocs fonctionnels / Building blocks
    - Moyens RH / Techno (process)

- Au niveau de chaque équipe
  - Collaboration sur ces thématiques
  - Les échanges entre labos du réseau µE / Autres
- AOB + Qui d'autre veut intervenir sur la µE pour ce réseau

Cryogenic Electronics

MAJ

1- **Cryo-ASIC designed @ IPNL and MicRhAu oriented on Neutrino Physic**

- Discussion starts with D.Dzahini and R.Sefri in 2006
- Main challenge : ENC = 1500e- @ 250 pF detector capacitance
- Several versions due to requirements and detector evolution
  - Wire
  - GEM
  - Unipolar and bipolar input signal
- Analog and digital block
  - CSA
  - Shaper
  - 50 Ohms Buffer
  - I2C (slow control part)

2 - **Knowledge**

- Model modification to improve corner frequency (1/f noise)
- Vth vs temperature
- R and C vs Temp

3 - **Technical choices**

- NMOS as input transistor (avoid power supplies problems)
- Differential structure (good for PSRR but not for noise)

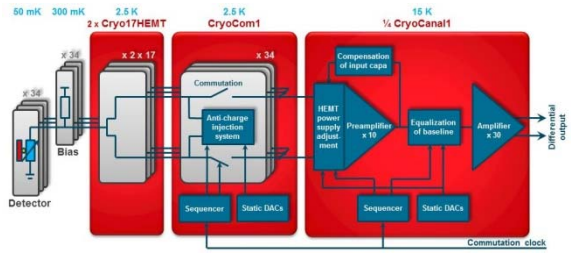
4 - **Next steps**

- Test setup @ variable cryogenic temperature and avoid soaking circuit in liquid N2
- WA105 project : production of 250 ASICs (end of 2015) on last version (test in progress)
- XTRACT chip for Subatech (TPC Xenon Liq, XEMIS2 project))
- ANR GENESIS for Nuclear Physic (HPGe detector) ? *Waiting for ANR*

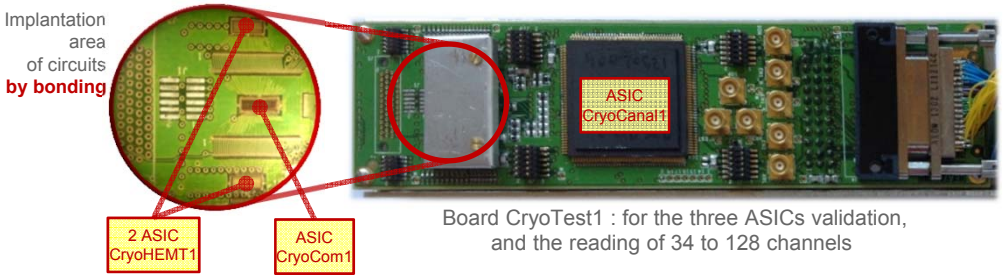
MAJ

-1-ASICs pour bolomètres X (X. De La Broise, F. Lugiez) pour applications spatiales

-Bilan des activités



Architecture of the cryoelectronics



Board CryoTest1 : for the three ASICs validation, and the reading of 34 to 128 channels

Les trois circuits (1 HEMT et 2 AMS SiGe 0.35) ont été produits, des échantillons ont été implantés sur une carte de test, et ils ont été **testés à très basse température** (4,2 K).

=>**Tous les tests fonctionnels sont concluants**: amplification, commutation de l'alimentation et multiplexage temporel à plus de 1 MHz, pour la lecture de capteurs haute impédance (~1 Mohm). Les performances en bruit sont en cours d'évaluation.

-Perspectives

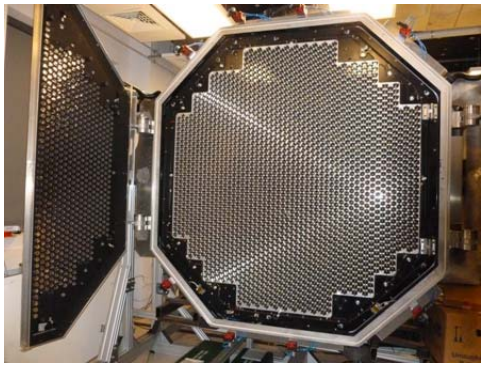
- Le développement des cartes finales pour la lecture d'une matrice complète de 1024 pixels, est en cours.
- Architectures des ASICs validée=> circuits finaux très proches.

-2- ASICs pour bolomètres sub-millimetrique pour appli spatiales

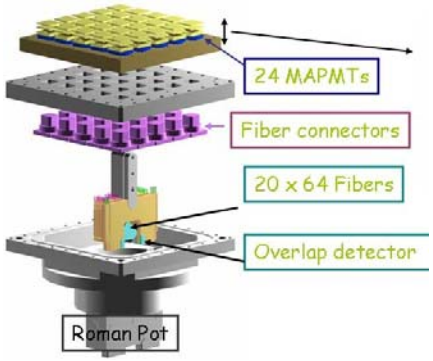
Conception d'ASIC CMOS matriciels fonctionnant a 50mK pour la lecture de matrice de bolomètres (sub) mm: démarrage de l'activité en septembre 2015.

Photo-detectors Network

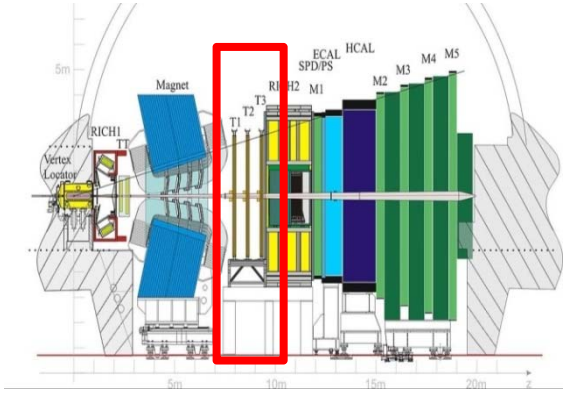
- **PMT, MA-PMT, MCP-PMT, Si-PM, Scintillators, …**
  - Overlap with Semiconductors Network (CCD, SiPM, APD)



HESSII camera, 2012 - Namibia
- 2048 PMTs , Diameter 2.3m, Weight 2000 kg



ATLAS Luminometer - CERN-
MA-PMT for Roman Pot

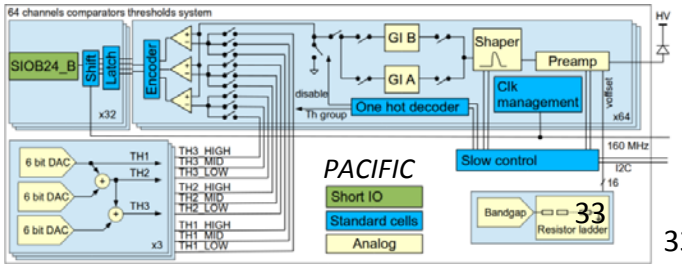


LHCb Tracker upgrade Phase 1 - CERN
FEE for SciFi + Si-PM , 2015

- **FEE increases in complexity**
- **Teams with critical size / collaborations**
- **2 categories of FEE**
  - Shapers and Peak Detectors circuits (IN2P3)
  - Waveform Sampling circuits (Irfu)
- **Successive improved generations**
- **Derived for different application fields**

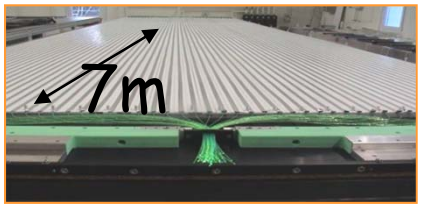
PACIFIC: Barcelona, Valencia, Heidelberg Universities, ETH Zurich & IN2P3 Collaboration

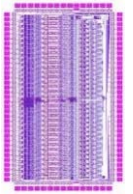
Detector	300 000 channels
PACIFIC chip (2015)	64 ch, TSMC 130 nm
Input Dynamic Range	0.5 to 32 pe
ADC resolution	Nonlinear, 2-bit, 40 MHz
SNR	≥ 10
Mx Pwr / Ch	< 10 mW



Shapers & Peak Detectors circuits

- **ROC chips : OPERA-ROC, early 2000**
  - For OPERA Target Tracker at Gran Sasso, 3000 chips

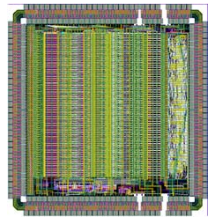




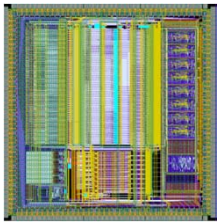
Chip	DType	Ch	Plrty	Dyn Range	Spec
MAROC	PM	64	< 0	5 fC- 5 pC	64 trigger outputs, internal 8/10/12-bit ADC for charge measurement
SPACIROC	PM	64	< 0	2 pC - 220 pC	Fast photon counting (50 Mhz)
PARISROC	PM	16	< 0	50 fC - 100 pC	Internal TDC (<1 ns), 16 trigger outputs
SPIROC	SiPM	36	> 0	10 fC -300 pC	36 HV SiPM tuning (8 bits), internal 12-bit ADC for charge & time measurement
EASIROC	SiPM	32	> 0	10 fC -300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs
CITIROC	SiPM	32	> 0	10 fC -300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs
PETIROC	SiPM	32	< 0	100 fC -300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs, internal 10-bit ADC for charge & time (25 ps)

- **Flexible Front-End → Variants suited to**
  - Detector type, # of channels, Input Dynamic Range
- **Adaptive Back-End**
  - 8/10/12-bits ADC for charge measurement
  - W /Wo time measurement, 1 ns / 25 ps TDC
  - Counting

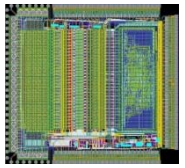
MAROC3



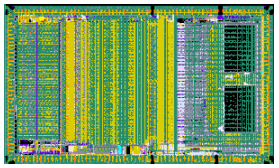
SPACIROC



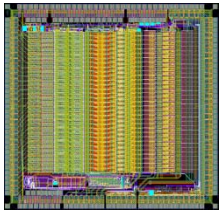
PETIROC



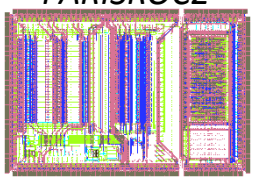
SPIROC2



EASIROC

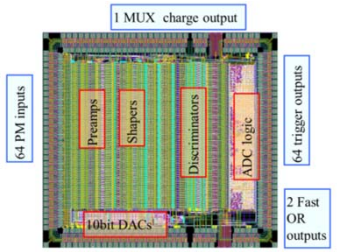


PARISROC2



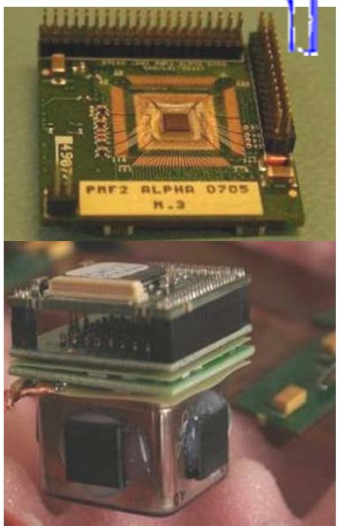
Multi-Anodes PMT Read-Out Chips

- **MAROC - From underground to space**
  - Produced for ATLAS Luminometer
    - 1000 chips, 2006
  - Improved Maroc3
    - 1000 chips (2010) for > 50 users
      - Double-Chooz, Neutrinos experiment
      - Memphyno, Water Cherenkov R&D
      - Medical Imaging, …



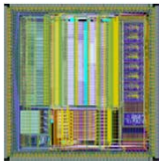
MAROC 3, 16 mm², 0.35 SiGe

64 channels (Z_{in} 50-100 Ω)
6-bit individual gain correction
Auto-trigger on 1/3 p.e. at 10 MHz
12-bit Wilkinson ADC Multiplexed on the Charge Output
Power = 3 mW/ch



MAROC 2 for ATLAS Luminometer

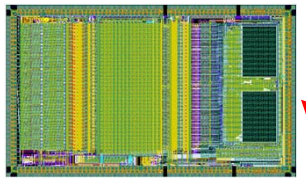
- **Modified for EUSO Balloon (Launched 08/2014) / JEM EUSO**
  - To observe Extensive Air Showers in the earth's atmosphere
- **SPACIROC** (Col. JAXA/Riken/Konan University)
  - Analog Front-End (64 ch): ~MAROC3
  - Back-End: Charge digitization replaced by TOT photoelectrons counting (<50MHz)
  - Improved power consumption < 1 mW/ch
  - Radiation tolerant : triple voting



SPACIROC

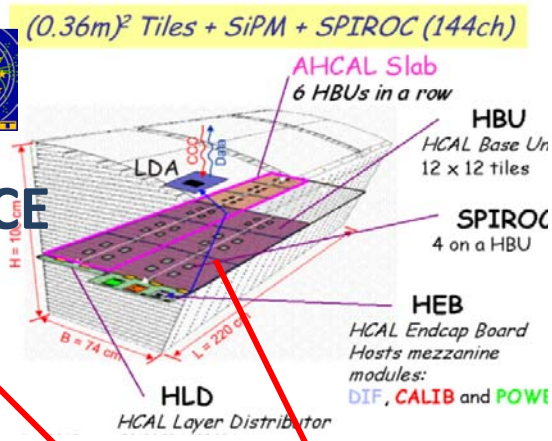
SiPM Readout chips

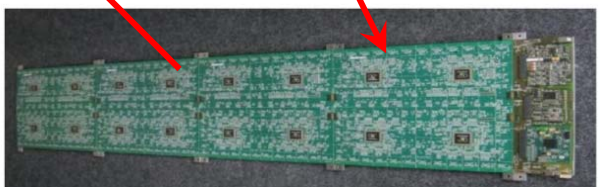
- **SPIROC for Analog hadronic calorimeter of CALICE**
  - F-E customized @ 36 channels
  - B-E implements Time Measurement
  - Embedded inside the detector
    - Power budget



SPIROC, 0.35 SiGe

36 ch., auto-trigger & 15bit readout
Energy measurement : 15 bits, 2 gains
Auto-trigger down to ½ p.e.
Time measurement up to ~1ns
Power: 25µW/ch (pulsed power)



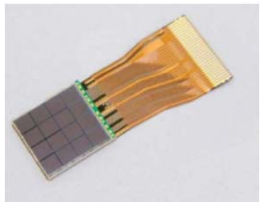


HCAL Base Units

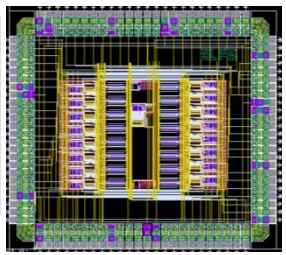
SiPM cameras for Cerenkov Telescope Array

- **Small Size Telescopes → CITIROC**
  - SPIROC derived
    - 32-ch, Charge & Trg , No ADC/TDC

- **Large Size Telescopes → ALPS R&D**
  - SiPM: an alternative to PMTs
    - Same detector among telescope classes
  - Creating a large SiPM sensor
    - Summing the pixel signals of a matrix



4x4 SiPM Hamamatsu matrix



ALPS 12mm2, SiGe 0.35µm, 07/2014

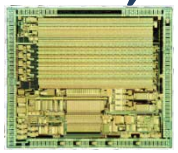
16 channels analog sum
Input range 0.2 to 2 10^3 p.e
Fast common trigger
Bias monitoring / pixel (8 bits)
Adjustable High & Low gain / pixel
Noisy pixel disabled

Switched Analog Memories

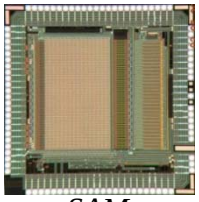
- **Fast Waveform Sampling → Amplitude & Time for signal reconstruction**
  - HAMAC by Irfu, for ATLAS LAr Calorimeter, 80 000 chips, 2002
- **Constant improvements: sampling speed, memory size, embedded A2D**

Irfu's chips for common, IN2P3/Irfu, detector developments

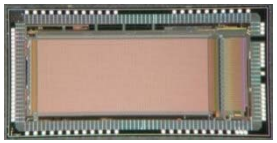
Analog Ring Sampler
4 Inputs @ 1 GS/s, 128 cells
AMS CMOS 0.8µm, 70 kT, 10 mm^2 , 2004
ANTARES & HESS I


ARS

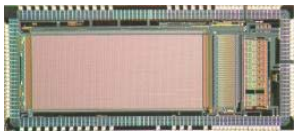
Swift Analog Memory
2 Inputs @2 GS/s, 256 cells
Embed Parallel 12 bits Wilkinson ADC
AMS CMOS 0.35µm., 50 kT, 11 mm^2, 2005
HESS II


SAM

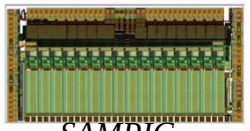
SAMLONG for SuperNEMO
2 Inputs @2 GS/s, 1024 cells
AMS CMOS 0.35µm, 300 kT, 18 mm^2, 2010-14
Implemented in VME Wave Catcher Boards


SAMLONG

NECTAR0
2 Inputs @2 GS/s in 1024 cells
Embed X X bits X ADC
AMS CMOS 0.35µm., 300 kT, 21 mm^2, 2010


NECTAR0

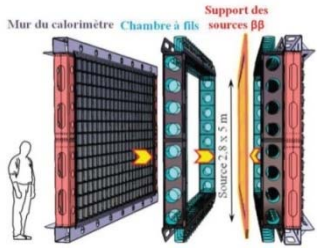
SAMPIC R&D, waveform based TDC
16 Inputs @10 GSPS for ~1 ps resolution
AMS CMOS 0.18µm, 7 mm^2 , 2013
ATLAS Foward Physics


SAMPIC


HESS I Camera module

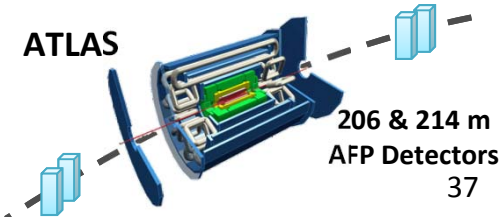

Wave Catcher -CAENversion-2014


NECTARCam



SuperNEMO demonstrator

cta
cherenkov telescope array



MAJ Photo NET
- Philippe - Laurent - Gisèle - Richard - Olivier -

- Point sur les circuits mentionnés
  - Bilan de réalisation du cahier des charges
  - Bilan de Production, de Mise en service (Durée de vie / Fiabilité)
  - Impact du circuit dans la communauté Nat/Internationale
- Evolution du circuit / du savoir-faire accumulé
  - Question: Aujourd'hui feriez-vous les mêmes choix?
  - Contraintes pour Evolution et **Breakthrough**
    - Architecture, Blocs fonctionnels / Building blocks
    - Moyens RH / Techno (process)

- Au niveau de chaque équipe
  - Collaboration sur ces thématiques
  - Les échanges entre labos du réseau µE / Autres
- AOB + Qui d'autre veut intervenir sur la µE pour ce réseau

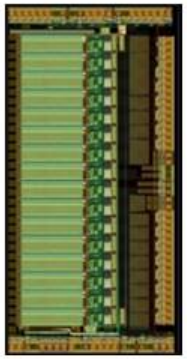
MAJ

SAMPIC: a 16-Channel, 10-GS/s Waveform-TDC for picosecond time measurement

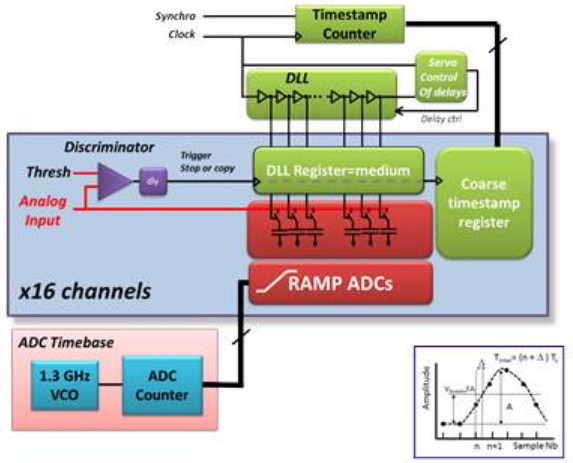
SAMPIC is a TDC directly working on analog signals !

- R&D project started in **January 2012, founded by P2IO labex**.
- **June 2013**: return from foundry of demonstrator ASIC (**SAMPIC0**) in AMS CMOS 0.18µm, 7mm²

⇒ validation of the WTDC principle, with fully integrated readout logics usable with detectors + test & acquisition board + acquisition software



- Works well with expected performance:
  - **7 to 11-bit Integrated Waveform Digitizer**
  - **1.6 GHz BW**
  - Sampling rate between **1.6 and 10 GS/s**
  - **100ns (7 bits) to 1.6µs (11 bits)** conversion time
  - **1 to 5 Gbits/s** output flow (LVDS)
  - Low power: **120 to 180 mW => ~10mW/channel**
  - **TDC time resolution is < 3.5ps rms!**



- **November 2014**: submission of **SAMPIC1**. **Chip received in April 2015 works well!**
  - Few bug corrections ok: Reset, Region of Interest, Central Trigger…
  - New design of the analog sampling cell is effective: better linearity and dynamic range
- **Mid 2015**: submission of **SAMPIC2** with many new features : reduced dead-time, independent channel ADC's, TOT measurement…

MAJ

SAMPIC: a 16-Channel, 10-GS/s Waveform-TDC for picosecond time measurement

Many applications…

- Bancs de test et tests sous faisceau de caractérisation de détecteurs ultra-rapides (diamants, MCPPMTs, Ultra Fast Silicon Detectors, SiPMs de course ...)
- Sous-détecteur TOTEM de CMS (*TOTal Elastic and diffractive cross section Measurement)* à ~200m de part et d'autre du grand détecteur pour voir les protons diffractés à petit angle et localiser les vertex → très grande précision requise < 5 ps rms pour le TDC
  → cartes en cours de réalisation
- ATLAS AFP (*Atlas Forward Proton*) : pareil que TOTEM
- Différents projets de TOF-PETs (NDAs en cours de signature…)
- Futur détecteur SHIP au CERN (fast timing detector pour trier les particules via leur temps de vol) et calorimètre en version double gain
- Futur détecteur CHIPS aux USA (manips Neutrinos, détecteur immergé dans l'eau)

MAJ

Feedback PACIFIC - 1

- **Point sur le circuit:**
  - **Prototype 64 voies (quasi) final envoyé en fonderie le 2 juin,**
  - **Le cahier des charges a beaucoup évolué au cours du projet**
  - **Production prévue pour l'automne 2016**
  - **Ce circuit sera monté sur le SciFi de LHCb**

Avis personnel: J'ai l'impression que les cahiers des charges sont de plus en plus flous et ont tendance à beaucoup changer/évoluer au cours de la vie d'un projet. C'est un problème car c'est assez incompatible avec la réduction du nombre de fonderie sur un projet.

- **Evolution du circuit/savoir faire accumulé:**
  - **Feriez vous les même choix : Non.**
    - **On nous a fortement conseillé de passer d'IBM à TSMC ce qui nous a fait perdre presque un an alors que la 130nm d'IBM tourne toujours.**
  - **Pas d'évolution prévue pour le moment, quelques pistes pour adapter le circuit à d'autre projet mais il est un peu tôt pour en parler (pas évident au vu du nbre de labo impliqué)**

MAJ

Feedback PACIFIC - 2

- **Au niveau de l'équipe:**
  - **Excellente collaboration entre 4 laboratoires de différents pays.**
  - **Très bénéfique pour notre visibilité au CERN.**
  - **Nombreux savoir faire accumulé/partagé tant au niveau technique que de la gestion de projet.**

Avis personnel:

- Avec des outils tel que SoS (fortement poussé par le CERN), il devient totalement transparent de travailler sur un même circuit avec des designers physiquement éloignés. Nos moyens n'allant pas en augmentant, pour moi, notre salut passera par là.
- Il est toujours surprenant de constater qu'il est plus facile de travailler avec des laboratoires étrangers qu'avec des laboratoires de notre institut…

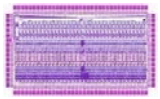
MAJ

CHIPS for MAPMT

OMEGA Microelectronics

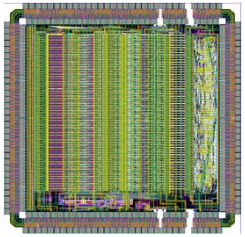
OPERA_ROC (2001)

32 Channels –
AMS BiCMOS 0.8 µm
3000 chips in 2002
OPERA Target tracker readout in Gran Sasso



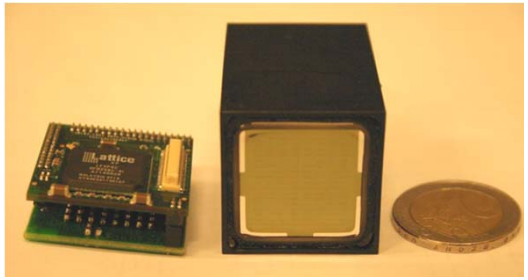
MAROC1 (2004)

Proto 64 channels
AMS SiGe 0.35 µm
(12 mm², Pw=5 mW/ch)



MAROC2 (2006)

1000 chips produced for ATLAS luminometer



MAROC3 (2010)

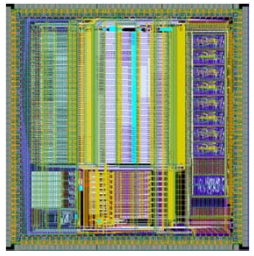
Lower power dissipation
Wilkinson ADC added
1000 chips produced
Double-Chooz, Menphyno, Juno, medical imaging (Valencia, ISS Roma)…

SPACIROC1 (2010)

64 channels for spatial use.
Front End similar to MAROC
Photo counting @ 50MHz
Digital part :Digitization,memorization
Power consumption < 1 mW/ch
AMS SiGe 0.35 µm 16mm2
1000 chips for EUSO Ballon (2014 flight) and TA
Collab APC, LAL, IRAP

SPACIROC2 (2011)

Proto for improvment
Phd work



SPACIROC3 (2014)

Photo counting @ 100 MHz
Innovative chip/detector
Défi instru. CNRS
Small production (mini euso)

CHIPS for PMT

MAJ

OMEGA Microelectronics

PARISROC1 (2008)

16 independent channels.

Auto triggered

Charge (10 bits) and time measurement (1ns)

AMS SiGe 0.35 µm 12mm2

Proto for PMm2 R&D (ANR)

Collab. LAL, LAPP, IPNO

PARISROC2 (2009)

V1 improvment- Phd work

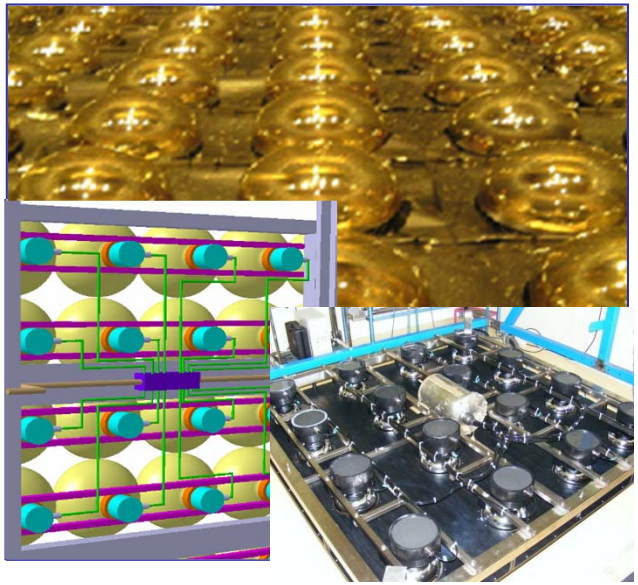
Small production for water cherenkov experiments.

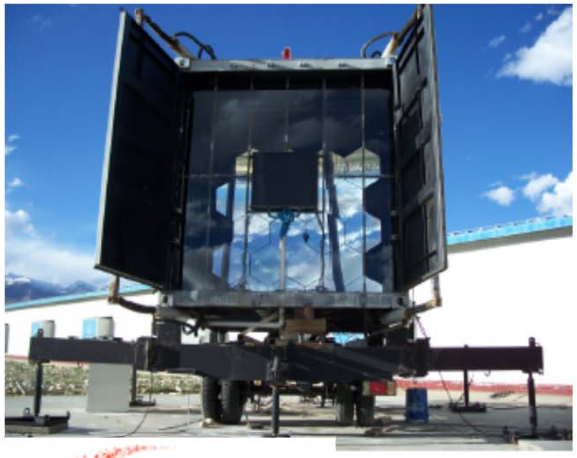
LHAASO (IHEP/IPNO) and LAGUNA-WA105 (APC)

CATIROC (2015)

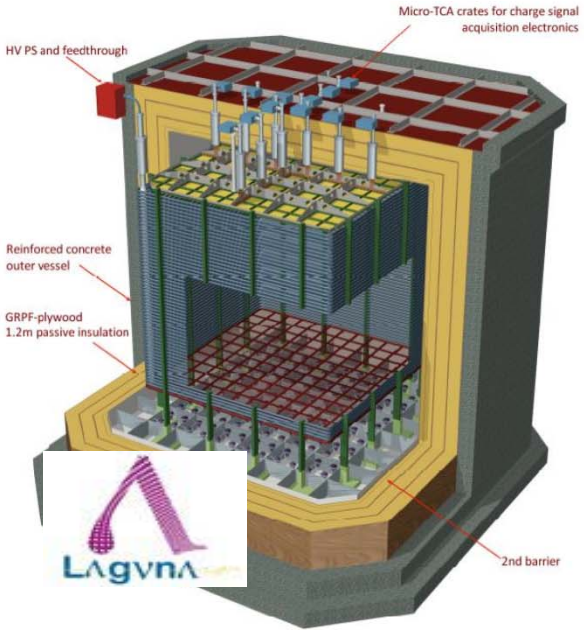
Parisroc evolution with new time measurement (100ps) and new charge measurement.

600 chips produced for LHAASO, JUNO





LHAASO



Chips for SiPM from SPIROC to TRIROC

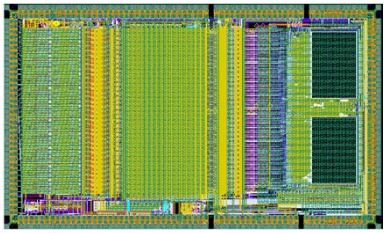
- **2005 : FLC_SiPM designed and produced for the ILC AHCAL (1 cubic meter, 38 layers, 2cm steel plates, 8000 tiles with SiPM) - 36 channels – 300 chips in AMS CMOS 0.8 µm**
  - **1st ASIC to readout SiPM**
- **SPIROC developed since 2007 for CALICE AHCAL EUDET techno. proto. and AIDA phys. prot.**

  several versions - 36 channels - AMS SiGe 0.35 µm – 32 mm2 – Coll. DESY, KEK

  Autotrigger 1/3 MIP- Digitize time to 1 ns

  Digitize charge on 15 bits - 16-depth analog memory

  Input 8bit DAC - Power pulse to 25 µW/ch

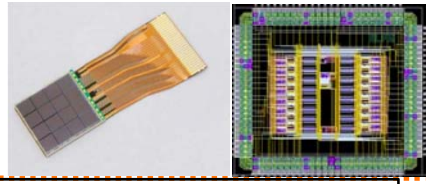


- **Variants of SPIROC: EASIROC designed in September 2009, CITIROC in 2013**

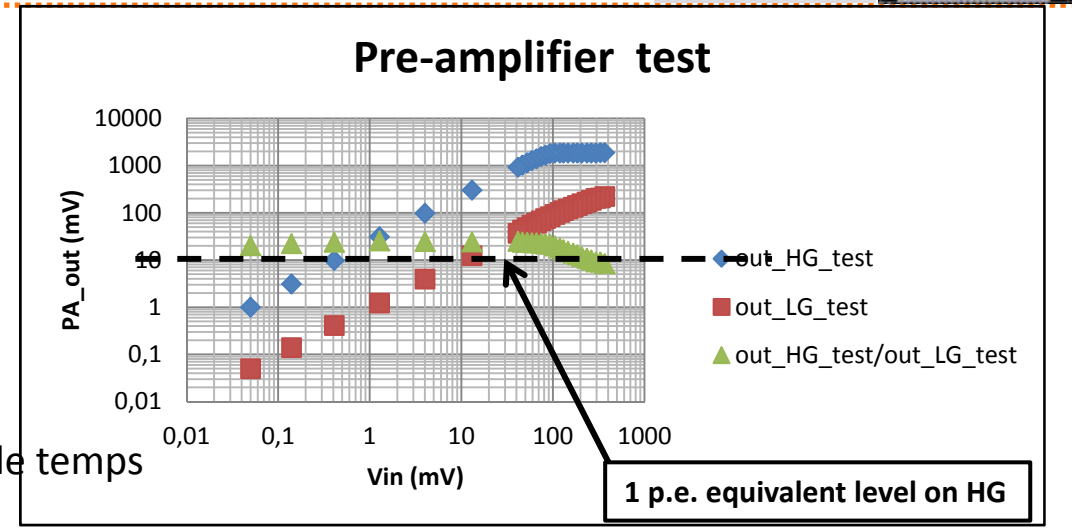
  "light" analog version of SPIROC for SiPM users (without ILC specific digital core)
- **Main applications using SPIROC/EASIROC/CITIROC chips for SiPM readout**
  - **Astrophysics: PEBS experiment (Aachen University), CTA**
  - **Medical imaging (Roma, Pisa, INMC Orsay, Valencia, etc.)**
  - **Nuclear physics: E40 experiment (KEK)**
  - **Volcanology: MuRay muon radiography of geological structures (INFN Napoli)**
- **Dedicated chip for fast timing and high timing resolution applications**
  - **PETIROC (November 2013)**
  - **TRIROC (March 2014) "FP7" project**

MAJ

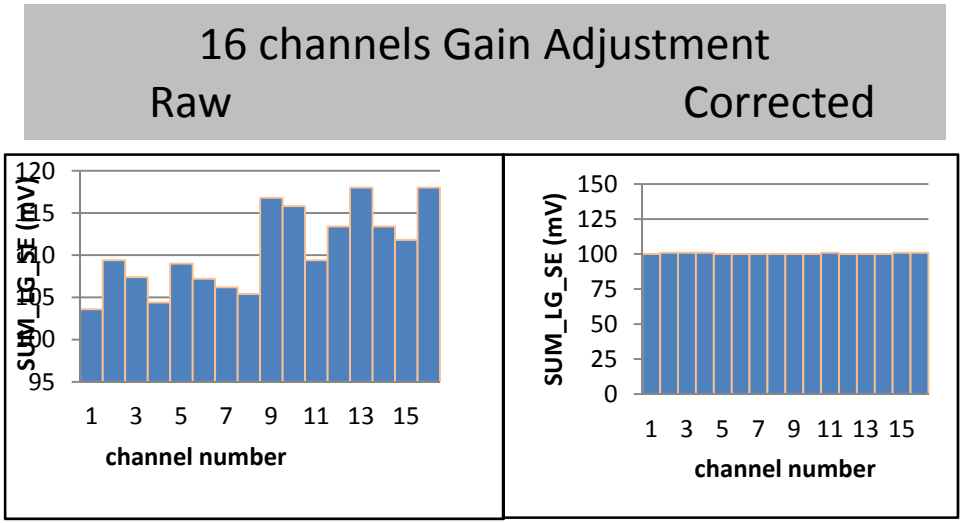
ALPS-LAPP



- Point sur le cahier des charges :
  - Dynamique OK
  - Contrôle gain OK
  - Contrôle « Overvoltage » OK
  - Préampli un peu lent
  - Pas de sorties différentielles … faute de temps



- Evolution
  - Architecture validée
  - Nouvelle version corrigée / améliorée
  - Renforcement de l'équipe obligatoire (fin de la thèse de Fatima Mehrez)
  - Soutien de CTA ?



- Equipes
  - Collaboration avec INFN Padova
  - Aide importante des collègues de l'IPNL sur les outils pour la finalisation du chip

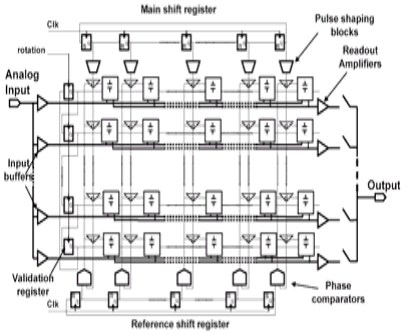
Merci Edouard!

Switched Analog Memories

MAJ

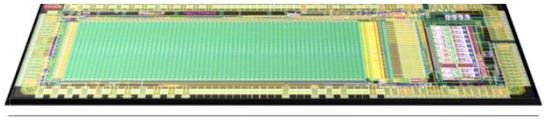
Medium Size Telescope NectarCAM

NECTAr chips



Principle of the matrix sampling structure

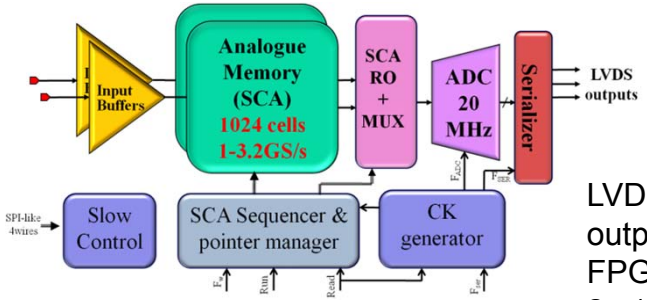
Realisation : Eric Delagnes



CMOS 0,35 µm Nectar Layout

Production phase :
> 60 000 chips
Yield : 80 %
Test production

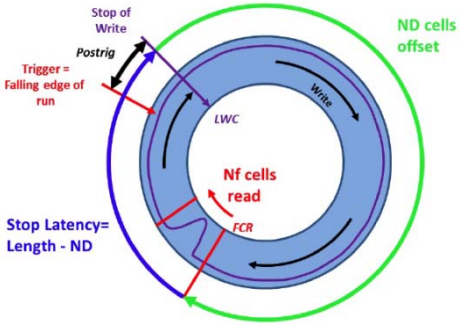
- ***0.5Gs/s-3GS/s analog memory (SCA) + (12bit/ 20 MHz ADC).***
  - ***2 fully differential channels (1024 cell memory each):***
  - **2 photodetector channels with "mono gain".**
  - **1 photodetector channel with 2 gains.**
- ***Usable as L1 buffer with programmable latency (ROI readout)***
- ***Target: Performances = those of SAM (HESS2) with less power (was 300mW***



Global view of the Nectar0 chip

ADC 20 MHz
Pipeline 12 bits
Fatah Rarbi
Daniel Dzahini

LVDS outputs to FPGA
2x 120 MHZ serial link.



Principle of operation as circular buffer

Gaseous Detectors Network

Drift **C**hambers

Drift chamber - SHARAQ spectrometer -Japan

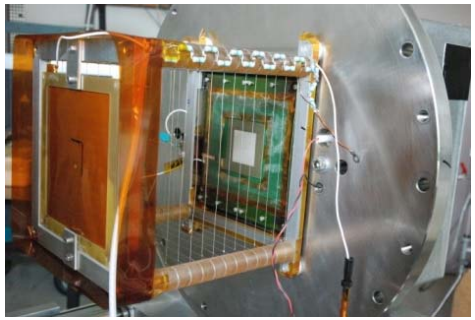
Multi **W**ire **P**roportional **C**hambers

MWPC 1m²
ALICE-Muon Arm - CERN

Micro **P**attern **G**aseous **D**etectors
- Micromegas or GEM -

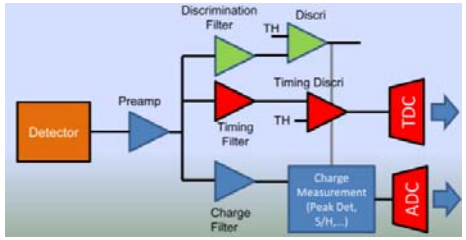
Micromegas
SDHCAL- ILC

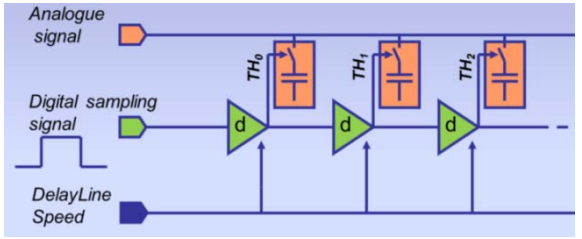
Ionizing **C**hambers
TPC (IO + MPGD or MWPC)



Micro TPC + Micromegas for MIMAC @ LSM Modane

- **FEE for Gaseous detectors is similar to FEE for photo-detectors**
  - Shapers and Peak Detectors & Waveform Samplers

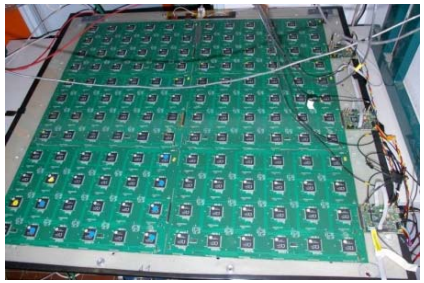




  - With additional constraints such as material and power budgets

Extended FEE for Gaseous Detectors

HARDROC: GRPC DHCAL - CALICE

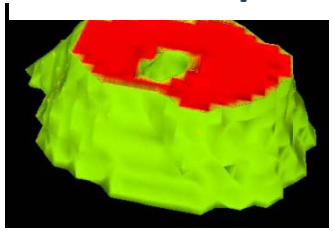


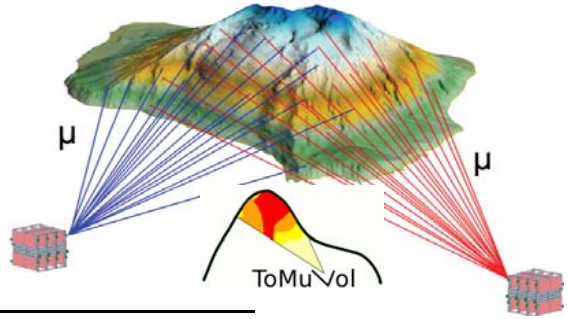
Embedded FEE in scalable GRPC detector layer

Demonstrator, 1 m³
40 layers
400 000 Channels

TOMUVOL: Volcano Tomography with Muons

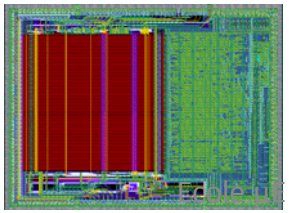
A DHCAL Spinoff





- 64 ch, 3 discri/ch
  - 3 encoded charge values
- Event memory
- Power pulsing
- 2010: 10 000 chips

HARDROC2

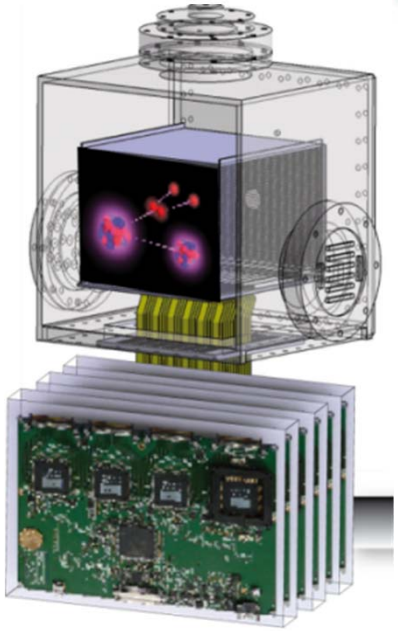


26 mm², SiGe 0.35 µm

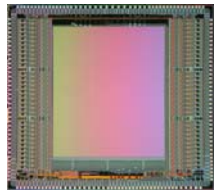
AGET for ACTAR TPC R&D

- To Study exotic nuclear structures @SPIRAL2
- AGET for the 2048 channels of the TPC
  - Variant of AFTER for µmegas @ T2K (6000 chips)

Active Target TPC



AGET 0.35 µm CMOS, 65 mm², 2010



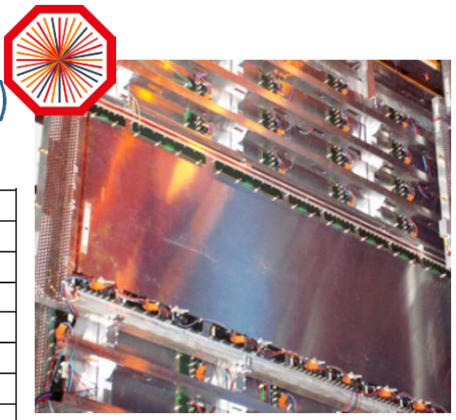
64-ch, Pos / Neg polarity
4 Ranges : 120 fC; 240 fC; 1 pC; 10 pC
16 Peaking Time Values (**50ns to 1µs**)
Fsampling: **1-100MHz**; Fread**: 25MHz**
Auto trig: discri/ch + DACthreshold
Ch RO: All, Hit, Specific channels
SCA cells readout: **128/256/512**

256 channels AsAd board
- 4 x AGET
- 12-bits, 25 MHz digitizer
- AGET steering, test, calibration

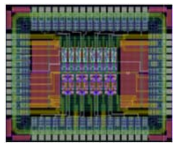
Designs for specific configurations

Trigger upgrade of Dimuon Spectrometer of ALICE

- FEERIC dedicated to new RPC in avalanche mode (aging improvement)
- To replace ADulT chips for current RPC in streamer mode
- To provide calibrated pulses to trigger logic
- >3000 chips to produce, test, install, 2015-18



FEERIC
4mm²
0.35µm
CMOS



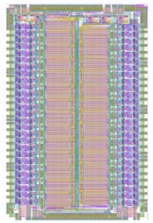
Test Board

Number of ch.	8
Input polarity	±
Dynamic range	Q=20 fC-3 pC
Input noise (rms)	$< 4fC$
Power cons.	$< 100mW/ch$
Power supply	3 V
One-shot	yes(100ns)
Time resolution (rms)	< 1 *ns*
Time walk	< 2 *ns*
Output format	LVDS, 23 ± 2 ns

TDC for SNEMO @ LSM

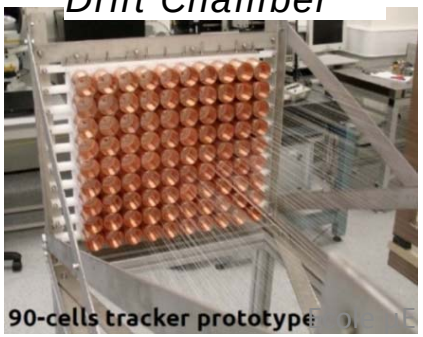
- 54 ch. TDC, 3.6 ns resolution
- Configurable Inputs - gain & discri. threshold - for anodic and cathodic signals
- 150 samples

Test board



0.35 CMOS
40 mm2
2011

Drift Chamber

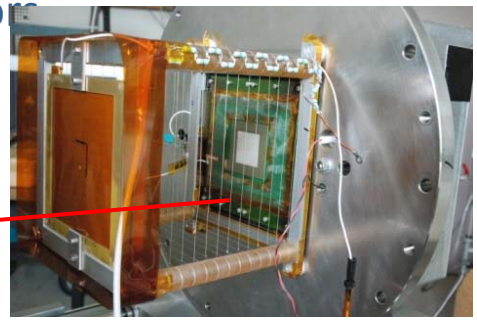


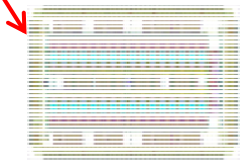
Manchester-UK courtesy

Micromegas TPC, MIMAC @ LSM

- 64 ch., Coincidences detect. + TOT measures
- 50 MHz discriminators
- 400 MHz serializer
- ~100 samples

256 channels board





.35 µm
SiGe BiCMOS
23 mm²
2010

MAJ Gas NET
- Gisèle - Olivier - Laurent - Sébastien - LPSC -

- Point sur les circuits mentionnés
  - Bilan de réalisation du cahier des charges
  - Bilan de Production, de Mise en service (Durée de vie / Fiabilité)
  - Impact du circuit dans la communauté Nat/Internationale
- Evolution du circuit / du savoir-faire accumulé
  - Question: Aujourd'hui feriez-vous les mêmes choix?
  - Contraintes pour Evolution et **Breakthrough**
    - Architecture, Blocs fonctionnels / Building blocks
    - Moyens RH / Techno (process)

- Au niveau de chaque équipe
  - Collaboration sur ces thématiques
  - Les échanges entre labos du réseau µE / Autres
- AOB + Qui d'autre veut intervenir sur la µE pour ce réseau

MAJ

Status FEAST / SuperNEMO

- SuperNEMO
  - ✓ Physique du neutrino (Etude de la double désintégration β sans neutrino)
  - ✓ Démonstrateur SuperNEMO
    - Construction 2015-2016 au LSM
    - ≈2000 voies pour le Tracker (150 ASICs)

FEAST

FEAST Production

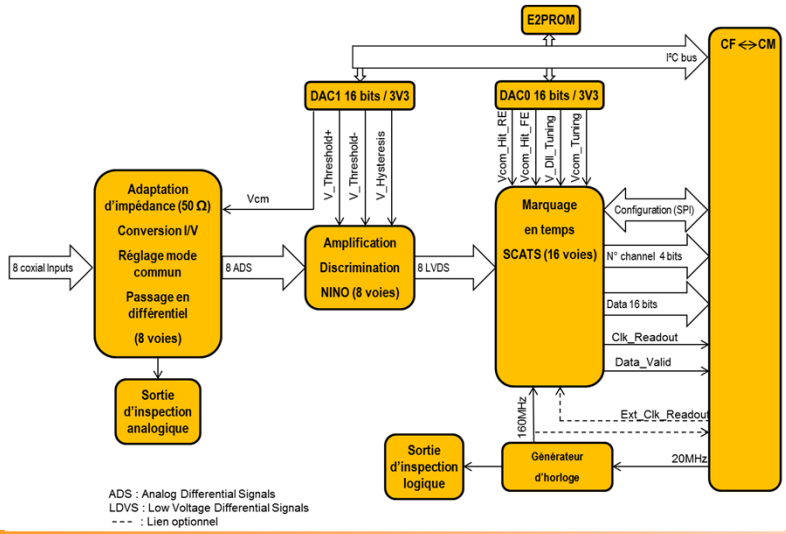
- FEAST
  - ✓ Techno: AMS 0,35µm CMOS
  - ✓ ASIC pour le Tracker
  - ✓ ASIC codeur de temps avec mise en forme analogique du signal à traiter
  - ✓ 54 voies indépendantes
  - ✓ 150 ASICs testés, en cours de câblage sur les 65 cartes Tracker (FEB)

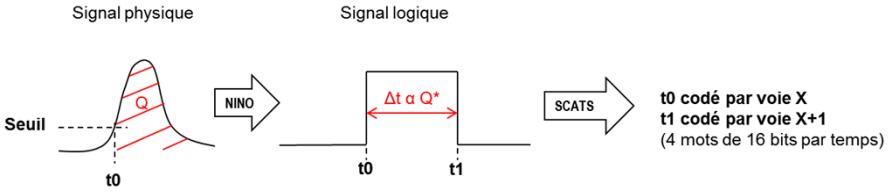
- Front-End Board Tracker (FEB)
  - ✓ Prise en charge par Université de Manchester
  - ✓ Ecriture du firmware par Manchester et LAL
  - ✓ dans les 2 ans à venir: Aide au débogage et à la mise en fonctionnement des cartes FEB, Participation à la mise en service du Tracker

MAJ

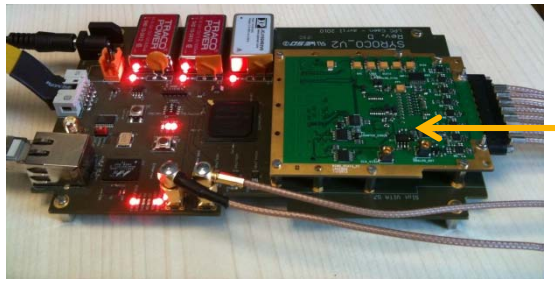
Carte ETC (Eight Time Channels) intégrant SCATS

- Localisation spatiale des particules avec détecteur diamant segmenté double face
- Système d'acquisition FASTER
- Caractéristiques carte ETC :
  - 8 voies de mesures de temps indépendantes
  - Seuil de déclenchement réglable : 10 fC à 100 fC
  - Résolution temporelle espérée ≈ 70 ps rms (sans prise en compte du walk)
  - Dynamique de comptage sélectionnable jusqu'à 20 jours (48 bits @ 160MHz)
  - Temps mort individuel d'une voie ≈ 50 ns
- Status :
  - Firmware en cours d'écriture et de test





Seuil réglable : 10 fC à 100 fC



MAJ

FEERIC

- **Point sur le circuit:**
  - Les performances mesurées de la version 3 ont été **validées**. FEERIC a fait l'objet d'une **revue au Cern** en mars dernier.
  - Une chambre **RPC complète de l'expérience Alice** au LHC a été équipée avec le nouvel ASIC; les performances obtenues dans le prochains mois (bruit → niveau mini. des seuils → HT de fonctionnement → durée de vie du détecteur) donneront ou non le "feu vert pout la production finale (≈ 4000 chips) fin 2015 ou début 2016
- **Evolution du circuit/savoir faire accumulé:**
  - Feriez vous les mêmes choix : **oui, sans doute …**
    - Il fallait faire mieux (amplification), plus rapidement (2 ans) et avec moins de ressources par rapport à la 1ère version du circuit(ADualT).
    - Cela a été possible grâce à la fiabilité de la techno (AMS), le **savoir-faire** acquis et une architecture conventionnelle.
    - **La modélisation aux interfaces (RPC, strip, PCB, ASIC) a été prise en compte (trop) tardivement.**
- **Collaborations, échanges**
  - Au début du projet, échanges avec les collègues de Bari (CMS) qui nous ont prêtés des circuits pour test sur RPC.
  - Pas d'autres collaborations nécessaire ensuite.

MAJ

FATALIC

- **Point sur le circuit (voir le poster):**
  - R&D débuté en 2010 sur la techno IBM.
  - Prototype final disponible pour les tests sur le démonstrateur au Cern cet automne.
- **Evolution du circuit/savoir faire accumulé:**
  - Feriez vous les mêmes choix : oui, sans doute ….
    - ASIC adapté à la grande gamme dynamique requise
    - Sortie des données numérisées → simplicité et fiabilité
    - Changement de nœud techno. (350→130): gain d'expérience
    - Ce projet a profité du R&D ILC/Calice (ADC)
- **Collaborations, échanges:**
  - Ce projet est né d'une collaboration informelle entre Chicago (JF Genat) et Clermont (J Lecoq). Chicago a abandonné le projet, nous nous sommes retrouvés seuls.
  - Echanges au sein du pôle MicRhAu.
  - Cern: support (léger) du Cern pour la prise en main de la techno IBM en 2010 et fourniture de PADs SLVS.

MAJ

ASICs pour détecteurs gazeux à l'IRFU

Production et test des puces en AMS 0,35 µm AGET pour le système GET et DREAM pour CLAS 12 fin 2014.

Puces	Techno	Testées	Rendement	Utilisateurs
AGET	AMS 0,35	2500	83 %	20
DREAM	AMS 0,35	1250	72 %	CLAS 12

AGET: Environ 20 utilisateurs (satisfaits) du système **G**eneric **E**lectronics for **T**pc (un utilisateur de plus la semaine dernière) pour 1300 puces AGET à travers le monde.

Financement GET par ANR. Collaboration nationale (CENBG,GANIL, IRFU) et internationale (EU,Japon). Projet aujourd'hui terminé.

⇒ On commence à réfléchir (on discute avec le CENBG) à la suite.

Evolution d'AGET: « spaceproofisation » pour le projet HARPO (LLR/IRFU)

DREAM: 30 cartes FEU (accueillant chacune 8 DREAM) déjà réalisées pour lire des micromegas.

Pour le spectromètre de CLAS 12 au J-Lab.

⇒ Installation partielle cet été pour un run de physique en 2016.

⇒ Installation complète en 2017.

Mais aussi pour tracker Asacusa au CERN.

HARDROC & MICROROC for CALICE SDHCAL readout

HARDROC1 : Hadronic Rpc Detector Read Out Chip
64 channels in AMS SiGe 350nm
semi digital readout with 3 thresholds
Auto trigger and full power pulsing
First proto in **2006**

HARDROC2 : 20mm2
auto trig on 10fc up to 20pc (3 thresholds)
Full power pulsing => 7 µW/ch
Chip embedded in detector
6 000 chips produced in **2010** → EUDET milestone

HARDROC3 : 30mm2
Independant channels with zero suppress
I2C link (@IPNL) for slow control and triple voting
600 chips produced in **2015** → AIDA milestone

1 m³ RPC detector, 40 layers
Hardroc2: 370 000 channels

@IPNL Lyon

MICROROC : Micromegas Read Out Chip
Very similar to HARDROC except for the input preamp (collab. with LAPP Annecy) and shapers (100-150 ns)
Auto trigger on 1fC up to 500fC
Pulsed power: 10 µW/ch (0.5 % duty cycle)
HV sparks protection (@ LAPP)
First proto in 2010
800 chips in 2011 (for 1m2 and 4m2 in TB)
300 chips in 2015

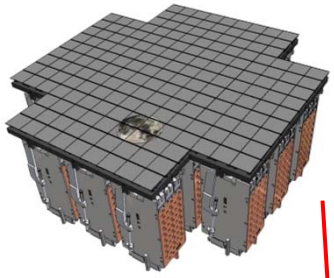
1m2 equipped with 144 MICROROC

@LAPP Annecy

Collab. IPNL, LLR, LAPP

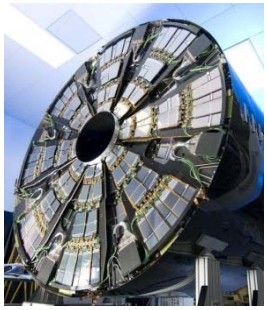
Semiconductors Network

CCD



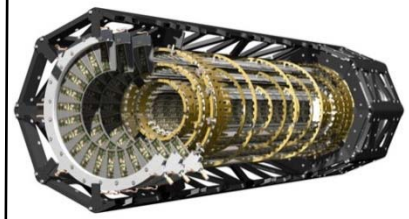
CCD for LSST - Chile
Studies &
Production testing

Silicon Strips



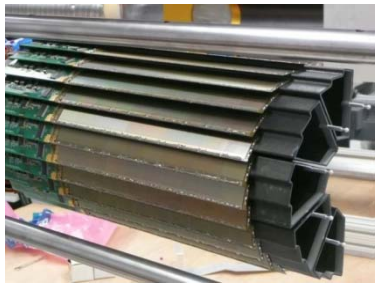
CMS Silicon Strips
TEC Petals:
Test & Construction

Hybrid **P**ixel **S**ensors



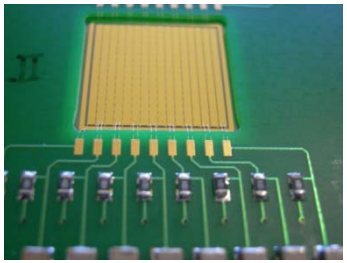
ATLAS Pixel Tracker
Test & Construction,
HPS design

CMOS **P**ixel **S**ensors



STAR PXL Tracker
CPS design

Diamond

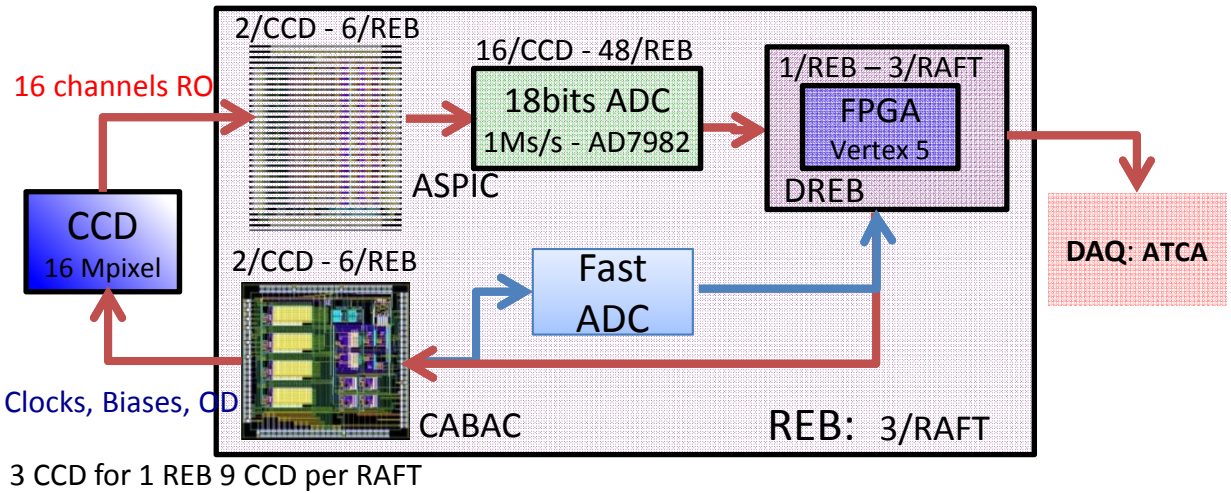


Beam profiler
SPIRAL-France
Double-sided multi-strip
detector prototype

8 channel FE board
Time & Energy measurement

Faster: SYROCO_AMC board @ GANIL

Readout & Steering ASICs on DAQ Board

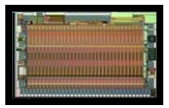
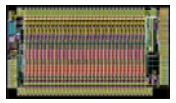


3 CCD for 1 REB 9 CCD per RAFT

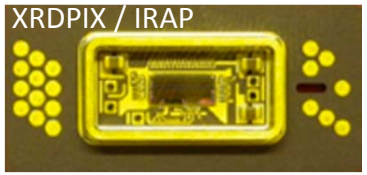
ASIC for space applications at IRFU

IDeF-X family for Cd(Zn)Te or Si - Drift D, Double Sided D

- CSA+Shaper+peak detectors architecture
- Self triggered with low detection threshold (2 keV with CdTe)
- Very low noise for high energy resolution spectro-imaging systems
- Commercial low cost CMOS technology (AMS 0.35 & 0.18, XFAB 0.18)
- Hardened design for “space proof” missions

	Chip	Det Type	Ch	Noise Floor (e-)	plrty	Dyn (ke-)	Power (mW/channel)	Output	Radiation
	ECLAIRs	Cd(Zn)Te	32	33	-	50	3,4	Mux diff	SEL hardened + SEU flag
	BD	Cd(Zn)Te DSSD	32	33	both	50	3,4	Mux diff	SEL hardened + SEU flag
	HD	Cd(Zn)Te	32	18	-	240	0.9	Mux diff	SEL free + SEU flag
	LXE	Cd(Zn)Te DSSD LiqAr TPC	32	33	both	240	2.2	// single	SEL free + SEU flag
	D^2R_1	Cd(Zn)Te DSSD	256	25	both	60	0.3	Mux per Line	SEL hardened + SEU flag

IDeF-X ECLAIRs

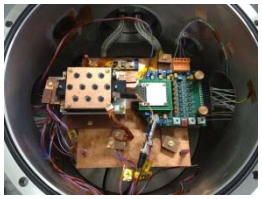


XRDPIX detection module for SVOM (CNES and CNSA mission)

IDeF-X HD

Micro gamma-camera for Solar Obiter (ESA Mission)

IDeF-X BD



ASTRO-H (JAXA mission): detector characterization

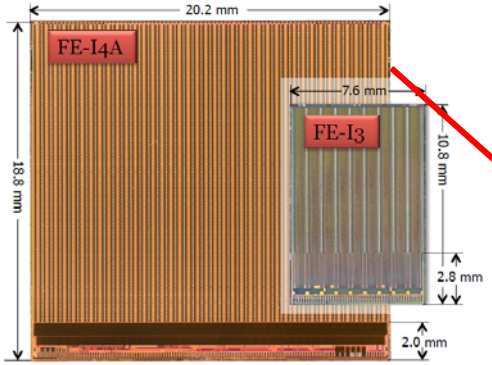
STEIN module for Solar Orbiter

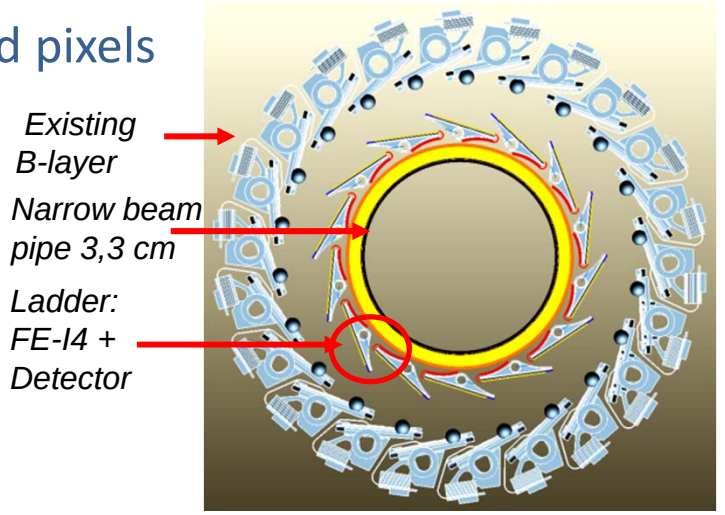
59

Hybrid Pixel Sensors

- **FE-I4 chip for Insertable B-Layer of ATLAS upgrade (Phase 0, 2014)**
  - IB-Layer: 16 ladders, 384 FE-I4 with associated pixels

Pixel size	50 x 250	µm²
Matrix array	80 x 336	pixel
Chip size	20.2 x 19.0	mm²
Active fraction	89	%
A - D currents	10 - 10	µA/pix
Analog voltage	1.4	V
Digital voltage	1.2	V
Process	130 nm	
Radiation Tol	> 200	Mrad





IBL on new beam pipe

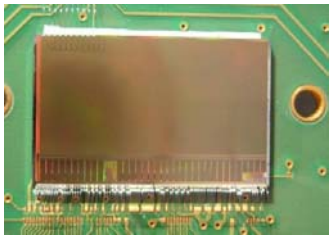
- **Building Blocks design**
  - Pixel level
    - Configuration memory
  - Common functionalities of FE-I4
    - Global configuration memory
    - 10-bit ADC Chip monitoring
    - Buffers for characterization

- **ATLAS/CMS - Phase 2**
  - Member of RD 53 for Pixel RO chip
    - WG1, Radiation test / qualification
    - WG3, Simulation-Verification test bench
    - WG5, Analog Design (pixel ADC)
    - WG6, IP blocks

- **Radiation dose & SEU effects measurements**

CMOS Pixel Sensors: A Long Term R&D

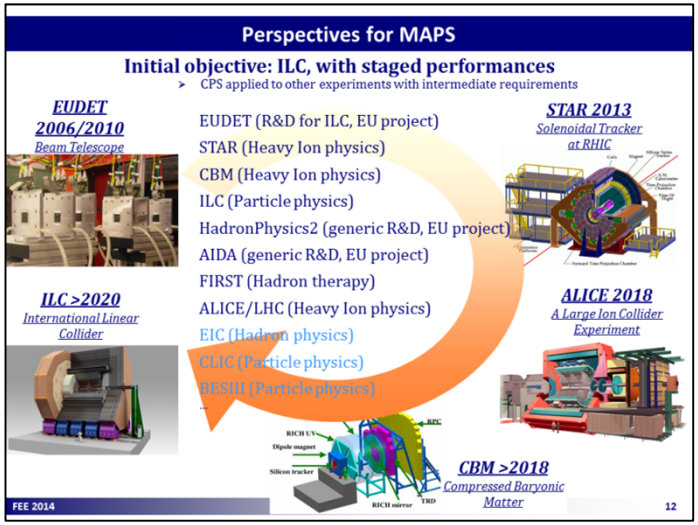
- **1999 R&D initiated with ILC as ultimate objective**
  - Developing CPS with staged performances
- **2008: Mimosa26 for EUDET telescope**
  - Major proof of concept achieved (IN2P3/Irfu)



Mimosa26
~2x1 cm²
660 kpixels

Eudet Telescope
6 reference planes of
Mimosa26, 50µm thin
$\sigma_{s.p.}$ 2 µm on DUT

- **CPS for experiments with increasingly demanding requirements**



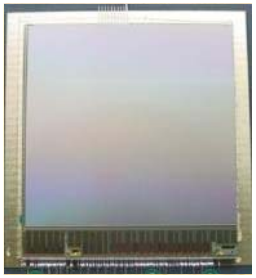
Expt System	σ_T µs	σ_{Sp} µm	TID Rad	Fluence n_{eq}/cm^2	T_{op} °C
STAR-PXL	<~ 200	~ 5	150 k	$3x10^{12}$	30
ALICE-ITS	≤ 30	~ 5	700 k	10^{13}	30
CBM-MVD	10-30	~ 5	<~10 M	<~ 10^{14}	<<0
ILD-VXD	<~2	<~ 3	O(100) k	O(10^{11})	<~30

Time

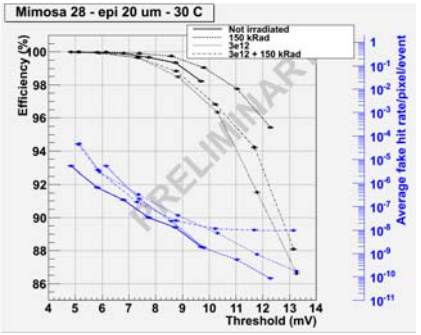
Synergies - Constraints

CPS for PXL detector @ STAR

- **Mimosa 28, ~4 cm², 1 Mpixels**
  - ~21 µm pitch, 50 µm thin, > 400 Ω.cm Hres Epi
  - $\sigma_{s.p.}$ ~>3.5 µm, Efficiency > 99%, T_{Ro} = 185 µs
  - Rad Tol= 150 krad, 3 10^{12} $n_{eq}.cm^{-2}$ @ +30°C



Mimosa 28, ~4 cm², 0.35 µm 2-well CIS , Hres epi layer



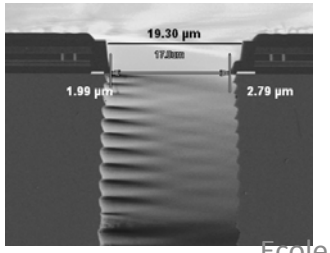
Detection efficiency &Fake rate

928 x 960 pixel array, pitch 20.7 µm
In pixel CDS + column discriminators
Zero suppression
FRead 160 MHz on 2 LVDS outputs
Sensor configuration via JTAG
~170 mW/cm² @ 3.3V @ 35°C
Integration time 185.6 µs, $\sigma_{s.p.}$ ~>3.5 µm

- **PXL installed in January 2014**

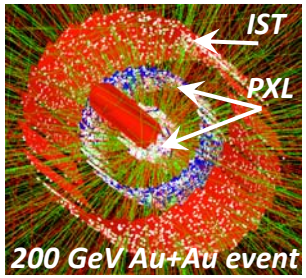
2 layers, radius: 2.8 & 8 cm, 40 ladders, 400 sensors, 0.15 m²

- **Edgeless for improved sensor abuttal**
  - Wafers are pre-diced with DRIE
  - Sensors are released during wafer thinning

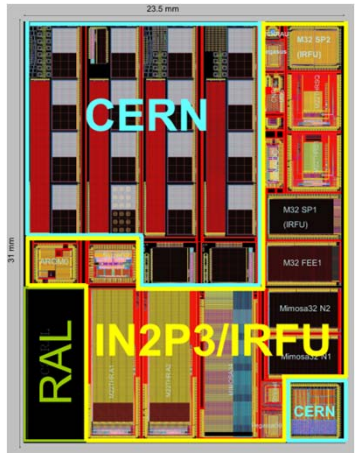


Wafer Scribe Lines pre-diced with DRIE AMS courtesy

Typical event of 4 months of data taking

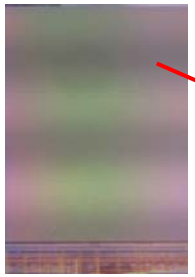


CPS for ALICE ITS upgrade

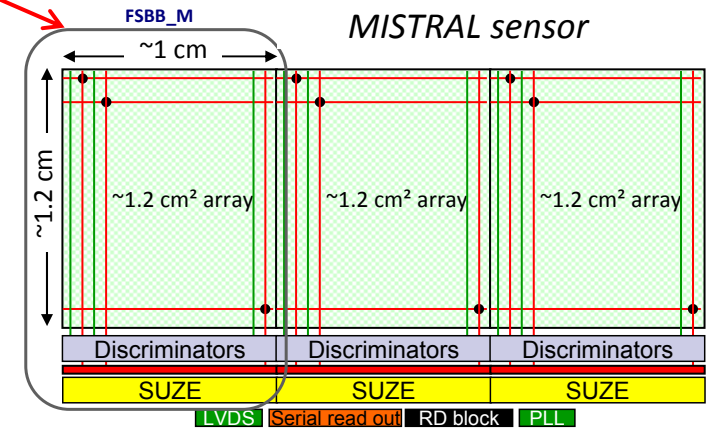


Q1 2013 run
4-well CIS 0.18 µm
3.1 x 2.3 cm² reticle

- **ITS upgrade: 10 m² of CPS to produce (2016)**
  - Towards a new state of the art (& challenge) based on the accumulated expertise on previous sensors
  - Common R&D with CERN on sensors developed in //
    - Synchronous Readout CPS (Mimosa 28 like)
      - Mature architecture → robust → MISTRAL -IN2P3 driven
    - Asynchronous Readout CPS
      - New & challenging, exploits process potential → ALPIDE - CERN driven
- **MISTRAL, based on 3 submatrices**
  - Full Scale Building Block (05/2014)
    - 160 kpixels matrix
    - 22 x 33 µm pitch → $\sigma_{s.p.}$ ~5 µm
    - Readout Time = 40µs
    - Noise: TN ~0.87 mV, FPN ~0.55 mV @ 30° C
    - Efficiency >99.5% (To Validate @BT 10/2014)
  - Address ALICE ITS requirements

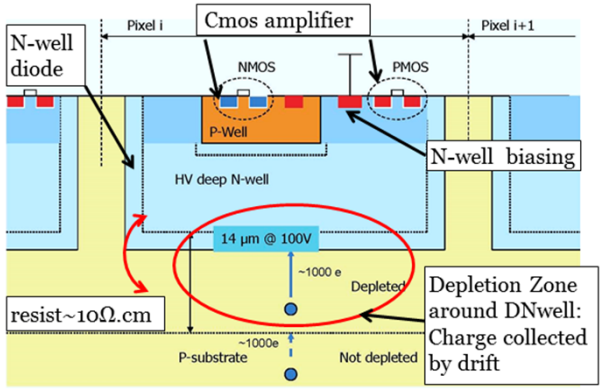


FSBB first prototype
0.18µm CIS Hres epi

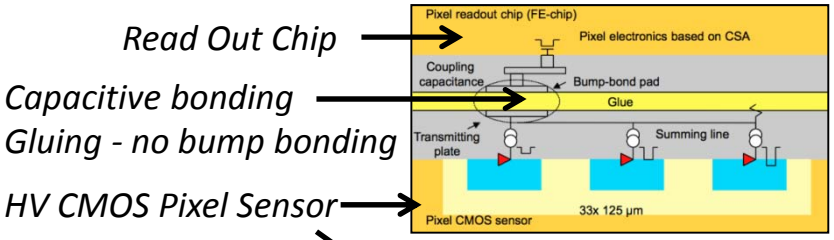


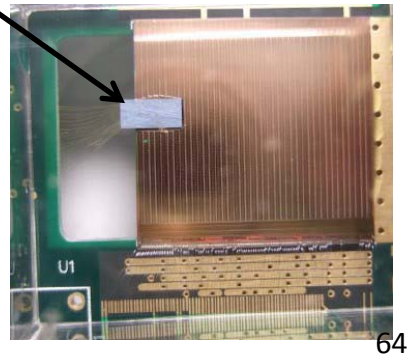
Hybrid R&D, RO chip + HV-CMOS sensor

- **Exploit Deep Nwell featured by industrial CMOS process**
  - DNW Sensing diode polarized @ few tens Volts
    → To collect charges by drift only
      - To improve speed & Radiation hardness
  - Embedded CMOS amplifier
      - Before interconnection to RO chip → Low noise



- **Expected performances**
  - Rad Hard Sensor up to 1 Grad
      - Thin depletion zone (10µm), low bias voltage
  - Small and fast pixels
      - 33 x 125 µm , (FEI-4: 50 x 250 µm)
  - Low material budget
      - Thinned down
  - Low cost
      - Standard process + cheap bonding





HV2FEI4p1 glued on FE-I4

MAJ Semi NET
- Philippe - LPC Caen - Olivier - Christine - Patrick-

- Point sur les circuits mentionnés
  - Bilan de réalisation du cahier des charges
  - Bilan de Production, de Mise en service (Durée de vie / Fiabilité)
  - Impact du circuit dans la communauté Nat/Internationale
- Evolution du circuit / du savoir-faire accumulé
  - Question: Aujourd'hui feriez-vous les mêmes choix?
  - Contraintes pour Evolution et **Breakthrough**
    - Architecture, Blocs fonctionnels / Building blocks
    - Moyens RH / Techno (process)

- Au niveau de chaque équipe
  - Collaboration sur ces thématiques
  - Les échanges entre labos du réseau µE / Autres
- AOB + Qui d'autre veut intervenir sur la µE pour ce réseau

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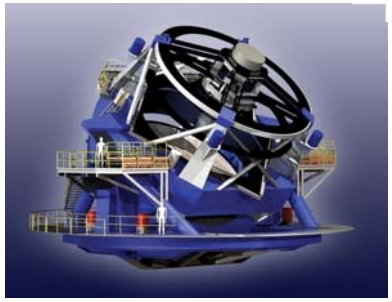
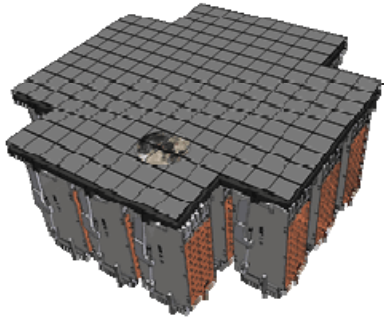
ASPIC & CABAC (depuis 2007)



Large Synoptic Survey Telescope - Chile



Focal plane array : 3.2-Gigapixel Camera

- Bilan
  - Cahiers des charges intégralement remplis
  - **Production et test de 1000 circuits en 2015 pour intégration finale mi-2016**
- Valorisation : projet de prématuration déposé au CNRS pour financer un « controleur-lecteur » de CCD ; en cours…
- Perspectives → projet DAMIC (Dark Matter in CCDs) **a novel dark matter experiment**
  - Accroitre l'intégration (éléments passifs dédiés à la charge de l'étage de sortie du CCD, capacité de liaison…)
  - Envisager le changement de technologie
    → AMS 0.18 HV : obsolescence de la 0.35

CdTe pour applications spatiales

-1-Solar Orbiter

IDeF-X HD Production des spectro-imageurs CALISTE Solar Orbiter (100 a produire en tout) contenant ASIC HD. Une quarantaine produite aujourd'hui. Rendement moins bon que prévu.

-2- R&T

D^2R_1 (ASIC matriciel 256 pixels en CMOS XFAB 0.18) malgré un ASIC très performant, toujours des problèmes d'hybridation au détecteur => pas de spectre digne de ce nom et plus de financement. L'existence de **D^2R_2** est remise en question.

OWB-1

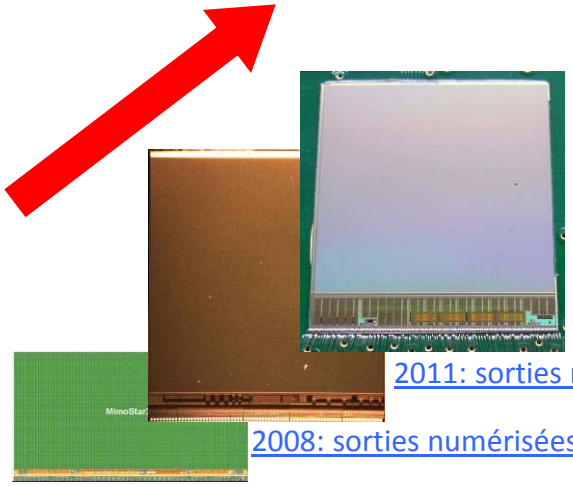
ADC (wilkinson + DLL) 32 voies pour applications spatiales:

AMS 0.35 durcie (latch-up+SEU) 13 bits, temps de codage de 2.5 µs (voir Poster F.Bouyjou) auto-calibration

Nombreuses applications potentielles mais rien d'engagé pour l'instant.

MAJ Bilan du Capteur ULTIMATE pour PXL-STAR

- *Trois générations de circuits de grandes tailles: MimoStar, Phase1, ULTIMATE-M28*



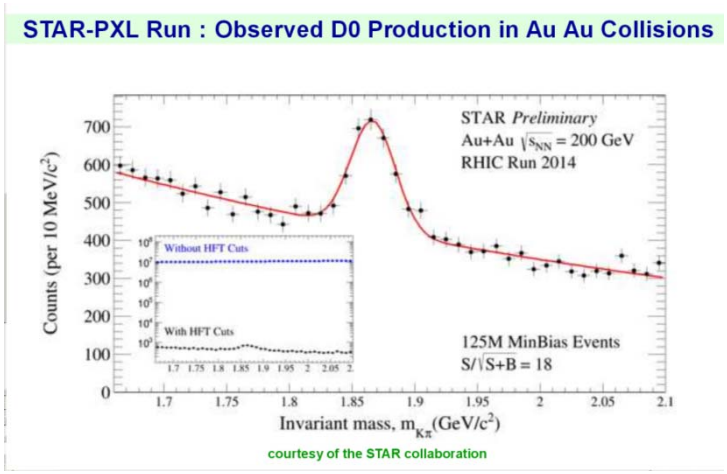
- *Cahier des charges qui a évolué grâce à l'avancement technique*
- *Production de 100 wafers pour l'Ultimate*
  - *25 restent à l'IPHC pour d'autres projets: (ex. BESIII)*
- *3 PXL détecteurs fabriqués (0.15 m² chacun) par les collègues de STAR*
  - *1er détecteur de vertex existant basé sur CPS*
  - *4 mois d'acquisition des données de physique de Mars à Juin 2014*

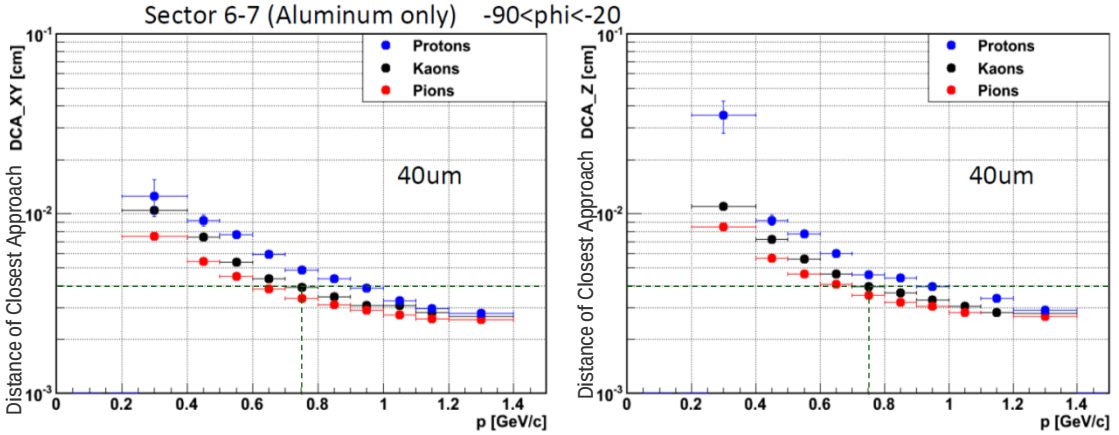
2011: sorties numérisées, avec la suppression de zéros ($t_{r.o.}$ ~ 0.2 ms)

2008: sorties numérisées -collaboration Irfu- , sans la suppression de zéros ($t_{r.o.}$ ~ 1 ms)

2006: sorties analogiques ($t_{r.o.}$ ~ 4 ms)

- *Résolution au point d'impact mesurée pour 700-800 MeV/c kaons:*





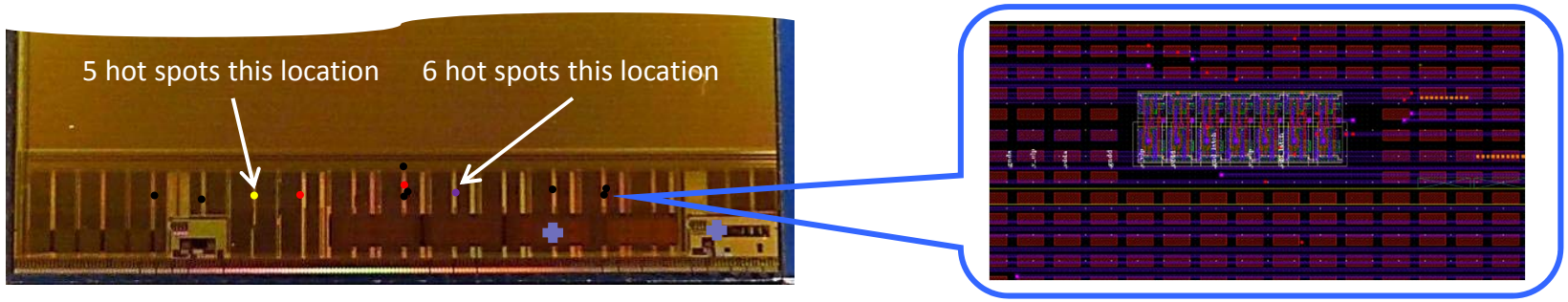
➔ $\sigma_{P.I.}$ ~ 40 µm obtenus dans le 2 directions comme prévu!

- *Aboutissement sur une expérience de 10 ans de R&D*

Bilan du Capteur ULTIMATE pour PXL-STAR

MAJ

- *Problème sur soft "latch-up"? Pourtant testé avant sans avoir constaté le problème*
  - *1er dommages observés dans le "Run" 15 GeV après un événement de perte de faisceau, qui se sont poursuivis durant la prise de données du "Run" 20 GeV*
    - *Augmentation du courant numérique*
    - *Principalement dans les échelles intérieures: 14% de la couche interne, 1% de la couche externe*
  - *"Solution": Latch-up seuils abaissés à 120 mA (initialement 400 mA et commun pour 10 capteurs) + Cycle de l'alimentation numérique et du rechargement de la configuration*
- *Refaire le test de "latch-up" sur les capteurs amincis et non amincis*
  - *Effets atténués de "latch-up" sur les capteurs non amincis!!! ➔ Etape manquée dans les tests*
  - *Hot spots: la plupart des points chauds sont alignés horizontalement ➔ clock tree: Buffer isolé*

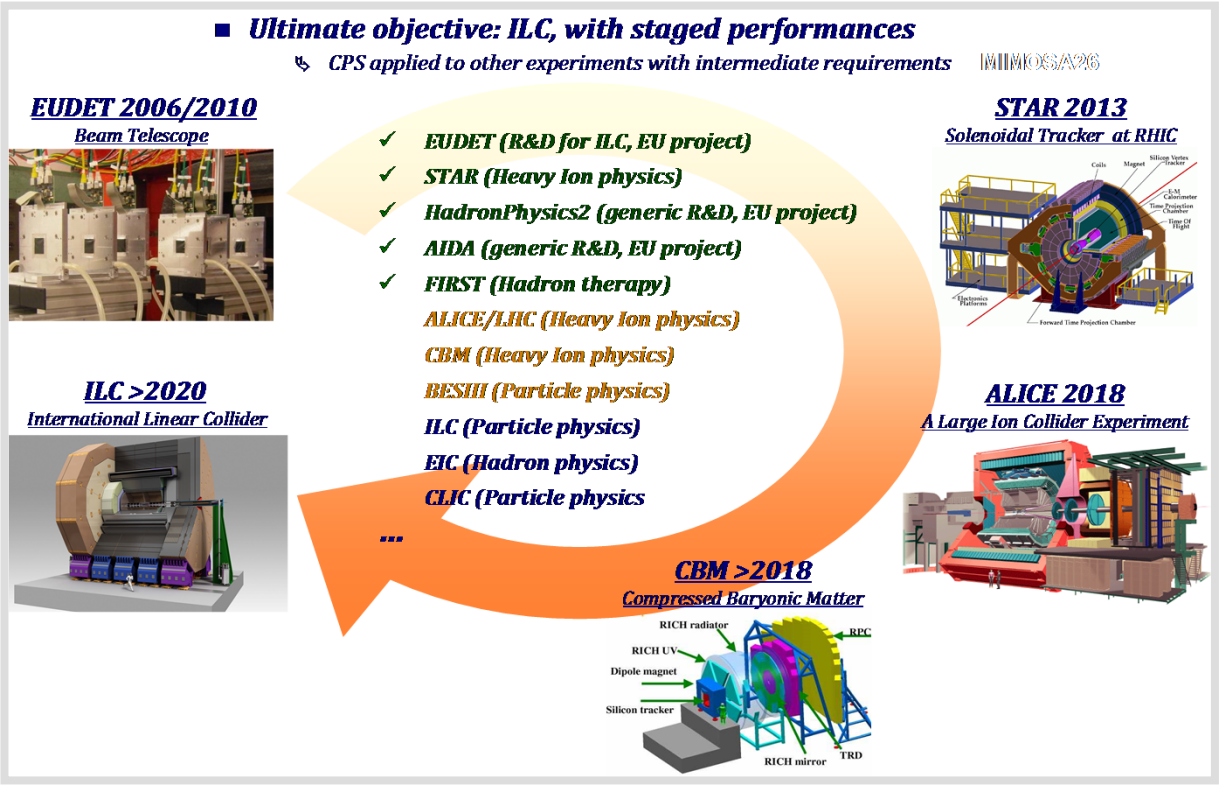


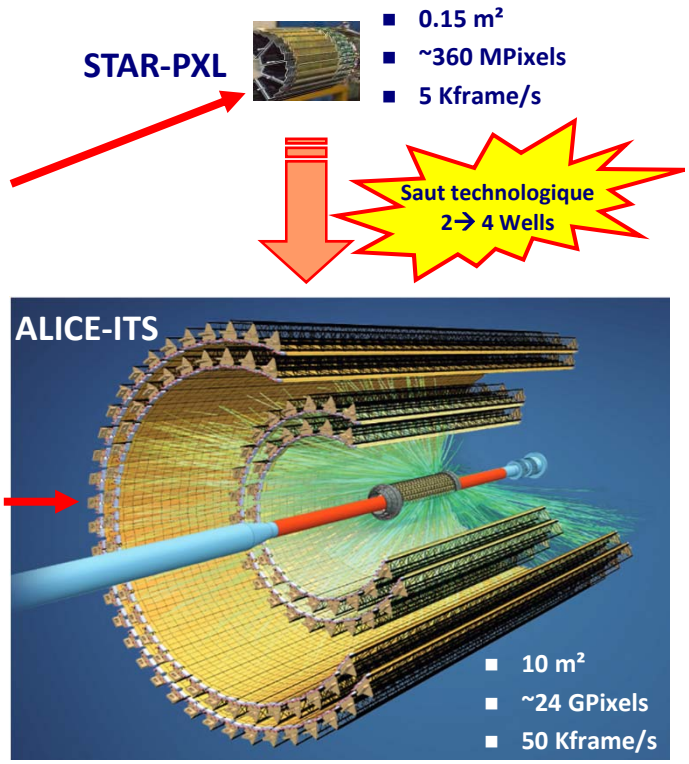
  - *Remarques et hypothèses:*
    - *"Buffer" lui-même a des contacts au substrat suffisants, mais …*
    - *Il y a des POLY remplis à main, et la densité est relativement élevée ➔ comportements de ces POLY flottants après irradiation ?*
  - *La recherche d'explications se poursuit*

Impacts

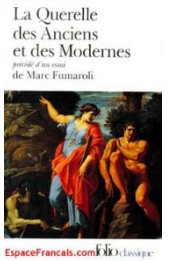
MAJ

- *Le développement d'ULTIMATE a bénéficié de la synergie entre les expériences*





- *Passage ITS-ALICE 2011 ➔ Grâce aux connaissances accumulées sur la conception et la caractérisation de PXL-STAR ➔ Les résultats des MIMOSA ont été à la base de la validation du TDR*
  - *Calendrier serré, 2 architectures développées en parallèle, 1 Classique, 1 Moderne ☺*
  - *Pour IPHC: Q1/2013 Eng Run 3,5 cm² de démonstrateurs; Q2/2013 MPW 60 mm²; Q1/2014 Eng Run FSBB 7 cm²; Q2/2014 MWP 100 mm²; Q2/2015 MISTRAL Run Eng 8 cm²*
  - *A partir Q2/2014 développements croisés*
    - *2 ingénieurs IPHC en R&D pour les pixels ALPIDE et module de contrôle et transfert de données ALPIDE incorporé dans MISTRAL*



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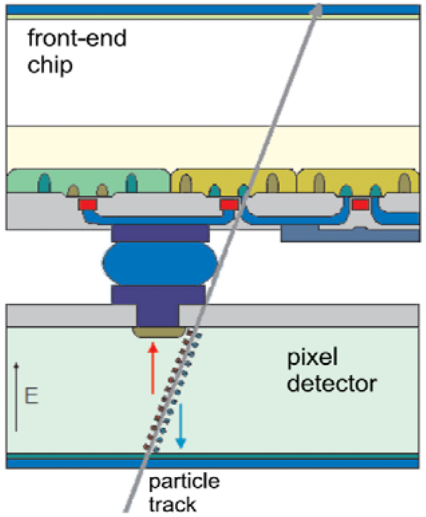
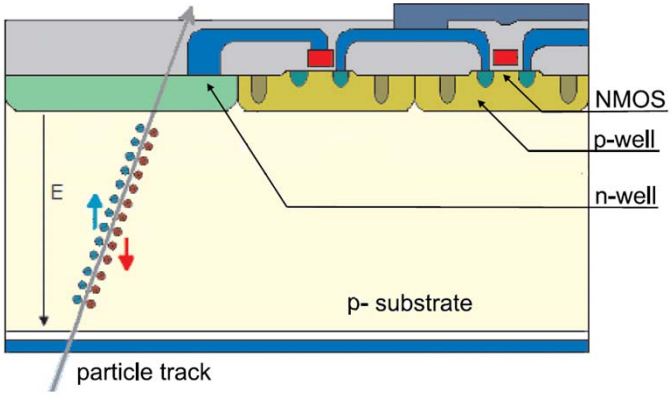
From Hybrid to Monolithic HVCMOS pixel





Hybrid Pixel Detectors Properties:

fine pitch flip-chip assembly of:
CMOS R/O chips (CSA + DSP per pixel)
Si (planar or 3D) or Diamond detectors
+ high density electronics
+ moderate - good SNR
- high material budget
- high cost (chip + sensor + hybridization)

Depleted MAPS for HL-LHC needed:

large depletion depth d ~$(\rho V)^{1/2}$
AND full CMOS
AND low power
AND low cost

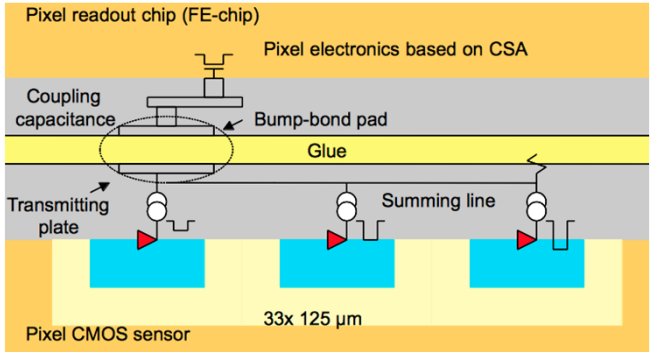
Questions:
→Radiation hardness (sensor / transistors).
→Signal to Noise Ratio / Efficiency.

courtesy of Bonn University

MAJ

Why HVCMOS pixels for HEP ?

- Commercial process in large 8 or 12 inch wafers and potentially much cheaper than customer HEP sensors.
- Potentially much cheaper bonding processes available.
  (capacitive coupling gluing, oxide/Cu-Cu bonding)
- Smaller pitch due separation between CMOS sensor/analog tier and digital tier: sub-pixels in CMOS tier.
- Thin sensor (15-100 µm) reduce clusters at large η.
  (improve cluster size, two tracks resolution, sensor radiation hardness).
- For initial prototypes, FE-I4 digital tier is available,
  for final FE-RD53 will be suitable.
- Low occupancy layers (outer pixel, even strips) can be made in one tier with classical column or periphery readout architecture reducing the cost for large areas.



MAJ

HVCMOS Demonstrator Working Group

- R&D started by Heidelberg-Berkley-Bonn-CERN-Geneva-Marseille since 2012.
- From June 2014 in the framework of ITK Pixel Module under chair of Norbert Wermes (Bonn) with many institutes : Karlsruhe-Berkley-Bonn-CERN-Geneva-Marseille-Gottingen-Prague-IRFU-Glasgow-Oxford-Liverpool-INFN-Genova-Milan-SLAC-UCSC-.....
- Address the development of Demonstrator Pixel module at end of 2015.
- Goal of preparing CMOS pixel option in the ITK Pixel TDR in 2017.
- Two main technology are explored for creating depletion region: HV (10-20 ohms.cm substrate and 30-90 V applied) or HR (0.1-3.0 Kohms. cm substrate) or both

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Specification of CMOS Pixel (CPIX) Demonstrator

- Design Task Force Nov 2014
- Pixel module of 1-2 cm^2
- Radiation tolerance more than 50 MRads TID and 10^{15} $neq.cm^{-2}$ NIEL
- Readout by the FE-I4 chip
- When possible also standalone readout
- Power less than 20 µA/pixel
- In-time efficiency more 95% after irradiation
- Bondable either by bumps or glue to FE-I4 with capacitive coupling
- Pin-out compatibility of demonstrators in different technologies for test by many groups

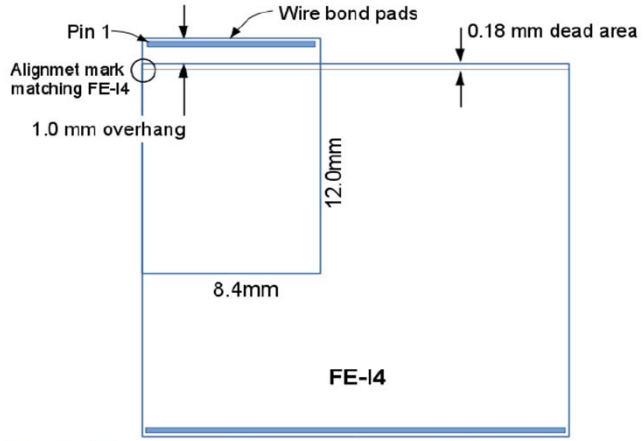

Fig. 1: Alignment of demonstrator to FE-I4 chip

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Planning for Demonstrator

- Aug-Nov 2014 Prototypes, test results, Task Force specifications and recommendations
- Feb-June 2015 design and submission in 2-3 technologies
- Sep-Oct 2015 Characterization in the Labs
- End 2015 Demonstration in test beams and irradiations

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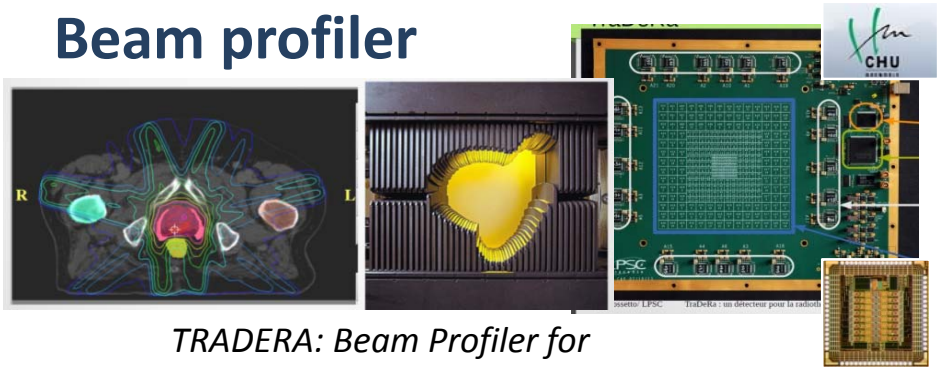
Target Demonstrator submissions

Technology	Prototype	Demo design	Reticule (Full/MLM)	Submission Goal
Fab B 350nm	KA, CPPM,GVA,CERN Also strips	KA(Peric) DESY, SLAC/UCSC,…	Engineering run Full reticule	March 2015
FabA 180nm	KA, CPPM,GVA,BN, CERN	KA(Peric) CPPM	Engineering run Full reticule	Fall 2015
FabH 130nm	CPPM	CPPM (Pangaud) IRFU, KA	Full reticule	Fall 2015 ?
Fab G 150nm	BN, CPPM,KA	BN(Kruger) SLAC/LBL CPPM	MLM4->MLM2	June 2015
FabD SOI 180nm	BN, CERN	BN(Hemperek)	MLM4	August 2015

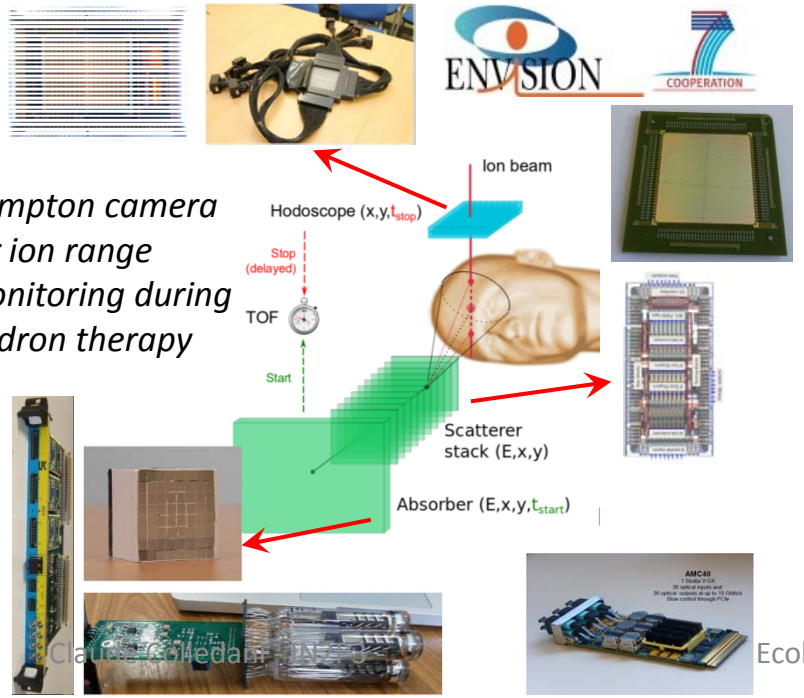
R&D for Societal Applications

Beam profiler



TRADERA: Beam Profiler for Intensity modulated radiation therapy

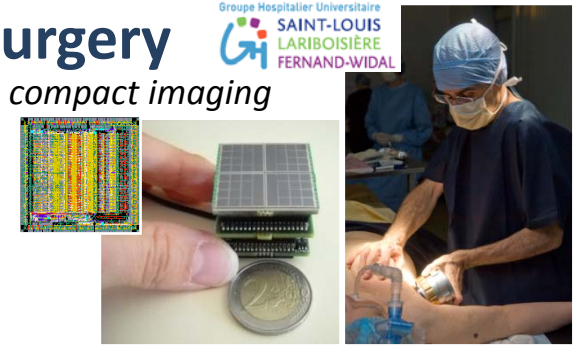
Deposited dose monitoring



Compton camera for ion range monitoring during hadron therapy

Radioguided surgery

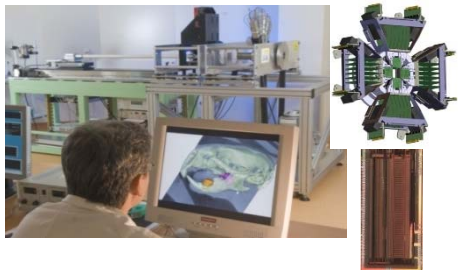
MAGICS: Peroperative compact imaging gamma camera. Sentinel lymph-node mapping protocol.



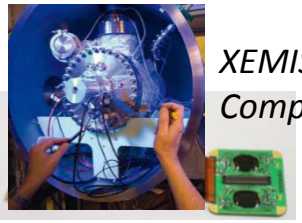
Imaging

- CT & SPECT scanners

IMABIO: Multimodal platform for small animal imaging µCT, µSPECT, µPET



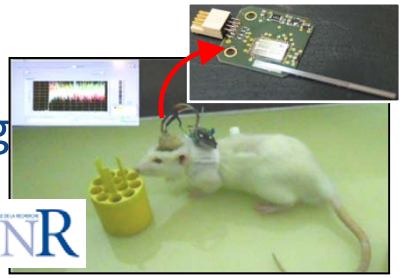
- PET scanners



XEMIS1: Liquid Xenon Compton camera

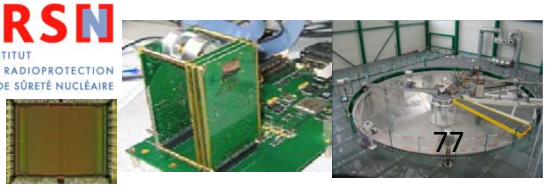
- In vivo neuroimaging

PICSIC: Brain implantable β+ radiosensitive probe



Dosimetry

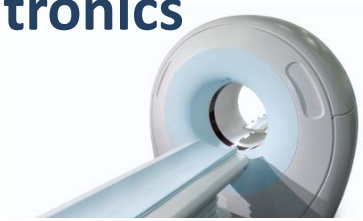
FASTPIXN: Neutron dosimetry for nuclear power plants survey



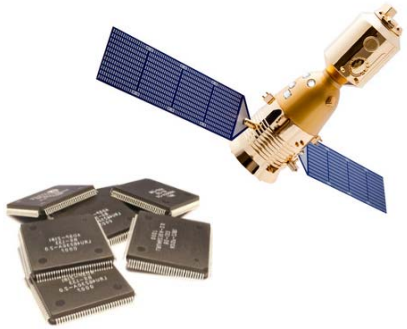
Technology transfer

Developing X ray imaging systems based on hybrid pixel detectors and dedicated to biomedical, material science

French-Swiss Public Interest Group Assisting Small-Medium size Enterprises to setup collaborative projects for innovative mechatronics



Designing high-end analog & mixed microelectronics for nuclear industry, space industry, medical imaging



Technology Transfer:

Not only positive feedback in terms of IP and royalties but also for PhD, postdoc fellowships and grants (Local, France, Europe)

MAJ Societal App
- Dans l'assemblée ceux qui sont concernés -

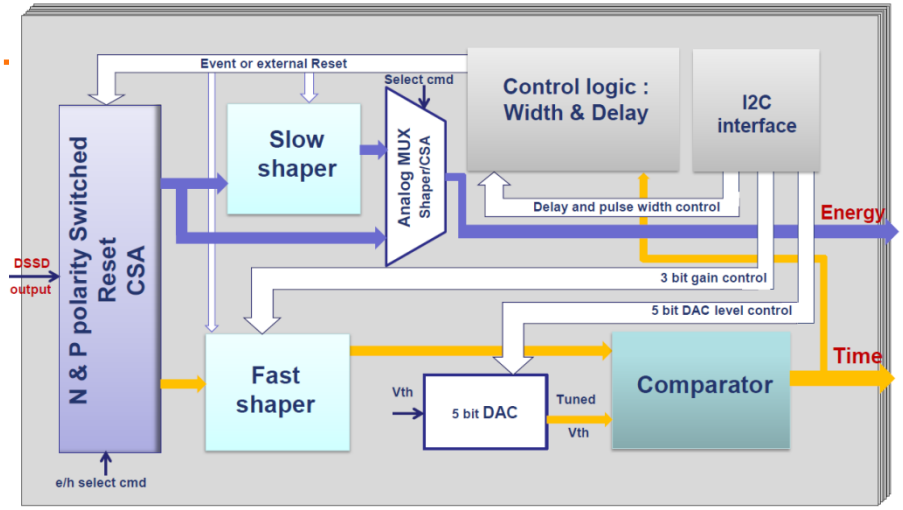
- Point sur les circuits mentionnés
  - Bilan de réalisation du cahier des charges
  - Bilan de Production, de Mise en service (Durée de vie / Fiabilité)
  - Impact du circuit dans la communauté Nat/Internationale
- Evolution du circuit / du savoir-faire accumulé
  - Question: Aujourd'hui feriez-vous les mêmes choix?
  - Contraintes pour Evolution et **Breakthrough**
    - Architecture, Blocs fonctionnels / Building blocks
    - Moyens RH / Techno (process)

- Au niveau de chaque équipe
  - Collaboration sur ces thématiques
  - Les échanges entre labos du réseau µE / Autres
- AOB + Qui d'autre veut intervenir sur la µE pour ce réseau

ASIC for silicon scatterer of Compton Camera in hadrontherapy

ASIC specifications :

- a second (final) ASIC version was realized in CMOS 0.35 µm process of AMS
- 8 input channels
- Double-sided Silicon Strip Detector (DSSD)
- February 2014 : 20 packaged chips (MQFP100)
- the ASIC was validated.



Block diagram of a complete readout chain

Production :

- 2014 : bonding of 7 large detectors (DSSD) on PCB cards at IPNL
- April 2015 : production of 180 additional chips to equip all the plans of the Silicon Scatterer
- March 2015 : realization of DAQ card which will compose plans of the silicon scatter detector
- The tests are scheduled for the 4th quarter of 2015

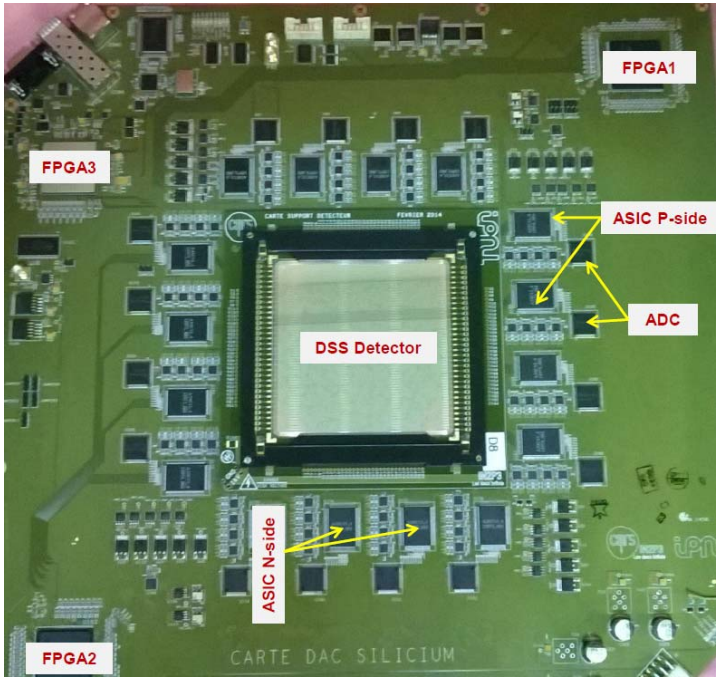


Photo of the DAQ card

Human resources and collaborations :

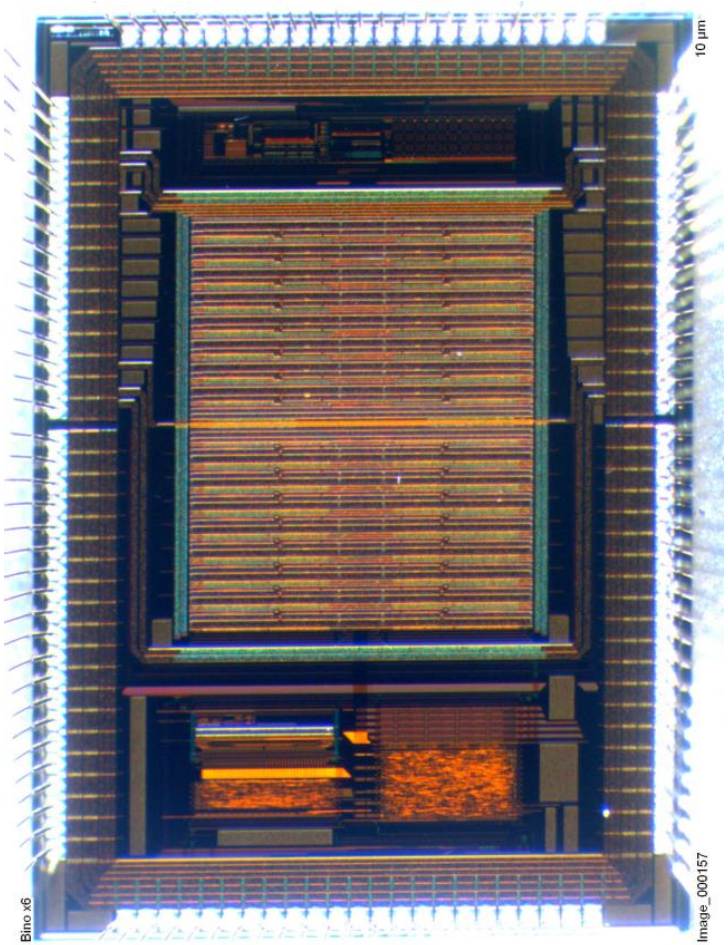
- This work is done thanks to IPNL electronics team (M.Dahoumane) and Cas-Phabio group.
- Tests and calibration will require more human resources !!!

MAJ

1- **HODOPIC: readout of a beam hodoscope with time tagging feature**
incident ions are tagged in X,Y position and time with a resolution < 1ns
max expected trigger rate: 100 MHz
Hodoscope detector composed by optical fibers + multi-anode PMs
32+32 channels/PM: fibers read from both ends
16 asics required for a Compton camera: production completed
Framework: hadrontherapy dose deposition imaging device (end 2016)

2 – **First silicon: HODOPIC is a multi-channel device integrating a time stamper unit**
design started after two evaluation prototypes integrating the front-end channel and a DLL
2010 1st evaluation chip -> 2013 HODOPIC design submission -> 2014 end functional tests
One designer (equivalent) / 4 years: (well known) AMS BiCMOS 0.35 um technology
Main HODOPIC internal blocks based on S.Deng PhD Thesis (2012)
Asynchronous architecture: clock distributed only within the time stamping unit

3 - Next steps :
HODOPIC tested with the hodoscope final detector with a physical source
More tests needed to characterise the front end board (two asics:board)



(L.Caponetto)

Technology Transfer

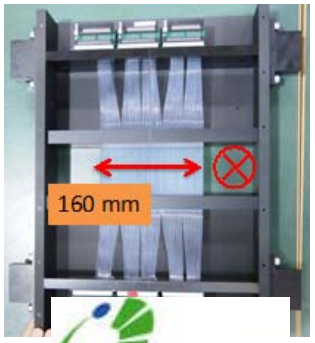
- Several chips transfered to other academic users
- Non-profit « academic price » : 100-150 €/chip, 1600 €/TB

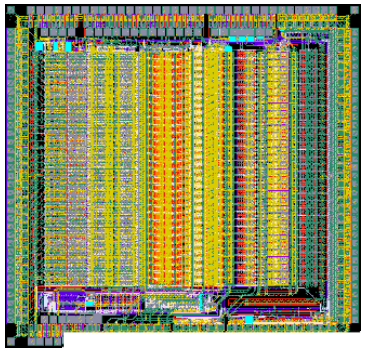
chip	year	IN2P3 users	external users
MAROC3	2010	**LAL**, APC, CSNSM	NEVIS, KEK, CERN, Roma, Seoul, Pisa, Bari, Genève, Mocow, Valencia, Kolkata, Durham, Bruxelles, München, Jülich, Valparaiso, Lisboa, Bristol, Frascatti, Budapest, Catania, Glasgow, Coimbra, Grenoble
HARDROC2B	2010	**IPNL**, LPCCF	
SPIROC2B	2010		**DESY (D)**, TOHOKU (JP), Bergen (N)
SKIROC2	2010	LAL, **LLR**	IHEP
SPACIROC1	2010	**APC**, LAL	
EASIROC	2010	**IMNC**, LAL, LLR,	Palermo, FNAL, KEK, München, Dijon, CERN, Roma, Aachen, Toulouse, Lyon, Seoul, Bari, Tokyo, Pusan, Kyushu, Osaka
PARISROC2	2010	**IPNO**, LAPP, LLR, APC	IHEP
CITIROC	2013		**INAF**, CERN, JLAB, Rio, Berne, Mendoza, Aachen
PETIROC2	2013	**IPNL**, LPCCF	KEK, Tohoku

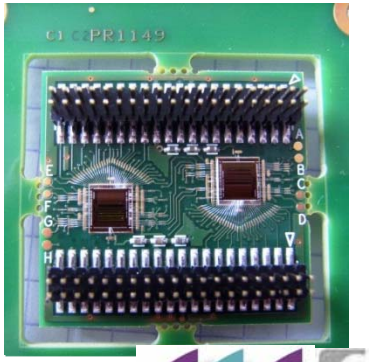
MAJ

EASIROC/CITIROC : users

OMEGA Microelectronics







J-PARC

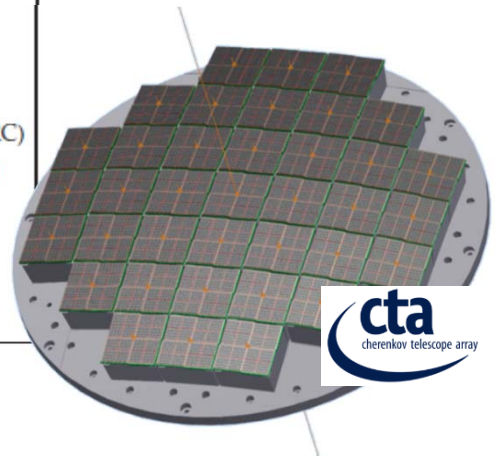
Users of EASIROC Modules

Name	Institute	Usage
A. Ishikawa	Tohoku	Fiber tracker (Silicon Test)
K. Ueno	KEK	Fiber tracker (COMET Test)
A. Sato	Osaka	Fiber tracker (COMET Test)
J. Tojo	Kyushu	Fiber tracker (COMET Test)
T. Kin	Kyushu	Fibertracker (Muon Radiography)
W. Ootani	Tokyo	MEG
M. Yokoyama	Tokyo	T2K upgrade
A. Minamino	Kyoto	T2K upgrade
H. Kawai	Chiba	Fiber tracker J-PARC E36
K. Kotera	Shinshu	PET/SPECT
K. Kojima	KEK	Muon detector (Material Science)
H. Nakayama	KEK	Radiation Monitor (Belle2)
A. Sakaguchi	Osaka	Fiber tracker (Nuclear Phys J-PARC)
H. Fujioka	Kyoto	Fiber counter (Nuclear Phys, GSI)
T. Murakami	Kyoto	Trigger counter (RIBF, heavy ion)
K. Hanagaki	Osaka	Fiber tracker (Silicon Test)
O. Jinnouchi	Tokyo Tech	Education
K. Yorita	Waseda	Education
T. Mibe	KEK	muon g-2

LAL LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

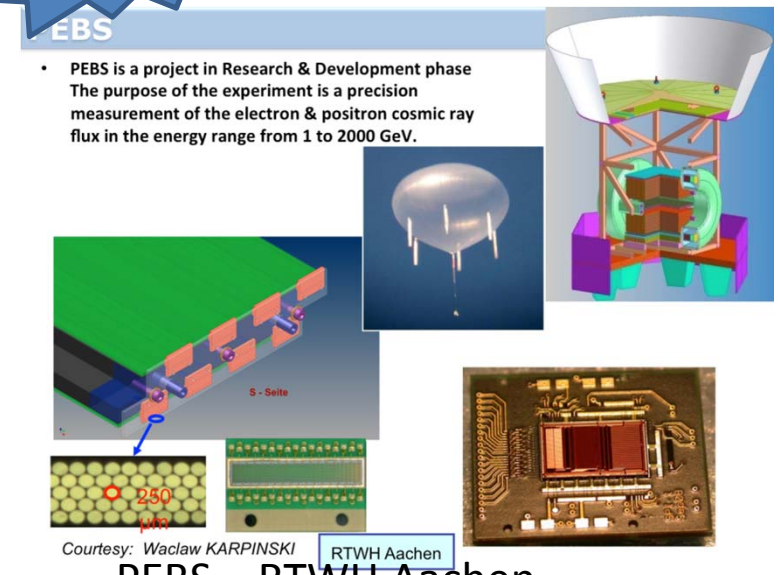
IMNC

J TECH / PUSAN UNIV / KOREA
TOKYO UNIVERSITY / JAPAN
IFC - INAF / PALERMO / ITALIA
IMNC / ORSAY / France
LLR / PALAISEAU / France
UNIVERSITY ROMA / Italy
INFN BARI / ITALY
IMNC / ORSAY / France
EHWA / KOREA
INL / LYON / France
TOULOUSE / France
CERN / SWITZERLAND
RWTH / AACHEN / GERMANY
INFN ROMA / ITALY
CERN / SWITZERLAND
UNIV. DIJON
KETEK / GERMANY
FERMILAB / USA
OMEGA / LLR
WEEROC -> IFC/INAF/PALERMO

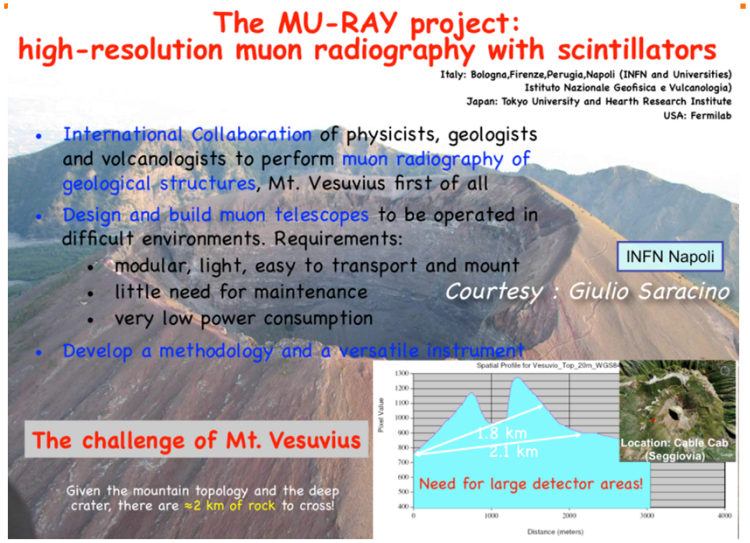


cta cherenkov telescope array

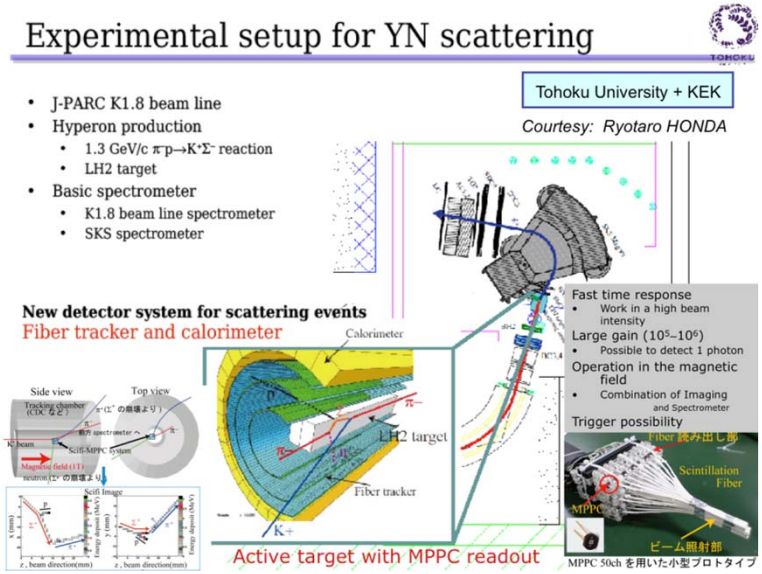
Experiments using EASIROC



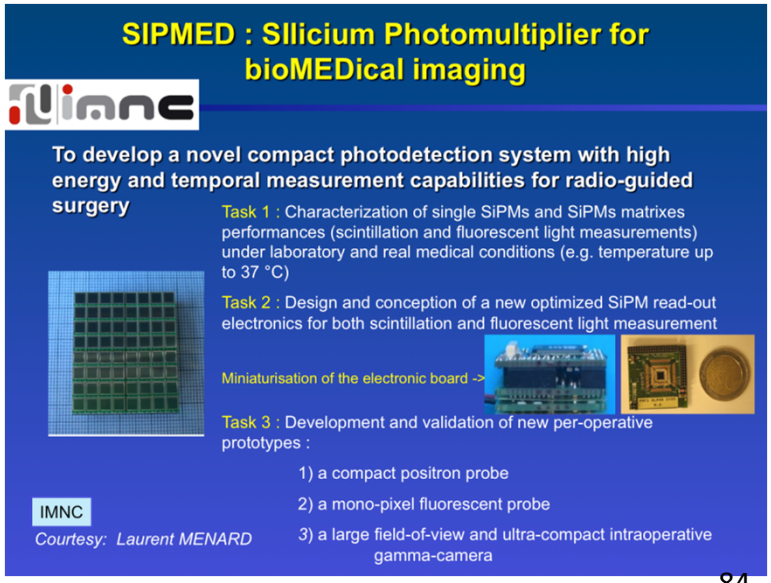
PEBS – RTWH Aachen



MU-RAY – INFN Napoli



J-PARC – Tohoku University & KEK



SIPMED – IMNC Orsay

MAJ

Valorisation industrielle

- WEEROC créé en 2012 pour valorisation industrielle
  - Fondateur J. Fleury, détachement 25-1 loi 82-610 du 15/7/1982
  - Licences Cadence industrielles
  - Contrat de transfert de compétences :

    CNRS-LAL/UPSud/WEEROC → CNRS-OMEGA/X/WEEROC
  - Ingénieurs OMEGA en 25-2 à 5%

- Contrats industriels d'ASICs pour 3 secteurs :
  - Spatial
  - Détecteurs de radiations
  - Imagerie médicale (FP7)

- Développements communs et co-propriété sur certains chips (CITIROC, PETIROC, TRIROC…)
  - Contrat de collaboration de recherche en cours…

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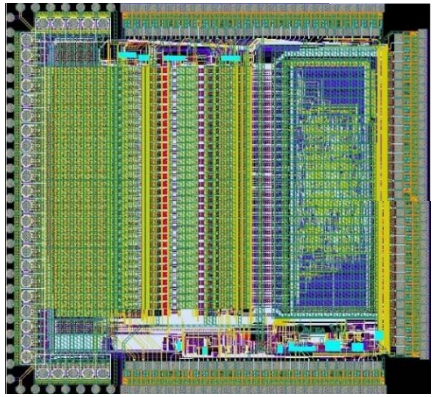
Valorisation : chips for PET SiPM

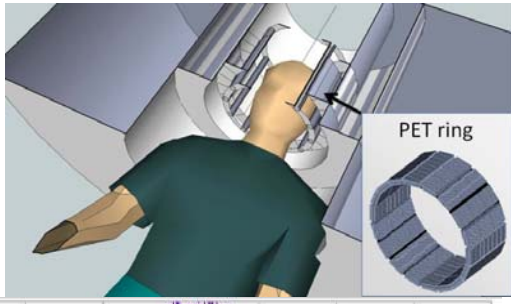
OMEGA Microelectronics

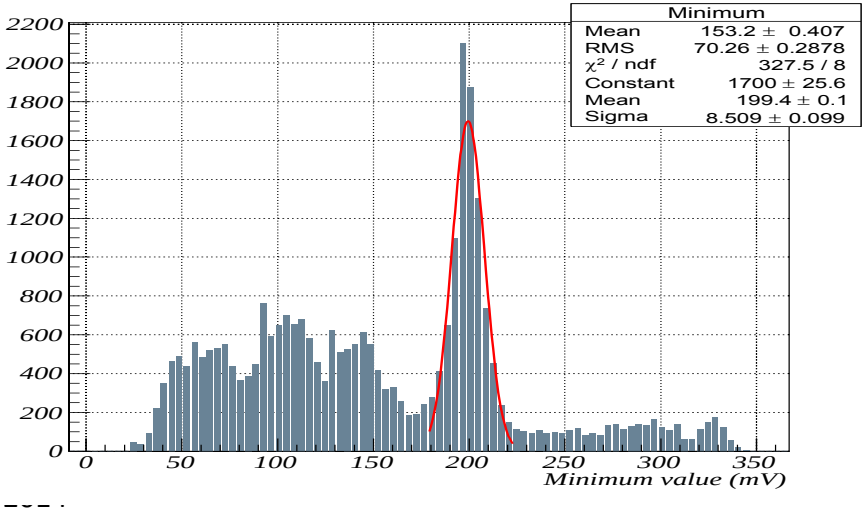
weeroc

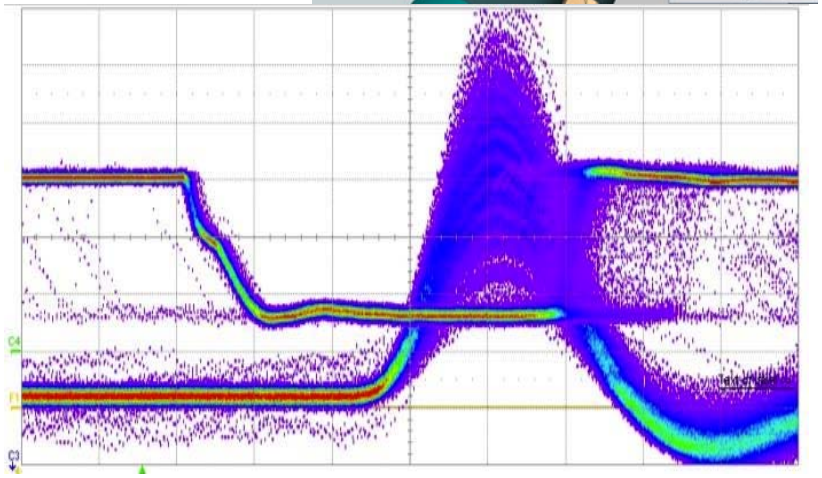
- PETIROC (nov 13)
  - 32 channels,
  - 1 GHz SiGe amplifiers/discriminators
  - Internal ADC/TDC 50ps
  - For PET and alos CMS muons/TOMUVOL (IPNL,LPCF)



- TRIROC EU Project (feb14)/WEEROC
  - 64 channels
  - Dual polarity







Summary

Numerous projects of physics, on large scope

➔ Instrumentation Network

ASIC developments

- Intense and diversified activity
- Permanent staff ➔ projects continuity
- Structured Design Team
- Evolutionary SoC / Sensors platforms
  ➔ It helps for technology diffusion

Personal comments

- *To improve the current organisation*
- *"Small teams - broad spectrum" is over, Large teams with specific expertise:*
  ➔ *Calorimetry, Cryogenics, Trackers, …*
  ➔ *ADC, TDC, Transmission, …*
  ***Ideal team**: BB + ASIC System Designers, Test Engineers, CAD tool Engineers*
- *ASIC complexity ↗ for every domains Φ*
  ➔ *State of Art R&D + Intensive D & R*
  ➔ *Limited set of nodes*

Microelectronics for CERN & LHC

- Important contribution of IN2P3 at early time of LHC
  - *It has structured the Microelectronics network*
- Upgrade phases, a high priority with substantial means and human resources
  - *Focus on specific technologies, such as Hybrid pixel / Cmos pixel Sensors*

Thank you for your attention

Thanks to the networks national contacts & colleagues for their input and help