The 65 nm CMOS technology for analog processing in mixed-signal pixel readout circuits

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CMOS scaling and front-end chips for silicon pixel sensors

- Industrial microelectronic technologies are continuously advancing and bringing CMOS towards the 10 nm frontier

- 65 nm CMOS has attracted a wide interest in view of the design of very compact front-end systems with advanced integrated functionalities, such as required by semiconductor pixel sensors with low pitch for applications in high energy physics (silicon vertex trackers) and photon science experiments (high resolution imagers)

- Digital figures of merit (speed, density, power dissipation) are driving the evolution of CMOS technologies. What about analog performance?

- For **analog applications** in which **speed and density** are important, scaling can be in principle beneficial, but what about critical performance parameters such as **noise, gain, radiation hardness**…?

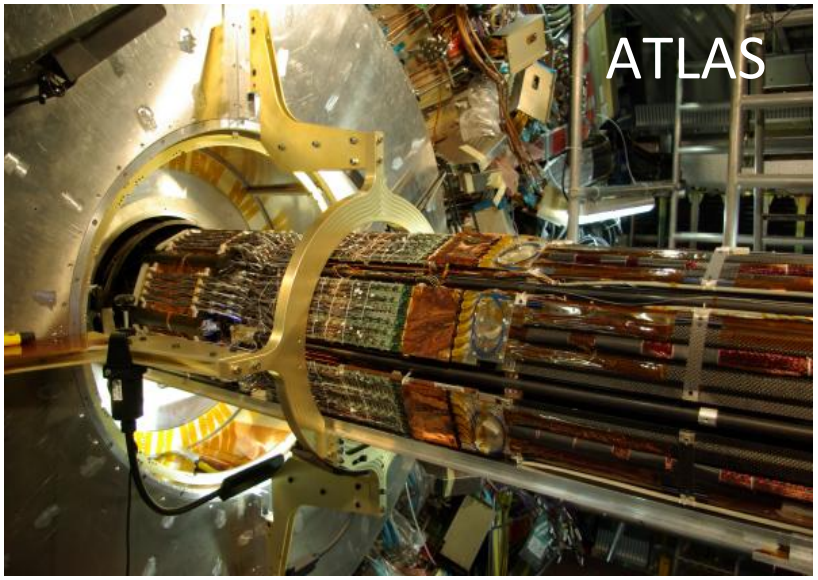
65 nm CMOS in the pixel detector microelectronics community

- Several pixel readout chips are currently designed by our community in the 65 nm CMOS node

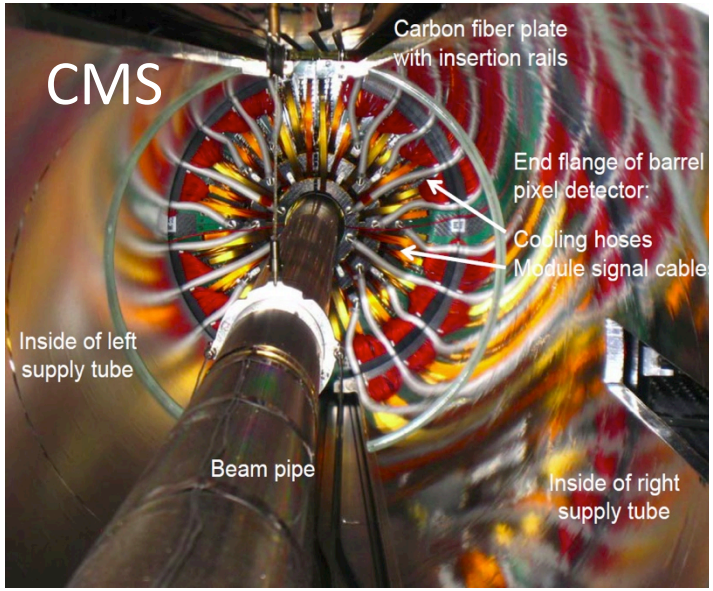
- In this talk, I will focus on two examples, representing two rather different application fields, which set diverse performance requirements: the **RD53 chip for pixels at HL-LHC**, and **the INFN PIXFEL chip for imaging at X-ray Free Electron Lasers**

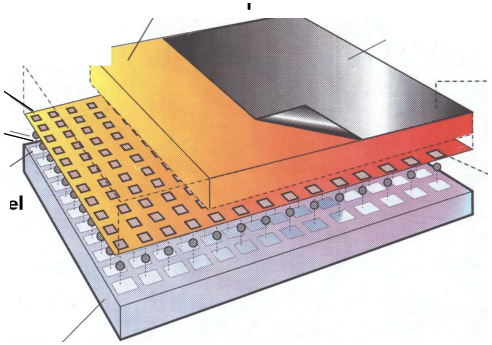
- I will not cover other very interesting developments based on 65 nm CMOS, such as the MPA chip for the Pixel-Strip modules of the phase-II upgrade of the CMS Outer Tracker and the CLICPIX chip for the vertex detector at CLIC.

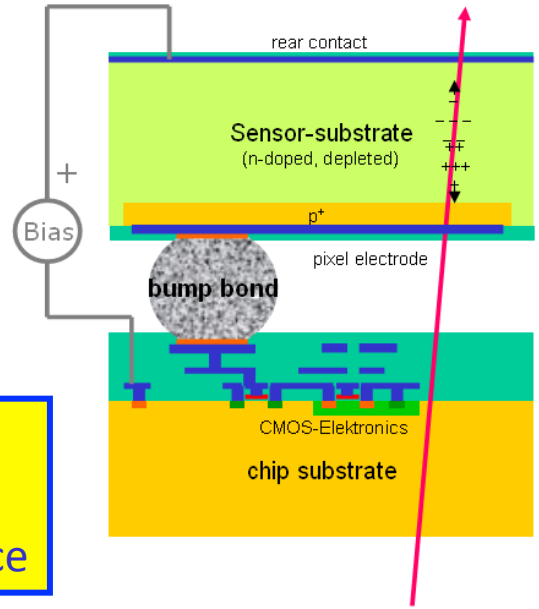
Pixel detectors at the LHC



all based on
"Hybrid Pixels"



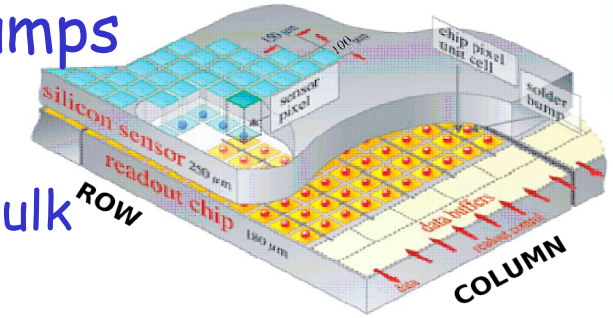




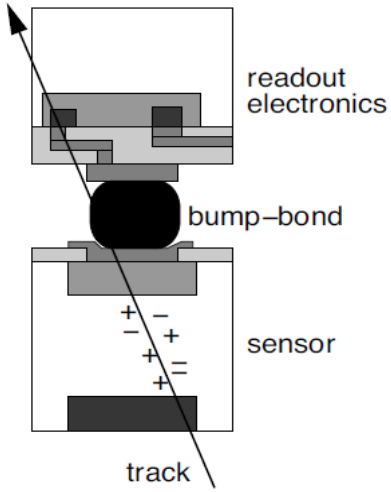
- amplification by a dedicated R/O chip
- 1-1 cell correspondence

Hybrid pixel sensors

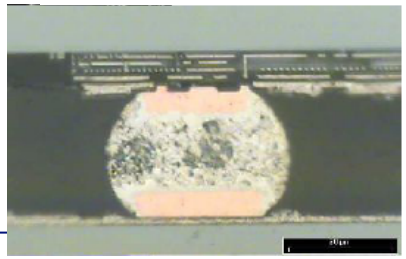
- A pixellated sensor chip is connected to a matching readout chip by an array of solder bumps



- **Sensors**
  - Particle sensitive volume is a high resistivity silicon bulk (1-10 kΩcm, 250 μm typical thickness, thinner for higher radiation hardness and less material), can be fully depleted for fast charge collection by drift
  - Typical pixel dimensions at LHC: 50 μm × 400 μm (will decrease for HL-LHC, probably to 50 μm × 50 μm)
  - Radiation-hard to 50 Mrad at LHC (1 Grad for HL-LHC)

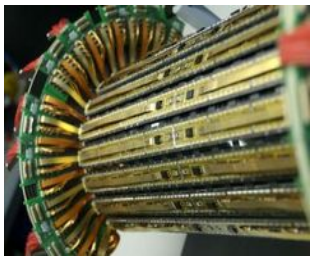


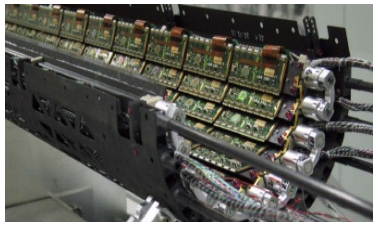
- **Front-end chips (Nanoscale CMOS)**
  - For any event (particle hit in the sensor) provide pixel position, timing, pulse amplitude
  - Only a small number of pixels are hit in any event
  - Analog pre-amplification, discrimination, time stamping, digitization, zero suppression (sparsification)…

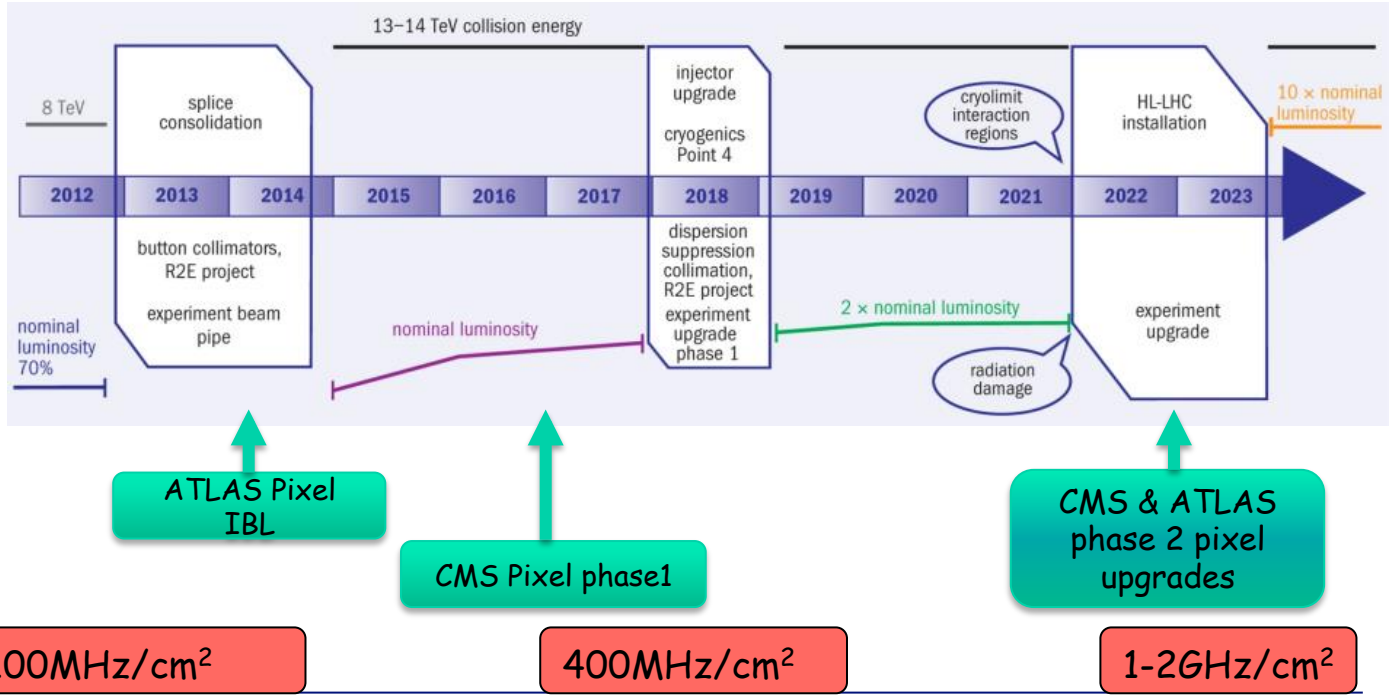


LHC pixel upgrades

- Current LHC pixel detectors have clearly demonstrated the feasibility and power of pixel detectors for tracking in high rate environments
- Phase1 upgrades: Additional pixel layer, ~4 x hit rates
  - ATLAS: Addition of Inner B Layer (IBL) with new 130nm pixel ASIC (FEI4)
  - CMS: New pixel detector with modified 250nm pixel ASIC (PSI46DIG)
- **Phase2 upgrades**: ~16 x hit rates, ~4 x better resolution, 10 x trigger rates, 16 x radiation tolerance, Increased forward coverage, less material, , ,
  - Installation: ~ 2022
  - Relies fully on significantly improved performance from next generation pixel chips.

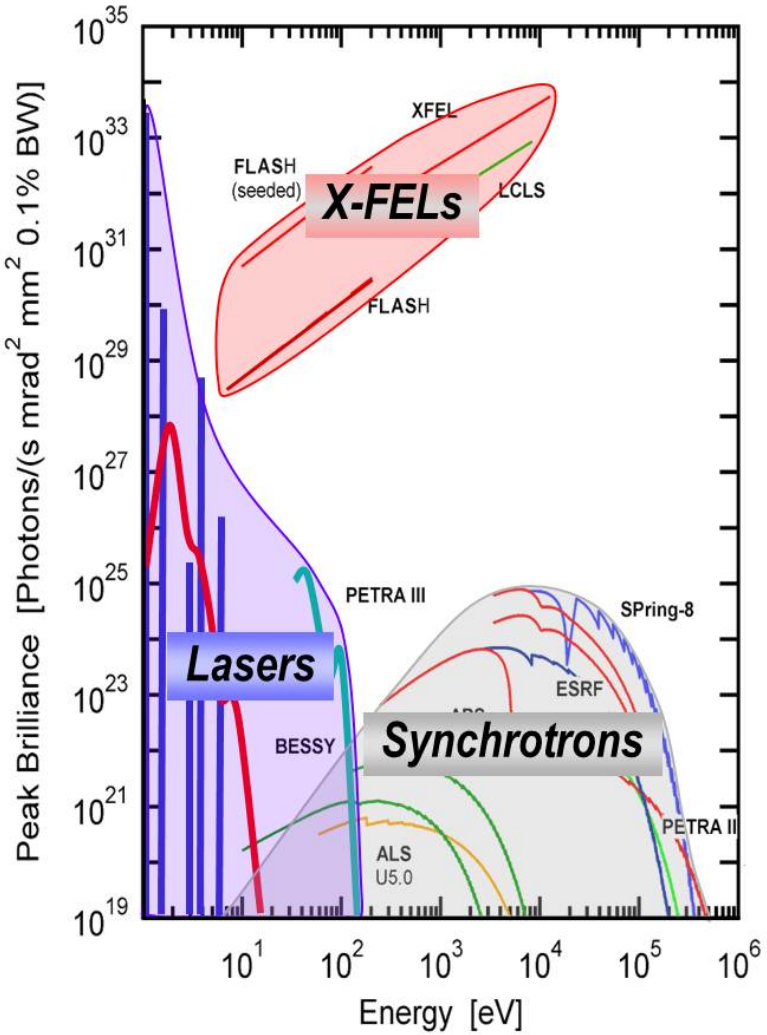






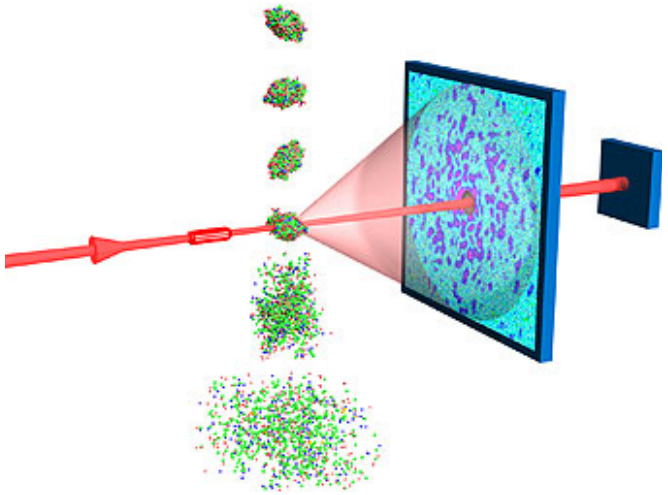
XFELs as probing tools

- X-rays have been a fundamental probing tool since their discovery
- With the advent of FELs, matter can be probed with X-ray beams with unique features: very high intensity (orders of magnitude larger than in synchrotron sources), coherent, ultrafast (down to 10 fs) pulses, broad energy range (100 eV – 10 keV)
- A number of facilities already operational (LCLS, FLASH, SACLA, FERMI), other being built (Eu-XFEL, SwissFEL) or upgraded (LCLS→LCLSII)
- Broad science base accessible at FELs: structural biology, chemistry, material science, atomic and molecular science (AMO)



2D X-ray imaging challenges

- Many measurements based on scattering of coherent X-ray pulses and detection of diffraction patterns with a large pixel camera
- New detectors are needed to comply with extremely challenging requirements
  - pulse structure: high rate single shot imaging (5 MHz), frame storage of a complete bunch train (2700 pulses)
  - dynamic range: single photon counting, integration of up to 10^4 ph/pixel/pulse
  - energy range: 0.25 keV to 25 keV
  - radiation hardness: 10 MGy to 1 GGy over three years of operation



  - angular resolution: 7 mrad to 4 urad ➔ pixel size from 700 um to 16 um (also depending on the distance from the sample)
  - angular coverage: diffraction experiments require a 0.1 nm resolution ➔ scattering angles of 120°

Advanced pixel detectors and readout microelectronics

Particle tracking at LHC- Phase II:

- Very high hit rates (1-2 GHz/cm^2), need of an intelligent pixel-level data processing
- Very high radiation levels (1 Grad Total Ionizing Dose, 10^{16} neutrons/cm^2)
- Small pixel cells to increase resolution and reduce occupancy (~50x50μm^2 or 25x100 μm^2)

➔ Large chips: > 2cm x 2cm, ½ - 1 Billion transistors

X-ray imaging at free electron laser facilities (next generation:

- Reduction of pixel size (100x100 μm^2 or even less), presently limited by the need of complex electronic functions in the pixel cell:
  - Large memory capacity to store images (at XFEL, ideally, 2700 frames at 4.5 MHz every 100 ms)
  - Advanced pixel-level processing (1 – 10000 photons dynamic range, 10-bit ADC, 5 MHz operation)

Microelectronics-oriented collaborative efforts in the high energy physics community

- AIDA WorkPackage3 (2011-2014) had the goal of facilitating the access of our community to advanced semiconductor technologies, from nanoscale CMOS to innovative interconnection processes.
- This included 65 nm CMOS for new mixed-signal integrated circuits with high density and high performance readout functions
- Design work was started at various institutions to develop blocks for analog and digital needs in HEP with full documentation and laboratory tests.
- The international collaboration **RD53** (2014-2016) was approved by CERN with the goal of developing a 65 nm demonstrator chip according to the specifications of the ATLAS/CMS phase-II upgrade of the innermost pixel layers in the Tracker
- This work will be also supported by **AIDA-2020 WP4** (2015 - 2019)

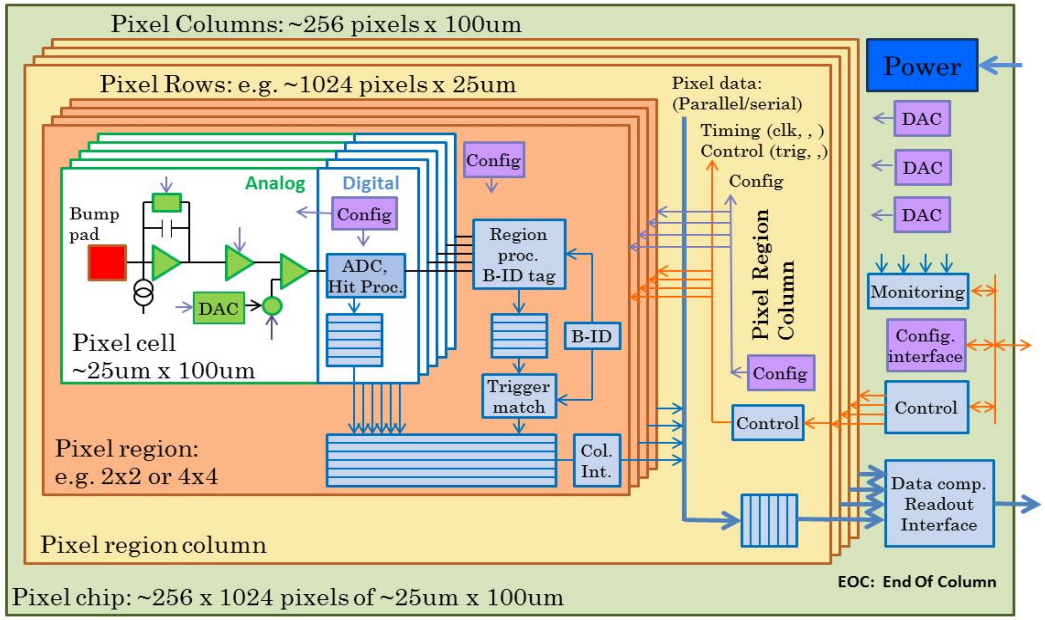
RD53: an ATLAS-CMS-LCD collaboration

- RD53 was organized to tackle the extreme and diverse challenges associated with the design of pixel readout chips for the innermost layers of particle trackers at future high energy physics experiments (LHC – phase II upgrade of ATLAS and CMS, CLIC)

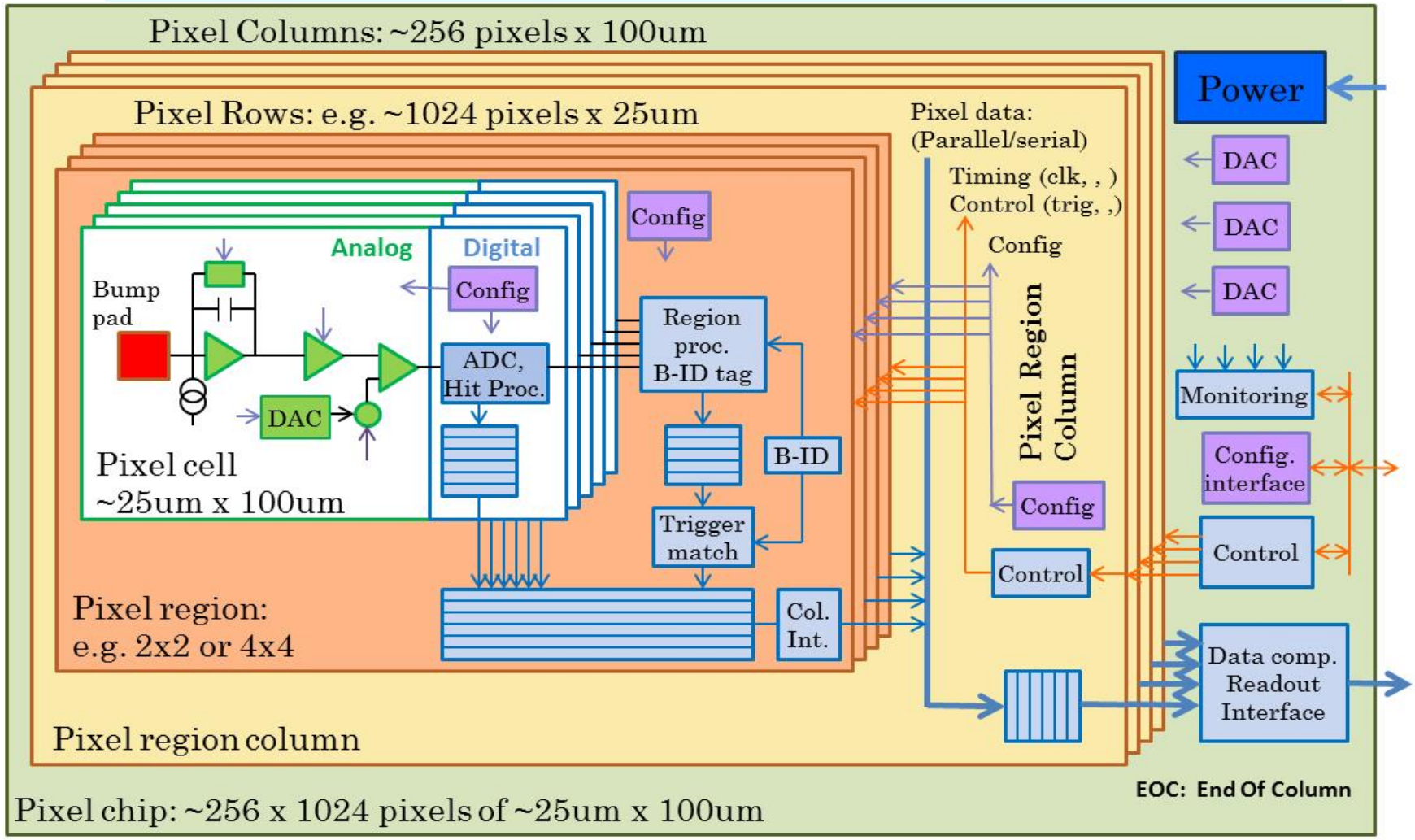
65 nm CMOS is the candidate technology to address the requirements of these applications.
It has to be fully studied and qualified in view of the design of these chips.

- ATLAS: CERN, Bonn, CPPM, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, Prague, RAL, UC Santa Cruz.
- CMS: Bari, Bergamo-Pavia, CERN, Fermilab, Padova, Perugia, Pisa, PSI, RAL, Sevilla, Torino.
- Collaborators: ~100, ~50% chip designers

A 50 μm x 50 μm mixed-signal pixel cell readout for the phase II upgrade of LHC in 65 nm CMOS



RD53 chip architecture



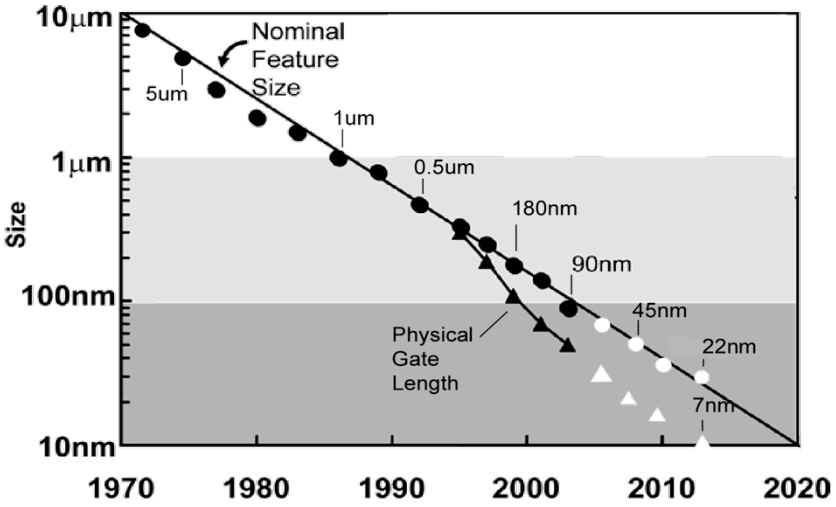
- 95% digital (as for FEI4)
- Charge digitization (TOT or ADC)
- ~256k pixel channels per chip

- Pixel regions with buffering
- Data compression in End Of Column
- Chip size: >20 x 20 mm^2

Low Power 65 nm CMOS

- Mature technology:
  - Available since ~2007
- High density and low power
  - High density vital for smaller pixels and increased data buffering during bunch trains
  - Low power tech critical to maintain acceptable power for higher pixel density and much higher data rates
- Long term availability
  - Strong technology node used extensively for industrial/automotive
- Significantly increased density, speed, and complexity compared to previous generations!

- **Access: CERN frame-contract with TSMC and IMEC**
  Design tool set, Shared MPW runs, Libraries, Design exchange within HEP community



The **Low Power (LP)** flavor (V_{DD} = 1.2 V) is less aggressive than other variants of the process (thicker gate oxide, smaller gate current, higher voltage), and more attractive for mixed-signal chips where analog performance is an essential feature.

Specifications for threshold setting, noise, power, speed in the ATLAS/CMS RD53 pixel analog front-end

Need of **detecting charge released by MIPs in heavily damaged sensors (4000 e-) at extreme irradiation levels without efficiency degradation**

- Threshold setting for higher tolerable noise occupancy: $Q_{th,min}$ = 1000 e-
- ENC < 150 e rms at C_D = 100 fF (mostly determined by series noise, ENC is proportional to C_D)
- Threshold dispersion after local tuning: σ_{Qth} < 40 e rms

  (includes contributions by discriminator threshold mismatch and pixel-to-pixel preamplifier gain variations)

These specifications are based on the so called 4σ rule (empirical):

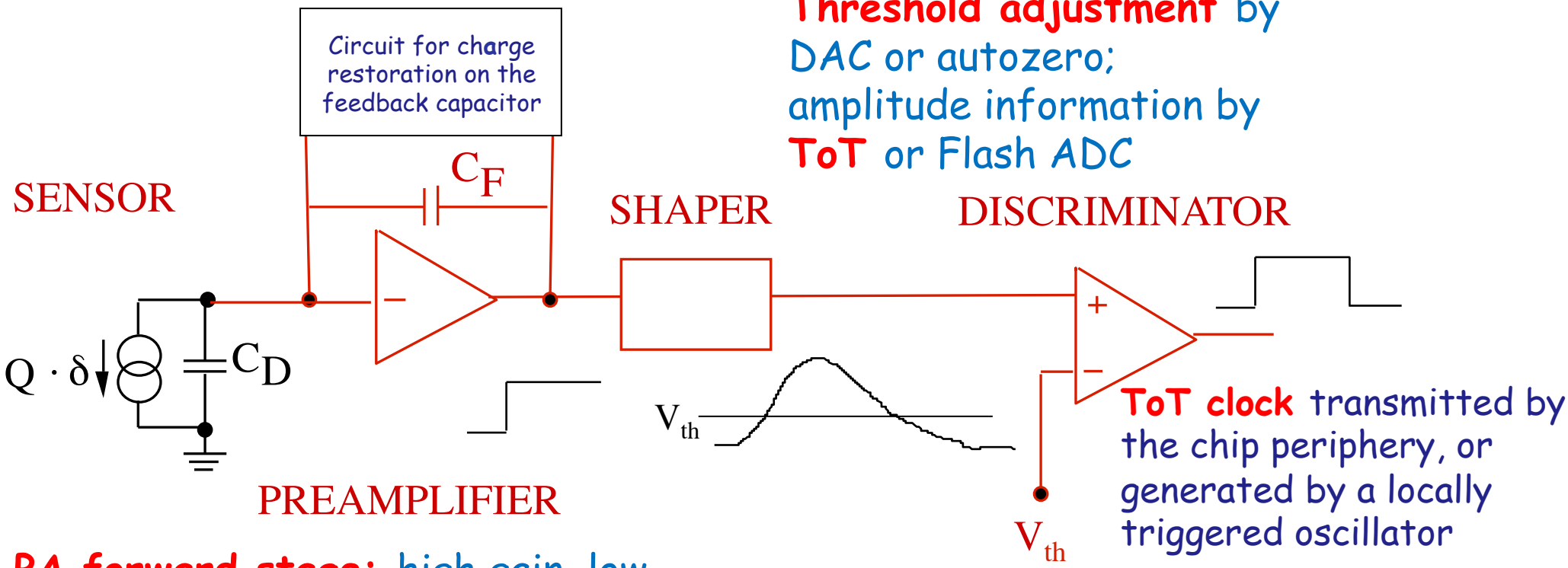
$Q_{th,\,min} > 4 \cdot ENC + 4 \cdot \sigma_{Qth}$. They have to be achieved by analog circuits integrated in **a small silicon area** and operating at **very low power**:

- Maximum power dissipation: 6 μW/pixel

(50 μm x 50 μm, or 25 μm x 100 μm)

- Maximum Hit time resolution = 25 ns, A/D conversion time < 400 ns

General schematics of a pixel analog front-end in 65 nm CMOS



Threshold adjustment by DAC or autozero; amplitude information by **ToT** or Flash ADC

ToT clock transmitted by the chip periphery, or generated by a locally triggered oscillator

PA forward stage: high gain, low noise

Charge restoration: handle sensor leakage current after extreme irradiation levels (max. 20 nA at 2×10^{16} n/cm^2)

Trend is to **skip the shaping stage** in the RD 53 HL-LHC pixel cell, mostly because of power constraints (noise filtering in the preamplifier, or correlated double sampling at the discriminator input)

Critical parameters for analog front-end design in 65 nm CMOS

- There are some critical performance parameters for analog design in nanoscale CMOS **(with focus on LP 65 nm)** for detector readout integrated circuits. Among them:

Intrinsic gain Thermal noise	Charge carriers in the device channel (short channel effects, strained silicon)
Gate leakage current 1/f noise	Interaction of charge carriers with the gate oxide; tools for evaluating the quality of the gate dielectric
Radiation hardness	Radiation-induced positive charge in the gate oxide and in lateral isolation oxides
Device matching	Random components of local process parameters dependent on device size

Designing amplifiers in 65 nm CMOS: the intrinsic gain

- It represents **the maximum gain that can be achieved with a single transistor amplifying stage**. It gives an indication concerning the design complexity that is necessary to implement a high gain amplifier.

$$g_m r_{DS} \propto \alpha L$$

- L is the transistor gate length, α is the CMOS process scaling factor. If L_{min} scales by $1/\alpha$ in agreement with scaling rules, $g_m r_{DS}$ stays constant.

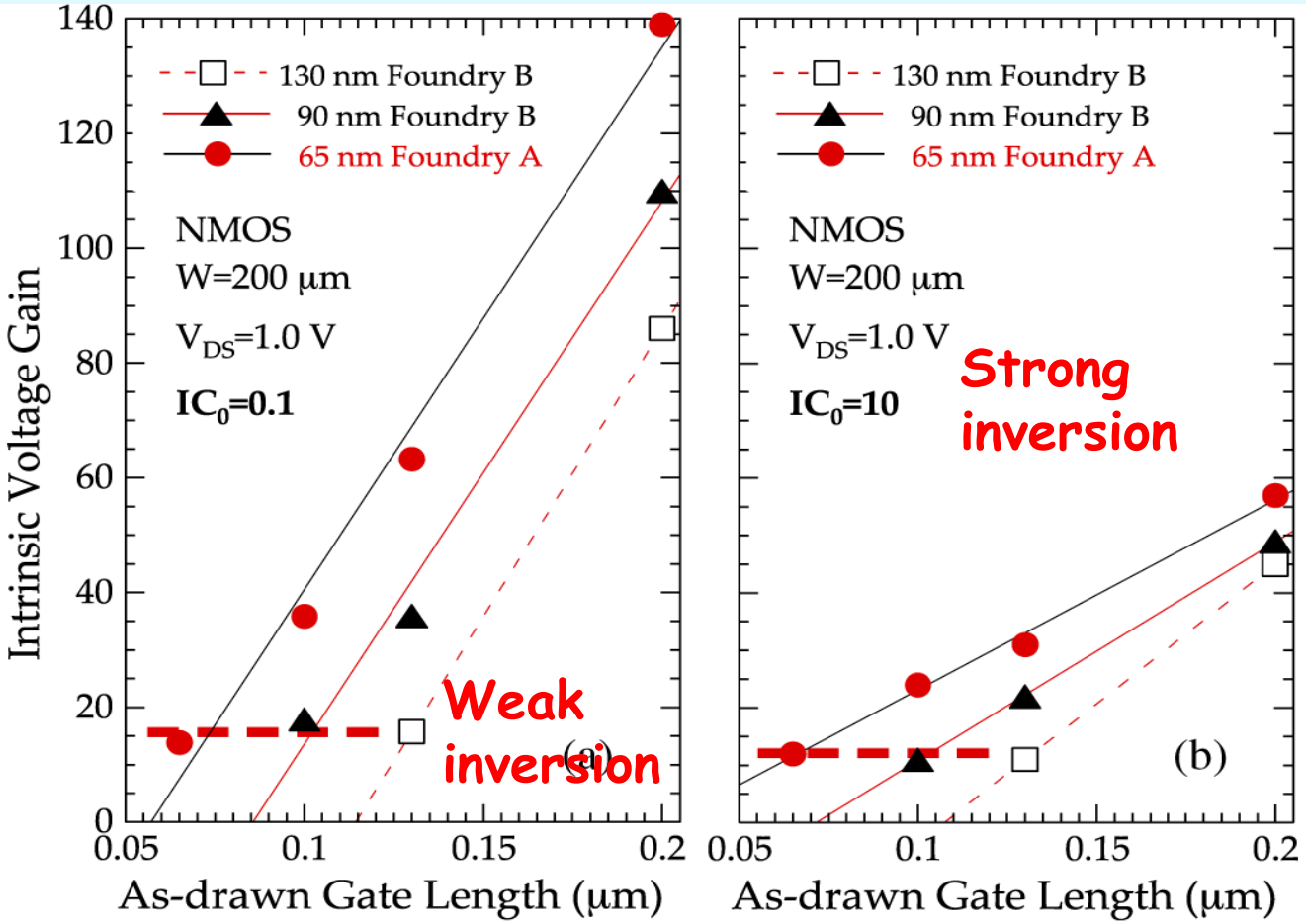
- Keeping the intrinsic gain constant with scaling below the 100 nm threshold (when you depart from classical scaling rules in advanced technologies) is considered as a major challenge which affects the design of analog circuits in nanoscale CMOS

- But Low Power CMOS processes do not follow aggressive scaling trends closely…

➔ **The value of the intrinsic gain is maintained across CMOS technology nodes from 130 nm to Low Power 65 nm if inversion conditions are the same.**

Intrinsic gain in the LP 65 nm CMOS

When the gate length L is reduced, the transistor stays in the same inversion conditions if the drain current I_D is correspondingly increased (at constant W).



M. Manghisoni, et al. "Assessment of a Low-Power 65 nm CMOS process for analog front-end design", IEEE Trans. Nucl. Sci., vol. 61, no. 1, February 2014, pp. 553-560.

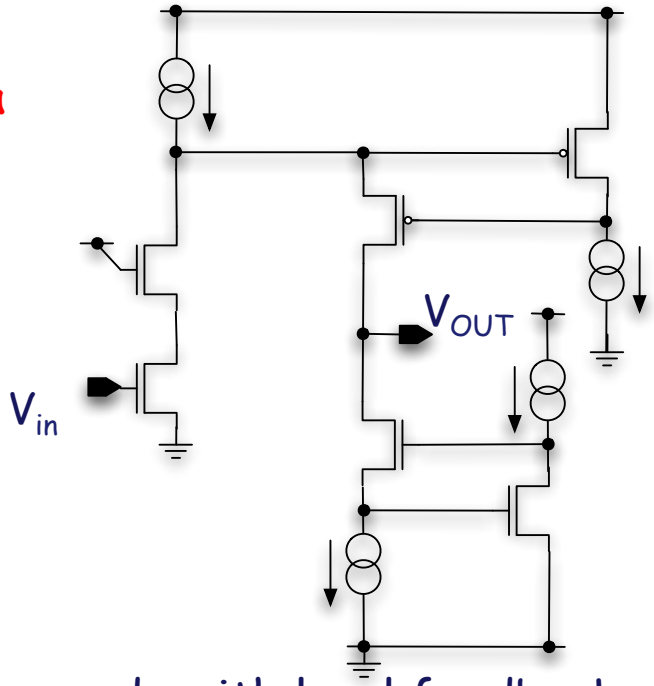
For the minimum gate length of the process, the same value of the intrinsic gain is achieved at the expense of an increased I_D. If this is not allowed because of power dissipation constraints, a value of L larger than the minimum one has to be used.

This is an example of the fact that **in analog circuits it is often impossible to take full benefit from CMOS scaling in terms of a reduced silicon area.** This is true also for other analog parameters (1/f noise, threshold dispersion,…)

Gain stages in RD53 pixel front-end circuits

- The good intrinsic gain properties of the LP 65 nm process make it possible to design amplifier stages with relatively simple schematics and an adequate forward gain in a low-power pixel front-end.

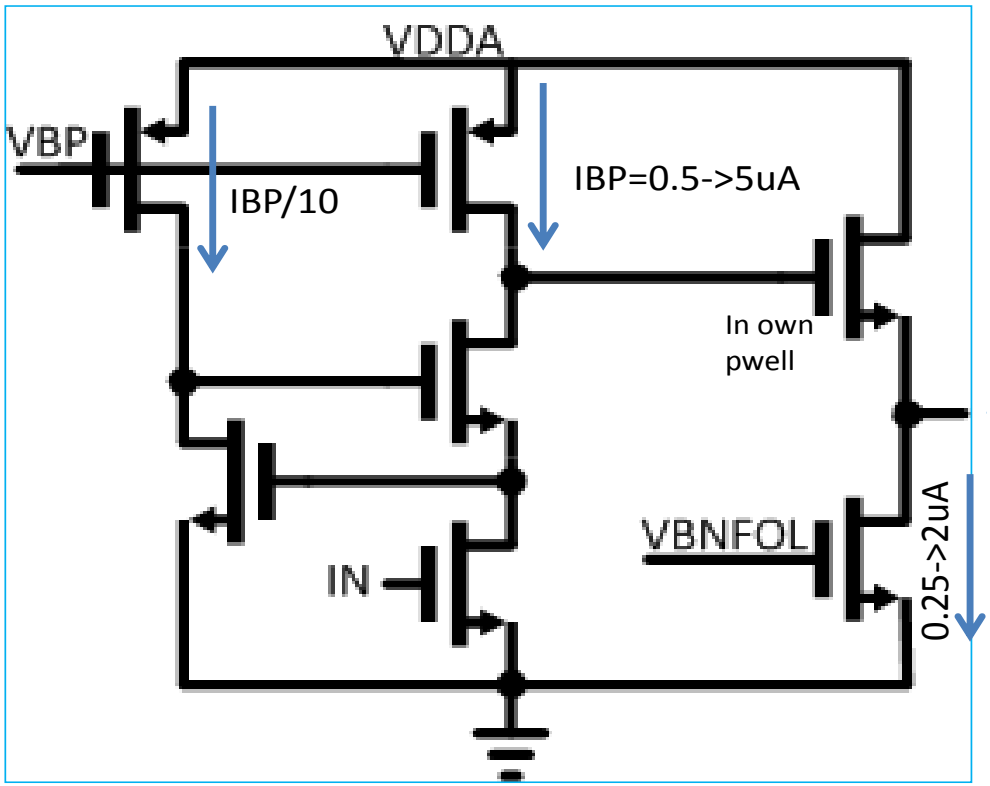
INFN-Pavia prototype



- Folded cascode with local feedback and act load
- Input device: W/L=9 μm/0.1 μm Power dissipation: ~3.6 uW

Low frequency gain ~100 dB, gain-bandwidth product 140 MHz

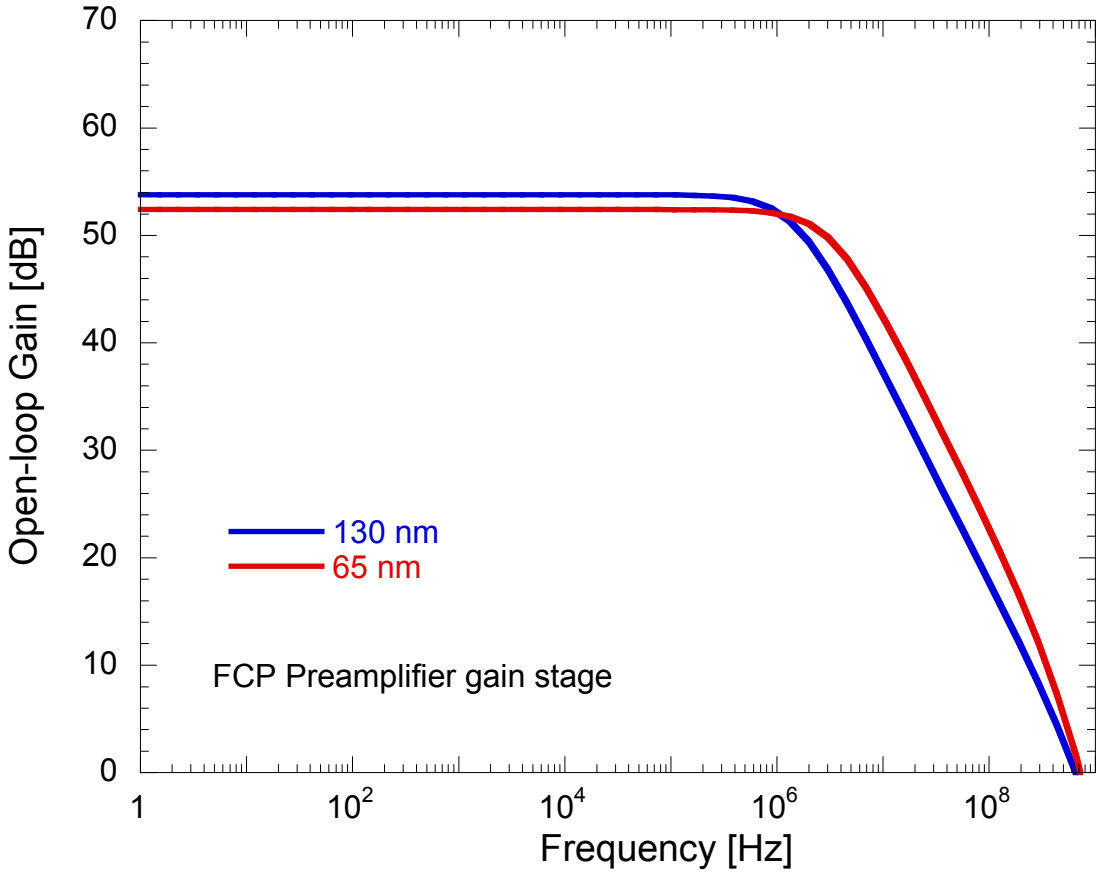
LBNL design



Gain stage with active cascode

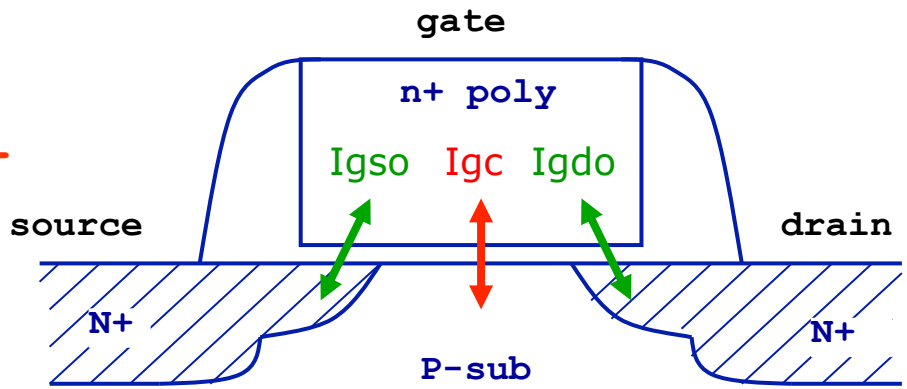
Open loop gain – 130 nm vs 65 nm inverting amplifier stage

✓**Example of an amplifier design in 65 nm**, where the same currents and inversion coefficients were used as in a 130 nm design of a regulated cascode amplifier, and transistor W and L were sized accordingly.



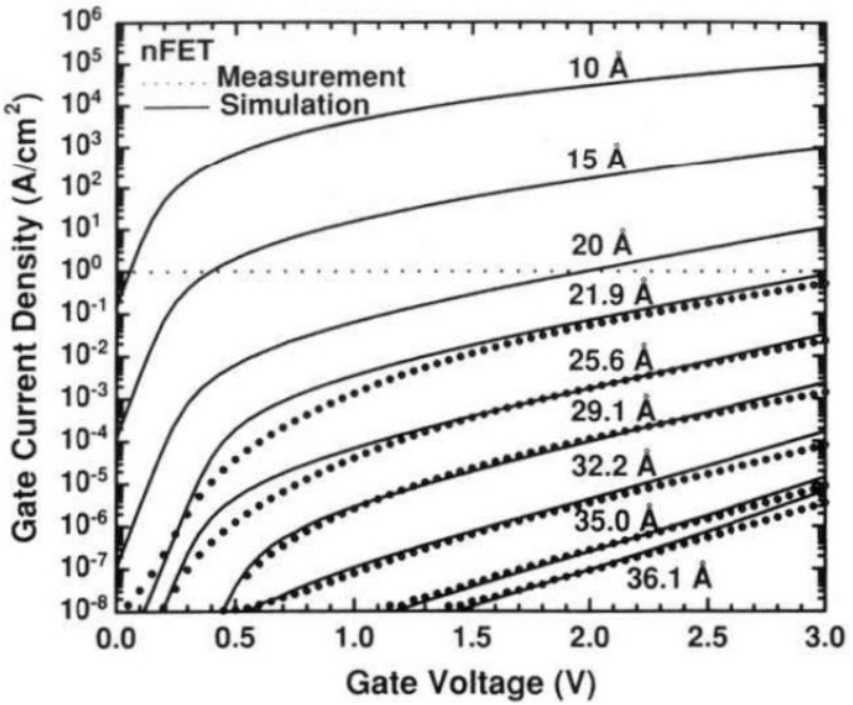
Gate current

- **Charge carriers have a nonzero probability** (larger for electrons with respect to holes) **of directly tunneling through a silicon dioxide layer with a physical thickness < 2 nm (100-nm scale CMOS).**



- ***A reduction of physical oxide thickness of a few Å may give several orders of magnitude increase in the gate current.***

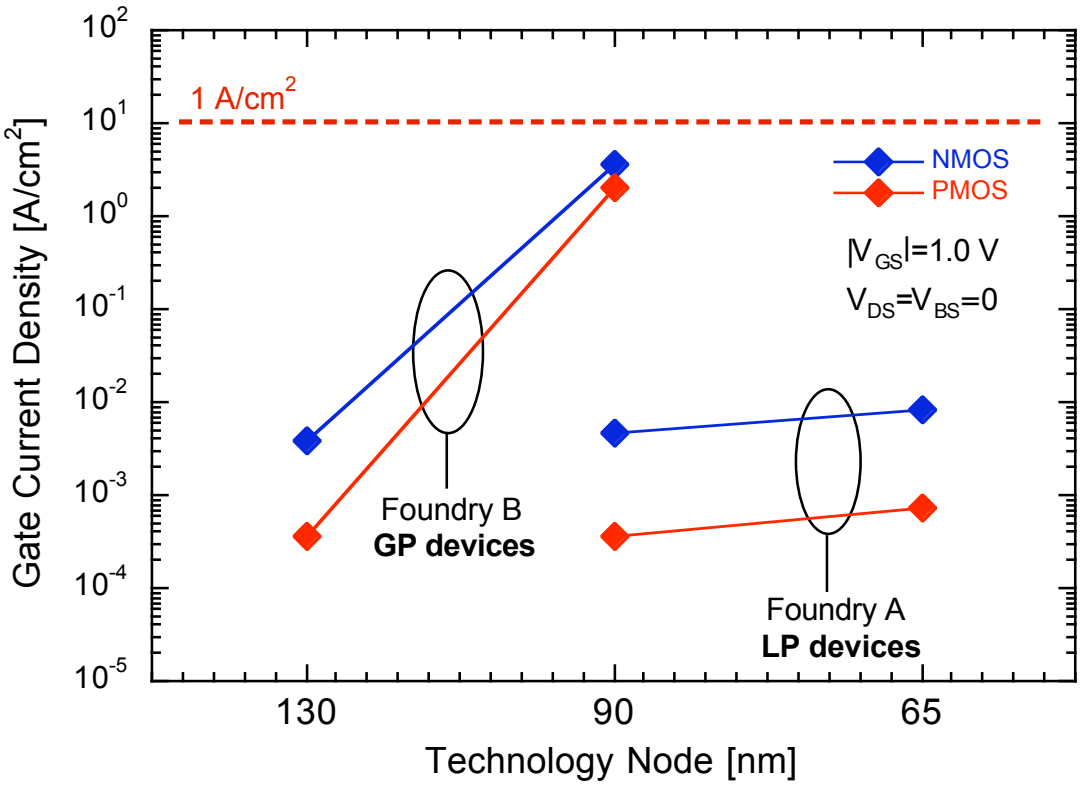
- This current results in an **increase of the static power consumption** (manageable limit of gate leakage current density = 1 A/cm^2) for digital circuits and might **degrade analog performance** (shot noise in the gate current, discharge of storing capacitors, current load on global voltage references,…)



- **Gate dielectric nitridation** increases the dielectric constant, allowing for films with a **larger physical thickness** as compared with SiO_2 ($C_{OX} = \varepsilon_{OX}/t_{OX}$). This **mitigates the gate leakage current**; however, its value can sizably change in devices from different foundries.

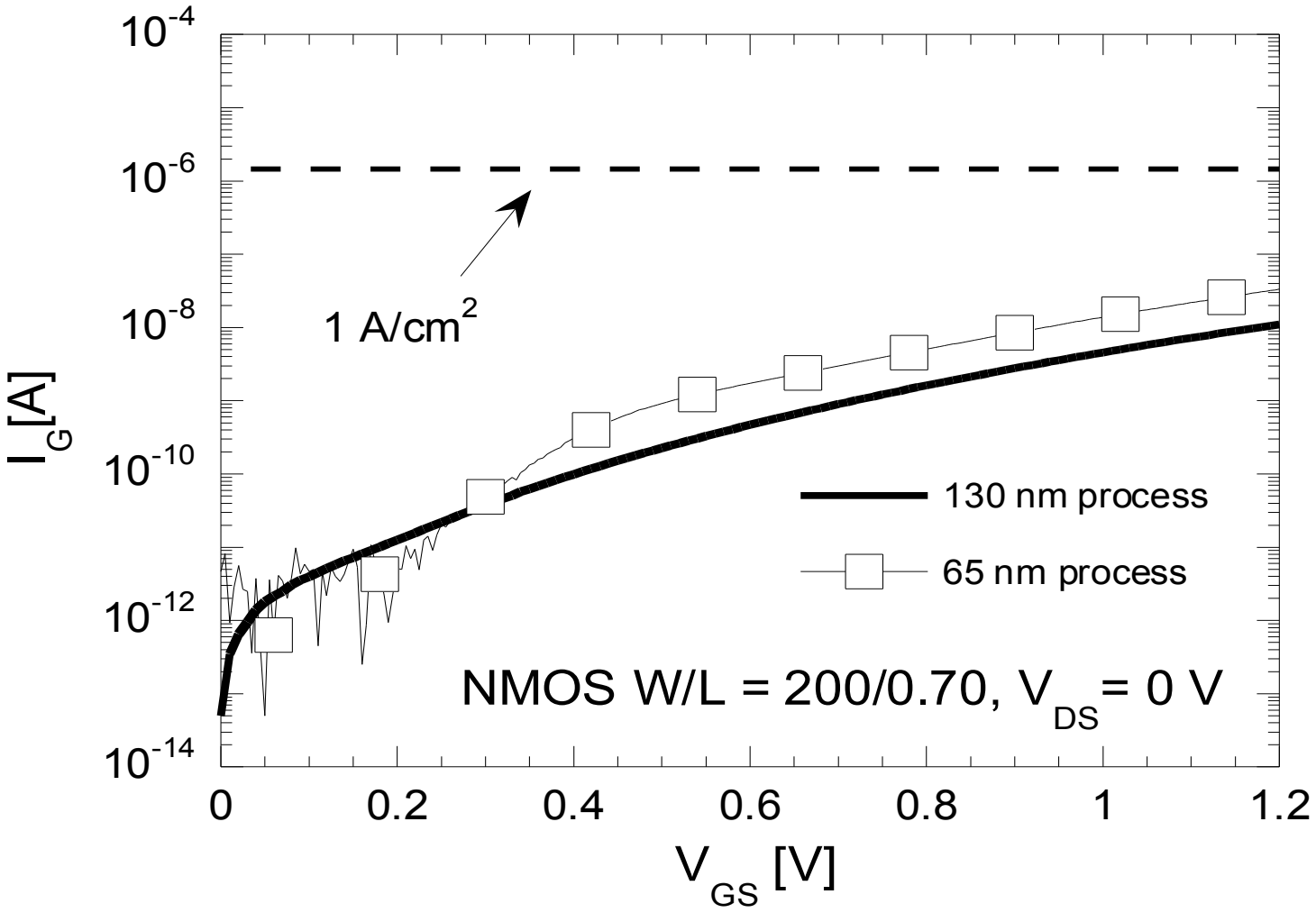
Gate leakage current in nanoscale CMOS flavours and generations

- Interestingly, the **gate leakage current is observed to decrease for the types of stresses adopted by the industry in advanced CMOS** (tensile and compressive stress for NMOS and PMOS, respectively)
- These types of stresses increase electron and hole populations in energy bands where they have low tunneling probability through SiO_2 (in addition to enhancing their mobility in the channel)
- We made tests on **130 nm and 90 nm GP (General Purpose) transistors** and on **65 nm LP (Low Power) transistors (V_{DD} = 1.2 V).** These LP devices were optimized for a reduced leakage (larger equivalent oxide thickness, different level of nitridation with respect to other flavours, different silicon stress).



Gate current in LP 65 nm CMOS

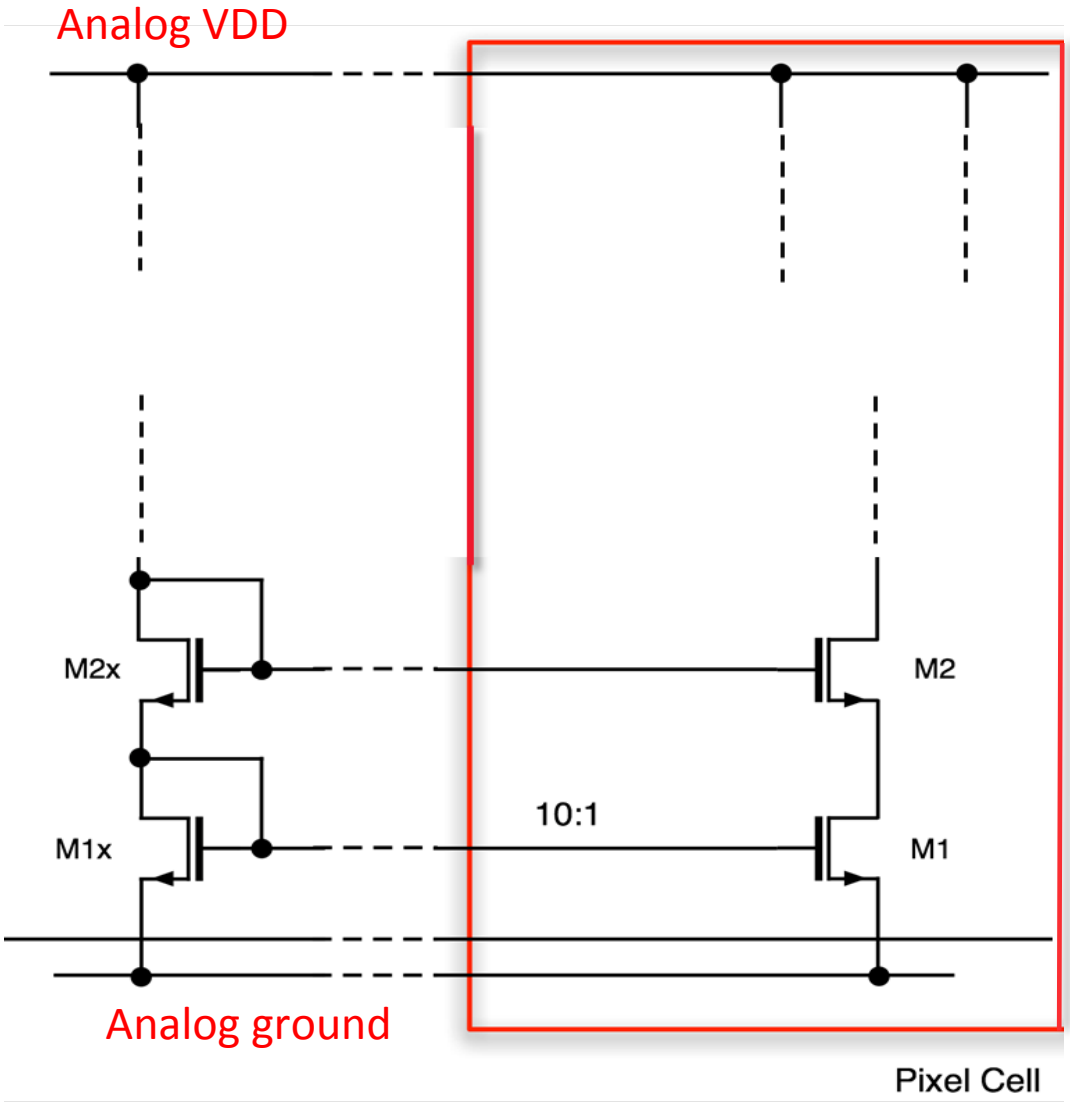
The value of the gate current is maintained across different CMOS technology nodes from 130 nm to 65 nm (Low Power version)



Gate current and global design of a CMOS readout chip

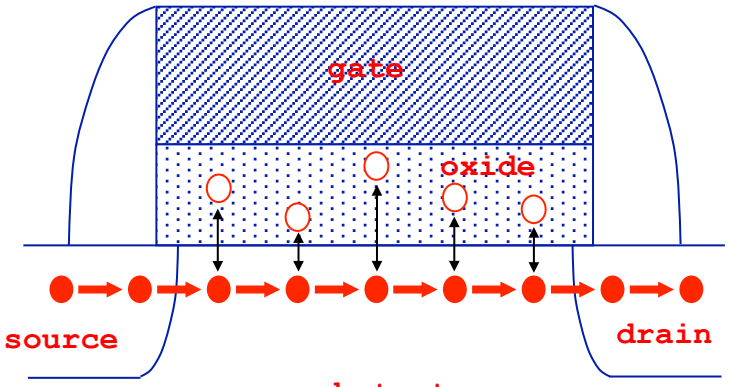
In a single transistor in the LP 65 nm process, the gate current has a very small value (of the order of 100 pA/μm^2 for the NMOS, 10 pA/μm^2 for the PMOS).

However, when bias voltages for analog front-end circuits have to be distributed across a large chip (e.g., a 4 cm^2 pixel readout integrated circuit), the total gate leakage current has to be taken into account in the design of reference voltage and current generators (typically, DACs) and current mirrors.

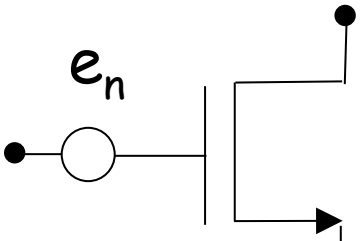


1/f noise: gate stack fabrication process

- Interaction between charge carriers in the MOSFET channel and traps close to the Si-SiO_2 interface leads to fluctuations in the drain current. This can be modeled with a 1/f term in the spectral density of the noise voltage generator in series with the gate.



- The process recipe for the gate stack (gate electrode and dielectric) may affect the density of oxide traps and their interaction with charge carriers in the channel, impacting on the 1/f noise spectral density.



$$\frac{\overline{de_n^2}}{df} = \frac{4kT\,\Gamma}{g_m} + \frac{K_f}{C_{OX}WLf^{\alpha_f}}$$

- For a physical oxide thickness < 2 nm (same order of the tunnelling distance) the traps at the interface between the gate dielectric and the gate electrode (fully silicided poly gates) can play a major role.

- 1/f noise may be affected by mechanical stress in the silicon channel (enhanced carrier mobility and drive current).

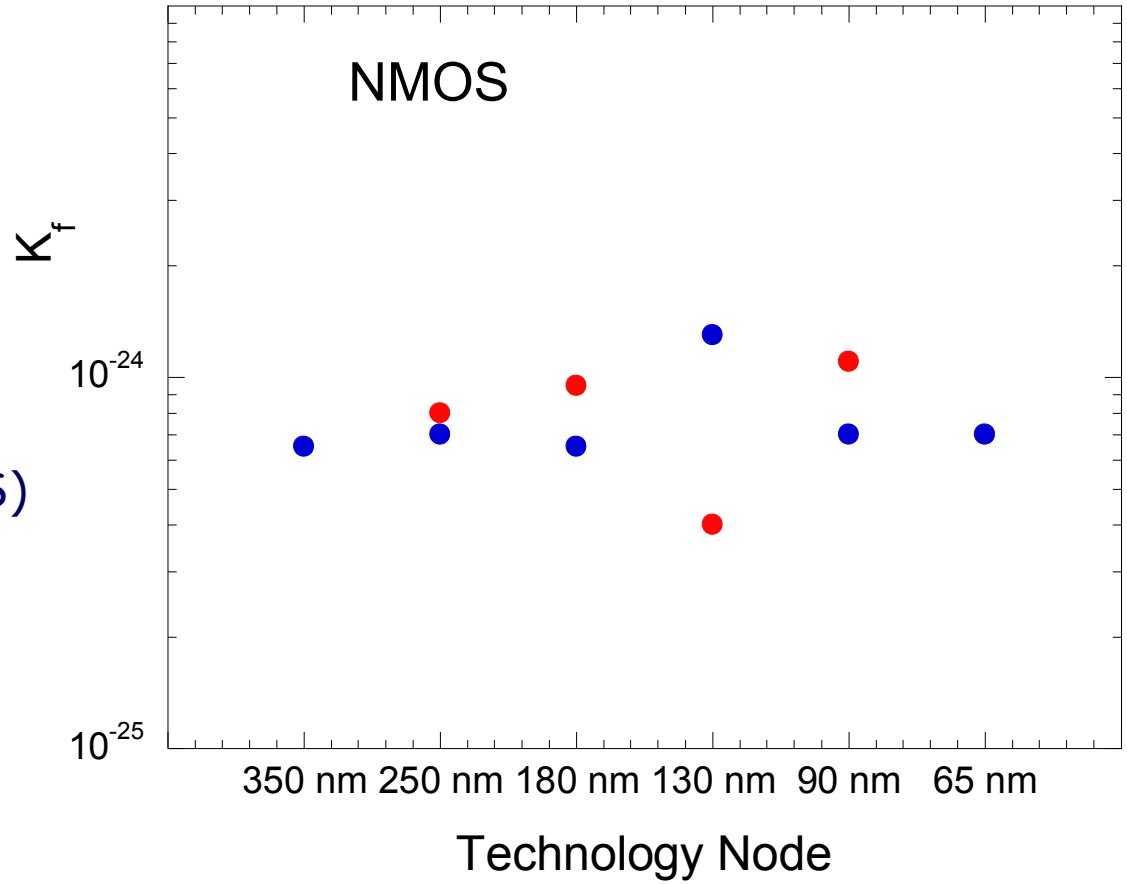
1/f noise from 350 nm to 65 nm NMOS

The 1/f noise parameter K_f does not show dramatic variations across different CMOS generations and foundries in NMOS.

$$S^2_{1/f}(f) = \frac{K_f}{C_{OX} W L f^{\alpha_f}}$$

- k_f 1/f noise parameter
- α_f 1/f noise slope-related coefficient

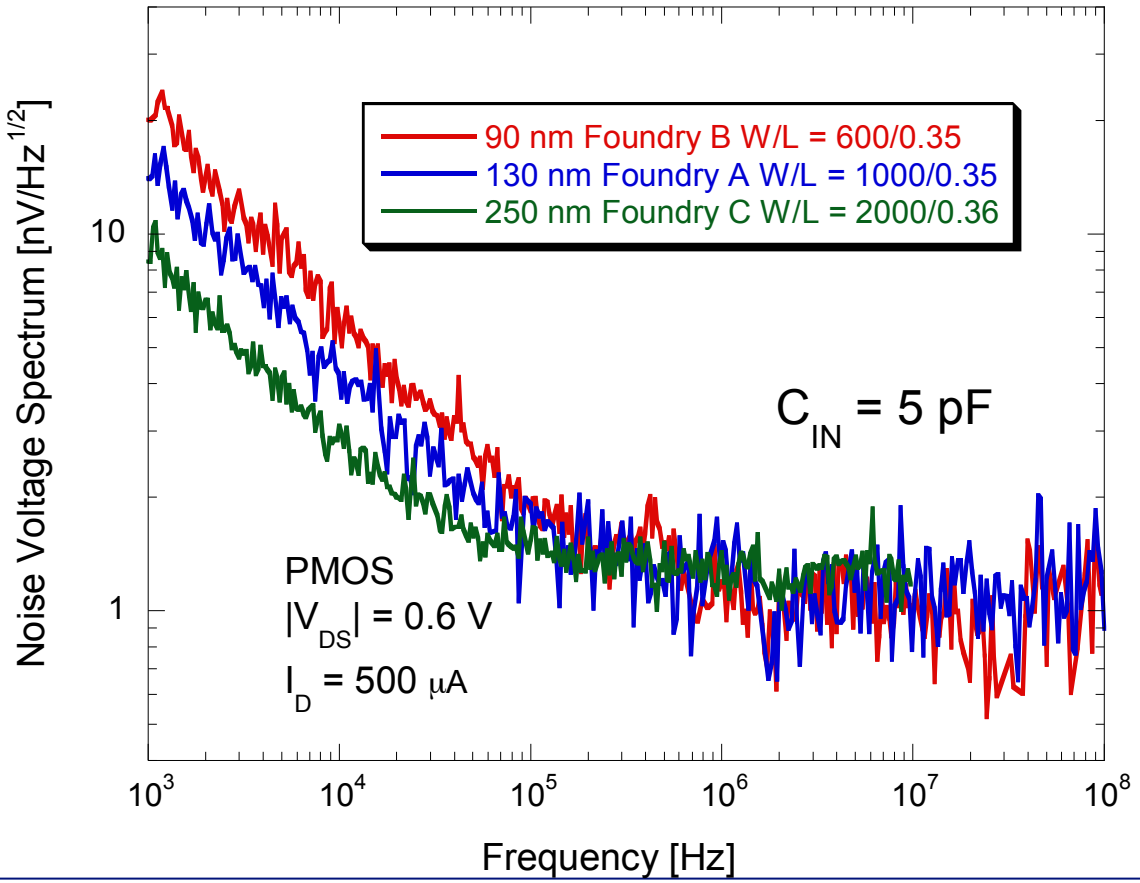
(≅ 0.85 in NMOS, ≅ 1 – 1.1 in PMOS)



1/f noise in PMOS:

CMOS generations from 250 nm to 90 nm

- 1/f noise appears to increase (for a same WLC_{OX}) with CMOS scaling

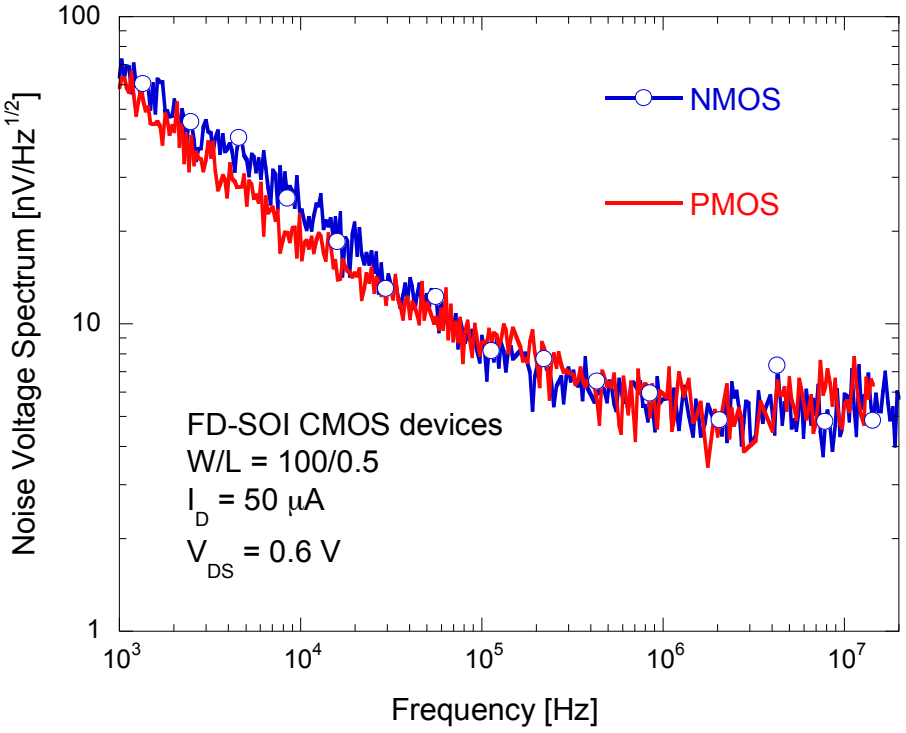


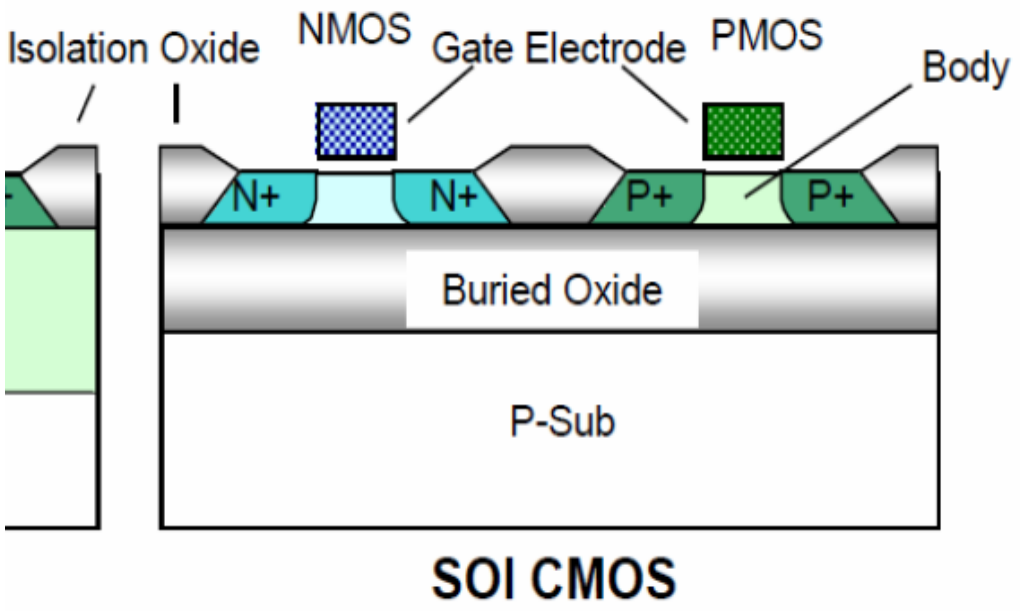
1/f noise: NMOS vs PMOS

- In bulk CMOS, the fact that PMOSFETs feature a smaller 1/f noise with respect to equally sized NMOSFETs was generally related to buried channel conduction.
- In deep submicron processes, it was expected that the PMOS would behave as a surface channel device, rather than a buried channel one as in older CMOS generations.
- With an inversion layer closer to the oxide interface, 1/f noise is expected to increase. Ultimately, PMOSFETs should feature the same 1/f noise properties as NMOSFETs. However, this was not observed in CMOS generations down to 130 nm and 90 nm.
- A possible interpretation can be related to the different interaction of electrons (NMOS) and holes (PMOS) with traps in the gate dielectric (different barrier energies experienced by holes and electrons across the Si/SiO_2 interface) .

NMOS and PMOS in an FD-SOI technology

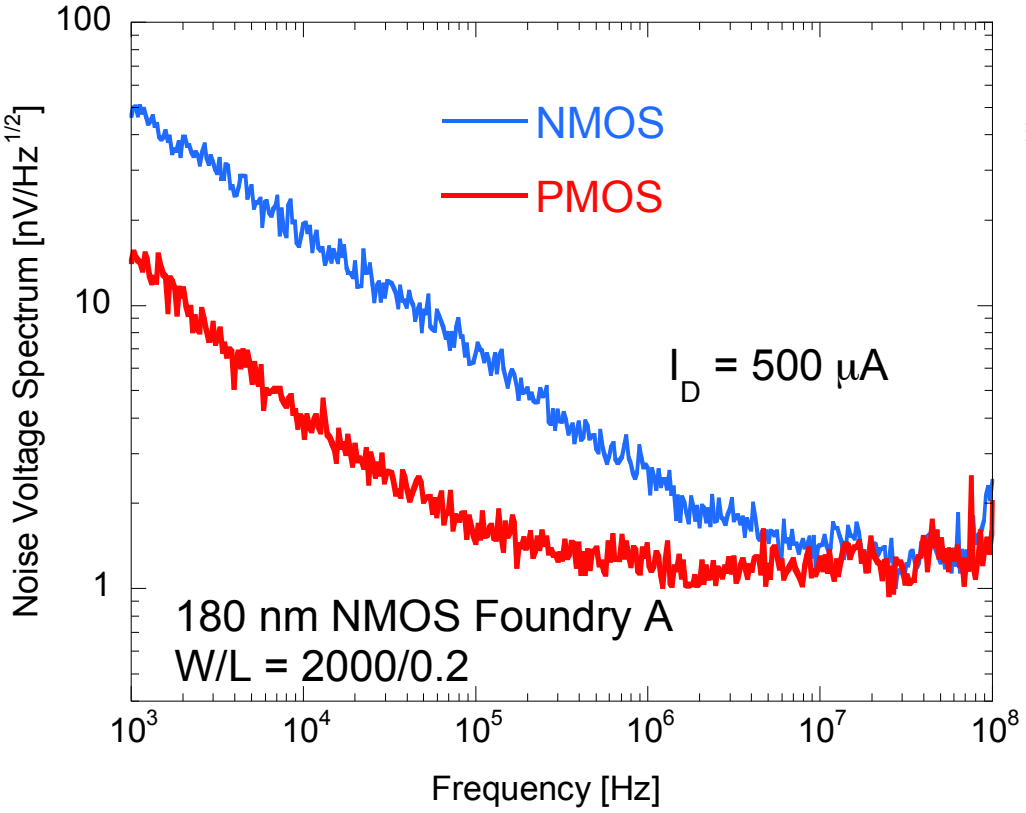
We previously found that NMOS and PMOS have the same 1/f noise only in one case, that is, in fully-depleted 180 nm CMOS SOI transistors. A possible explanation was that in a very thin silicon film (40 nm) conduction takes place very close to the Si-SiO_2 interface.



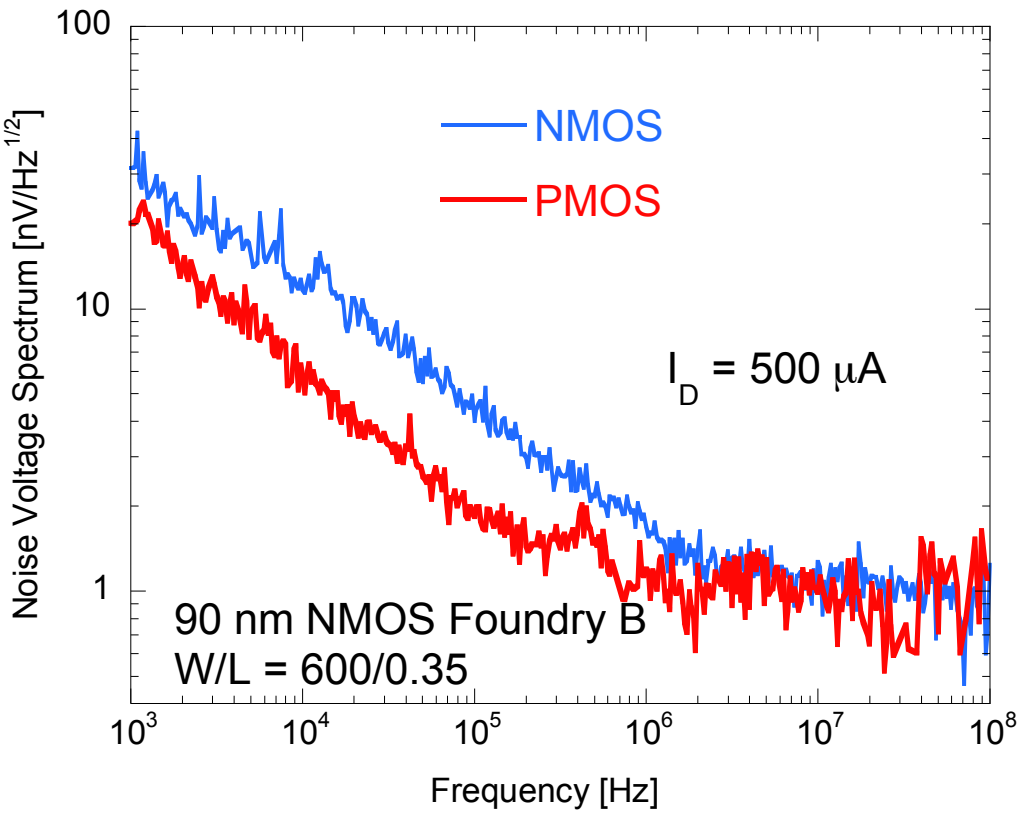


1/f noise: NMOS vs PMOS

In bulk CMOS processes close to the 100 nm threshold, the PMOS still has a lower 1/f noise than the NMOS. However, this difference tends to decrease with newer CMOS generations.



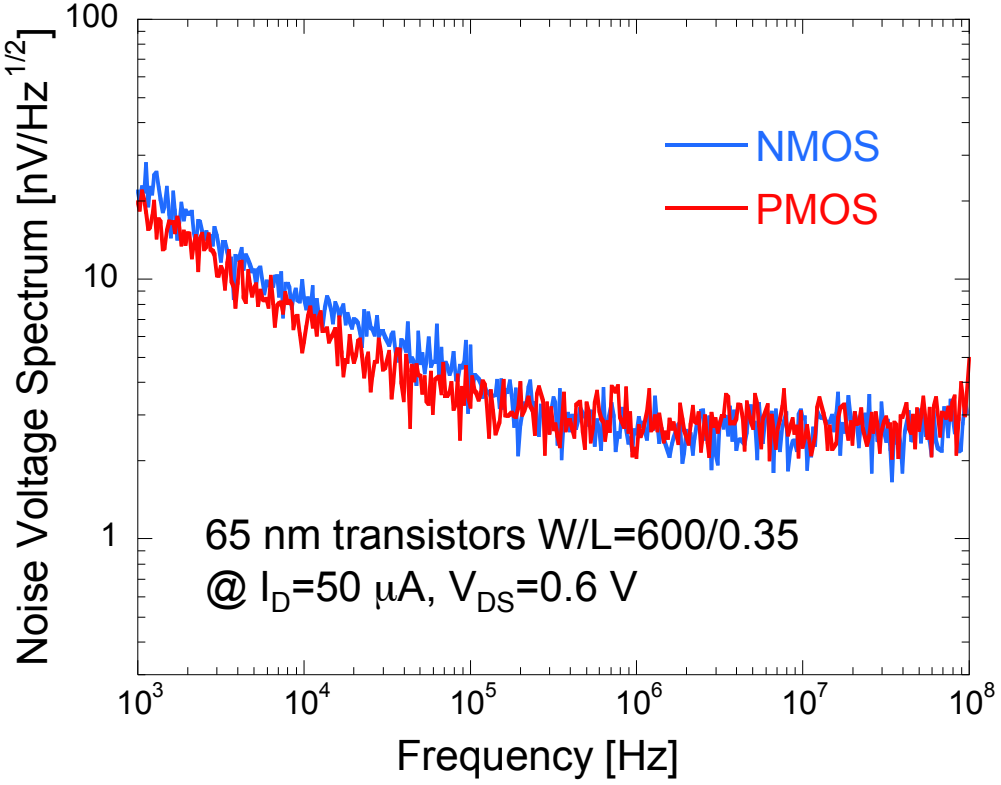
180 nm

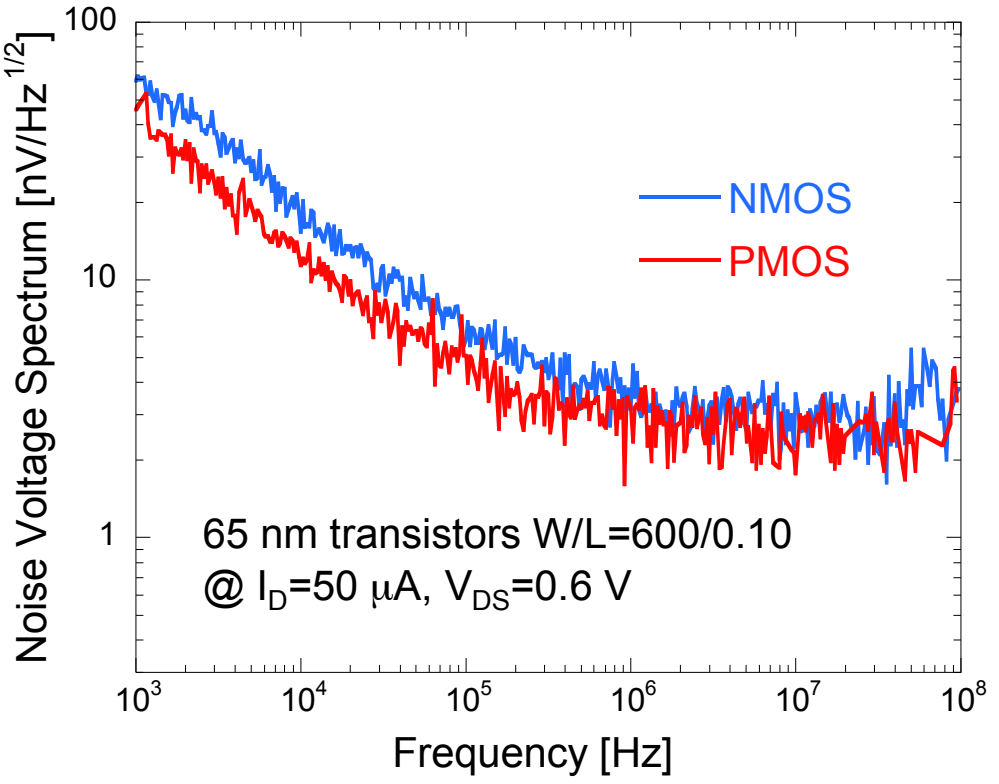


90 nm

65 nm LP process: 1/f noise

- In the 65 nm LP process by Foundry B, **NMOS and PMOS have similar 1/f noise** (especially longer transistors).
- This could be explained by a "surface channel" behavior for both devices, and/or by the fact that the gate dielectric nitridation decreases the barrier energy experienced by holes across the silicon-dielectric interface. This would make it easier for the PMOS channel to exchange charges with oxide traps.





Thermal noise and CMOS scaling

- The origin of thermal noise can be traced to the random thermal motion of carriers in the device channel.
- When the MOSFET is biased in saturation ($V_{DS} > V_{DS,sat}$), the following equation can be used for the power spectral density of thermal noise in all inversion conditions:

$$S_W^2 = 4k_B T\Gamma \frac{1}{g_m}$$

$$\Gamma = \alpha_W n \gamma$$

- k_B = Boltzmann's constant
- T = absolute temperature
- $n = 1 + \frac{g_{mb}}{g_m}$

  (n = 1 – 1.5; proportional to the inverse of the slope of the I_D-V_{GS} curve in the subthreshold region)

- γ = channel thermal noise coefficient (depends on inversion region; varies with the inversion layer charge: = 1/2 in weak inversion, = 2/3 in strong inversion)
- α_W = excess noise coefficient

Excess thermal noise coefficient

$$S_W^2 = 4k_B T n \gamma \frac{1}{g_m} \alpha_W$$

α_W = 1 for long-channel devices. Short-channel devices can be noisier (α_W > 1) mainly because of two effects related to high longitudinal electric fields (E = V_{DS}/L) in the channel.

- Reduction of charge carrier mobility:

  at increasing field strength the carrier velocity is saturated at $v_{sat}=\mu_0 E_C$ (μ_0 low-field mobility, E_C critical field strength)

$$\mu = \frac{\mu_0}{1 + \frac{E}{E_C}}$$

- Increase of charge carrier temperature:

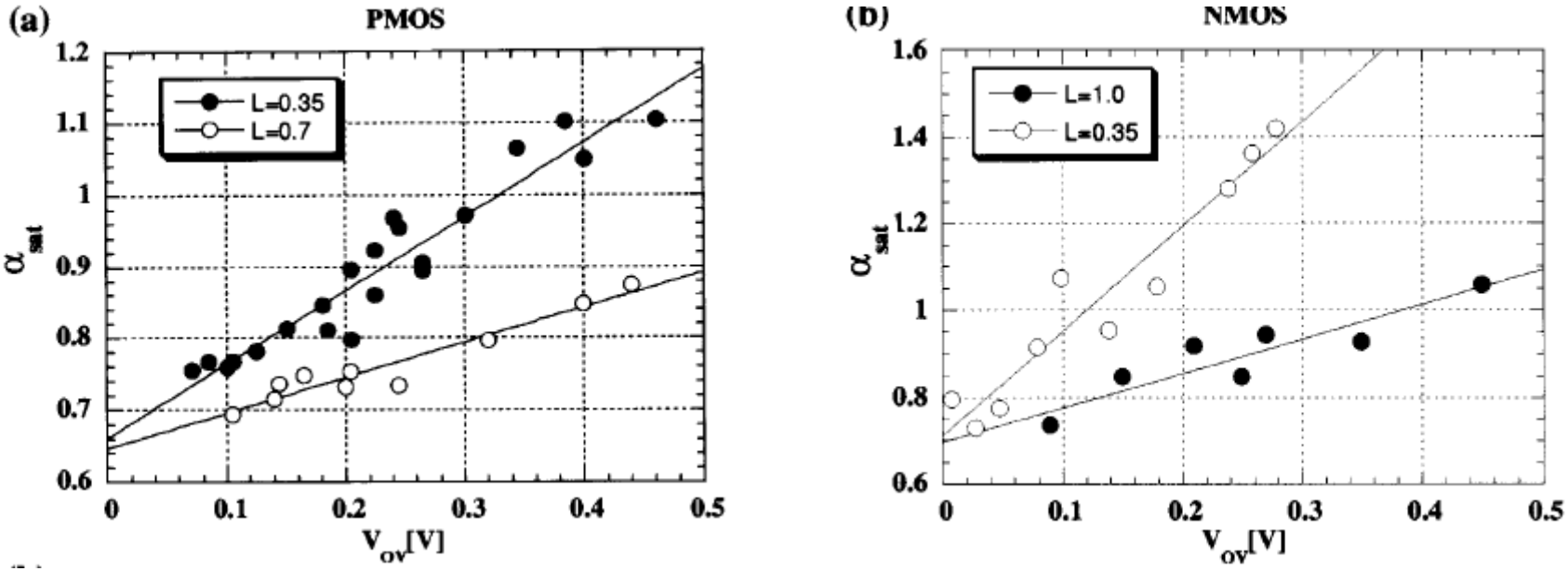
  at increasing field strength the temperature T_e of carriers in the channel increases with respect to the temperature T of the device lattice

$$\frac{T_e}{T} = \left(1 + \frac{E}{E_C}\right)^b$$

Excess thermal noise coefficient

In saturation, the longitudinal electric field is $E = (V_{GS} - V_{TH})/L$.

It can be shown that short-channel phenomena affect thermal noise only if the value of the ratio E/E_C is not negligible, which does not happen if the device is biased in weak/moderate inversion.



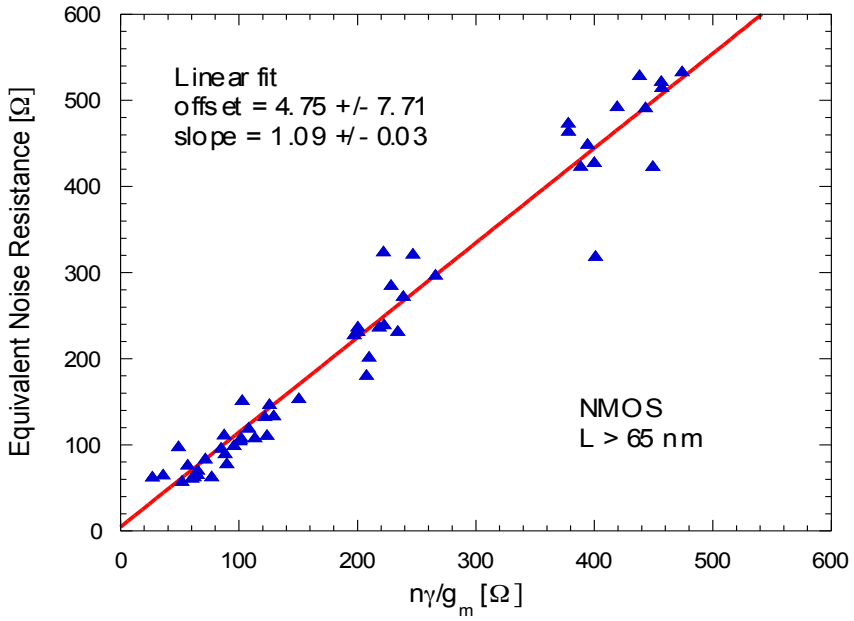
350 nm CMOS

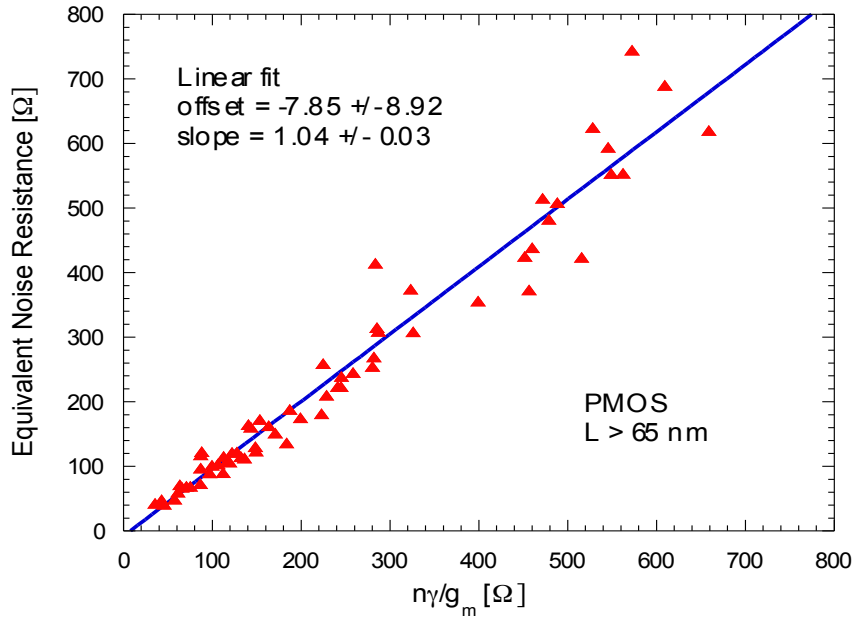
White noise in 65 nm CMOS

Evaluated in terms of the **equivalent channel thermal noise resistance**:

$$R_{eq} = \frac{S_W^2}{4k_B T} = \alpha_W \frac{n\gamma}{g_m}$$

- α_w excess noise coefficient
- n proportional to $I_D(V_{GS})$ subthreshold characteristic
- γ channel thermal noise coeff.





α_w close to unity for NMOS and PMOS with L > 65 nm → **no sizeable short channel effects** in the considered operating regions (except for 65 nm devices with $\alpha_w \approx 1.3$)

Negligible contributions from **parasitic resistances**

White noise in 65 nm CMOS

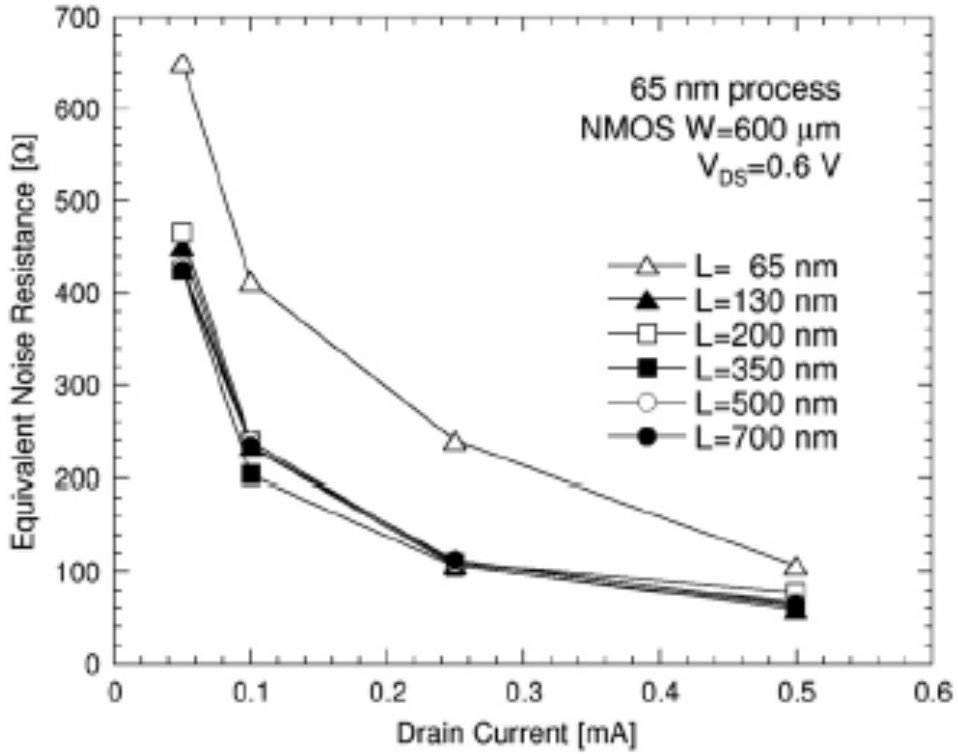
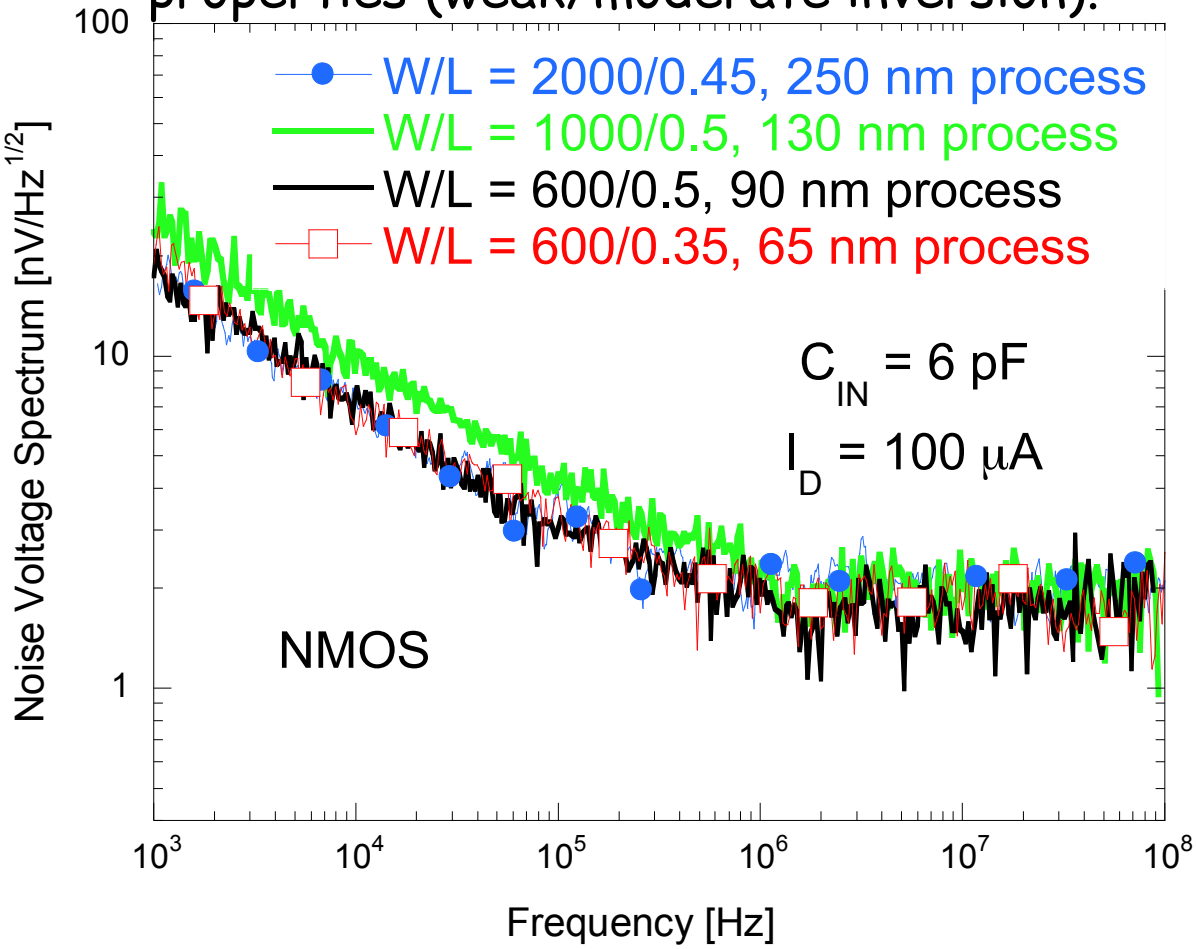


Fig. 7. Equivalent channel thermal noise resistance R_{eq} for NMOS devices belonging to the 65 nm process (V_{DS}=0.6V).

Noise in NMOS: CMOS generations from 250 nm to 65 nm

- 1/f noise has approximately the same magnitude (for a same WLC_{OX}) across different CMOS generations. White noise has also very similar properties (weak/moderate inversion).



1/f noise

$$S^2_{1/f}(f) = \frac{K_f}{C_{OX} W L f^{\alpha_f}}$$

- k_f 1/f noise parameter
- α_f 1/f noise slope-related coefficient

Channel thermal noise

$$S^2_W = \frac{4 k_B T \Gamma}{g_m}, \qquad \Gamma = \alpha_W n \gamma$$

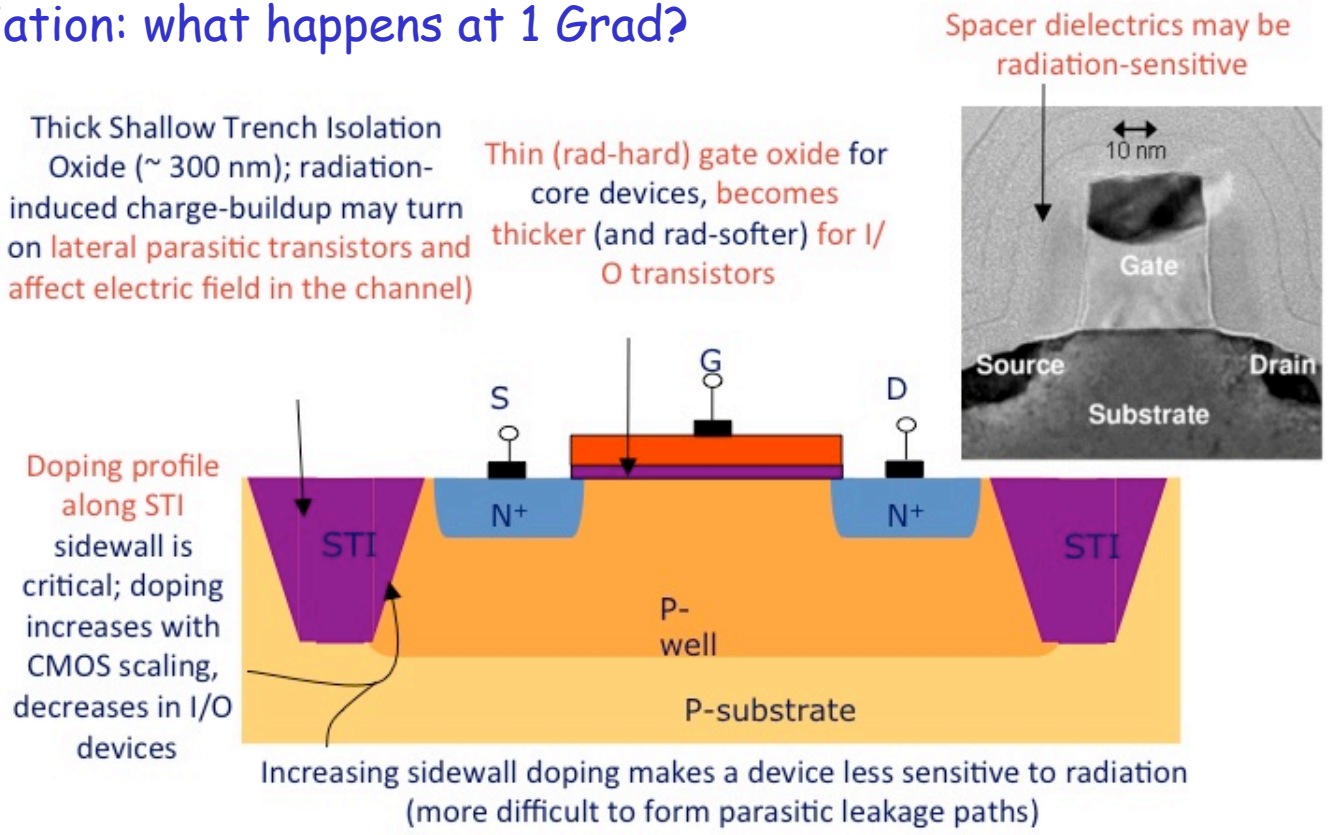
- k_B Boltzmann's constant
- T absolute temperature
- α_w excess noise coefficient
- γ channel thermal noise coefficient

In weak inversion: $g_m = \frac{I_D}{n V_T}$

65 nm CMOS at extreme radiation levels

- At the HL-LHC design luminosity, for an operational lifetime of 10 years, the innermost pixel layer will be exposed to a total ionizing dose of 1 Grad, and to an equivalent fluence of 1-MeV neutrons of 2 x 10^{16} n/cm^2.
- If unacceptable degradation, **a replacement strategy** must be applied for inner pixel layers.
- Nanoscale CMOS (with very thin gate oxide) has a large intrinsic degree of tolerance to ionizing radiation: what happens at 1 Grad?

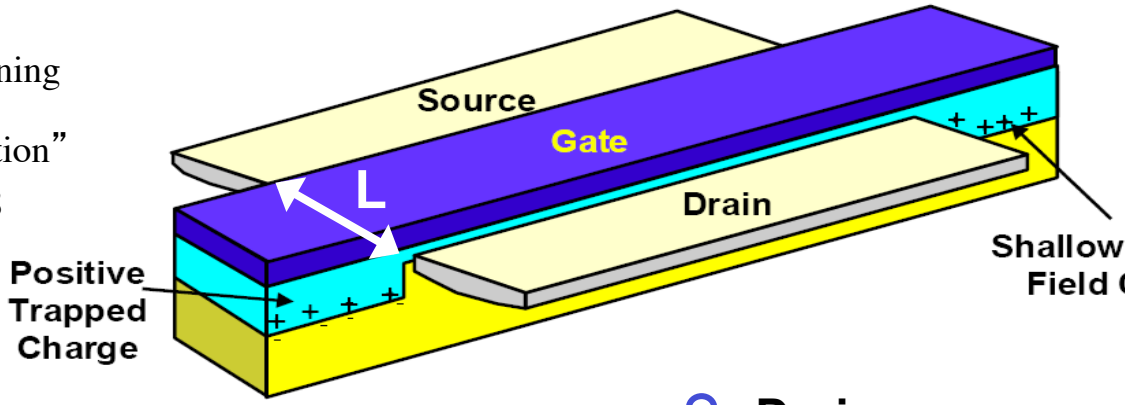
- Radiation induced electric charge is associated with thick lateral isolation oxides
- CMOS is usually not affected by non ionizing radiation: what happens at 2 x 10^{16} n/cm^2?



NMOSFETs and lateral leakage

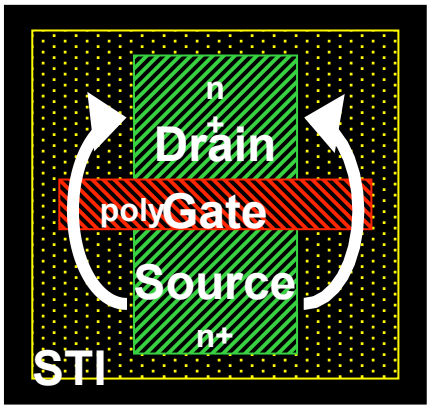
In NMOSFETs edge effects due to radiation-induced positive charge in the STI oxide generate sidewall leakage paths.

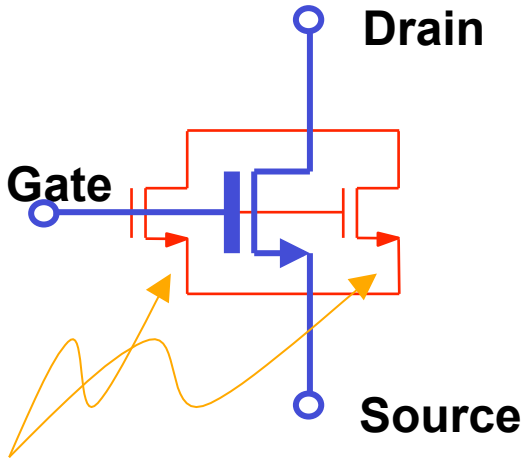
Shaneyfelt et al,
"Challenges in Hardening Technologies using Shallow-Trench Isolation"
IEEE TNS, Dec. 1998



Lateral transistors have the same gate length as the main MOSFET

NMOS finger

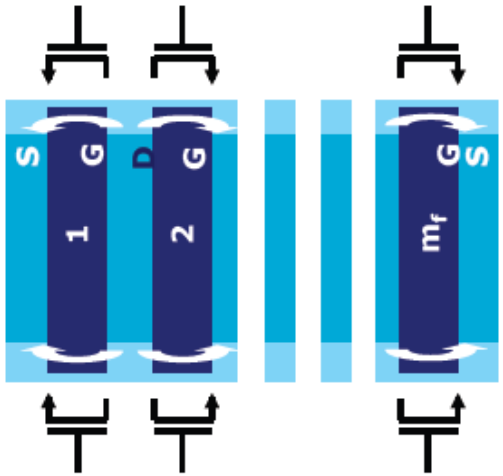




Lateral parasitic devices

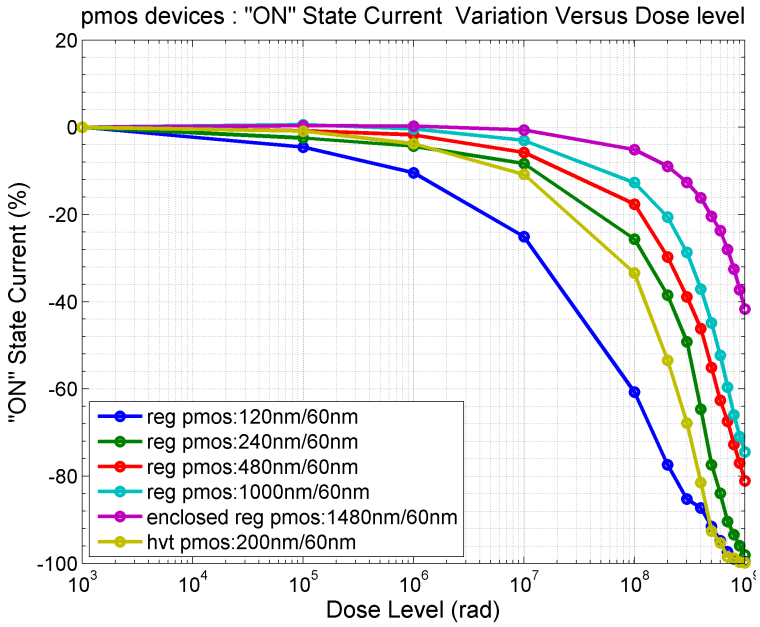
Main transistor finger

Multifinger NMOS



The analog front-end at extreme total ionizing dose

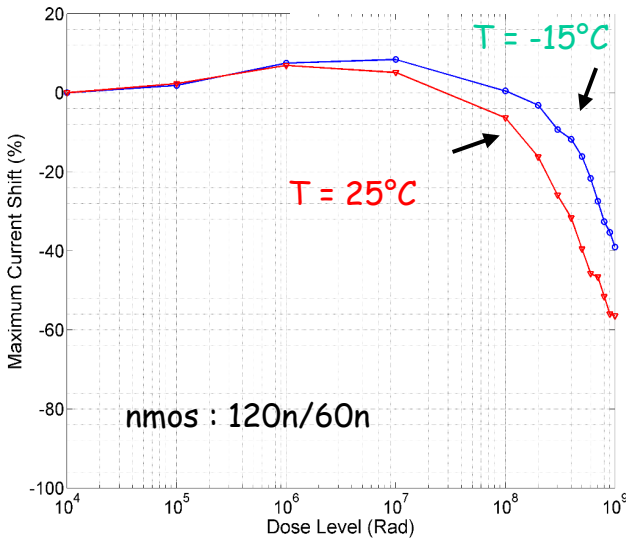
- Among other effects, PMOSFETs (especially minimum size ones) show a large transconductance degradation, which becomes very steep over 100 Mrad (partial recover after annealing)
- This is probably not so critical for the design of analog blocks, where minimum size transistors can be avoided if necessary; the study of radiation effects on noise is ongoing
- Damage mechanisms have yet to be fully understood; they appear to be **less severe at** the foreseen operating temperature of the pixel detector at HL-LHC (**about -15 °C**)

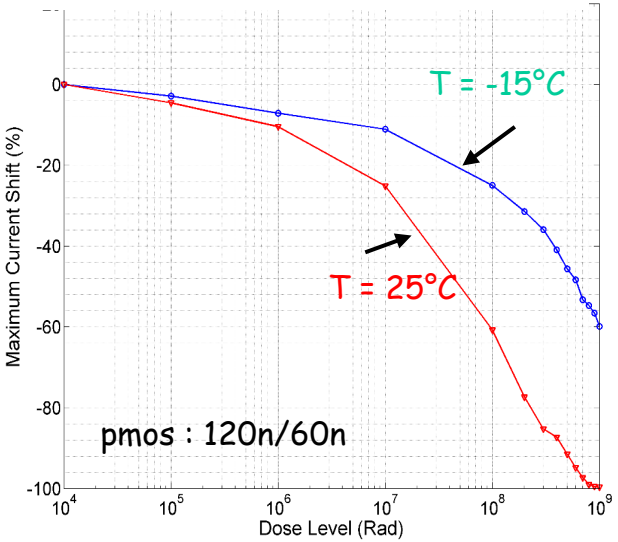


V. Re – IN2P3 M

CPPM data with X-rays

(Fermilab and Padova studying radiation effects with other sources)





Total ionizing dose effects on noise in LP 65 nm CMOS

- Noise is a crucial parameter for the performance of the analog front-end (affects minimum threshold setting in particle tracking applications, single photon resolution in X-ray imaging)

- The study of total dose effects on the noise of CMOS transistors can be an effective tool to understand radiation damage mechanisms

- As an example, we developed a model (which worked fine at 10 Mrad TID) for the contribution of lateral parasitic transistors to the total noise of an irradiated NMOS

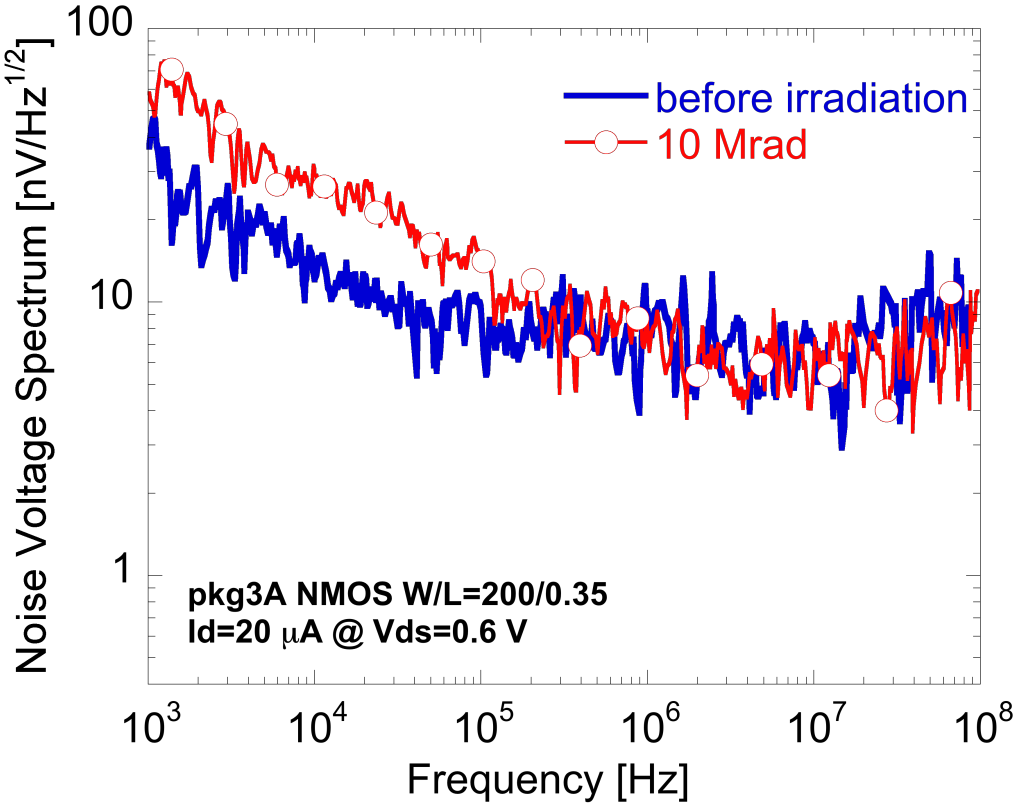
White noise

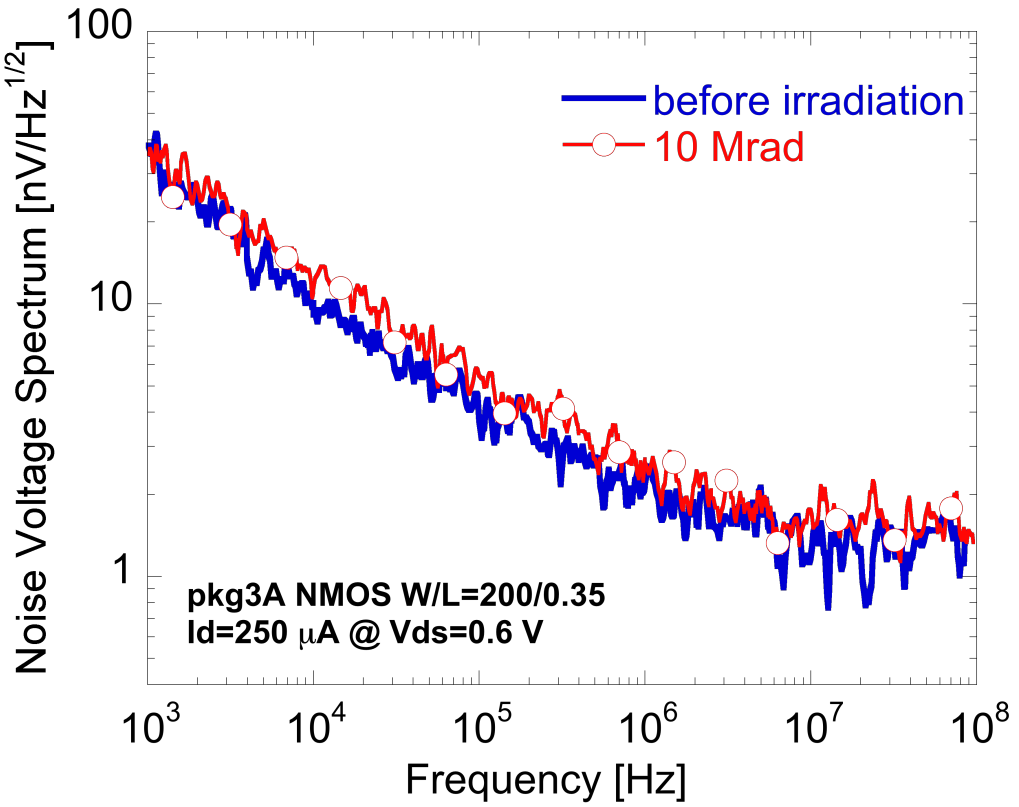
$$\frac{S_{W,post}^2}{S_{W,pre}^2} = \frac{g_{m,main,pre}}{g_{m,main,post} + g_{m,lat}}$$

1/f noise

$$\frac{S_{1/f,post}^2}{S_{1/f,pre}^2} \approx 1 + \frac{A_{f,lat}}{A_f}\left(\frac{g_{m,lat}}{g_m}\right)^2$$

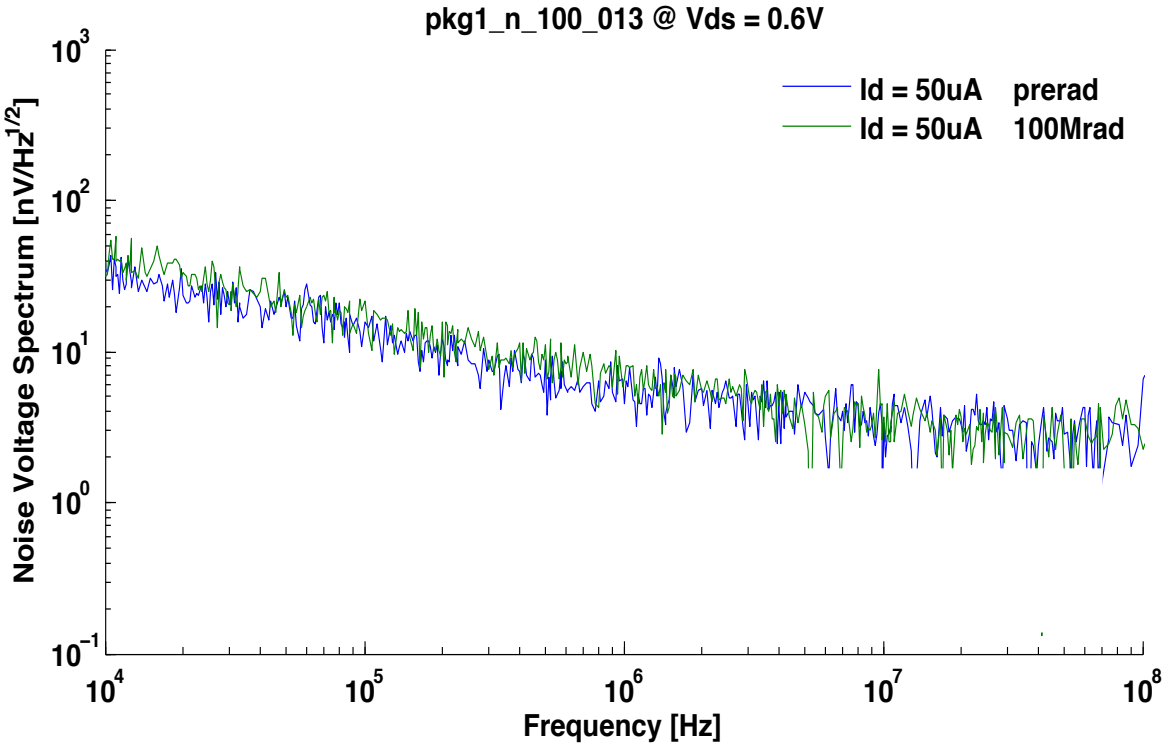
Radiation effects on noise
LP 65 nm technology – 10 Mrad





- **Moderate 1/f noise increase** at low current density, due to the contribution of lateral parasitic devices
- At **higher currents** the degradation is almost negligible because the impact of the parasitic lateral devices on the overall drain current is much smaller
- **No increase** in the **white noise** region is detected

Radiation effects on noise - NMOS

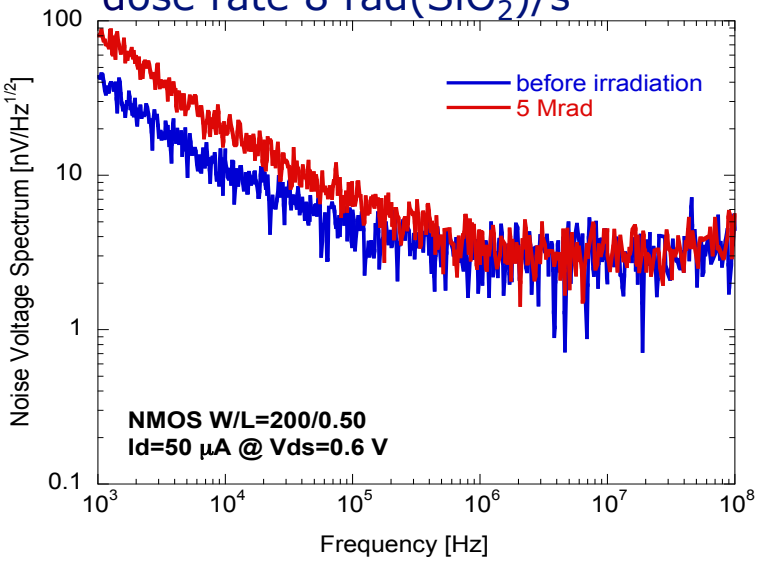


- **No or very little increase of white and 1/f noise terms is detected at 50 and 100 Mrad**

- We found a nonnegligible effect on 1/f noise at much lower doses (irradiation campaign to 10 Mrad TID in 2009-2010)

- We will analyze data to find if there is a correlation with effects on static characteristics at different TID values

^{60}Co γ-rays
dose rate 8 rad(SiO_2)/s



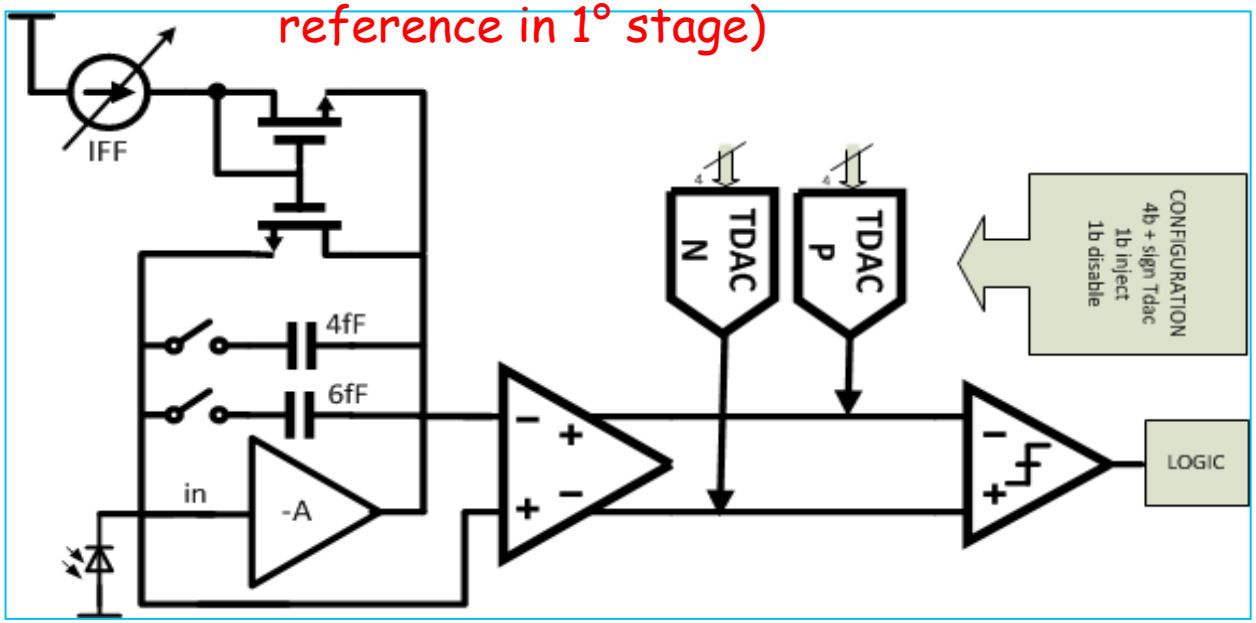
Analog design in 65 nm CMOS in RD53

- The **Analog Working Group of RD53** is studying the best design choices for the front-end stages, that interface the silicon sensor with the large and mostly digital readout chip
- Severe constraints for noise, power, speed, silicon area, immunity to digital interferences have to be taken into account in the classical analog blocks (preamplifier, discriminator,…)
- Scaling of transistor size to the nanoscale region also stimulates analog design ideas that depart from the usual schemes of pixel front-end circuits, going beyond a simple translation of old schematics into a more advanced technology. Among them:
  - ❑ Switched-capacitor techniques
    (avoid local tuning in the pixel cell and additional hardware)
  - ❑ Fully differential architectures
    (increase immunity to interferences)
  - ❑ Current-mode schemes
  - ❑ …..

Analog channel in the pixel readout cell: asynchronous or synchronous?

- The classical continuous-time analog processing channel is a well-established solution for pixel sensors in high-energy physics
- To reduce power (and area), this channel includes just two stages (charge-sensitive preamplifier + asynchronous comparator), and A/D conversion may be based on a time-over threshold measurement.

LBNL design, Preamp with constant current feedback, 2-stage continuous-time comparator (PA input used as reference in 1° stage)

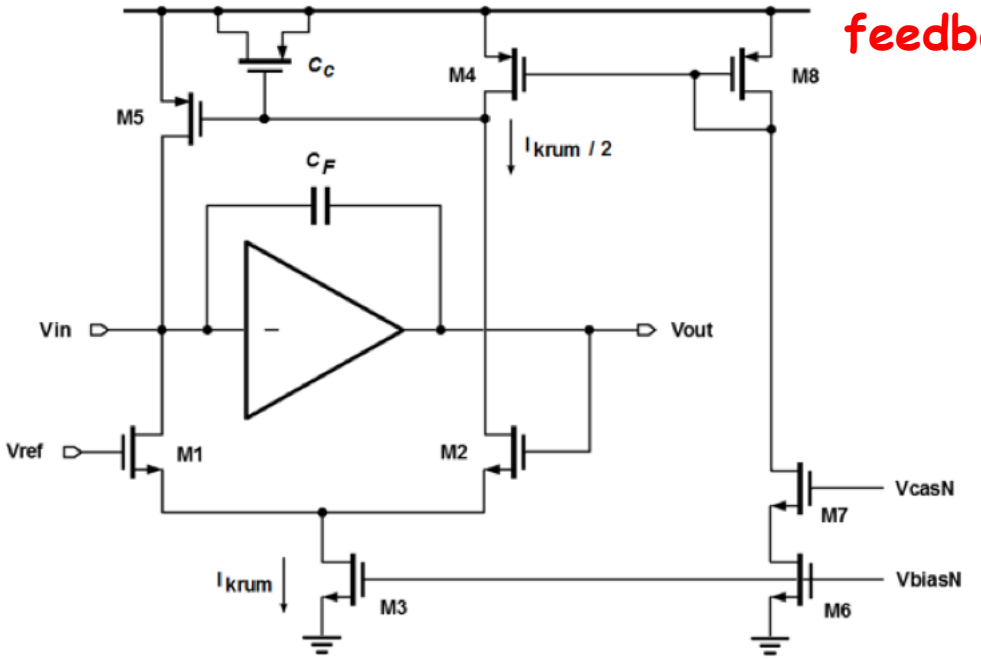


- In an advanced CMOS process, a synchronous architecture may be a good alternative, with self-calibration and discrete-time signal processing features (correlated double sampling, autozeroing) clocked by the bunch-crossing cadence
- **Diverse options are being explored, with interesting alternatives to classical analog pixel cell schemes**

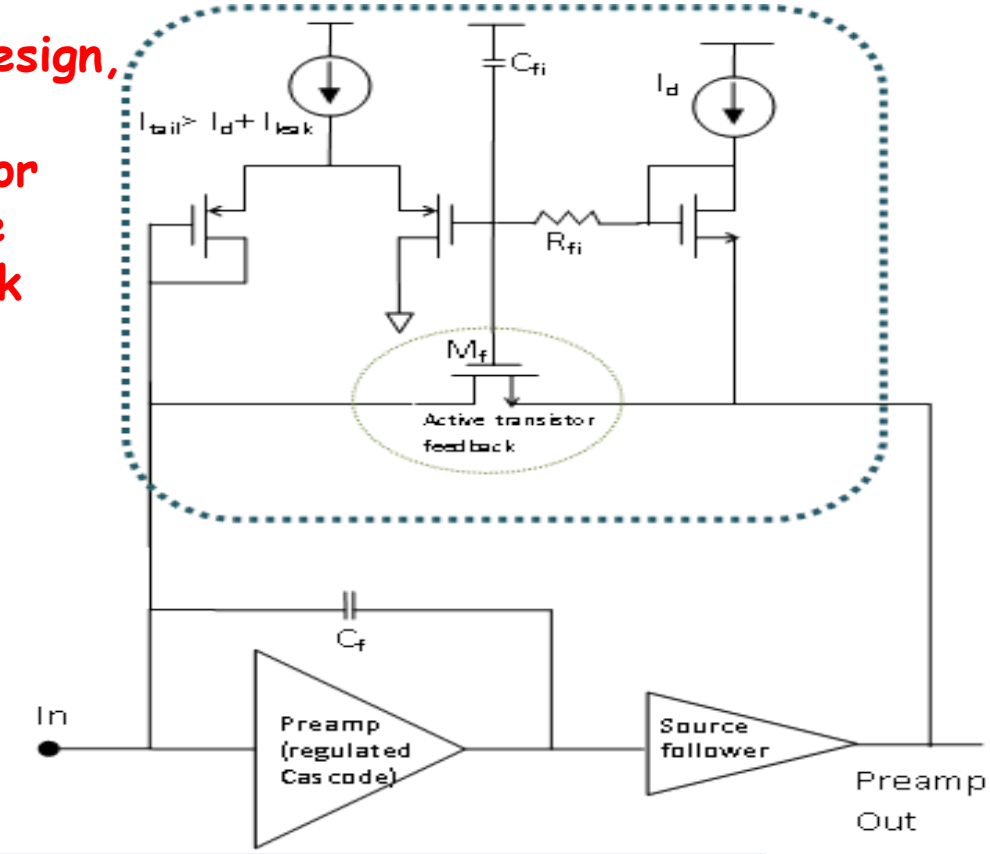
Preamplifier feedback and compensation of sensor leakage current

- Several schemes for the feedback network are being proposed and studied (Krummenacher feedback, current mirror constant current feedback, active transistor resistive feedback)
- Presently, the spec is 20 nA max leakage at $2 \cdot 10^{16}$ n/cm^2

Torino design, Krummenacher feedback

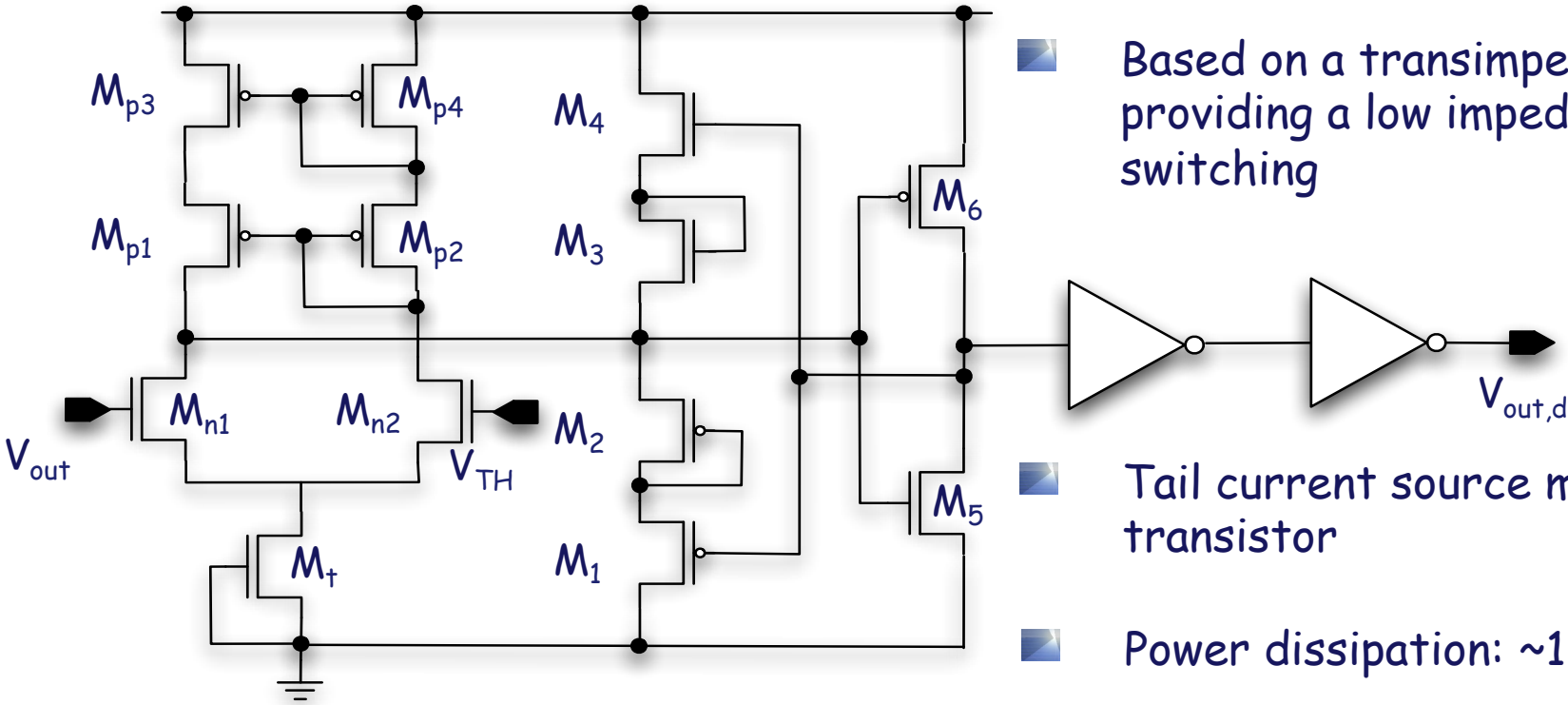


FNAL design, active transistor resistive feedback



Asynchronous discriminators

Based on a transimpedance amplifier providing a low impedance path for fast switching

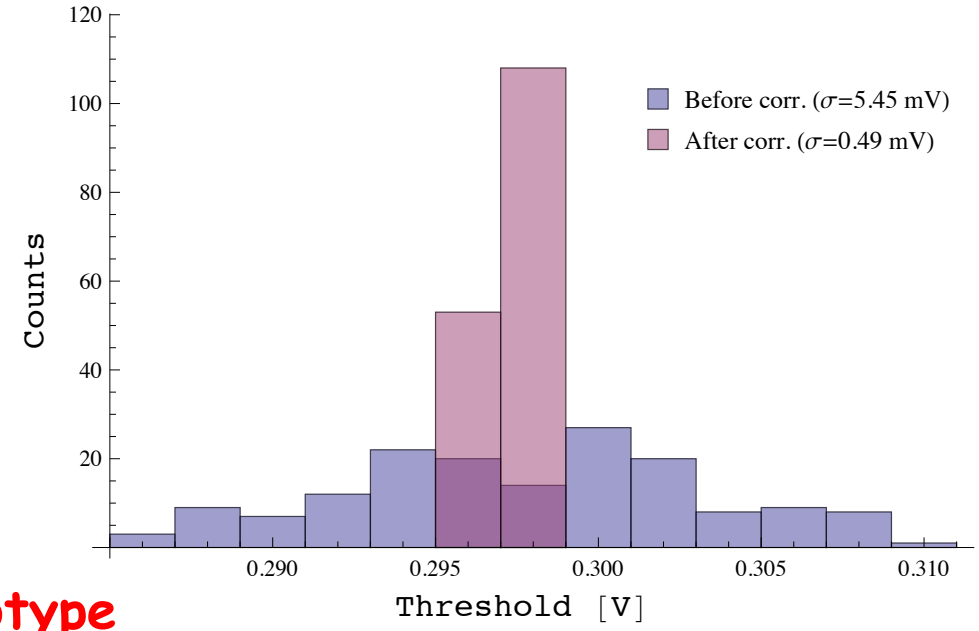


- Based on a transimpedance amplifier providing a low impedance path for fast switching
- Tail current source made with a native transistor
- Power dissipation: ~1.1 uW

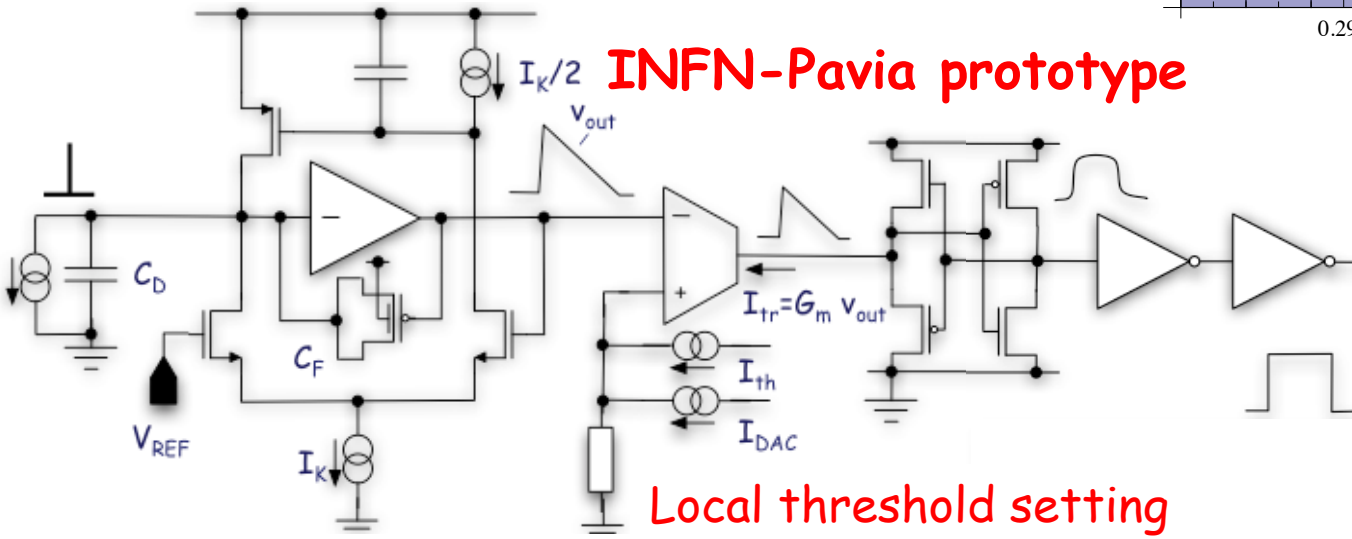
INFN-Pavia design

Digital calibration of the discriminator threshold in an asynchronous front-end

Nonidealities of nanoscale CMOS transistors may be addressed by appropriate design techniques. This includes the digital calibration of analog circuits. In an analog front-end channel, the discriminator threshold may be finely adjusted by a local digital-to-analog converter (DAC).



INFN-Pavia prototype



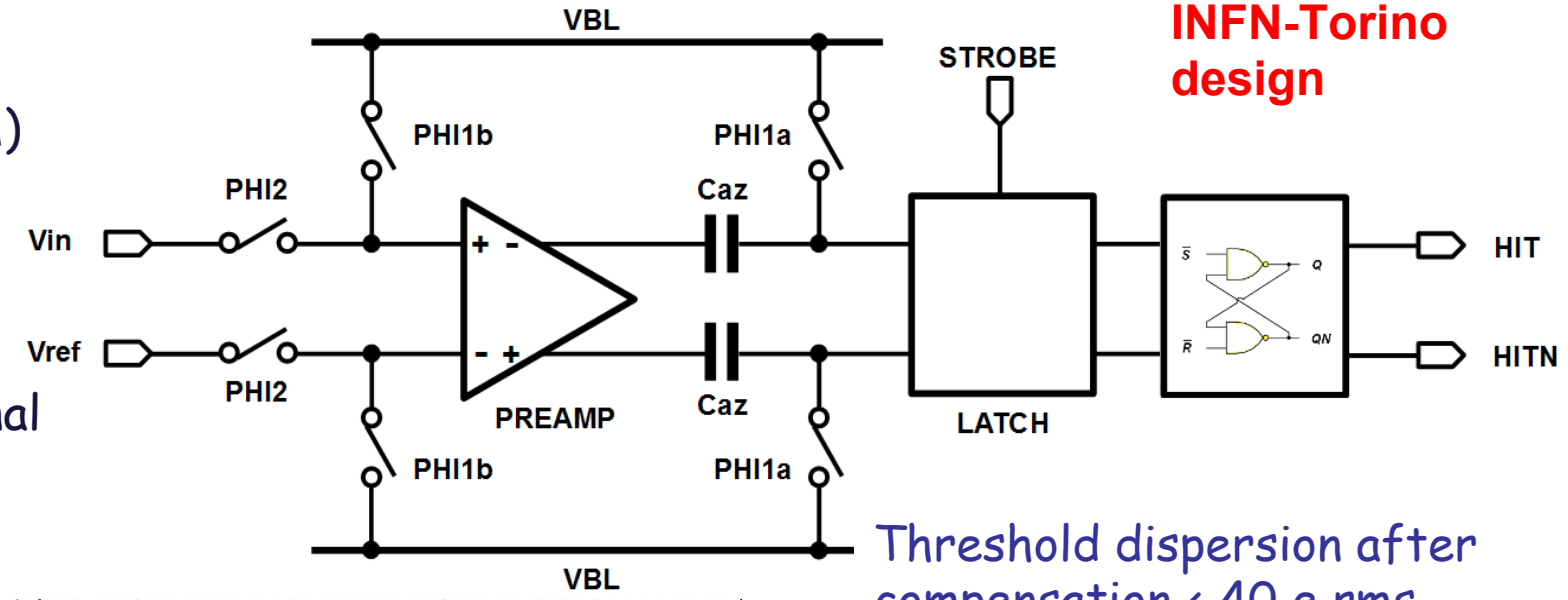
Local threshold setting through a 4-bit current steering DAC

65 nm continuous-time analog front-end channel for HL-LHC pixels

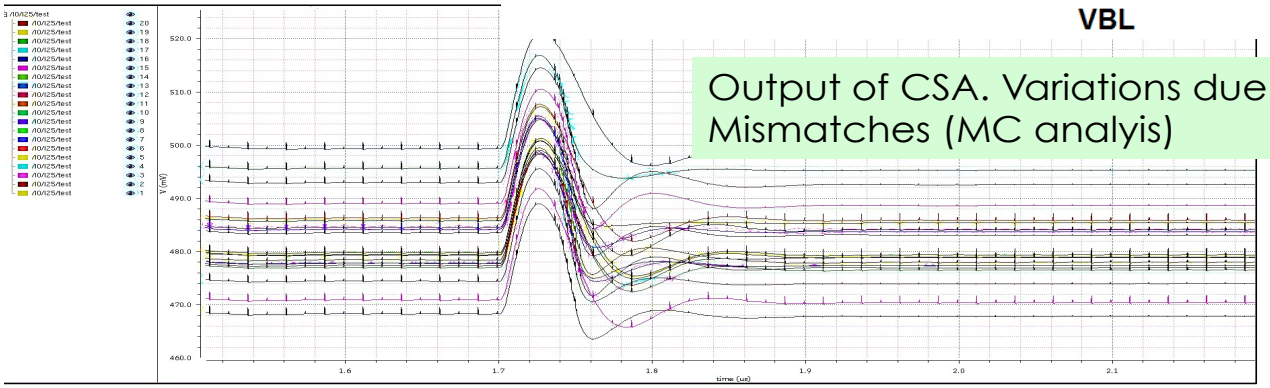
Threshold dispersion:
Before correction 380 e rms
After DAC correction 35 e rms

Synchronous discriminators

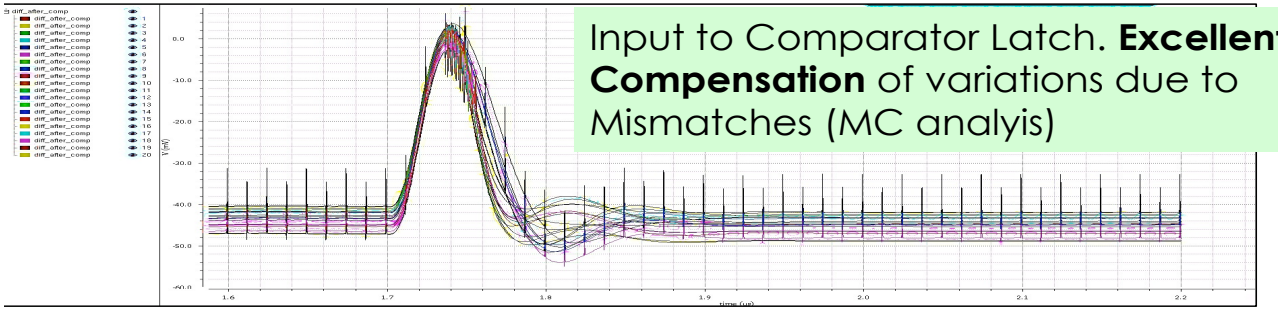
Offset (and mismatch) cancellation based on comparator autozero (store offset on a capacitor, and then substract it from signal +offset)



INFN-Torino design



Output of CSA. Variations due to Mismatches (MC analyis)



Input to Comparator Latch. **Excellent off-set Compensation** of variations due to Mismatches (MC analyis)

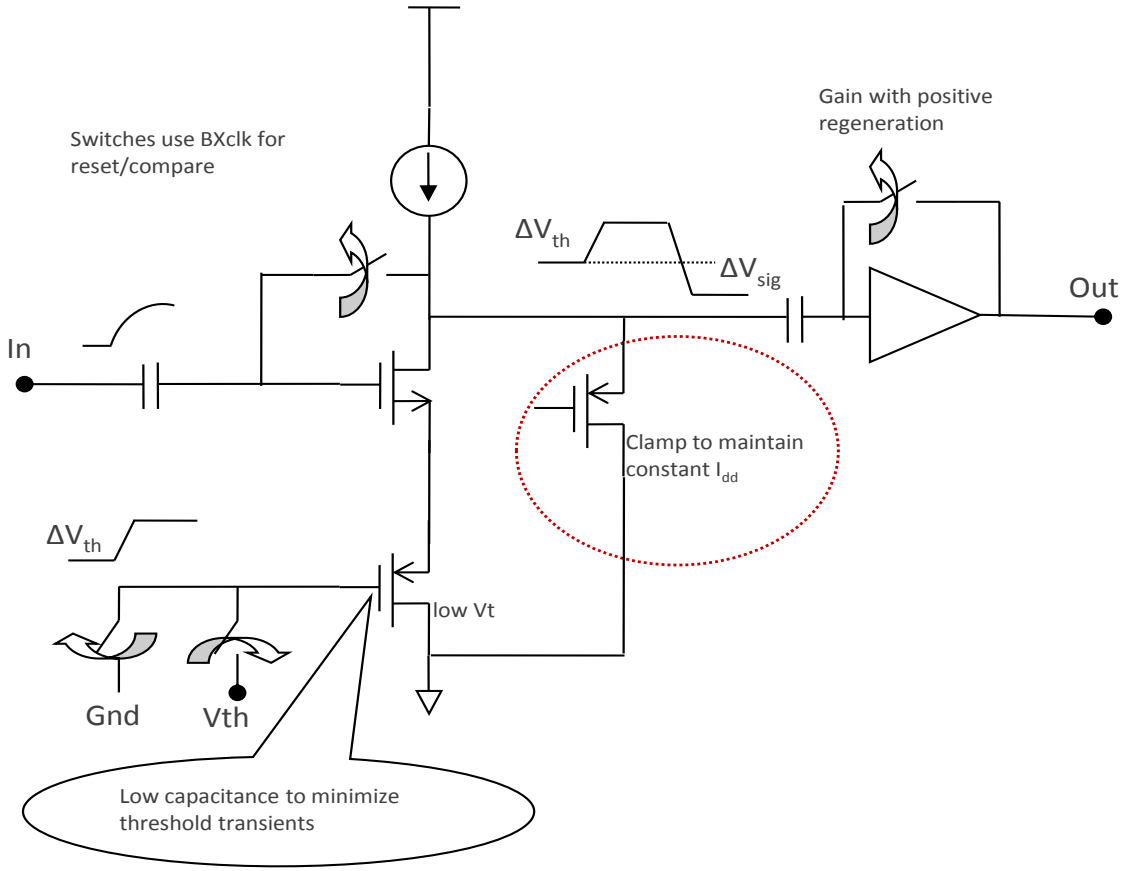
Threshold dispersion after compensation < 40 e rms

Design compatible with Fast-ToT thanks to locally generated clock. Example: for Qin = 30ke$^-$, ToT = 250ns

ENC = 110 e rms @ C_D = 100 fF

A fast and compact synchronous discriminator

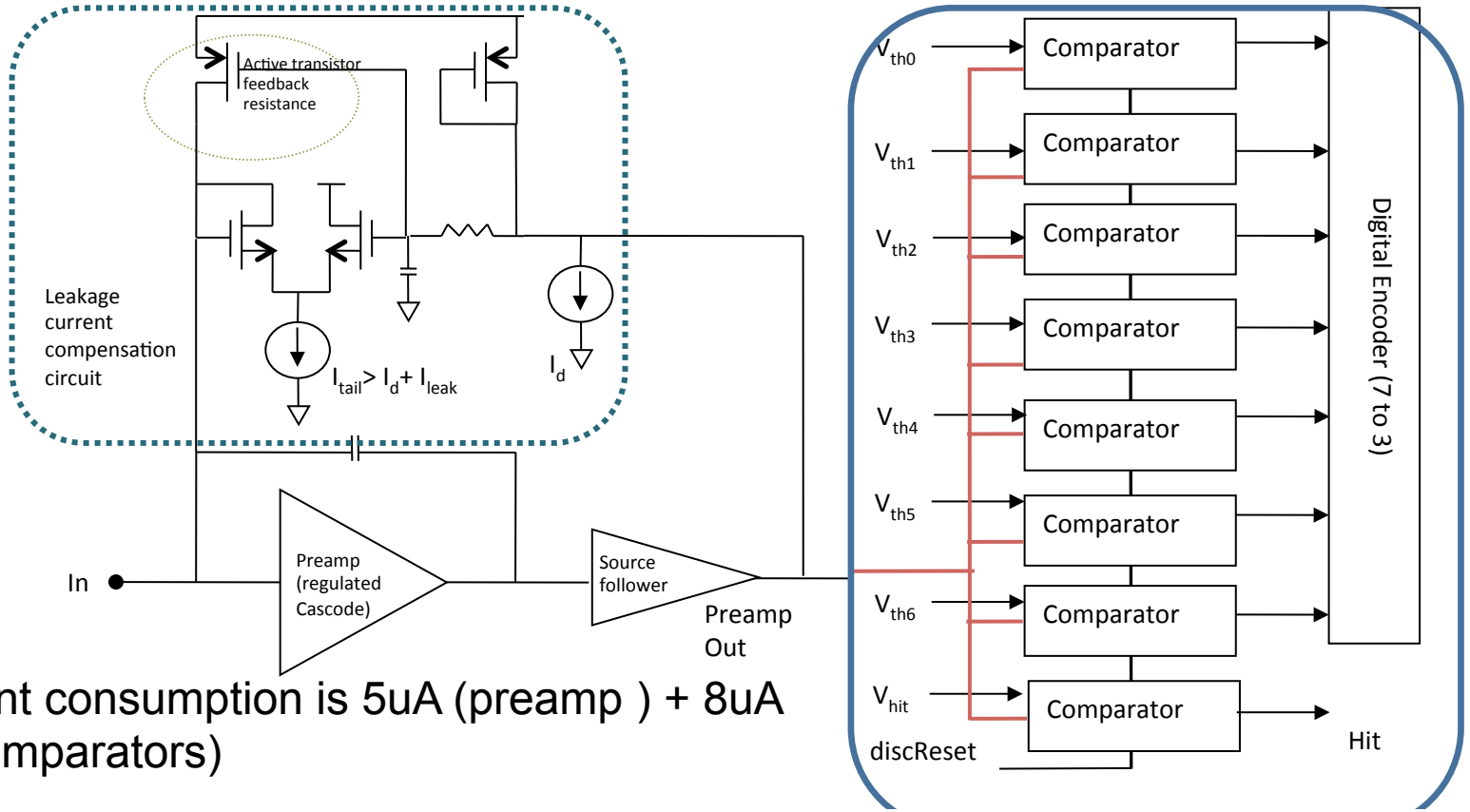
Fermilab design in 130 nm CMOS, being converted to 65 nm in a collaborative Fermilab-INFN effort



- Compact, single-ended architecture
- Correlated double sampling:
  - Auto-zeroed
  - Increased pileup immunity
  - Signal filtering
  - No need for trimming DACs
- 12.5ns reset phase; 12.5ns active comparison
- Low-power, fast, insensitive to corners
- Additional gain and positive regeneration in 2nd stage.
- BXclk must be well controlled across a large chip
- 1.5µW/comparator

Zero FE dead time (can latch hits in adjacent crossings)

Is a Flash ADC affordable in the pixel cell?



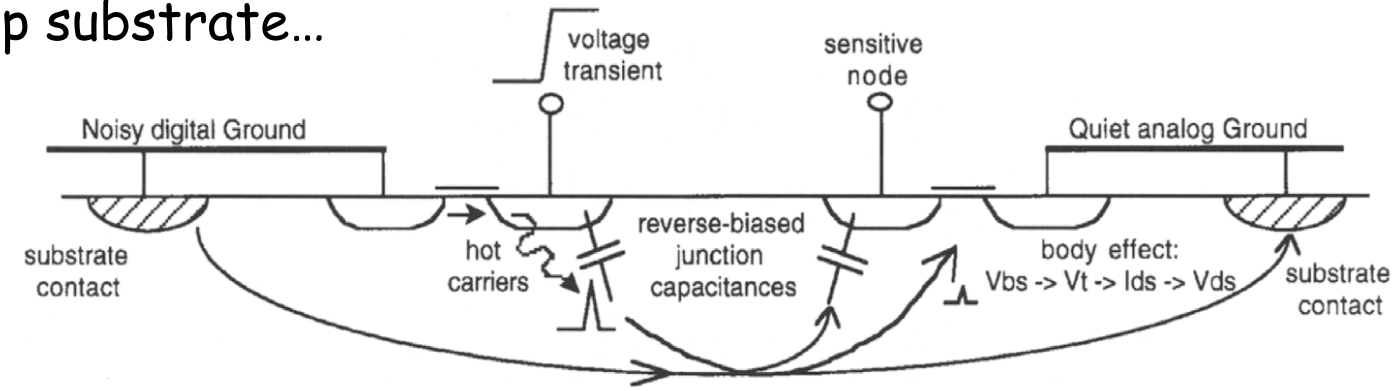
- Current consumption is 5uA (preamp) + 8uA (all comparators)

- **Translating from 130 nm to 65 nm (Fermilab-INFN Pavia collaboration)**, improves speed and threshold dispersion (35 e rms) performance

- The Flash ADC may be attractive in 65 nm, provided that a 3-bit charge resolution is enough for physics needs. Present specification is ≥ 5 bits, achievable with a ToT counter

Digital-to-analog interferences

- There are many ways by which interferences can propagate through the chip substrate…



- These effects can be mitigated by using differential, low-level digital signals (LVDS), by isolation techniques, by layout tricks (separated analog and digital power and signal routing) …

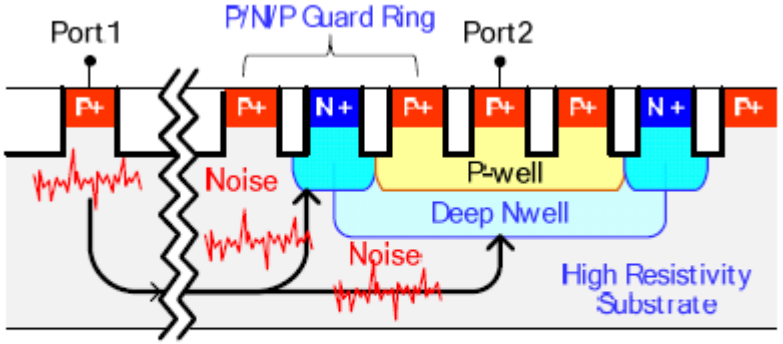


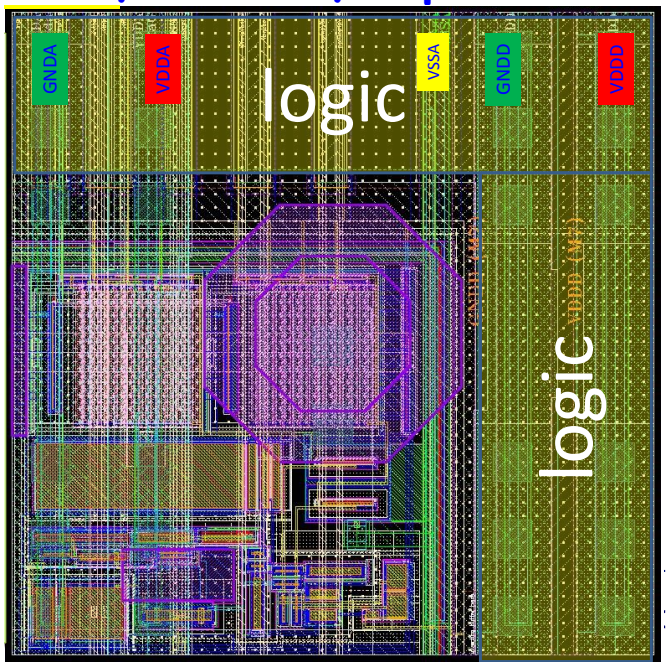
Figure 6: Illustration of the three main isolation techniques; PNP guard ring, deep NWELL and high resitivity substrate.

I. A. Young (Intel), "Analog mixed –signal circuits in advanced nanoscale CMOS technologies for microprocessors and SoC", 2010 ESSCIRC

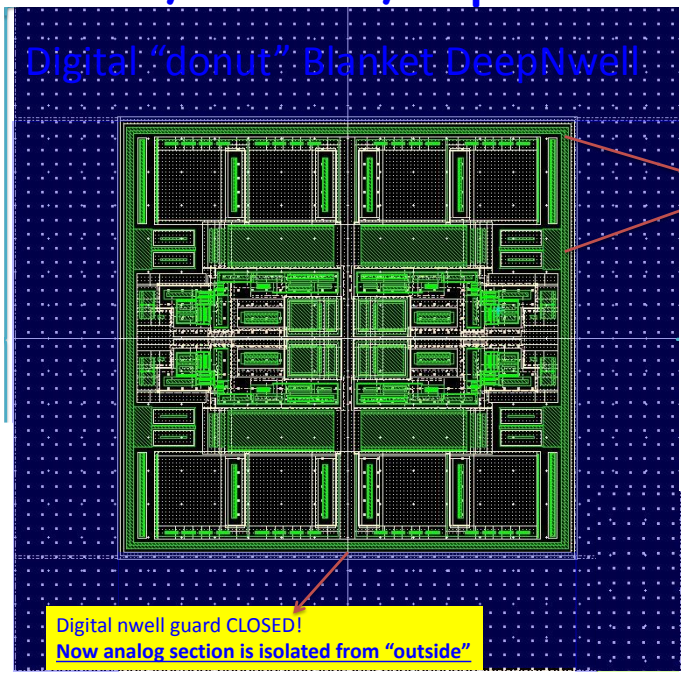
Pixel analog front-end inside the large RD53 mixed-signal (mostly digital) integrated circuit

- In modern pixel readout chips, the analog front-end cell is embedded in an extremely complex microelectronic system, where analog and digital circuits coexist in the same small readout cell
- A correct layout is crucial to avoid digital interferences in the low-noise analog front-end; immunity to disturbances on analog supply lines ("PSRR") is also essential
- The "analog island" concept (A.Mekkaoui, LBNL)

50 μm x 50 μm pixel cell



Four 50 μm x 50 μm pixel cells



Plans of RD53

- The challenge of analog design in 65 nm CMOS for pixel readout at the HL-LHC is being tackled by our community of microelectronic designers in a collaborative way (RD53, the INFN project CHIPIX65)
- Current goal: developing/qualifying technology, tools, architecture and building blocks required to design next generation pixel chips for very high rates and radiation
- First round of submissions in 2014, first prototypes currently being characterized, other submissions in Spring and Fall 2015
- These prototypes will allow us to evaluate the best solutions for the architecture of the analog front-end

➔ **Full pixel chip prototype submission in 2016**

Pixel analog front-end for particle trackers versus front-end for X-ray imaging

- For **tracking**, the main specifications of the analog front-end concern the threshold setting (maximize efficiency, minimize noise occupancy), the power dissipation (requirements on delivery of power and cooling to the chip) and the speed (latch hit with the correct time stamp)

- For **X-ray imaging at FELs**, essential parameters are the analog resolution (very low electronic noise for single photon detection), the dynamic range (capability of handling a large number of photons; large number of ADC bits, with a fast conversion time), the linearity (in the lower end of the dynamic range)

- Next slides discuss how 65 nm CMOS may be a tool to achieve the required analog performance in a 100 μm x 100 μm readout cell for an X-ray hybrid pixel detector for X-FELs ➔ the **INFN PIXFEL project**

INFN PixFEL project profile

- Goal of the project: high performance X-ray imaging instrumentation for the experiments at the next generation of free electron laser facilities
  - Small pitch active edge silicon pixel sensors
  - **65 nm CMOS technology for pixel readout electronics**
  - 3D integration techniques for the vertical interconnection of sensor and readout electronics layers

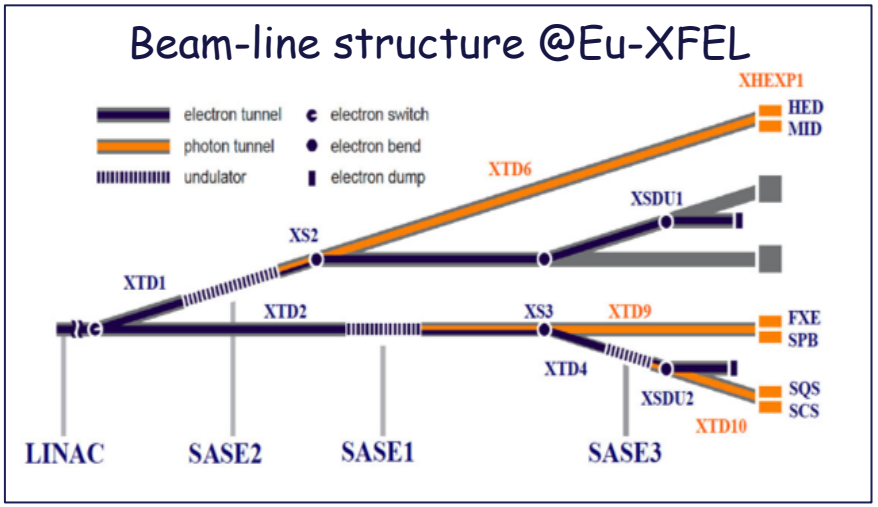
- Participating INFN groups
  - INFN Pavia: Lodovico Ratti, Massimo Manghisoni, Daniele Comotti, Francesco De Canio, Lorenzo Fabris, Marco Grassi, Piero Malcovati, Valerio Re, Gianluca Traversi
  - INFN Pisa: Giuliana Rizzo, Giovanni Batignani, Stefano Bettarini, Giulia Casarosa, Francesco Forti, Marcello Giorgi, Eugenio Paoloni, Fabio Morsani
  - INFN Trento: Lucio Pancheri, Gian-Franco Dalla Betta, Giorgio Fontana, Ekaterina Panina, Giovanni Verzellesi, Xu Hesong

Beam-line and beam-time structure at X-ray FELs

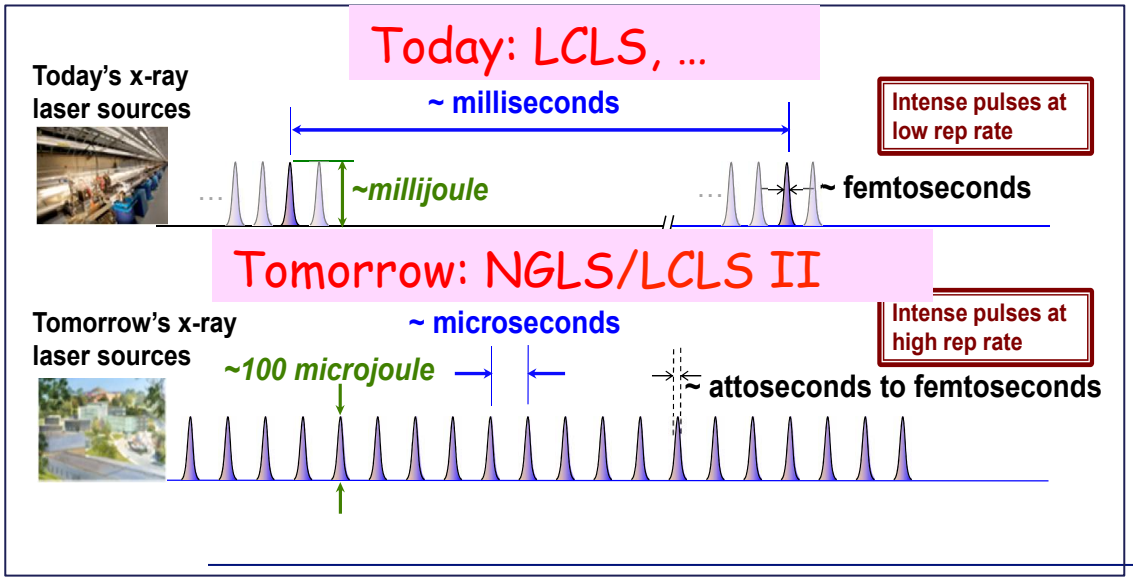
Beam lines with different photon energies available at each facility

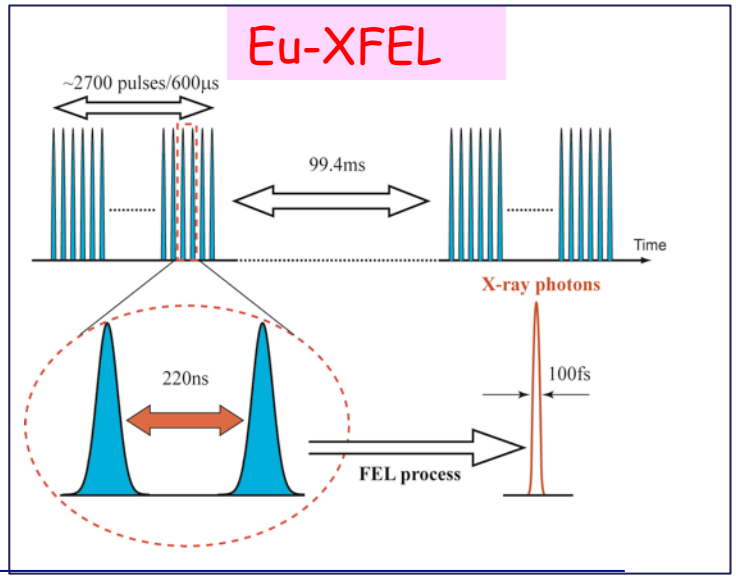
Very different beam structure from one FEL facility to the other

Each pulse is always very short
LCLS: continuous operation @ 120Hz
XFEL: 220ns spacing, with time to readout
Future (i.e. LCLS II): continuous 1MHz spacing



Most challenging for detectors are Eu-XFEL & LCLS II, taken as target for PixFEL

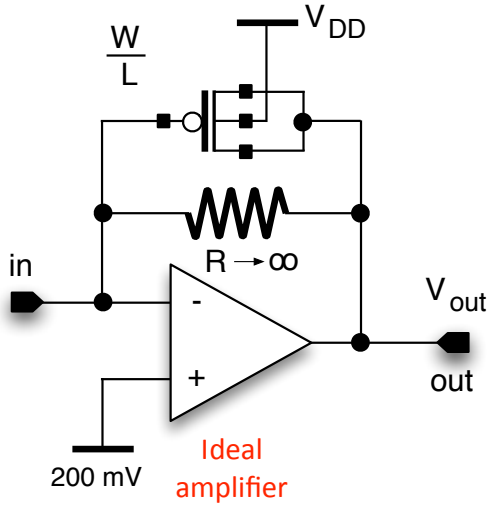


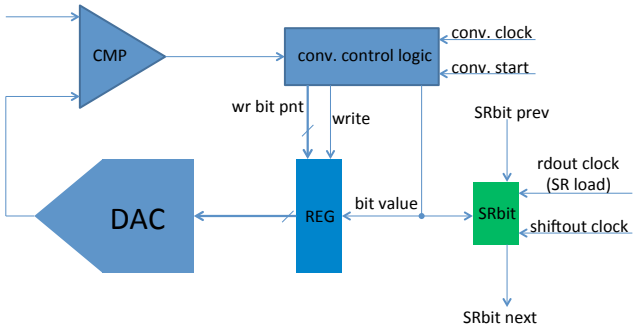


PixFEL detector design and technology

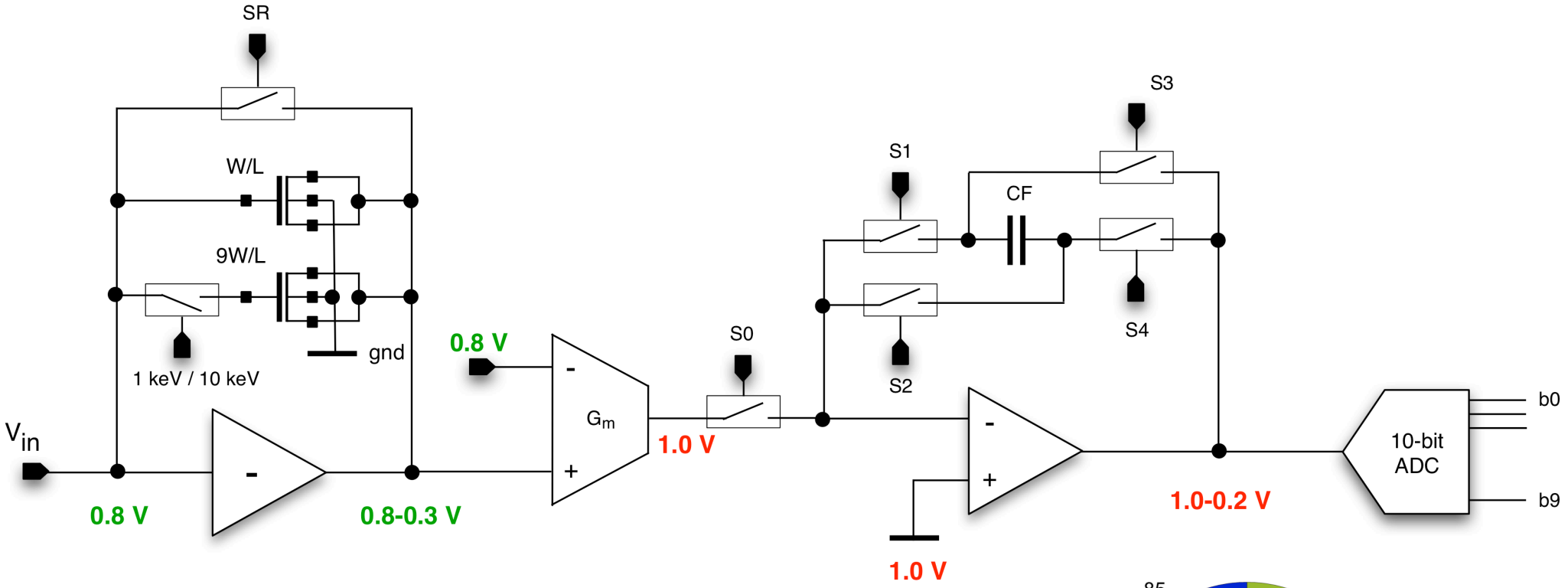
Multilayer device: active edge thick pixel sensor, two tiers CMOS readout chip (analog+digital/memory), fabricated in 65 nm CMOS, to increase memory and functionality in a small pixel pitch of 100 μm.

- Wide dynamic range, 1-10^4:
  → Preamplifier with gain compression
- A/D conversion in 200 ns
  → Successive approximation 10 bit ADC
- Pitch: 100 μm
  → 65 nm CMOS readout chip to increase functional density
- Readout and memory: 1k frame depth
  → Use 3D integration to increase depth by adding a memory layer

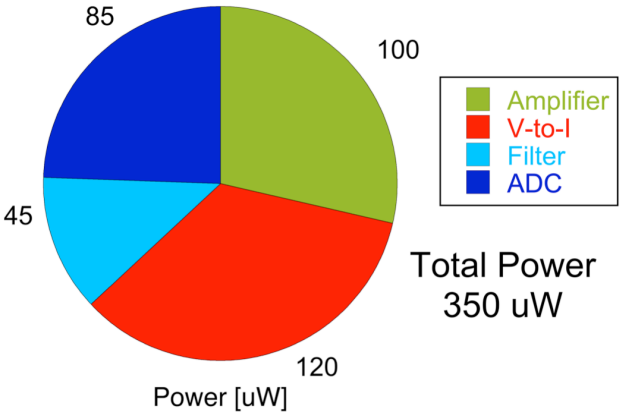




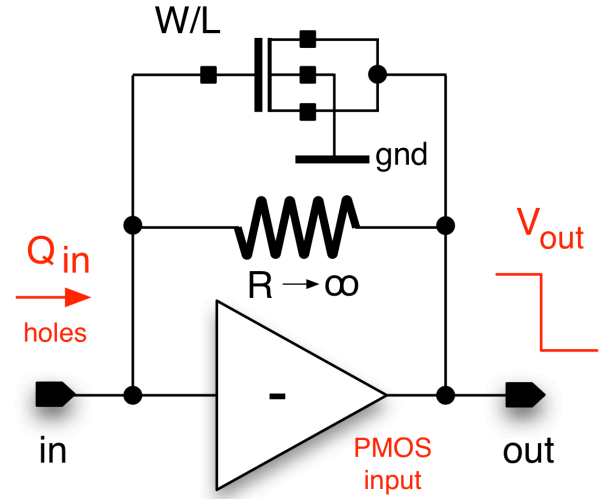
Readout channel

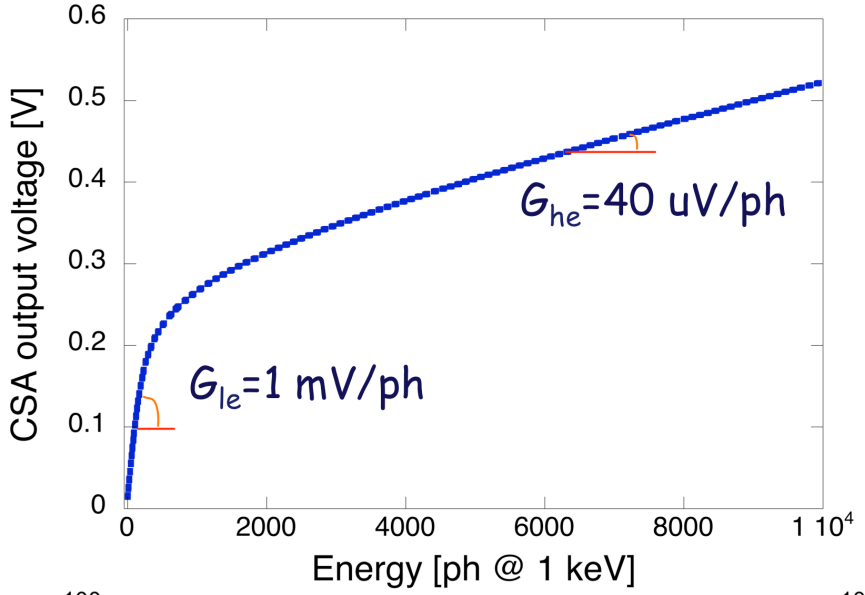


- Charge sensitive amplifier - dynamic signal compression
- Transconductor - voltage to current conversion
- Time invariant filter – changeable gain and integration time
- Analog-to-digital conversion - 10 bit SAR ADC
- Technology – 65 nm CMOS

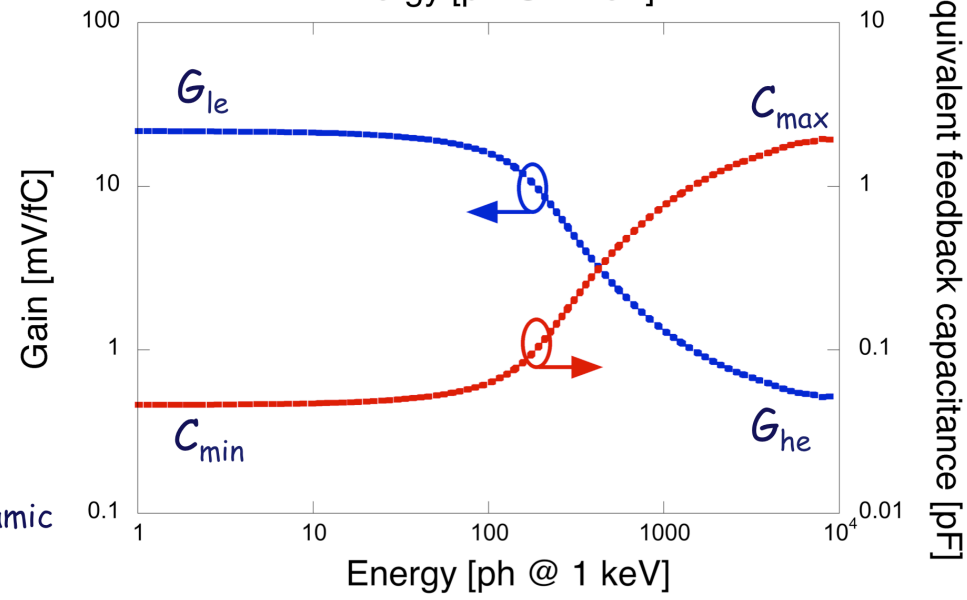


Dynamic compression





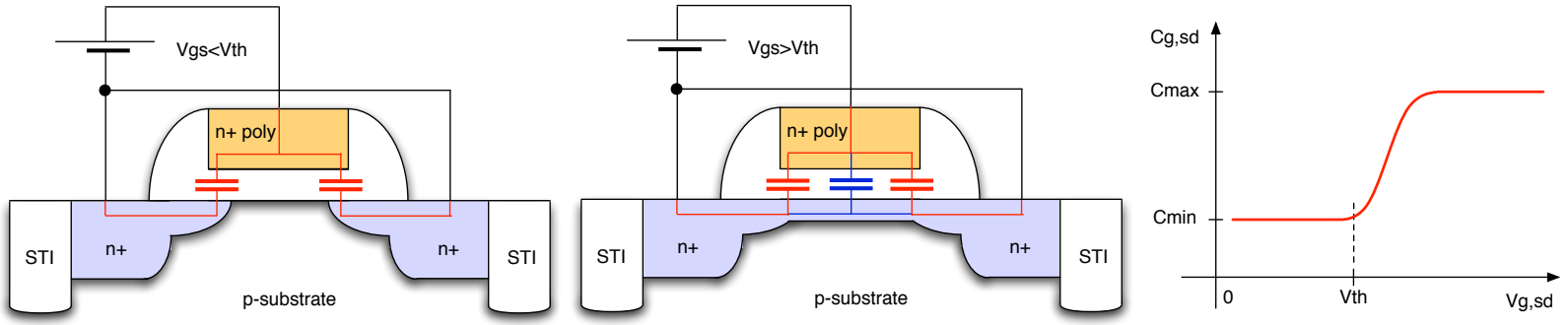
- Based on the non linear feature of a MOSFET operated in inversion mode
  - $|\Delta v_{out}| << V_{Th}$ ➔ $C_f = C_{min}$, $Gain = G_{le}$
  - $|\Delta V_{out}| >> V_{th}$ ➔ $C_f = C_{max}$, $Gain = G_{he}$
- Suitable choice of W and L to configure the gain in the low and high energy regime, under the constraint set by the preamplifier output range



D. Comotti, "Low noise readout channel with a novel dynamic signal compression for future XFEL applications", N18-2

Inversion-mode MOS capacitor

Drain and source shorted to form one capacitor terminal, the gate forms the other



- $0 < V_{G,SD} << V_{Th} \rightarrow C_{G,SD}$ is set at its minimum and it is mainly due to the overlap gate-to-source $C_{gs,ov}$ and gate-to-drain $C_{gd,ov}$ capacitances:

$$C_{min} \approx C_{gs,ov} + C_{gd,ov} = 2W\Delta LC_{ox}$$

  W = channel width, ΔL = extension of the overlap region, C_{ox} = gate oxide capacitance per unit area

- $V_{G,SD} >> V_{Th} \rightarrow C_{G,SD}$ shows a maximum value which is mainly given by the gate-to-channel C_{gc} capacitance

$$C_{max} \approx C_{gc} = WLC_{ox}.$$

Basic idea: exploit the non-linear features of MOS capacitors to dynamically change the gain of Charge Sensitive Amplifier with the input signal amplitude

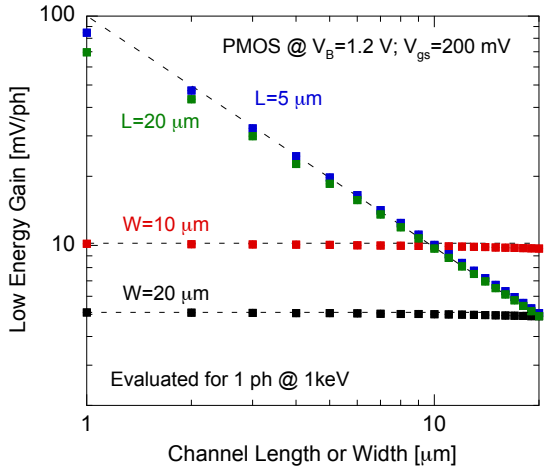
Gain setting

Low Energy Gain (G_{le}) ($E<10$ ph at 1 keV)

If $V_{out} << V_{th} \Rightarrow C_{gs} = C_{min} \approx C_{gsovl} + C_{gdovl} = 2W\Delta LC_{OX}$

$$G_{le} = 280q \frac{1}{2\Delta LC_{OX}} \frac{1}{W}$$

$\Rightarrow G_{le}$ adjusted with the MOS channel width W

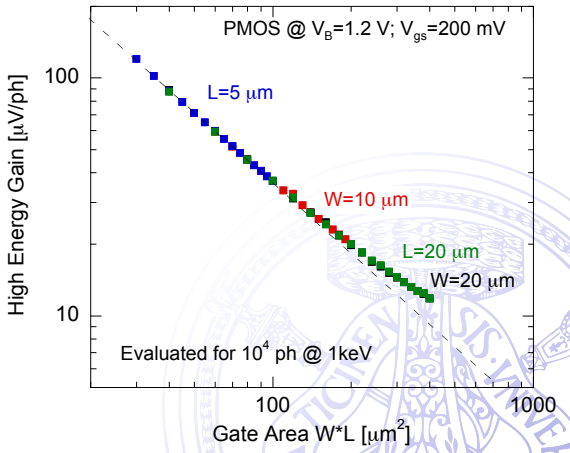


High Energy Gain (G_{he}) ($E>10^3$ ph at 1 keV)

If $V_{out} > V_{th} \Rightarrow C_{gs} = C_{max} \approx C_{gs} + C_{gd} = WLC_{OX}$

$$G_{he} = 280q \frac{1}{C_{OX}} \frac{1}{WL}$$

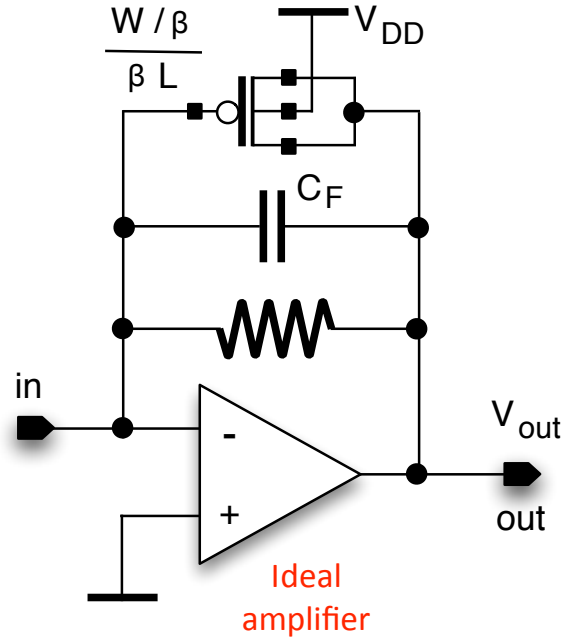
$\Rightarrow G_{he}$ adjusted with the MOS channel length L



Signal compression factor: $k = \frac{G_{le}}{G_{he}} = \frac{C_{max}}{C_{min}} \approx \frac{L}{2\Delta L} \Rightarrow$ depends on L only

Improved Low Energy gain precision

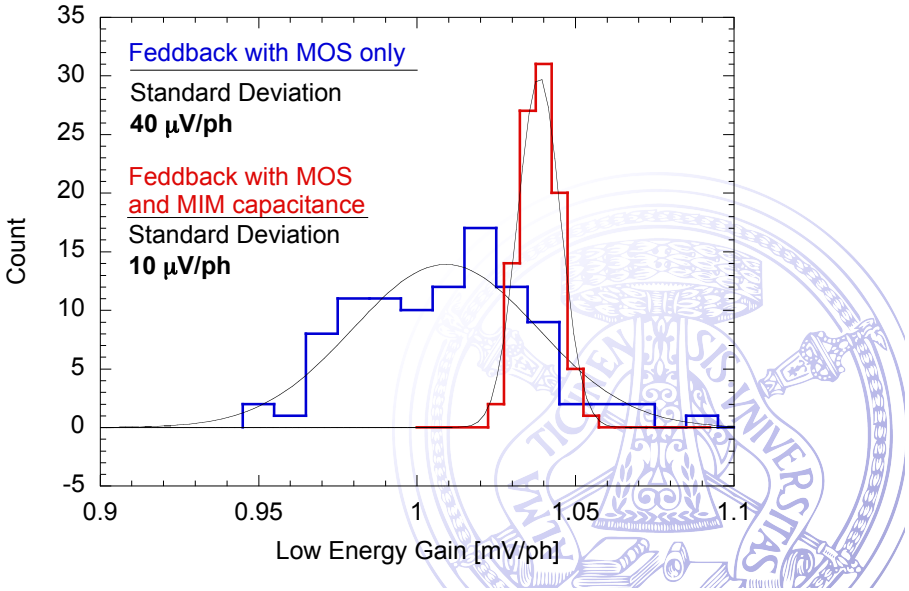
Additional capacitance C_F in parallel to the feedback MOS



$$C_F = \left(1 - \frac{1}{\beta}\right) C_{min}$$

$$W \rightarrow \frac{W}{\beta} \quad \text{and} \quad L \rightarrow \beta \cdot L$$

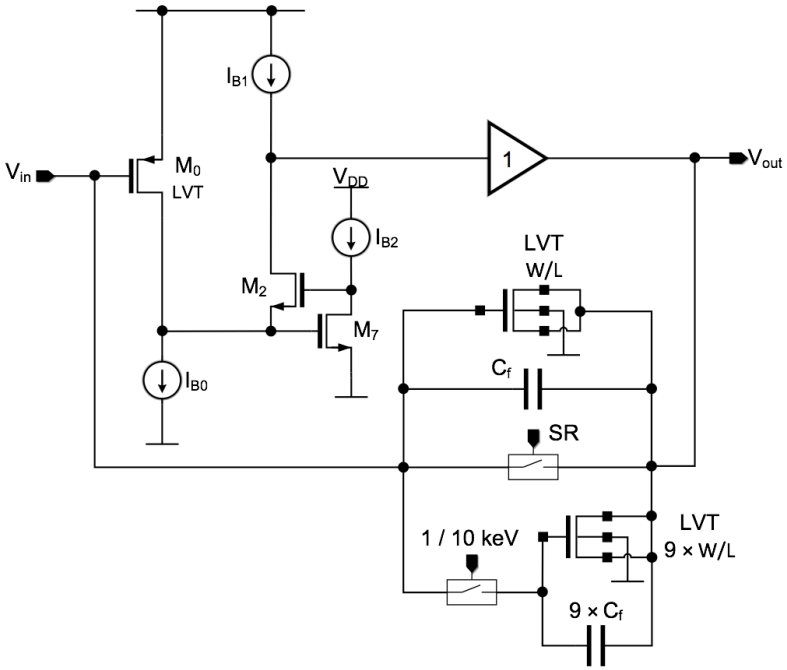
with $\beta > 1$ (the higher the value of β, the lower the dispersion)



Improved feedback for β=5

- C_F=34 fF MIM cap
- W=20 μm and L=5 μm

CSA with signal compression - Overview



Input signal and gain:

- 10^4 photons at either 1 keV or 10 keV
- Low energy gain: $g_{le} \approx 1\,{}^{mV}/_{\mathrm{ph}}$
- 500 mV output range with $V_{kink} \approx 250$ mV $\Rightarrow$ High energy gain: $\approx 25\,{}^{\mu V}/_{\mathrm{ph}}$

Feedback MOS

- NMOS ${}^{W}/_{L}$=40/4 (1keV and 10keV)
- NMOS ${}^{W}/_{L}$=9$\times$40/4 (10keV)

Forward gain stage

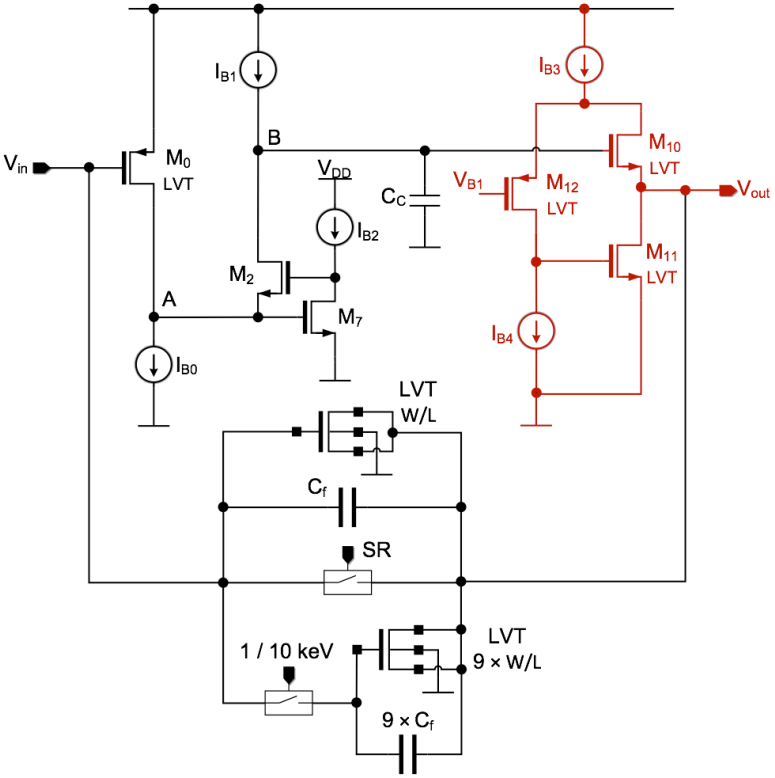
- Active folded cascode (with local feedback) loaded by an active load
- Input device PMOS W/L=40/0.15

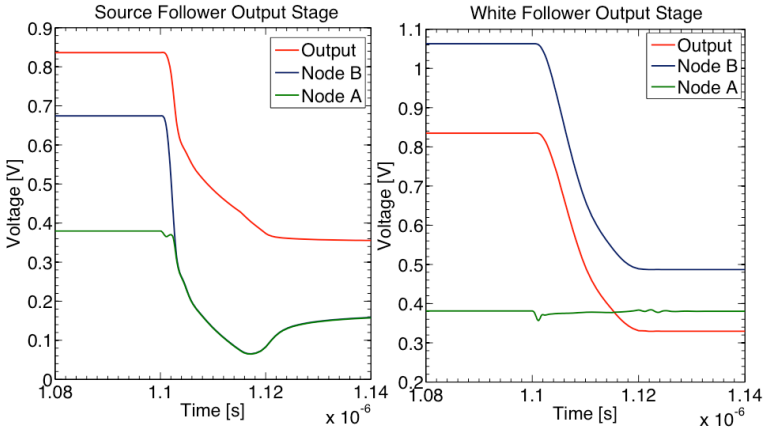
C_{ef} ranges between about 40 fF (1 ph @ 1 keV) and 20 pF (10^4 ph @ 10 keV) $\Rightarrow$ key issues:

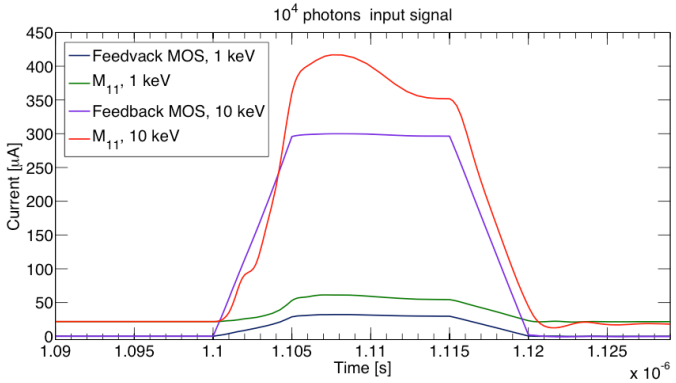
- High peaks of current during the signal settling $\Rightarrow$ driving capability of the output stage
- Fast charge restoration at higher energies
- Phase margin variation

CSA output stage

- Very high peaks of current (up to 400 μA) to be sink by the output stage
- Standard PMOS based source follower not suitable
- $\Rightarrow$ improved output stage based on the White follower [3] configuration







[3] Pullia, A.; Zocca, F., "Fast low-impedance output stage for CMOS charge preamplifiers able to work at cryogenic temperatures," NSS/MIC, 2009 IEEE

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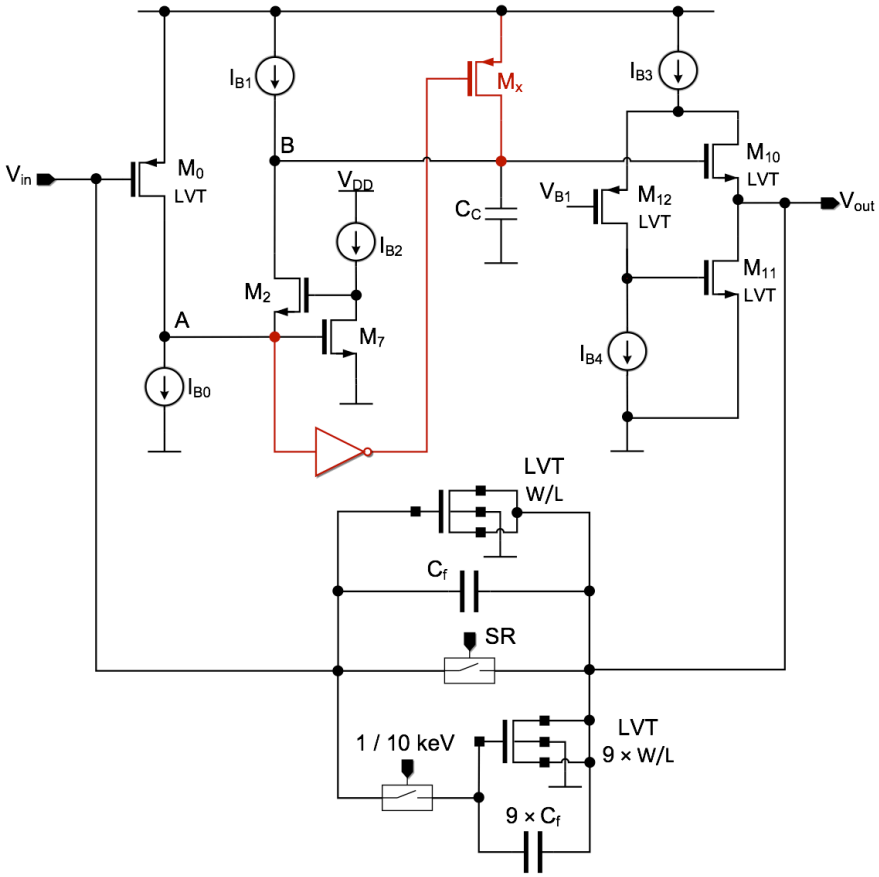
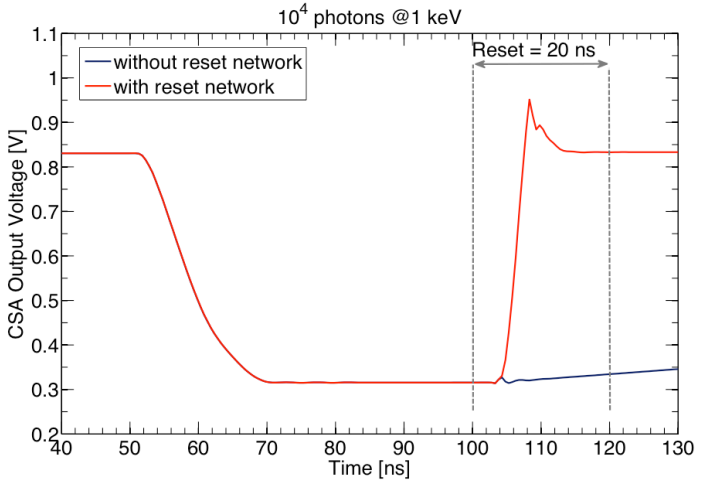
CSA Reset

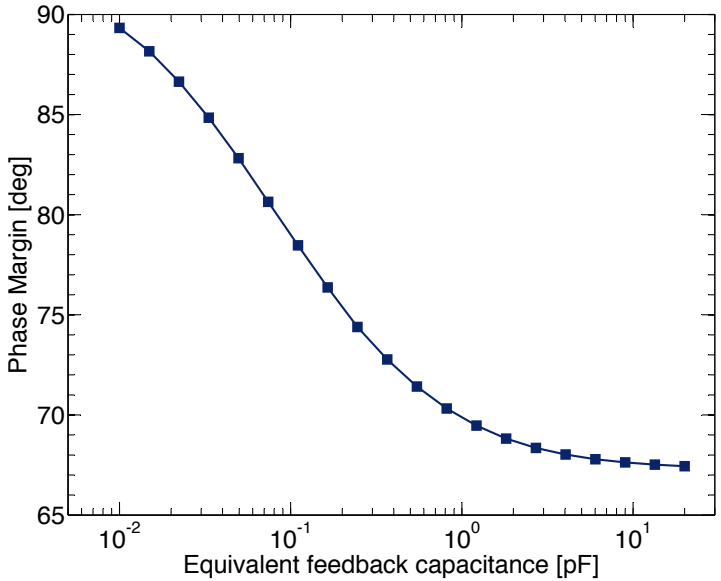


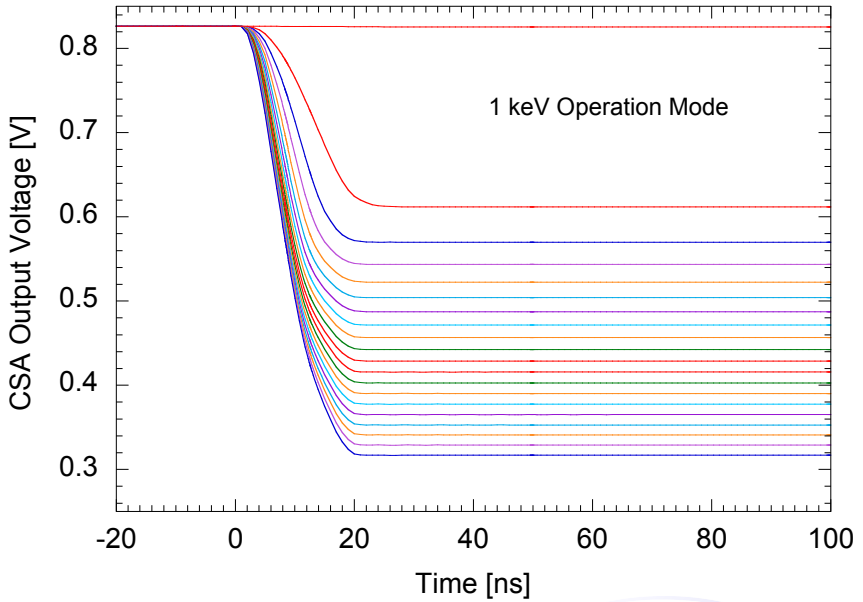
Reset phase:

- Node B slew rate limited by I_{B1}
- $\Rightarrow$ M_0 current increases $\Rightarrow$ Voltage at node A approaches V_{DD}
- $\Rightarrow$ Additional reset network (in red) to speed up the charge of node B



CSA features and transient response

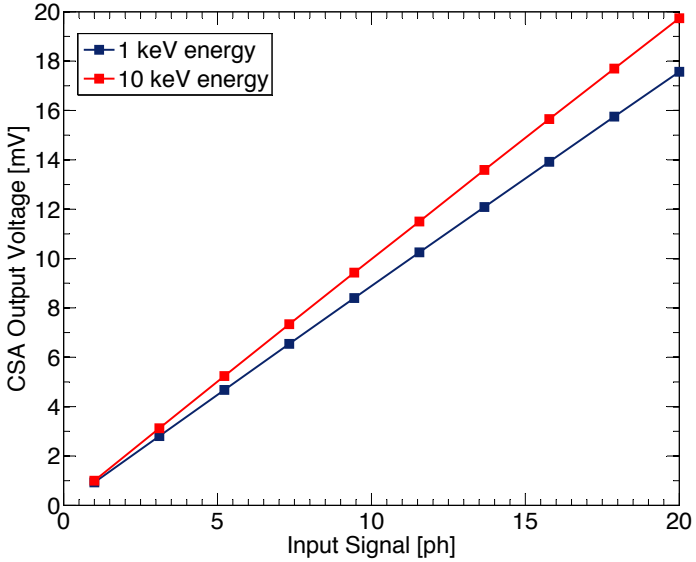


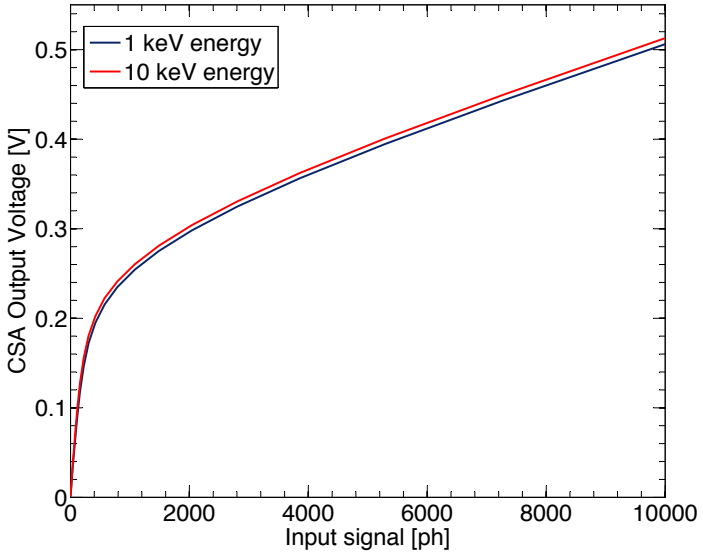


Amplifier main features	
Open Loop DC Gain	60 dB
Open Loop GBP	140 MHz
Phase Margin (Cef=10pF)	70 deg
Power Consumption	90 μW

- Fall time: $t_f \leq 20$ ns for a detector signal collected in 15 ns
- Compatible with the 4.5 MHz burst mode operation of the Eu-XFEL

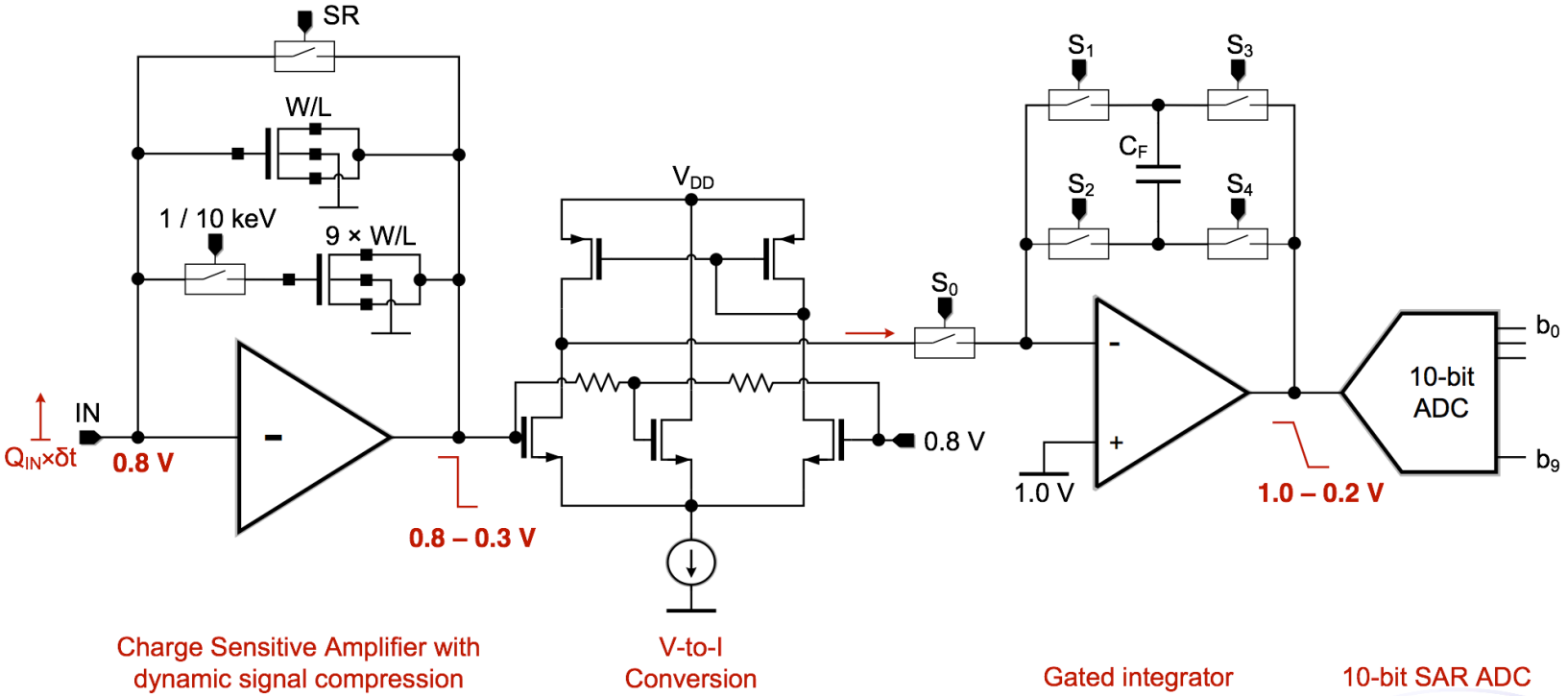
CSA dynamic range





- Low energy gain: $G_{le} \approx 1.0$ mV/ph
- Linearity: Non linearity lower than 0.06 ph in the first 20 photons range
- High energy gain: $G_{he} \approx 25$ μV/ph
- Compression factor: $k \approx 40$
- Dynamic range: the CSA covers the full dynamic range of 10^4 photons in about 500 mV

PixFEL readout channel

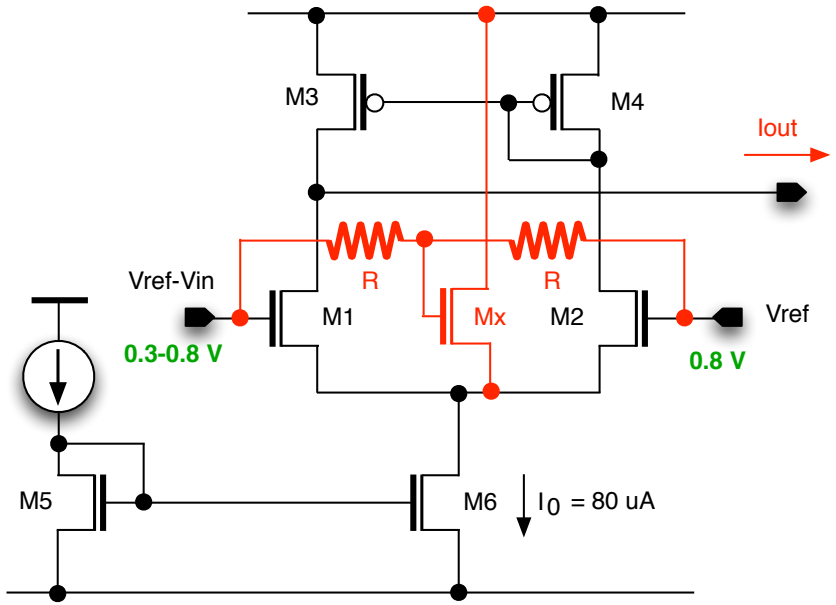


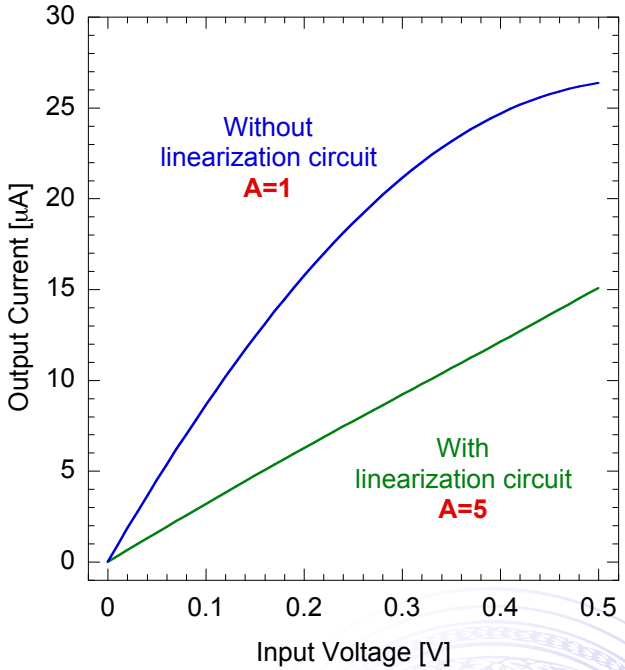
- Charge-sensitive preamplifier with dynamic signal compression
- Transconductor for voltage-to-current conversion
- Time-variant filter with integration time selection options, featuring a trapezoidal weighting function[2]
- Analog-to-Digital conversion by means of a 10 bit SAR ADC

[2] L. Bombelli, C. Fiorini, S. Facchinetti, M. Porro, G. De Vita, "A fast current readout strategy for the XFEL DePFET detector", *Nucl. Instr. Meth.*, *NIM*, vol. 624, pp. 360-366, 2010.

Transconductor for V-to-I conversion

Wide input range (0.5 V) ⇒ additional circuit (in red) to linearize the characteristic



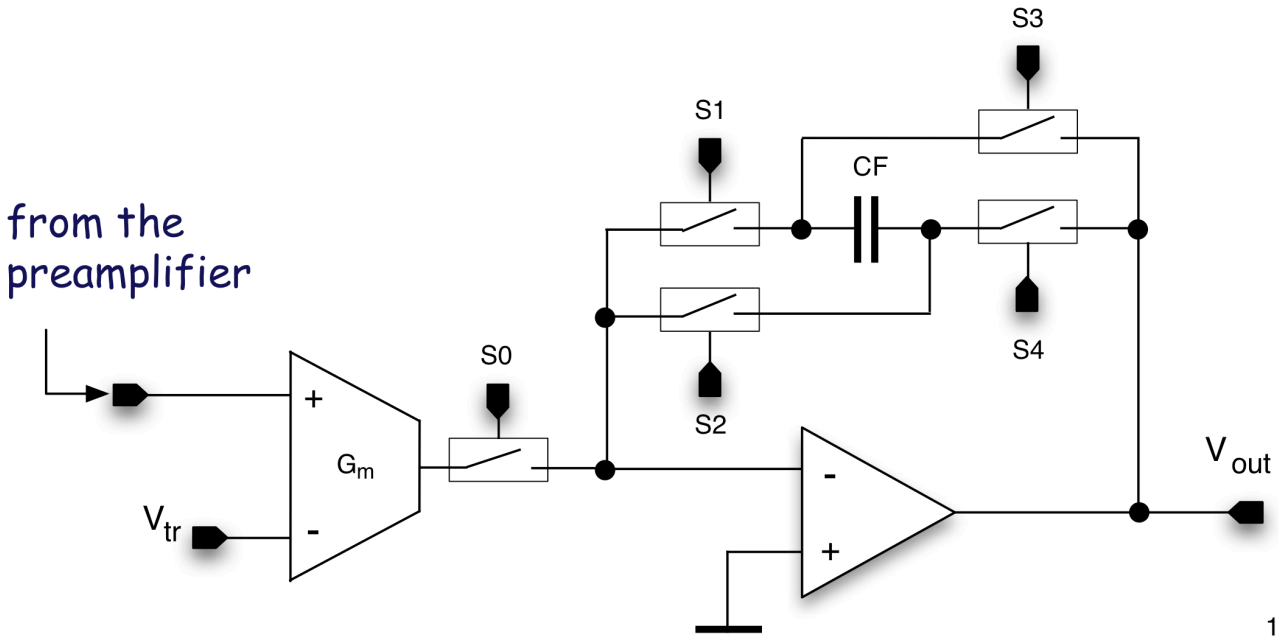


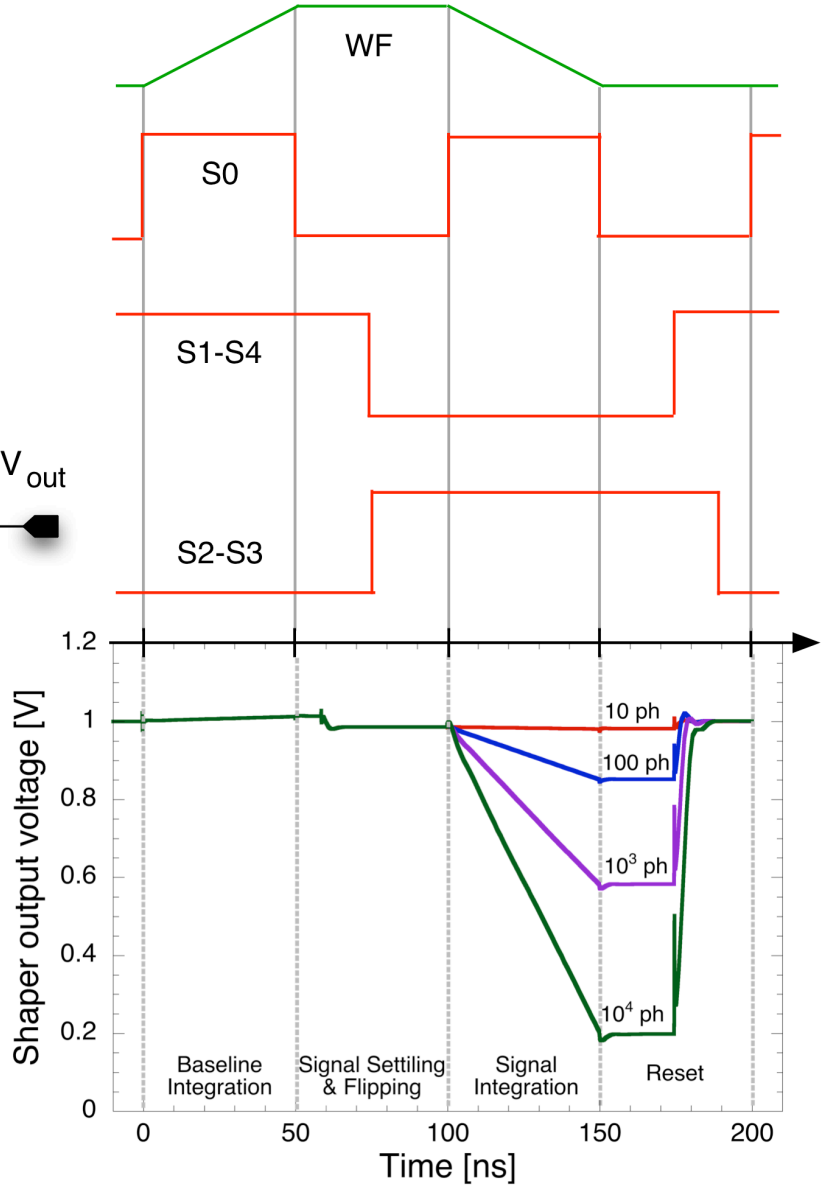
$$I_{out} = \frac{\sqrt{2\beta_{1,2} I_0}}{A} V_{in} \sqrt{1 - \frac{\beta_{1,2} V_{in}^2}{2 I_0}} \quad \text{with} \quad A = \sqrt{1 + \frac{\beta_X}{2\beta_{1,2}}}$$

where $\beta_i = \frac{1}{2} \mu_0 C_{ox} \frac{W_i}{L_i}$

V-to-I main features	
Gain	30 µA/V
Power	120 µW

Flip capacitor filter





- Flip capacitor filter (L. Bombelli et al., NIMA, vol. 624, pp. 360-366, 2010)
  - events with a known repetition rate → time-variant shaping
  - trapezoidal weighting function by feedback capacitor flipping
  - performs correlated double sampling (CDS)

Noise and Signal-to-Noise Ratio

Integration time = 55 ns

C_T = 240 fF
(detector, strays, preamplifier input capacitance)

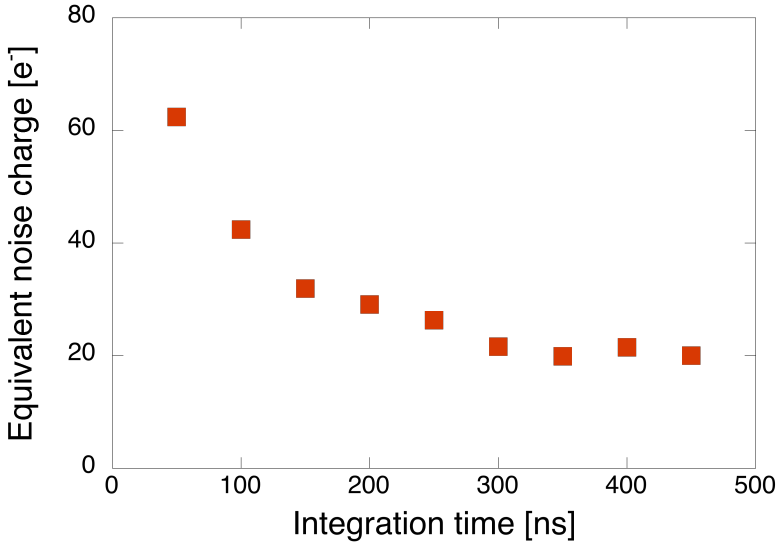
ENC contribution by the charge sensitive amplifier = 50 e rms
(with a slope of 156 e /pF)

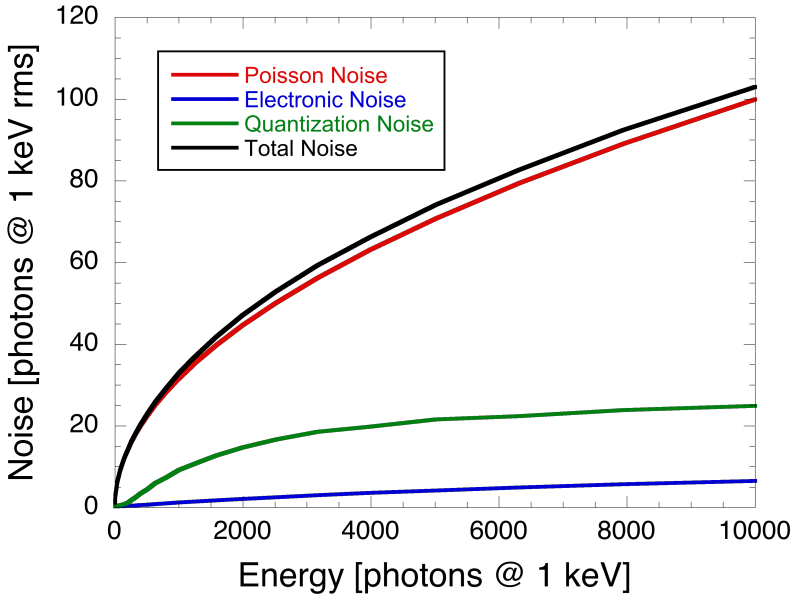
SNR = 5.6
compatible with single photon resolution at 1 keV, considering that 1 photon at 1 keV generates a charge of 277 electrons.

Noise analysis

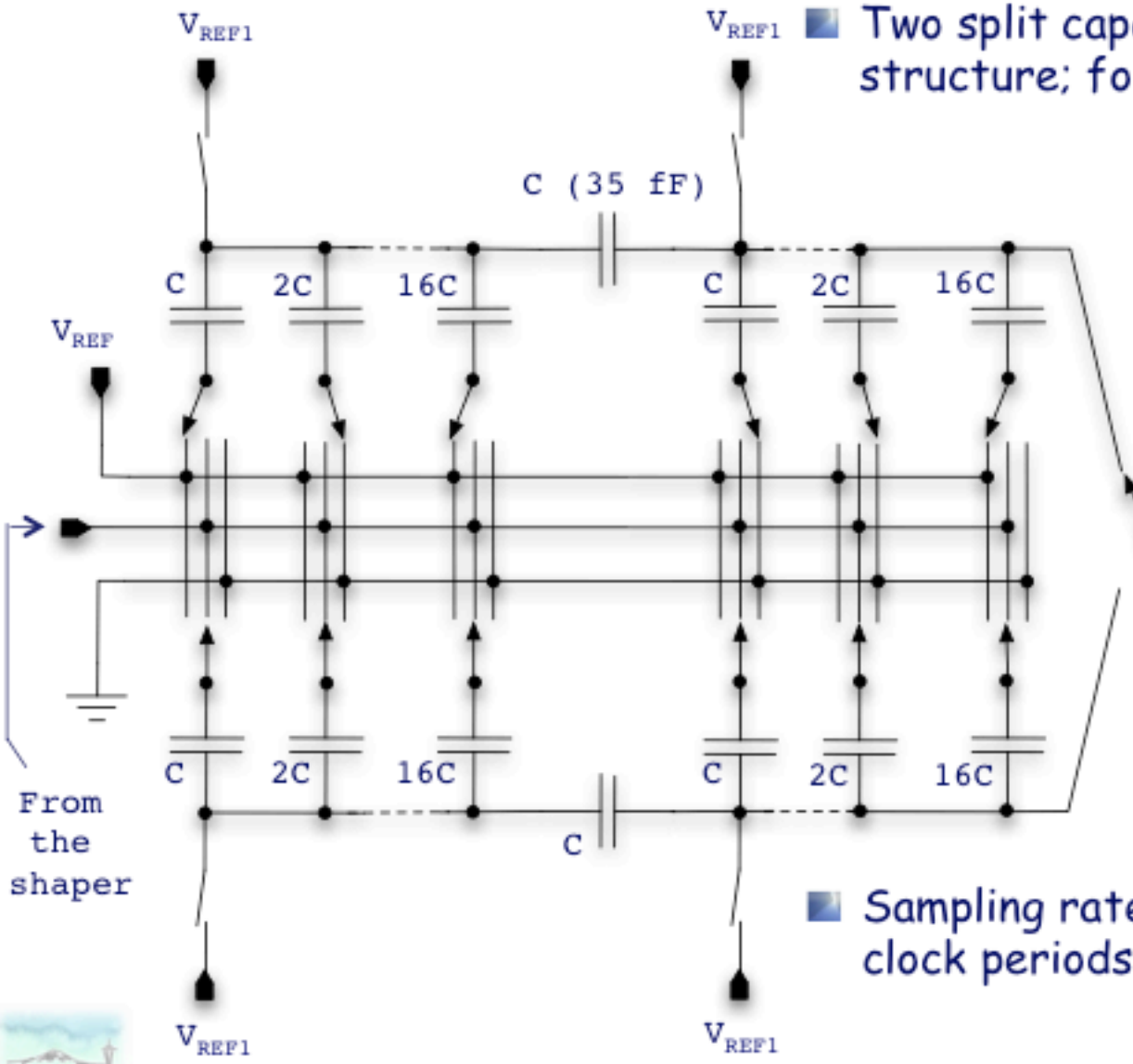
- Electronic noise
  - due to the analog front-end
  - increases with increasing signal (the feedback capacitance increases)
  - ENC=60 e^- rms @ τ=50 ns
- Quantization noise
  - due to the ADC
  - negligible for small number of photons
  - #photons per bin/sqrt(12) for large numbers of photons
- Poisson distributed noise of the photon generation process

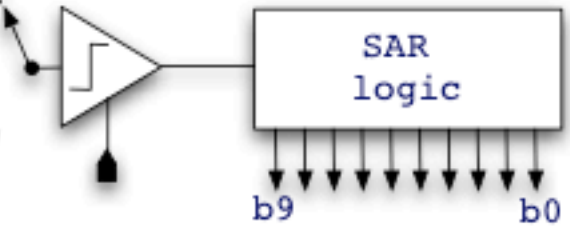
System performance is dominated by Poisson noise





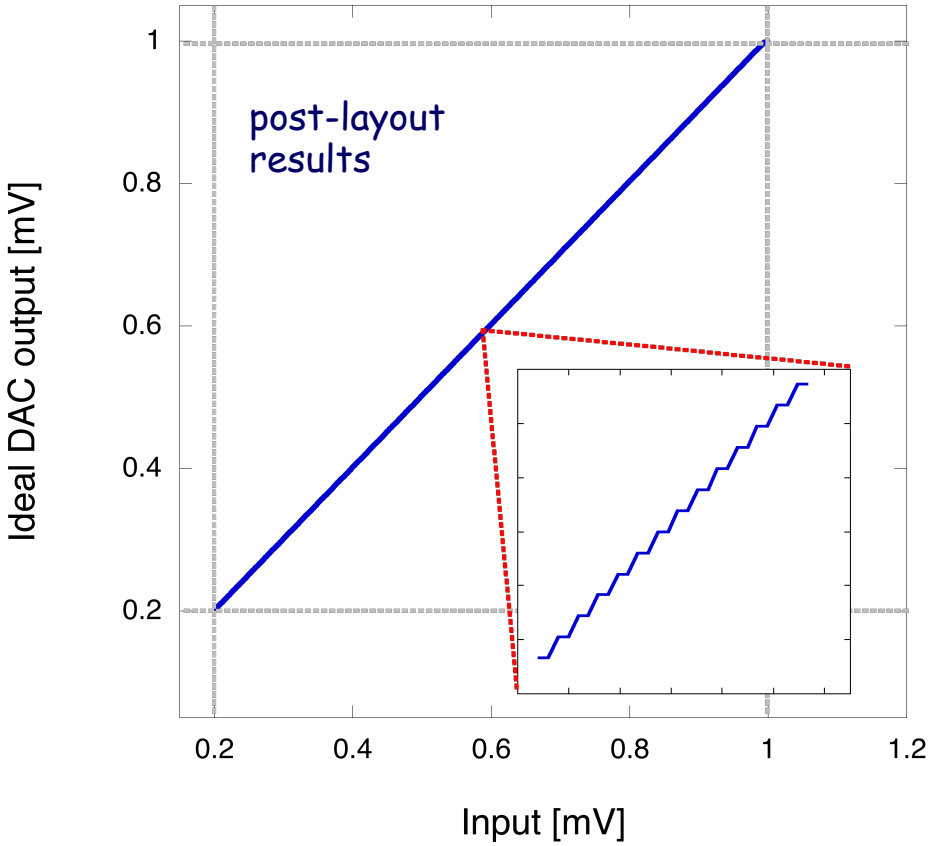
10 bit time-interleaved SAR ADC





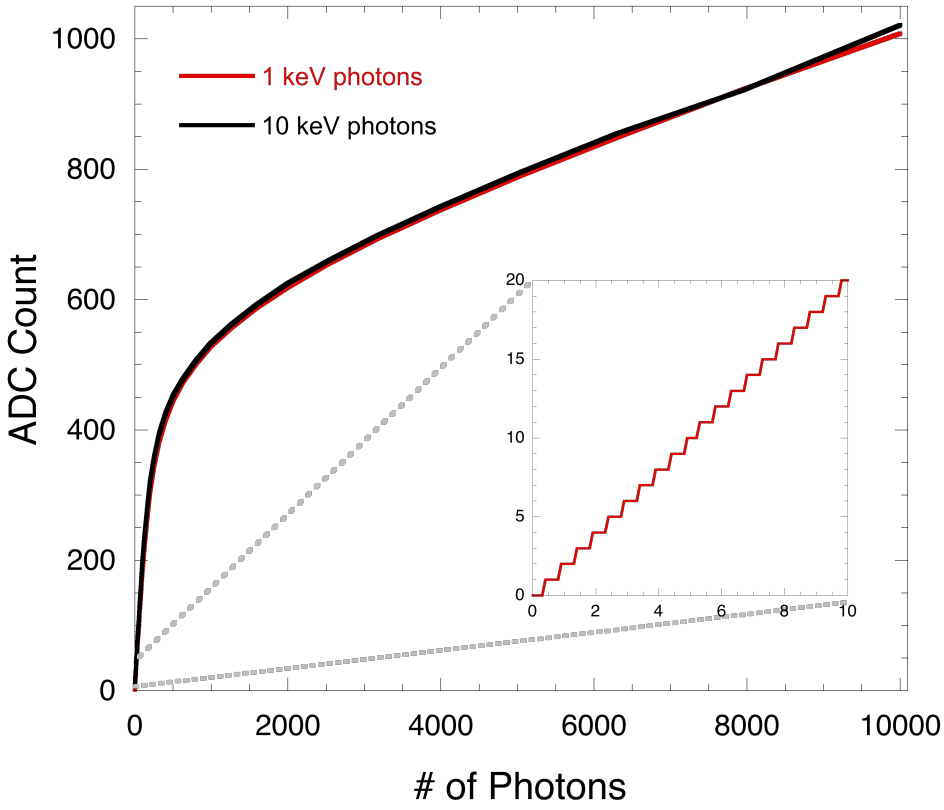
- Two split capacitive DACs in a time-interleaved structure; for each DAC
  - pre-charge during one sampling period
  - conversion during the subsequent period
- No need for a dedicated stage to charge the DAC (~2.3 pF)
- Avoid large current peaks due to fast capacitance charge
- Sampling rate of 5 MHz, 10 bit conversion in 11 clock periods (~18 ns)

ADC performance



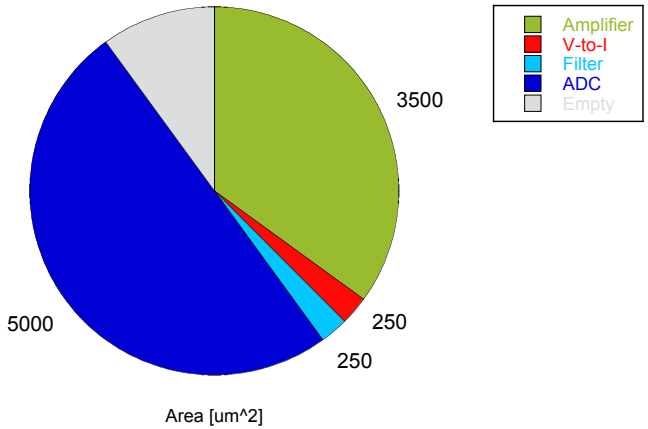
- SNR=60dB (ENOB=9.6), offset=2.6 mV

- 0.2 V-1 V input dynamic range
- INL_{MAX}=0.14 LSB, DNL_{MAX}=0.125 LSB from schematic simulations, <0.5 LSB in post layout simulations (no missing codes)

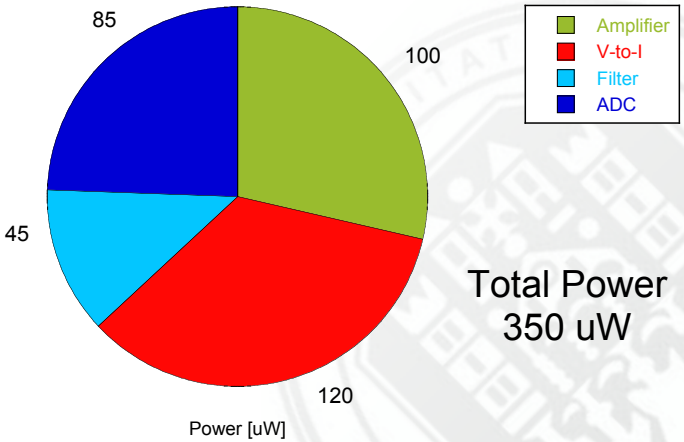


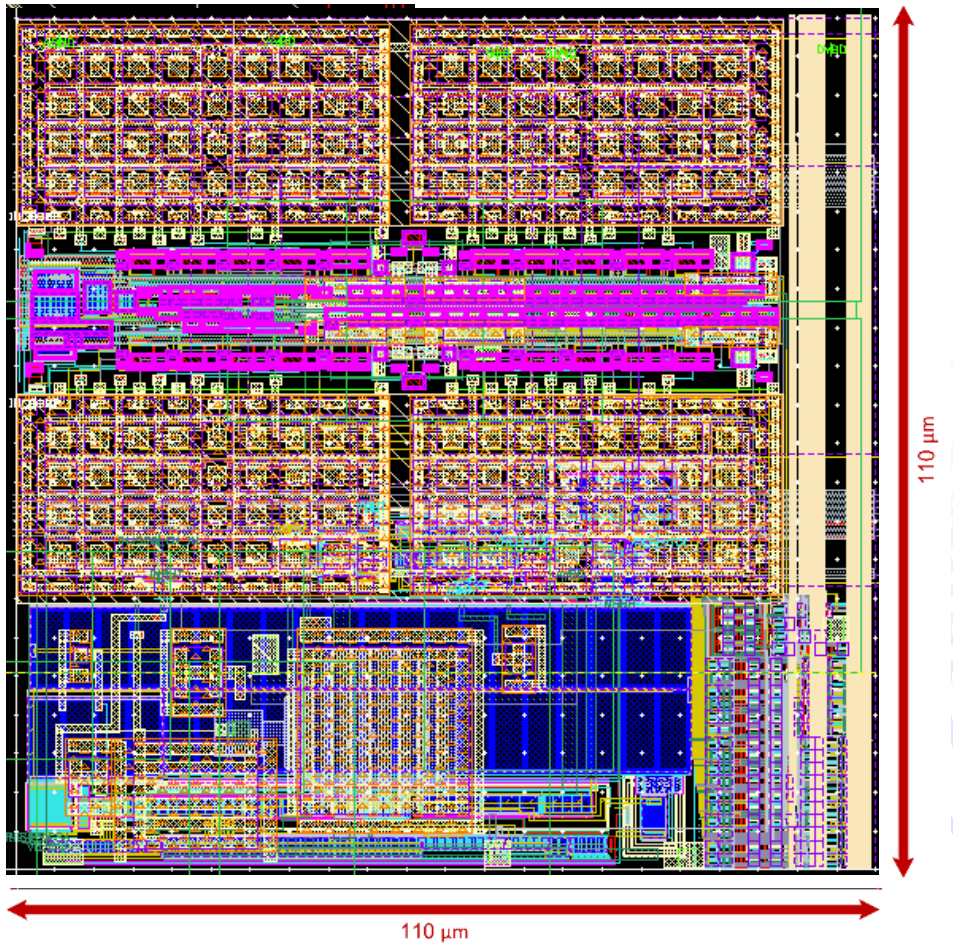
The pixel readout cell

Area occupancy



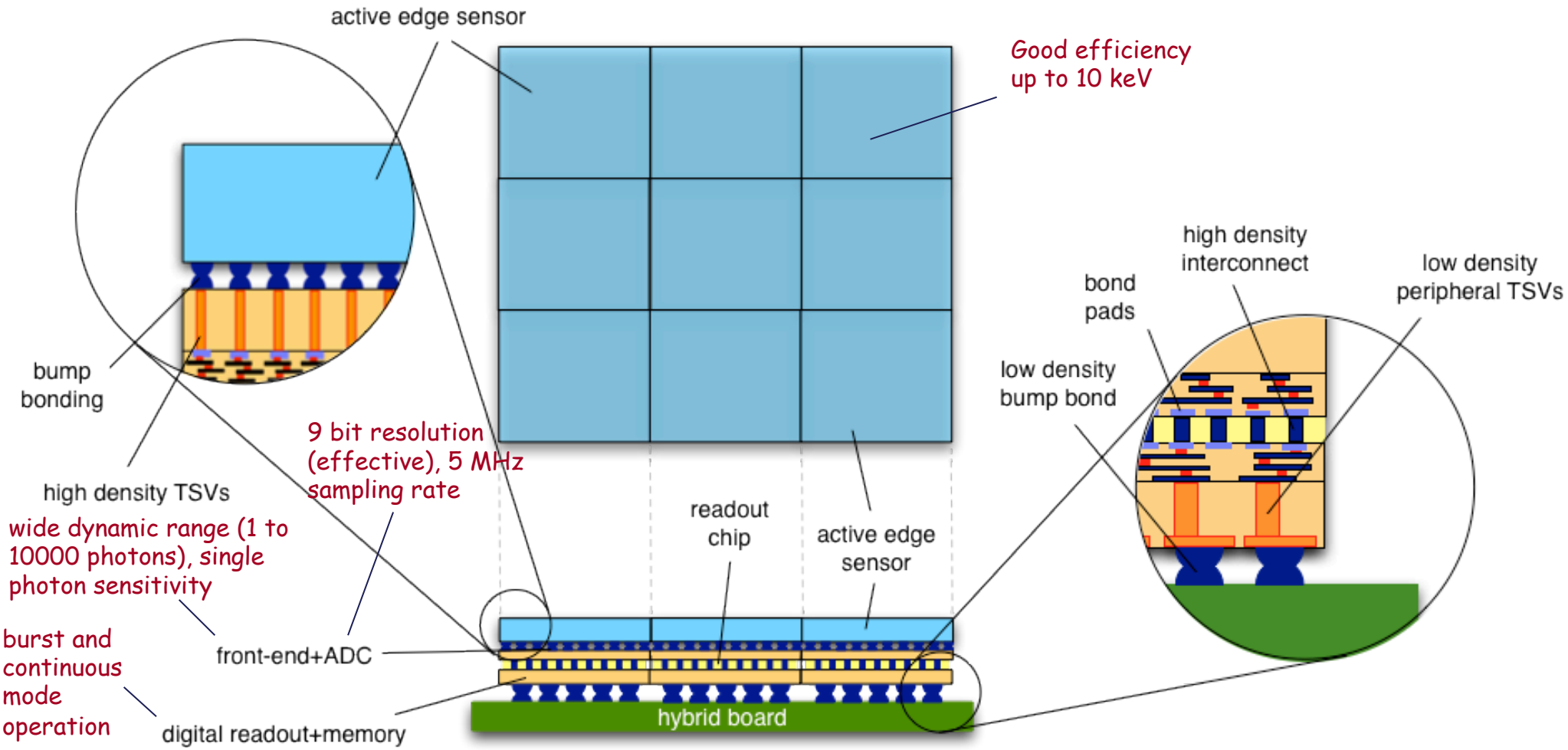
Power Consumption





Long term goals of the PIXFEL project

- Develop a four-side buttable module for the assembly of large area detectors with no or minimum dead area to be used at FEL experiments



Conclusions

- At the 65 nm node, low-noise design of analog circuits in mixed-signal detector readout chips is challenging but, according to the study of key analog parameters, appears to be still viable in the Low Power technology flavor.
- Classical analog problems (signal amplification and filtering, noise optimization, minimization of threshold dispersion) require clever solutions
- Microelectronic technology will drive the evolution of particle detection systems as it has done in the last decades
- In the next couple of years, large size 65 nm mixed-signal readout chips for pixel detectors in high energy physics and photon science will be available

Backup slides

Noise spectra at minimum channel length in various CMOS generations

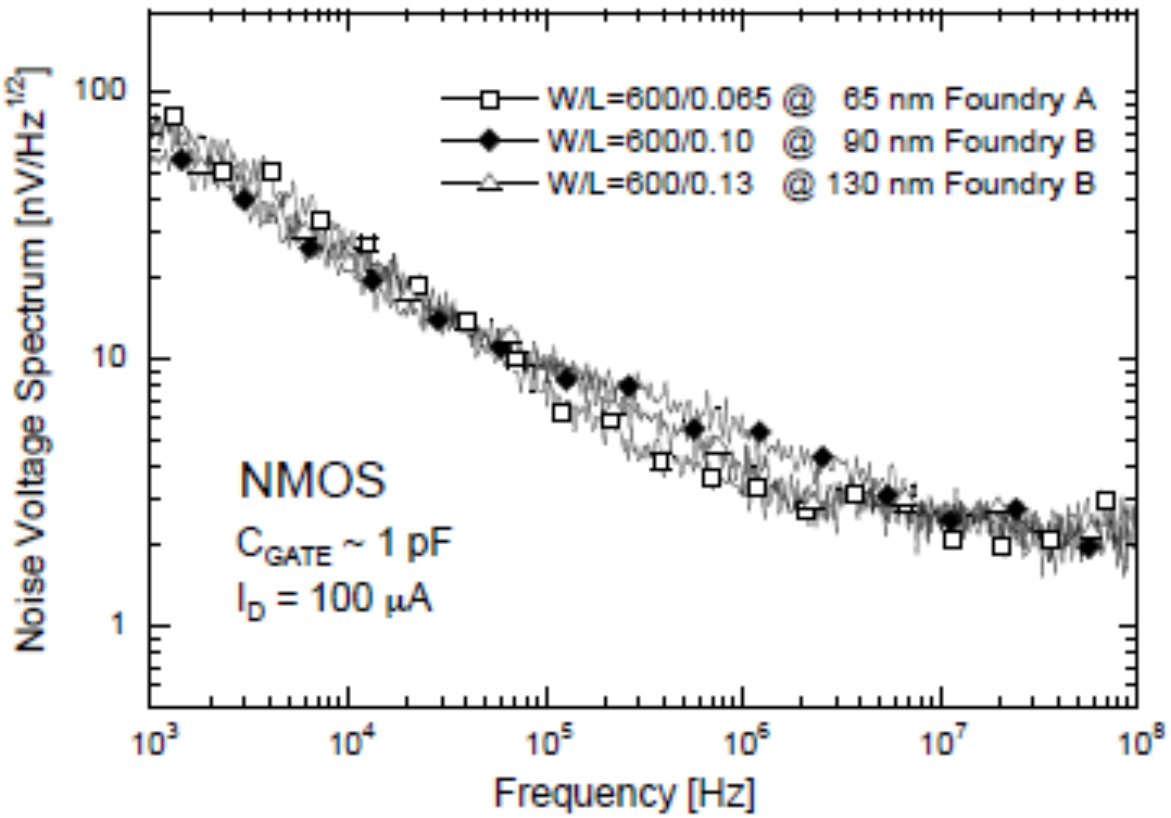


Fig. 3. Noise voltage spectra of NMOS with same gate capacitance belonging to the 130, 90 and 65 nm CMOS technology nodes.

- As for the noise, the discriminator threshold and its dispersion (divided by the analog channel charge sensitivity) can be treated in term of input-referred charges, Q_{th} and σ_{qth} respectively.

- For a second-order semigaussian shaper, and series white noise as the dominant contribution to ENC, the frequency of noise hits can be calculated as:

$$f_n = \frac{\sqrt{3}}{\pi t_p} e^{-\frac{Q_{th}^2}{2ENC^2}}$$

- In practical conditions, the number of noise hits can be kept at acceptably low values by satisfying this condition:

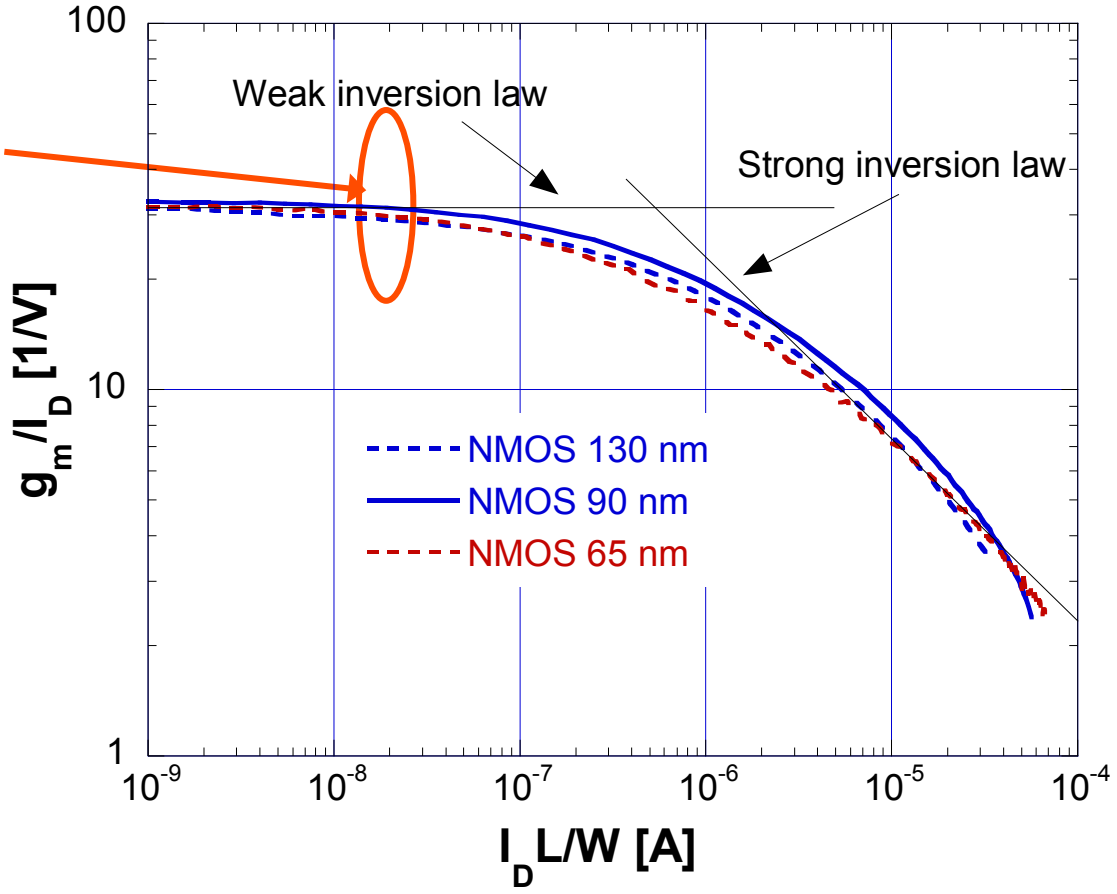
$$Q_{th}^{sig} > 4\left(ENC+\sigma_{qth}\right)$$

- To maintain an adequate efficiency, a channel-by-channel threshold adjustment may be necessary (threshold DAC in the pixel cell)

MOSFET essential parameters: the transconductance g_m

Operating point for W/L =400/0.2 (strips), I_D = 40 μA

W/L =20/0.1 (pixels), I_D = 4 μA



- Under reasonable power dissipation constraints, devices in deep submicron CMOS operate in the weak inversion region
- In weak inversion:

$$g_m = \frac{I_D}{nV_T}$$

(n =1.2 in 100-nm scale CMOS)